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DATASHEET

RX63T Group
Renesas MCUs

R01DS0087EJ0100
Rev.1.00
Aug 28, 2012

100-MHz 32-bit RX MCU, on-chip FPU, 165 DMIPS, 12-bit ADC (3 S/H circuits, double data register, amplifier, comparator): two units, 10-bit ADC one unit, the three ADC units are capable of simultaneous 7-ch. sampling, 100-MHz PWM (two three-phase complementary channels and four single-phase complementary channels or three three-phase complementary channels and one single-phase complementary channel)

Features

■ 32-bit RX CPU core
- Max. operating frequency: 100 MHz
  Capable of 165 DMIPS in operation at 100 MHz
- Single precision 32-bit IEEE-754 floating point
- Two types of multiply-and-accumulation unit (between memories and between registers)
- 32-bit multiplier (fastest instruction execution takes one CPU clock cycle)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions: Ultra-compact code
- Supports the memory protection unit (MPU)
- Two types of debugging interfaces: JTAG and FINE (two-line)

■ Low-power design and architecture
- Operation from a single 2.7- to 3.6-V supply
- Four low-power modes

■ On-chip main flash memory, no wait states
- 100-MHz operation, 10-ns read cycle (no wait states)
- 64-Kbyte/48-Kbyte/32-Kbyte capacities
- User code is programmable by on-board or off-board programming.

■ On-chip data flash memory
- 8 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM, no wait states
- 8-Kbyte capacities
- For instructions and operands
- Can provide backup on deep software standby

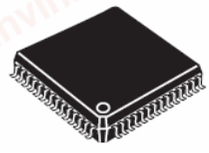
■ DMA
- DMAC: Incorporates four channels
- DTC

■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- External crystal oscillator or internal PLL for operation at 8 to 12.5 MHz
- Internal 125-kHz LOCO
- Dedicated 125-kHz LOCO for the IWDT
- Clock frequency accuracy measurement circuit (CAC)

■ Independent watchdog timer
- 125-kHz LOCO clock operation

■ Useful functions for IEC60730 compliance
- Oscillation-stop detection, frequency measurement, CRC, IWDT, self-diagnostic function for the A/D converter, etc.



PLQP0064KB-A 10 × 10mm, 0.5mm pitch
PLQP0048KB-A 7 x 7mm, 0.5mm pitch

■ Up to five communications interfaces
- SCI with multiple functionalities (up to 3 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simple SPI, simple I^2C, and extended serial mode.
- I^2C bus interface for transfer at up to 400 kbps (1 channels)
- RSPI for high-speed transfer (1 channels)

■ Up to 16 extended-function timers
- 16-bit MTU3: 100-MHz operation, input capture, output compare, two three-phase complementary PWM output channels, complementary PWM imposing no load on the CPU, phase-counting mode
- 100-MHz operation, input capture, output compare, four complementary single-phase PWM output channels, or one three-phase complementary PWM output channel and one single-phase complementary PWM output channel, complementary PWM imposing no load on the CPU, operation linked with comparator (for counting and control of PWM-signal negation), detection of abnormal oscillation frequencies (for IEC 60730 compliance) (4 channels)
- 16-bit compare-match timers (4 channels)

■ 12-bit A/D converter for 1-MHz operation, with 8 channels
- Up to 3 12-bit channels, and incorporating 1 sample-and-hold circuits
- Self-diagnosis (for IEC60730 compliance)
- ADC: Three sample-and-hold circuits, double data registers, comparators (on 3 channels)

■ Register write protection function can protect values in important registers against overwriting.

■ Up to 48 pins for GPIO
- 5-V tolerance, open drain, input pull-up

■ Operating temp. range
- –40°C to +85°C

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1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.
Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package and the ROM capacity. For details, see Table 1.2, Functions of RX63T Group Products.

Table 1.1 Outline of Specifications (1/4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision floating point (32-bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 64/48/32 Kbytes. • 100 MHz, no-wait access • On-board programming: 2 types
	RAM	• Capacity: 8 Kbytes • 100 MHz, no-wait access
	E^2 DataFlash	• Capacity: 8 Kbytes • Program/erase count: 100,000
MCU operating mode		Single-chip mode.
Clock	Clock generation circuit	• Main clock oscillator, low on-chip oscillator, PLL frequency synthesizer, and dedicated on-chip oscillator for the IWDT • Main-clock oscillation stop detection • Independent settings for the system clock (ICLK), peripheral module clock (PCLKA), peripheral module clock (PCLKB), FlashIF clock (FCLK) and clock for S12AD (PCLKD) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz The multi-function timer pulse unit 3 and the general PWM timer run in synchronization with the peripheral module clock (PCLKA): Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): Up to 50 MHz Flash IF run in synchronization with the FlashIF clock (FCLK): Up to 50 MHz The 12-bit A/D converter runs in synchronization with the clock for S12AD (PCLKD): Up to 50 MHz
	Clock frequency accuracy measurement circuit (CAC)	The frequency of the following clocks can be measured; the main clock oscillator, PCC circuit, and low clock oscillator dedicated for the IWDT.
Reset		Pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset

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Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
Interrupt	Interrupt controller (ICUA)	• Peripheral function interrupts: 106 sources • External interrupts: 6 (pins IRQ0 to IRQ5) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software interrupt activation register settings, external interrupts, and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	• 64-pin LQFP I/O pins: 39 Input pin: 9 Open-drain outputs: 2 5-V tolerance: 38 • 48-pin LQFP I/O pins: 25 Input pins: 7 Open-drain outputs: 2 5-V tolerance: 24
Timers	Multi-function timer pulse unit 3 (MTU3)	• (16 bits × 8 channels) • Maximum of 16 pulse-input/output and 3 pulse-input possible • Select eight clocks from among ten count clocks (PCLKA/1, PCLKA/4, PCLKA/16, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, and MTCLKD) for each channel (seven clocks for channel 1, four clocks for channel 5, and six clocks for channel 6 or 7) • 24 output compare/input capture registers • Counter-clearing operation (simultaneous clearing on compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous input and output to registers in synchronization with counter operations • Buffer operation specifiable • Capable of cascade-connected operation • 38 sources • Automatic transfer of register data • Pulse output modes Topple, PWM, complementary PWM, and reset-synchronous PWM modes • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion

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Table 1.1 Outline of Specifications (3/4)

Classification	Module/Function	Description
Timers	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins • 4 pins for input from signal sources: POE0, POE8, POE10, and POE11 • Initiation on detection of short-circuited outputs (detection of PWM outputs having simultaneously become an active level.) • Initiation by comparator-detection, oscillation-stoppage detection, or software • Software control of the states of pins for output control can also be added.
	General PWM timer (GPT)	• 16 bits x 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four count clocks (PCLKA/1, PCLKA/4, PCLKA/8, and PCLKA/16) for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Output of the internal comparator detection, software, and compare-match • The main clock can be used as a counter clock for measuring the timing of the edges of signals produced by frequency-dividing the dedicated low-speed clock signal for the IWDT (to detect abnormal oscillation).
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDT)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDT)	• 14 bits × 1 channel • Counter-input clock: Dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256
Communication function	Serial communications interfaces (SCIc, SCId)	• 3 channels (SCIc: 2 channels + SCId: 1 channel) • SCIc Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Simple I^2C Simple SPI • SCId (The following functions are added to SCIc) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interfaces (RIIC)	• 1 channel Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 400 kbps

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Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
Communication function	Serial peripheral interfaces (RSPI)	• 1 channel • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception
12-bit A/D converter (S12ADB)		• 12 bits (8 channels x 1 unit) • 12-bit resolution • Conversion time 1.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 50 MHz • Operating modes Scan mode (single-cycle scan mode/continuous scan mode/group scan mode) Group A priority control (only for the group scan mode) • Sample-and-hold function A common sample-and-hold circuit for units is included. Additionally, sample-and-hold circuit for each unit is included. (three channels per unit) • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0). • Double trigger mode (duplication of A/D converted data) • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Window comparators (three channels per unit)
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Data operating circuit (DOC)		• Comparison, addition, and subtraction of 16-bit data
Operating frequency		Up to 100MHz
Power supply voltage		VCC = 2.7 to 3.6V, AVCC0 = 3.0 to 3.6V, VREFH0 = 3.0V to AVCC0
Operating temperature		- 40 to 85 (products with wide-temperature-range spec.)
Package		64-pin LQFP (PLQP0064KB-A) 48-pin LQFP (PLQP0048KB-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

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Table 1.2 Functions of RX63T Group Products

Functions		RX63TGroup	
Package		**64Pins**	**48Pins**
DMA	DMA controller	ch0 to 3	
	Data transfer controller	Supported	
Timers	Multi-function timer pulse unit 3	ch. 0 to 7	
	Port output enable 3	Supported (for POE pins)	
	General PWM timer	ch. 0 to 3	
	Compare match timer	ch. 0 to 3	
	Watchdog timer	Supported	
	Independent watchdog timer	Supported	
Communication function	Serial communications interfaces (SCIc)	ch. 0,1	
	Serial communications interfaces (SCId)	ch. 12	
	I^2C bus interfaces	ch. 0	
	Serial peripheral interfaces	ch. 0	
12-bit A/D converter		AN000 to 007	AN000 to 004, 007
Clock frequency accuracy measurement circuit		Supported	
CRC calculato		Supported	
Data operating circuit		Supported	

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1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part number.

Table 1.3 List of Products

Group	Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	E2 DataFlash	Operating Frequency (Max.)
RX63T	R5F563T6EDFM	PLQP0064KB-A	64 Kbytes	8 Kbytes	8 Kbytes	100 MHz
	R5F563T5EDFM	PLQP0064KB-A	48 Kbytes	8 Kbytes	8 Kbytes	100 MHz
	R5F563T4EDFM	PLQP0064KB-A	32 Kbytes	8 Kbytes	8 Kbytes	100 MHz
	R5F563T6EDFL	PLQP0048KB-A	64 Kbytes	8 Kbytes	8 Kbytes	100 MHz
	R5F563T5EDFL	PLQP0048KB-A	48 Kbytes	8 Kbytes	8 Kbytes	100 MHz
	R5F563T4EDFL	PLQP0048KB-A	32 Kbytes	8 Kbytes	8 Kbytes	100 MHz

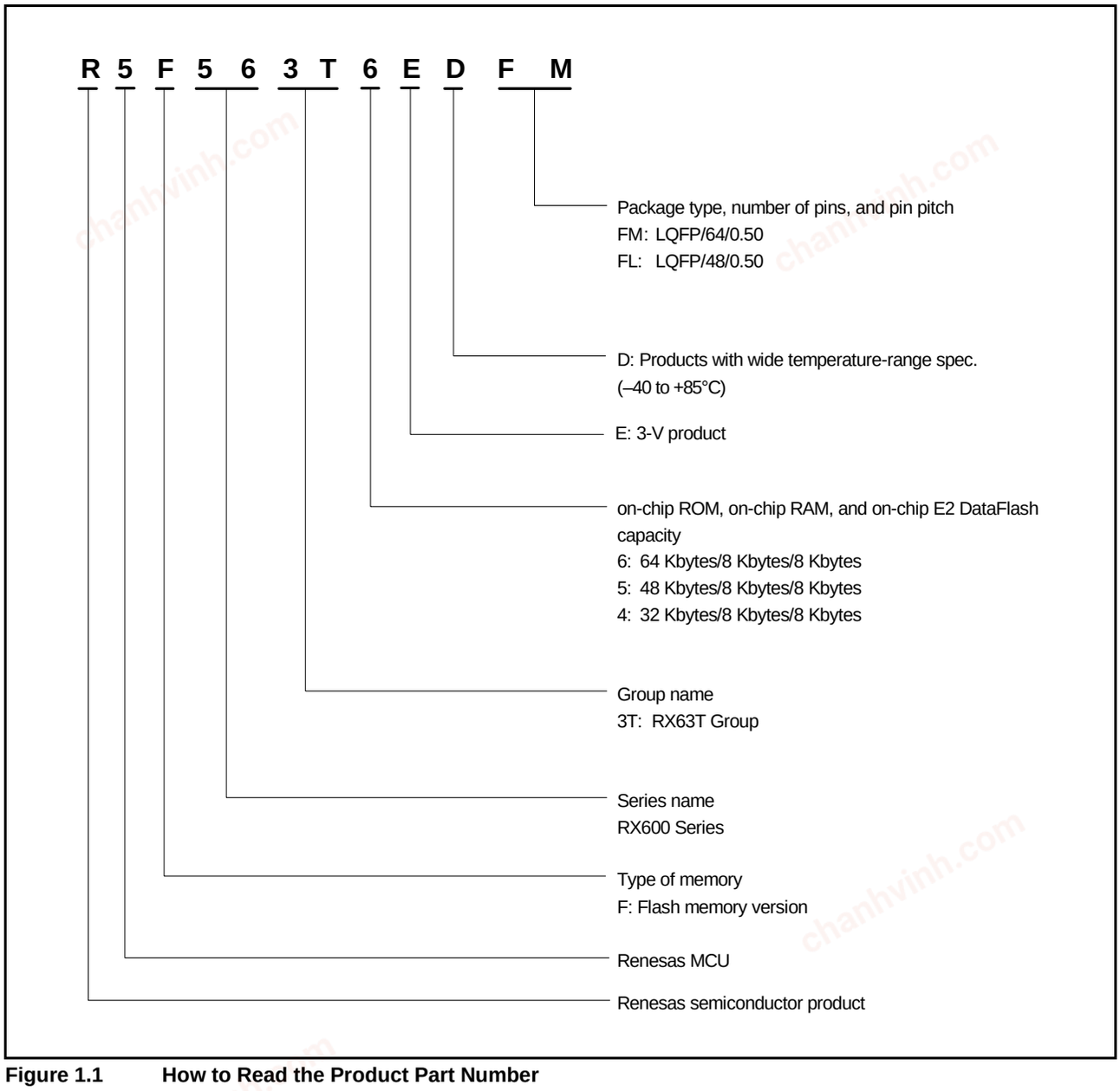


Figure 1.1 How to Read the Product Part Number

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1.3 Block Diagram

Figure 1.2 shows a block diagram.

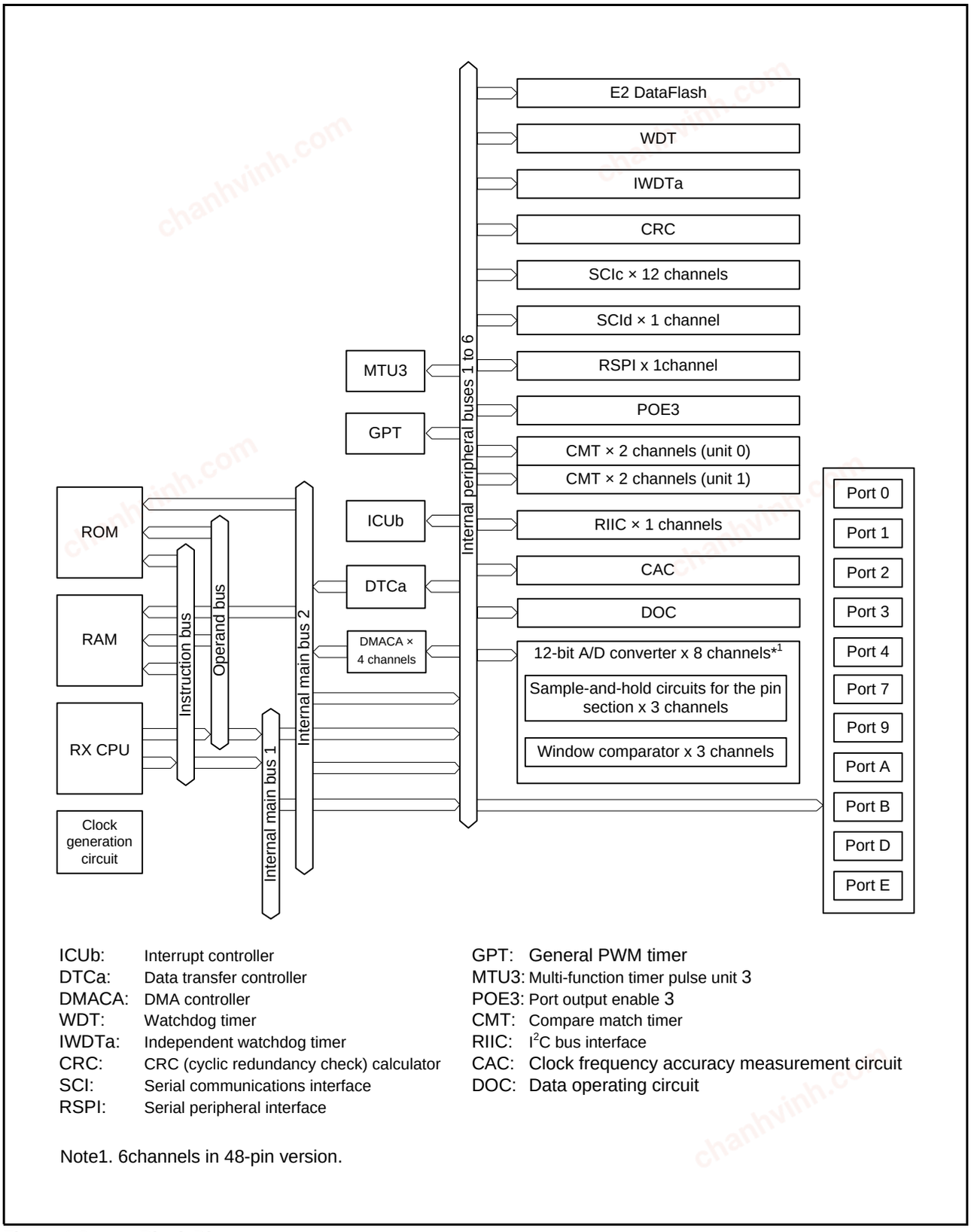


Figure 1.2 Block Diagram

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1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	—	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin
	VSS	—	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
Clock frequency accuracy measurement circuit	CACREF	Input	Trigger input pin for the clock frequency accuracy measurement
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
Interrupt	NMI	Input	Non-maskable interrupt request signal.
	IRQ0 to IRQ5	Input	Maskable interrupt request signals.
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD input capture input/output compare output/ PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB21 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins.
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins.
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/ PWM output pins.
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/ PWM output pins.
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals.
Port output enable 3	POE0#, POE8# POE10#, POE11#	Input	Input pins for request signals to place the MTU3 and GPT pins in the high impedance state.

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Table 1.4 Pin Functions (2/3)

Classifications	Pin Name	I/O	Description
General PWM timer	GTIOC0A, GTIOC0B	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC1A, GTIOC1B	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC2A, GTIOC2B	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins.
	GTETRG	Input	External trigger input pin for the GPT
Serial communications interface (SCIc)	Asynchronous mode/clock synchronous mode		
	SCK0, SCK1	I/O	Input/output pins for clock signals.
	RXD0, RXD1	Input	Input pins for data reception.
	TXD0, TXD1	Output	Output pins for data transmission.
	CTS0#, CTS1#	Input	Transfer start control input pins
	RTS0#, RTS1#	Output	Transfer start control output pins
	Simple I^2C mode		
	SSCL0, SSCL1	I/O	Input/output pins for the I^2C clock
	SSDA0, SSDA1	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK0, SCK1	I/O	Input/output pins for the clock
	SMISO0, SMISO1	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1	I/O	Input/output pins for master transmit data.
	SS0#, SS1#	Input	Input pins for chip select signals
Serial communications interface (SCId)	Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for clock signals.
	RXD12	Input	Input pin for data reception.
	TXD12	Output	Output pin for data transmission.
	CTS12#	Input	Transfer start control input pins
	RTS12#	Output	Transfer start control output pins
	Simple I^2C mode		
	SSCL12	I/O	Input/output pins for the I^2C clock
	SSDA12	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK12	I/O	Input/output pins for the clock
	SMISO12	I/O	Input/output pins for slave transmit data.
	SMOSI12	I/O	Input/output pins for master transmit data.
	SS12#	Input	Input pins for chip select signals
	Extended serial mode		
	RXDX12	Input	Input pin for receive data
	TXDX12	Output	Output pin for transmit data
	SIOX12	I/O	Input/output pin for transfer data
I^2C bus interface	SCL	I/O	Clock input/output pin. N-channel open drain can directly drive buses.
	SDA	I/O	Data input/output pin. N-channel open drain can directly drive buses.

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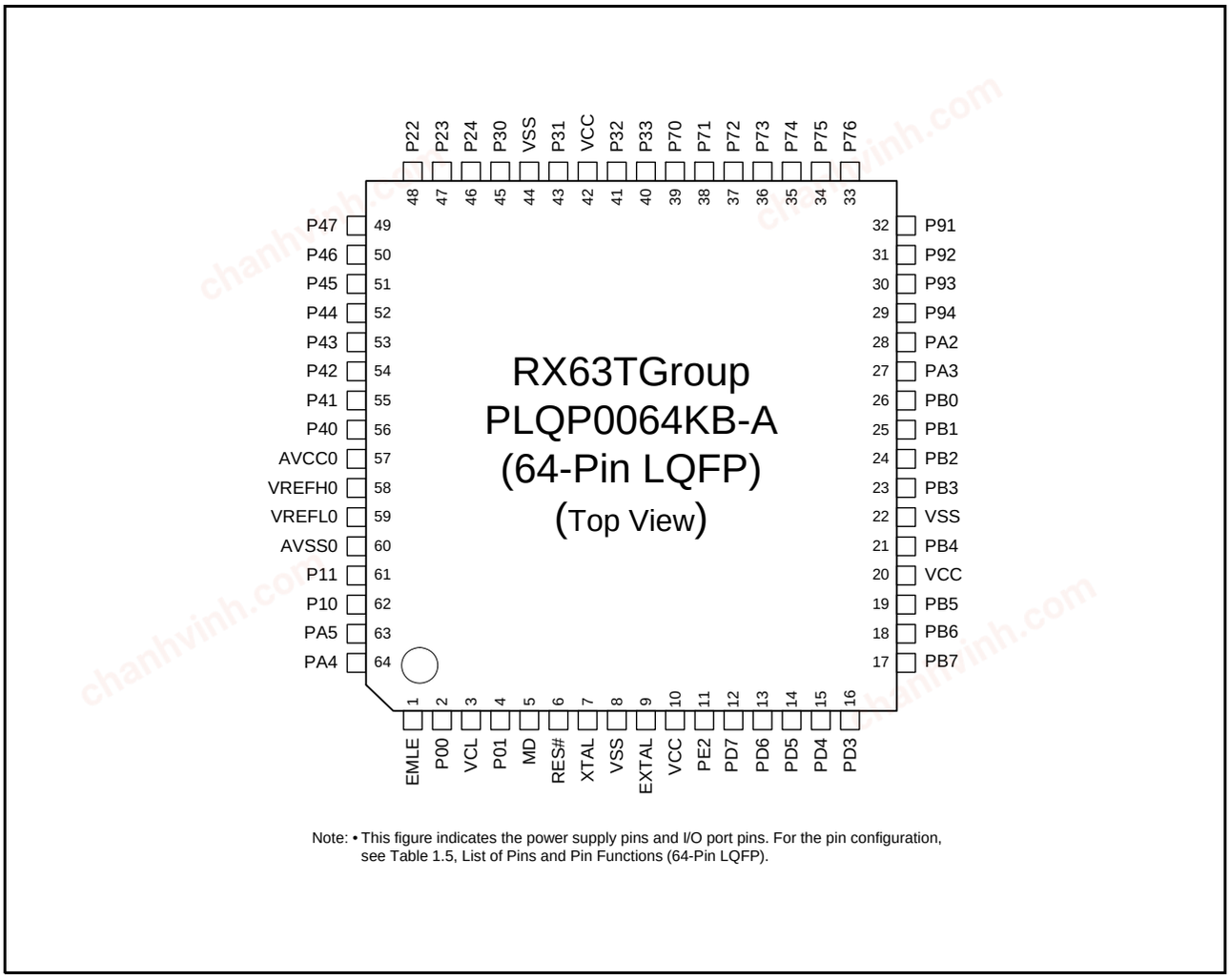
Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCKA	I/O	Clock input/output pin.
	MOSIA	I/O	Inputs or outputs data output from the master.
	MISOA	I/O	Inputs or outputs data output from the slave.
	SSLA0	I/O	Input or output pins for slave selection
	SSLA1 to SSLA3	Output	Output pins for slave selection
12-bit A/D converter	AN000 to AN007	Input	Input pins for the analog signals to be processed by the A/D converter. The AN005 and AN006 pins are not included in the 48-pin version.
	ADTRG0#	Input	Input pin for the external trigger signal that starts the A/D conversion.
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
Analog power supply	AVCC0	—	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	—	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	—	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	—	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
I/O ports	P00, P01	I/O	2-bit input/output pins. Not included in the 48-pin version.
	P10, P11	I/O	2-bit input/output pins. Not included in the 48-pin version.
	P22 to P24	I/O	3-bit input/output pins.
	P30 to P33	I/O	4-bit input pins. The P31 to P33 pins are not included in the 48-pin version.
	P40 to P47	Input	8-bit input pins. The P45 and P46 pins are not included in the 48-pin version.
	P70 to P76	I/O	7-bit input/output pins.
	P91 to P94	I/O	4-bit input/output pins. Not included in the 48-pin version.
	PA2 to PA5	I/O	4-bit input pins. The PA4 and PA5 pins are not included in the 48-pin version.
	PB0 to PB7	I/O	8-bit input pins. The PB7 pin is not included in the 48-pin version.
	PD3 to PD7	I/O	5-bit input/output pins.
	PE2	Input	1-bit input/output pin.

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1.5 Pin Assignments

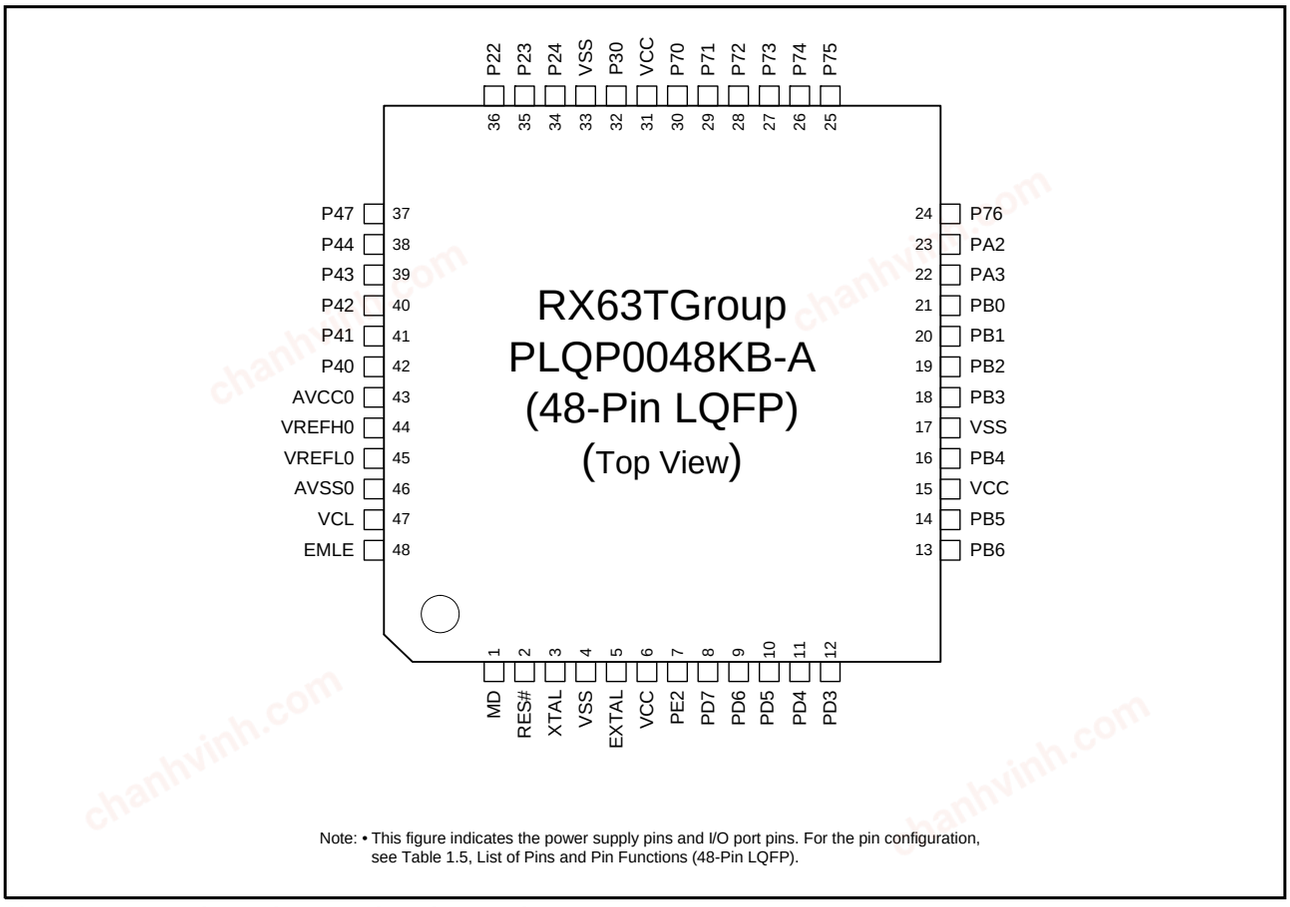
Figure 1.3 to Figure 1.4 show the pin assignments. Table 1.5 to Table 1.6 show the lists of pins and pin functions.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (64-Pin LQFP).

Figure 1.3 Pin Assignment (64-Pin LQFP)

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Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (48-Pin LQFP).

Figure 1.4 Pin Assignment (48-Pin LQFP)

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Table 1.5 List of Pins and Pin Functions (64-Pin LQFP) (1/3)

Pin No. 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
1	EMLE							
2		P00		GTIOC3A	CTS0# RTS0# SS0#		IRQ2-DS	
3	VCL							
4		P01		GTIOC3B CACREF			IRQ4-DS	
5	MD FINED							
6	RES#							
7	XTAL							
8	VSS							
9	EXTAL							
10	VCC							
11		PE2	POE10#				NMI	
12	TRST#	PD7		GTIOC0A	CTS0# RTS0# SS0#			
13	TMS	PD6		GTIOC0B				
14	TDI	PD5		GTIOC1A	RXD1 SMISO1 SSCL1			
15	TCK FINEC	PD4		GTIOC1B	SCK1			
16	TDO	PD3		GTIOC2A	TXD1 SMOSI1 SSDA1			
17		PB7		GTIOC2B	SCK12			
18		PB6		GTIOC2B	RXD12 SMISO12 SSCL12 RXDX12			
19		PB5	POE11#		TXD12 SMOSI12 SSDA12 TXDX12 SIOX12		IRQ0	
20	VCC							
21		PB4	POE8#	GTETRG	CTS12# RTS12# SS12#		IRQ3-DS	
22	VSS							
23		PB3		MTIOC0A MTCLKA CACREF	SCK0			
24		PB2		MTIOC0B MTCLKB	TXD0 SMOSI0 SSDA0	SDA		
25		PB1		MTIOC0C	RXD0 SMISO0 SSCL0	SCL		

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Table 1.5 List of Pins and Pin Functions (64-Pin LQFP) (2/3)

Pin No. 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
26		PB0		MTIOC0D		MOSIA		
27		PA3		MTIOC2A		SSLA0		
28		PA2		MTIOC2B		SSLA1		
29		P94			TXD1 SMOSI1 SSDA1			
30		P93			RXD1 SMISO1 SSCL1		IRQ1	
31		P92			SCK1			
32		P91			CTS1# RTS1# SS1#			
33		P76		MTIOC4D GTIOC2B				
34		P75		MTIOC4C GTIOC1B				
35		P74		MTIOC3D GTIOC0B				
36		P73		MTIOC4B GTIOC2A				
37		P72		MTIOC4A GTIOC1A				
38		P71		MTIOC3B GTIOC0A				
39		P70	POE0#		CTS1# RTS1# SS1#		IRQ5-DS	
40		P33		MTIOC3A		SSLA3		
41		P32		MTIOC3C		SSLA2		
42	VCC							
43		P31		MTIOC0A		SSLA1		
44	VSS							
45		P30		MTIOC0B MTCLKD	TXD0 SMOSI0 SSDA0	SSLA0		
46		P24		MTIC5U MTCLKC	RXD0 SMISO0 SSCL0	RSPCKA		
47		P23		MTIC5V MTCLKB CACREF	SCK0	MOSIA		
48		P22		MTIC5W MTCLKA	CTS0# RTS0# SS0#	MISOA		
49		P47						AN007 CVREFH
50		P46						AN006
51		P45						AN005
52		P44						AN004

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Table 1.5 List of Pins and Pin Functions (64-Pin LQFP) (3/3)

Pin No. 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
53		P43						AN003 CVREFL
54		P42						AN002
55		P41						AN001
56		P40						AN000
57	AVCC0							
58	VREFH0							
59	VREFL0							
60	AVSS0							
61		P11		MTCLKC			IRQ1-DS	
62		P10		MTCLKD			IRQ0-DS	
63		PA5		MTIOC1A		MISOA		
64		PA4		MTIOC1B		RSPCKA		ADTRG0#

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Table 1.6 List of Pins and Pin Functions (48-Pin LQFP) (1/2)

Pin No. 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
1	MD FINED							
2	RES#							
3	XTAL							
4	VSS							
5	EXTAL							
6	VCC							
7		PE2	POE10#				NMI	
8	TRST#	PD7		GTIOC0A	CTS0# RTS0# SS0#			
9	TMS	PD6		GTIOC0B				
10	TDI	PD5		GTIOC1A	RXD1 SMISO1 SSCL1			
11	TCK FINEC	PD4		GTIOC1B	SCK1			
12	TDO	PD3		GTIOC2A	TXD1 SMOSI1 SSDA1			
13		PB6		GTIOC2B	RXD12 SMISO12 SSCL12 RXDX12			
14		PB5	POE11#		TXD12 SMOSI12 SSDA12 TXDX12 SIOX12		IRQ0	
15	VCC							
16		PB4	POE8#	GTETRG	CTS12# RTS12# SS12#		IRQ3-DS	
17	VSS							
18		PB3		MTIOC0A MTCLKA CACREF	SCK0			
19		PB2		MTIOC0B MTCLKB	TXD0 SMOSI0 SSDA0	SDA		
20		PB1		MTIOC0C	RXD0 SMISO0 SSCL0	SCL		
21		PB0		MTIOC0D	SCK12	MOSIA		
22		PA3		MTIOC2A		SSLA0		
23		PA2		MTIOC2B		SSLA1		
24		P76		MTIOC4D GTIOC2B				
25		P75		MTIOC4C GTIOC1B				

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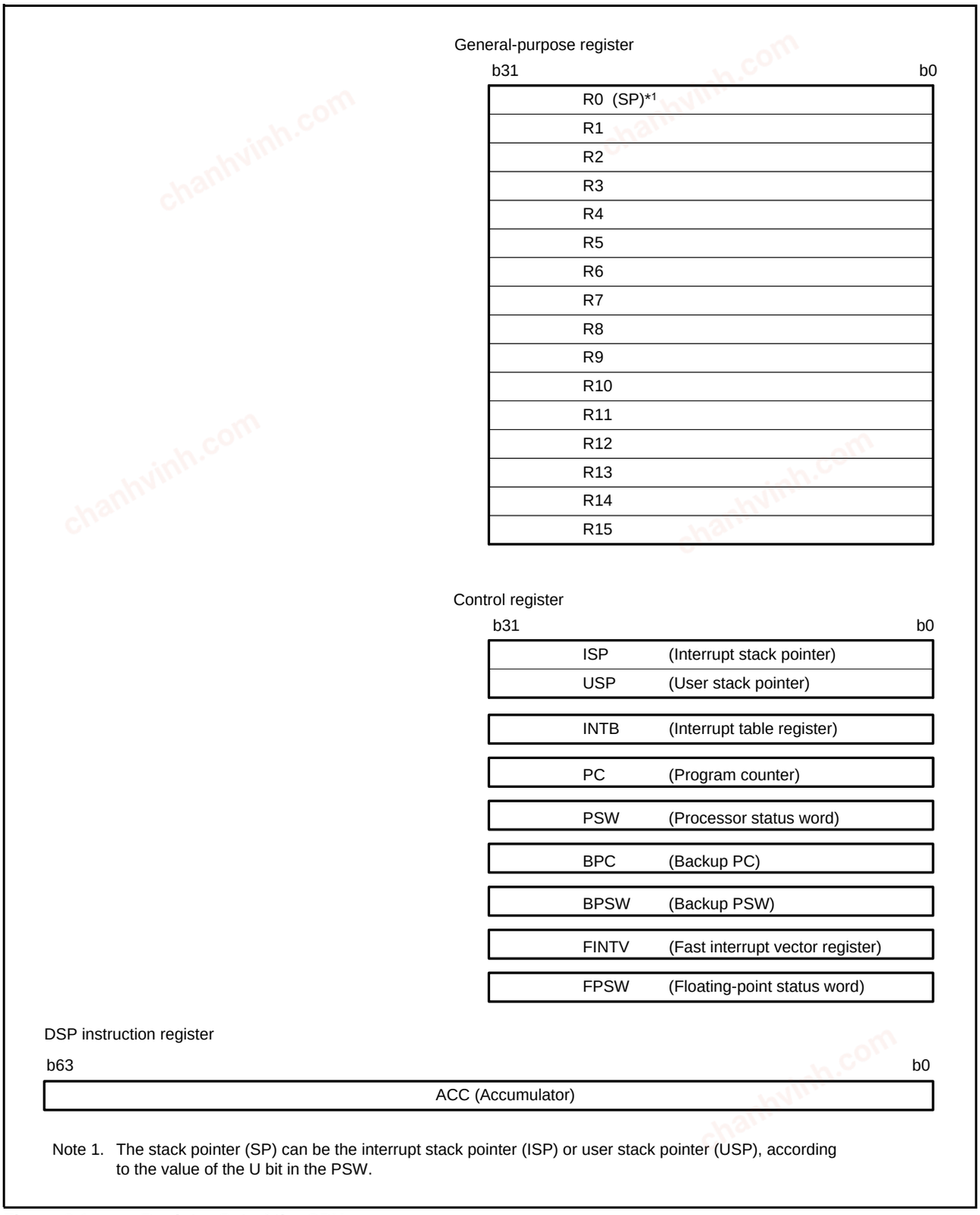
Table 1.6 List of Pins and Pin Functions (48-Pin LQFP) (2/2)

Pin No. 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
26		P74		MTIOC3D GTIOC0B				
27		P73		MTIOC4B GTIOC2A				
28		P72		MTIOC4A GTIOC1A				
29		P71		MTIOC3B GTIOC0A				
30		P70	POE0#		CTS1# RTS1# SS1#		IRQ5-DS	
31	VCC							
32		P30		MTIOC0B MTCLKD	TXD0 SMOSI0 SSDA0	SSLA0		
33	VSS							
34		P24		MTIC5U MTCLKC	RXD0 SMISO0 SSCL0	RSPCKA		
35		P23		MTIC5V MTCLKB	DCK0	MOSIA		
36		P22		MTIC5W MTCLKA	CTS0# RTS0# SS0#	MISOA		
37		P47						AN007 CVREFH
38		P44						AN004
39		P43						AN003 CVREFL
40		P42						AN002
41		P41						AN001
42		P40						AN000
43	AVCC0							
44	VREFH0							
45	VREFL0							
46	AVSS0							
47	VCL							
48	EMLE							

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2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

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2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

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2.2.1 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

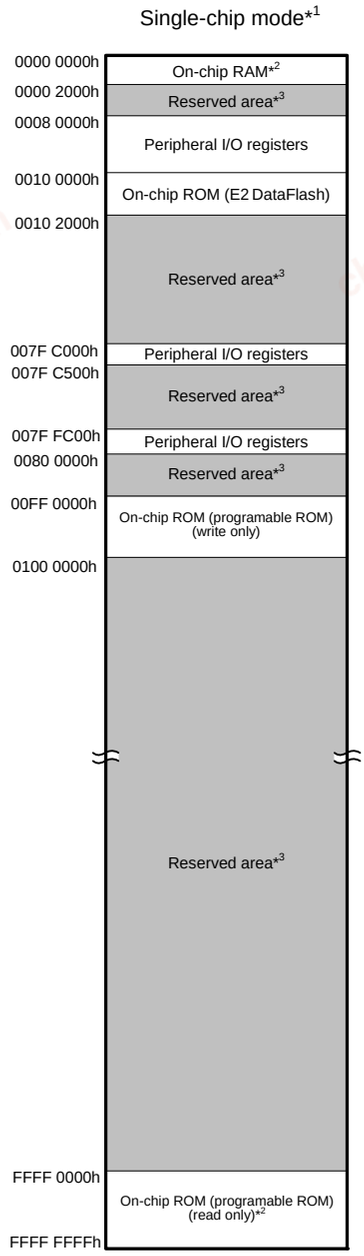
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3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas. Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

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Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

On-chip ROM (bytes)		On-chip RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
64K	FFFF 0000h to FFFF FFFFh	8K	0000 0000h to 0000 1FFFh
48K	FFFF 4000h to FFFF FFFFh		
32K	FFFF 8000h to FFFF FFFFh		

Note:•See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

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4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

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- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with bus access from the different bus master (DMAC or DTC).

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4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK		Operating Modes
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK		
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK		
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK		Low Power Consumption
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK		
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK		
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK		
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK		Clock Generation Circuit
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16	3 ICLK		
0008 0028h	SYSTEM	PLL control register	PLLCR	16	16	3 ICLK		
0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8	3 ICLK		
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8	3 ICLK		
0008 0034h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	8	8	3 ICLK		
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8	3 ICLK		
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8	3 ICLK		
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8	3 ICLK		
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8	3 ICLK		Low Power Consumption
0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8	3 ICLK		
0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8	3 ICLK		Resets
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16	3 ICLK		
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit control register 1	LVD1CR1	8	8	3 ICLK		LVDA
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit status register	LVD1SR	8	8	3 ICLK		
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit control register 1	LVD2CR1	8	8	3 ICLK		
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit status register	LVD2SR	8	8	3 ICLK		
0008 03FEh	SYSTEM	Protect register	PRCR	16	16	3 ICLK		Register Write Protection Function
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK		
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK		
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK		
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16	2 ICLK		
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32	2 ICLK		DMACA
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32	2 ICLK		
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK		
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK		
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK		

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Table 4.1 List of I/O Registers (Address Order) (2/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK		DMACA
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK		
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK		
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK		
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK		
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK		
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK		
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK		
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2200h	DMAC	DMA module activation register	DMAST	8	8	2 ICLK		
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK		DTCa
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK		
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK		
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK		
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK		
0008 6400h	MPU	Region-0 start page number register	RSPAGE0	32	32	1ICLK		MPU
0008 6404h	MPU	Region-0 end page number register	REPAGE0	32	32	1ICLK		
0008 6408h	MPU	Region-1 start page number register	RSPAGE1	32	32	1ICLK		
0008 640Ch	MPU	Region-1 end page number register	REPAGE1	32	32	1ICLK		
0008 6410h	MPU	Region-2 start page number register	RSPAGE2	32	32	1ICLK		
0008 6414h	MPU	Region-2 end page number register	REPAGE2	32	32	1ICLK		
0008 6418h	MPU	Region-3 start page number register	RSPAGE3	32	32	1ICLK		
0008 641Ch	MPU	Region-3 end page number register	REPAGE3	32	32	1ICLK		
0008 6420h	MPU	Region-4 start page number register	RSPAGE4	32	32	1ICLK		
0008 6424h	MPU	Region-4 end page number register	REPAGE4	32	32	1ICLK		
0008 6428h	MPU	Region-5 start page number register	RSPAGE5	32	32	1ICLK		
0008 642Ch	MPU	Region-5 end page number register	REPAGE5	32	32	1ICLK		
0008 6430h	MPU	Region-6 start page number register	RSPAGE6	32	32	1ICLK		

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Table 4.1 List of I/O Registers (Address Order) (3/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 6434h	MPU	Region-6 end page number register	REPAGE6	32	32	1ICLK		MPU
0008 6438h	MPU	Region-7 start page number register	RSPAGE7	32	32	1ICLK		
0008 643Ch	MPU	Region-7 end page number register	REPAGE7	32	32	1ICLK		
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1ICLK		
0008 6504h	MPU	Background access control register	MPBAC	32	32	1ICLK		
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1ICLK		
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1ICLK		
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1ICLK		
0008 6520h	MPU	Region search address register	MPSA	32	32	1ICLK		
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1ICLK		
0008 6526h	MPU	Region invalidation operation register	MPOPI	16	16	1ICLK		
0008 6528h	MPU	Instruction-hit region register	MHITI	32	32	1ICLK		
0008 652Ch	MPU	Data-hit region register	MHITD	32	32	1ICLK		
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK		ICUb
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK		
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK		
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK		
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK		
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK		
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK		
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK		
0008 7024h	ICU	Interrupt request register 036	IR036	8	8	2 ICLK		
0008 7025h	ICU	Interrupt request register 037	IR037	8	8	2 ICLK		
0008 7026h	ICU	Interrupt request register 038	IR038	8	8	2 ICLK		
0008 7027h	ICU	Interrupt request register 039	IR039	8	8	2 ICLK		
0008 7028h	ICU	Interrupt request register 040	IR040	8	8	2 ICLK		
0008 7029h	ICU	Interrupt request register 041	IR041	8	8	2 ICLK		
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK		
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK		
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK		
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK		
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK		
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK		
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK		
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK		
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK		
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK		
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK		
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK		
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK		
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK		
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK		
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK		
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK		
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK		
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK		
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK		
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK		
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK		

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Table 4.1 List of I/O Registers (Address Order) (4/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK		ICUb
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK		
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK		
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK		
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK		
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK		
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK		
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK		
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK		
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8	2 ICLK		
0008 7090h	ICU	Interrupt request register 144	IR144	8	8	2 ICLK		
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK		
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK		
0008 7093h	ICU	Interrupt request register 147	IR147	8	8	2 ICLK		
0008 7094h	ICU	Interrupt request register 148	IR148	8	8	2 ICLK		
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK		
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2 ICLK		
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2 ICLK		
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2 ICLK		
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2 ICLK		
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2 ICLK		
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2 ICLK		
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2 ICLK		
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2 ICLK		
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2 ICLK		
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2 ICLK		
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2 ICLK		
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8	2 ICLK		
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8	2 ICLK		
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2 ICLK		
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2 ICLK		
0008 70A8h	ICU	Interrupt request register 168	IR168	8	8	2 ICLK		
0008 70A9h	ICU	Interrupt request register 169	IR169	8	8	2 ICLK		
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK		
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2 ICLK		
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2 ICLK		
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK		
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK		
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK		
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8	2 ICLK		
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2 ICLK		
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2 ICLK		
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2 ICLK		
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2 ICLK		
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK		
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK		
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK		
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK		
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK		
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK		

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Table 4.1 List of I/O Registers (Address Order) (5/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2 ICLK		ICUb
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2 ICLK		
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2 ICLK		
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2 ICLK		
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8	2 ICLK		
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8	2 ICLK		
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8	2 ICLK		
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8	2 ICLK		
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2 ICLK		
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2 ICLK		
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2 ICLK		
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2 ICLK		
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2 ICLK		
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2 ICLK		
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2 ICLK		
0008 70F2h	ICU	Interrupt request register 242	IR242	8	8	2 ICLK		
0008 70F4h	ICU	Interrupt request register 244	IR244	8	8	2 ICLK		
0008 70F5h	ICU	Interrupt request register 245	IR245	8	8	2 ICLK		
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK		
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK		
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK		
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8	2 ICLK		
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8	2 ICLK		
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8	2 ICLK		
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK		
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK		
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK		
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK		
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK		
0008 7127h	ICU	DTC activation enable register 039	DTCER039	8	8	2 ICLK		
0008 7128h	ICU	DTC activation enable register 040	DTCER040	8	8	2 ICLK		
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK		
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK		
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK		
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK		
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK		
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK		
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK		
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK		
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK		
0008 717Fh	ICU	DTC activation enable register 127	DTCER127	8	8	2 ICLK		
0008 7180h	ICU	DTC activation enable register 128	DTCER128	8	8	2 ICLK		
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK		
0008 7185h	ICU	DTC activation enable register 133	DTCER133	8	8	2 ICLK		
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK		
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK		
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK		
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK		
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2 ICLK		
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2 ICLK		

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Table 4.1 List of I/O Registers (Address Order) (6/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2 ICLK		ICUb
0008 7192h	ICU	DTC activation enable register 146	DTCER146	8	8	2 ICLK		
0008 7193h	ICU	DTC activation enable register 147	DTCER147	8	8	2 ICLK		
0008 7194h	ICU	DTC activation enable register 148	DTCER148	8	8	2 ICLK		
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2 ICLK		
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2 ICLK		
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8	2 ICLK		
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8	2 ICLK		
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2 ICLK		
0008 719Ah	ICU	DTC activation enable register 154	DTCER154	8	8	2 ICLK		
0008 719Bh	ICU	DTC activation enable register 155	DTCER155	8	8	2 ICLK		
0008 719Ch	ICU	DTC activation enable register 156	DTCER156	8	8	2 ICLK		
0008 719Dh	ICU	DTC activation enable register 157	DTCER157	8	8	2 ICLK		
0008 71A1h	ICU	DTC activation enable register 161	DTCER161	8	8	2 ICLK		
0008 71A2h	ICU	DTC activation enable register 162	DTCER162	8	8	2 ICLK		
0008 71A3h	ICU	DTC activation enable register 163	DTCER163	8	8	2 ICLK		
0008 71A4h	ICU	DTC activation enable register 164	DTCER164	8	8	2 ICLK		
0008 71A5h	ICU	DTC activation enable register 165	DTCER165	8	8	2 ICLK		
0008 71ABh	ICU	DTC activation enable register 171	DTCER171	8	8	2 ICLK		
0008 71ACh	ICU	DTC activation enable register 172	DTCER172	8	8	2 ICLK		
0008 71ADh	ICU	DTC activation enable register 173	DTCER173	8	8	2 ICLK		
0008 71C3h	ICU	DTC activation enable register 195	DTCER195	8	8	2 ICLK		
0008 71C4h	ICU	DTC activation enable register 196	DTCER196	8	8	2 ICLK		
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2 ICLK		
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2 ICLK		
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2 ICLK		
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2 ICLK		
0008 71D6h	ICU	DTC activation enable register 214	DTCER214	8	8	2 ICLK		
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK		
0008 71D9h	ICU	DTC activation enable register 217	DTCER217	8	8	2 ICLK		
0008 71DAh	ICU	DTC activation enable register 218	DTCER218	8	8	2 ICLK		
0008 71E2h	ICU	DTC activation enable register 226	DTCER226	8	8	2 ICLK		
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK		
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8	2 ICLK		
0008 71E5h	ICU	DTC activation enable register 229	DTCER229	8	8	2 ICLK		
0008 71E6h	ICU	DTC activation enable register 230	DTCER230	8	8	2 ICLK		
0008 71E7h	ICU	DTC activation enable register 231	DTCER231	8	8	2 ICLK		
0008 71E8h	ICU	DTC activation enable register 232	DTCER232	8	8	2 ICLK		
0008 71E9h	ICU	DTC activation enable register 233	DTCER233	8	8	2 ICLK		
0008 71EAh	ICU	DTC activation enable register 234	DTCER234	8	8	2 ICLK		
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK		
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK		
0008 71EEh	ICU	DTC activation enable register 238	DTCER238	8	8	2 ICLK		
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK		
0008 71F0h	ICU	DTC activation enable register 240	DTCER240	8	8	2 ICLK		
0008 71F1h	ICU	DTC activation enable register 241	DTCER241	8	8	2 ICLK		
0008 71F2h	ICU	DTC activation enable register 242	DTCER242	8	8	2 ICLK		
0008 71F4h	ICU	DTC activation enable register 244	DTCER244	8	8	2 ICLK		
0008 71F5h	ICU	DTC activation enable register 245	DTCER245	8	8	2 ICLK		
0008 71F6h	ICU	DTC activation enable register 246	DTCER246	8	8	2 ICLK		

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Table 4.1 List of I/O Registers (Address Order) (7/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK		ICUb
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK		
0008 71FAh	ICU	DTC activation enable register 250	DTCER250	8	8	2 ICLK		
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8	2 ICLK		
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK		
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK		
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2 ICLK		
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK		
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK		
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK		
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK		
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK		
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK		
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK		
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK		
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK		
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK		
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK		
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK		
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK		
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK		
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK		
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK		
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK		
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK		
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK		
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK		
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK		
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK		
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8	2 ICLK		
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8	2 ICLK		
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8	2 ICLK		
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8	2 ICLK		
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8	2 ICLK		
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8	2 ICLK		
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8	2 ICLK		
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8	2 ICLK		
0008 7324h	ICU	Interrupt source priority register 036	IPR036	8	8	2 ICLK		
0008 7327h	ICU	Interrupt source priority register 039	IPR039	8	8	2 ICLK		
0008 7328h	ICU	Interrupt source priority register 040	IPR040	8	8	2 ICLK		
0008 7329h	ICU	Interrupt source priority register 041	IPR041	8	8	2 ICLK		
0008 7339h	ICU	Interrupt source priority register 057	IPR057	8	8	2 ICLK		
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	2 ICLK		
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	2 ICLK		
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	2 ICLK		
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	2 ICLK		
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	2 ICLK		
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	2 ICLK		
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	2 ICLK		
0008 7367h	ICU	Interrupt source priority register 103	IPR103	8	8	2 ICLK		

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Table 4.1 List of I/O Registers (Address Order) (8/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	2 ICLK		ICUb
0008 737Ah	ICU	Interrupt source priority register 122	IPR122	8	8	2 ICLK		
0008 737Eh	ICU	Interrupt source priority register 126	IPR126	8	8	2 ICLK		
0008 7382h	ICU	Interrupt source priority register 130	IPR130	8	8	2 ICLK		
0008 7385h	ICU	Interrupt source priority register 133	IPR133	8	8	2 ICLK		
0008 7387h	ICU	Interrupt source priority register 135	IPR135	8	8	2 ICLK		
0008 7389h	ICU	Interrupt source priority register 137	IPR137	8	8	2 ICLK		
0008 738Bh	ICU	Interrupt source priority register 139	IPR139	8	8	2 ICLK		
0008 738Dh	ICU	Interrupt source priority register 141	IPR141	8	8	2 ICLK		
0008 7391h	ICU	Interrupt source priority register 145	IPR145	8	8	2 ICLK		
0008 7392h	ICU	Interrupt source priority register 146	IPR146	8	8	2 ICLK		
0008 7396h	ICU	Interrupt source priority register 150	IPR150	8	8	2 ICLK		
0008 7397h	ICU	Interrupt source priority register 151	IPR151	8	8	2 ICLK		
0008 739Ah	ICU	Interrupt source priority register 154	IPR154	8	8	2 ICLK		
0008 739Eh	ICU	Interrupt source priority register 158	IPR158	8	8	2 ICLK		
0008 73A1h	ICU	Interrupt source priority register 161	IPR161	8	8	2 ICLK		
0008 73A3h	ICU	Interrupt source priority register 163	IPR163	8	8	2 ICLK		
0008 73A5h	ICU	Interrupt source priority register 165	IPR165	8	8	2 ICLK		
0008 73A6h	ICU	Interrupt source priority register 166	IPR166	8	8	2 ICLK		
0008 73ABh	ICU	Interrupt source priority register 171	IPR171	8	8	2 ICLK		
0008 73ACh	ICU	Interrupt source priority register 172	IPR172	8	8	2 ICLK		
0008 73ADh	ICU	Interrupt source priority register 173	IPR173	8	8	2 ICLK		
0008 73C2h	ICU	Interrupt source priority register 194	IPR194	8	8	2 ICLK		
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8	2 ICLK		
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8	2 ICLK		
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8	2 ICLK		
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8	2 ICLK		
0008 73D6h	ICU	Interrupt source priority register 214	IPR214	8	8	2 ICLK		
0008 73D9h	ICU	Interrupt source priority register 217	IPR217	8	8	2 ICLK		
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8	2 ICLK		
0008 73E5h	ICU	Interrupt source priority register 229	IPR229	8	8	2 ICLK		
0008 73E8h	ICU	Interrupt source priority register 232	IPR232	8	8	2 ICLK		
0008 73EBh	ICU	Interrupt source priority register 235	IPR235	8	8	2 ICLK		
0008 73EEh	ICU	Interrupt source priority register 238	IPR238	8	8	2 ICLK		
0008 73F1h	ICU	Interrupt source priority register 241	IPR241	8	8	2 ICLK		
0008 73F4h	ICU	Interrupt source priority register 244	IPR244	8	8	2 ICLK		
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8	2 ICLK		
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8	2 ICLK		
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8	2 ICLK		
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8	2 ICLK		
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8	2 ICLK		
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8	2 ICLK		
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK		
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK		
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK		
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK		
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK		
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK		
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8	2 ICLK		
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16	2 ICLK		

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Table 4.1 List of I/O Registers (Address Order) (9/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK		ICUb
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK		
0008 7582h	ICU	Non-maskable interrupt status register	NMICLR	8	8	2 ICLK		
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK		
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8	2 ICLK		
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	8	8	2 ICLK		
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	
0008 8036h	IWDT	IWDT reset control register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8038h	IWDT	IWDT count stop control register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK	
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8300h	RIIC0	I^2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8301h	RIIC0	I^2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8302h	RIIC0	I^2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8303h	RIIC0	I^2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8304h	RIIC0	I^2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8305h	RIIC0	I^2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8306h	RIIC0	I^2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8307h	RIIC0	I^2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8308h	RIIC0	I^2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8309h	RIIC0	I^2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Timeout internal counter L	TMOCNTL	16	16	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Timeout internal counter U	TMOCNTU	16	16	2, 3 PCLKB	2 ICLK	
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (10/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8310h	RIIC0	I^2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8311h	RIIC0	I^2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8312h	RIIC0	I^2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8313h	RIIC0	I^2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	RSPI
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 9000h	S12ADB	A/D control register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	S12ADB
0008 9004h	S12ADB	A/D channel select register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK	
0008 9008h	S12ADB	A/D-converted value addition mode select register	ADADS	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ch	S12ADB	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK	
0008 900Eh	S12ADB	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK	
0008 9010h	S12ADB	A/D start trigger select register	ADSTRGR	8	8	2, 3 PCLKB	2 ICLK	
0008 9014h	S12ADB	A/D channel select control register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK	
0008 9018h	S12ADB	A/D data-doubling register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Eh	S12ADB	A/D self-diagnosis data register	ADRD	16	16	2, 3 PCLKB	2 ICLK	
0008 9020h	S12ADB	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	
0008 9022h	S12ADB	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	
0008 9024h	S12ADB	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	
0008 9026h	S12ADB	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9028h	S12ADB	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ah	S12ADB	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ch	S12ADB	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	
0008 902Eh	S12ADB	A/D data register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	
0008 9060h	S12ADB	A/D sampling state register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK	
0008 9066h	S12ADB	Sample-and-hold circuit control register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK	
0008 9073h	S12ADB	A/D sampling state register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	
00089074h	S12ADB	A/D sampling state register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	
00089075h	S12ADB	A/D sampling state register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	
00089076h	S12ADB	A/D sampling state register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	
00089077h	S12ADB	A/D sampling state register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (11/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
00089078h	S12ADB	A/D sampling state register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12ADB
00089079h	S12ADB	A/D sampling state register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	
0008 9080h	S12ADB	A/D group-scan priority-control register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	
0008 9084h	S12ADB	A/D data-doubling register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	
0008 9086h	S12ADB	A/D data-doubling register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	
0008 90E0h	S12ADB	Comparator operating-mode selection register 0	ADCMPMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 90E2h	S12ADB	Comparator operating-mode selection register 1	ADCMPMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 90E4h	S12ADB	Comparator filter-mode register 0	ADCMPNR0	16	16	2, 3 PCLKB	2 ICLK	
0008 90E8h	S12ADB	Comparator detection flag register	ADCMPFR	16	16	2, 3 PCLKB	2 ICLK	
0008 90EAh	S12ADB	Comparator interrupt selection register	ADCMPSEL	16	16	2, 3 PCLKB	2 ICLK	
0008 A000h	SCI0	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 A001h	SCI0	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A002h	SCI0	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A003h	SCI0	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A004h	SCI0	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A005h	SCI0	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A006h	SCI0	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A007h	SCI0	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A008h	SCI0	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A009h	SCI0	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Ah	SCI0	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Bh	SCI0	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Ch	SCI0	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Dh	SCI0	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A020h	SCI1	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A021h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A022h	SCI1	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A023h	SCI1	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A024h	SCI1	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A025h	SCI1	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A026h	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A027h	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A028h	SCI1	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A029h	SCI1	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A02Ah	SCI1	I^2C bus mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A02Bh	SCI1	I^2C bus mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A02Ch	SCI1	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A02Dh	SCI1	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK	CAC
0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK	
0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK	
0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK	
0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK	
0008 B006h	CAC	CAC upper-limit value setting register	CAULVD	16	16	2, 3 PCLKB	2 ICLK	
0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK	
0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK	
0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK	DOC
0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK	
0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (12/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B300h	SCI12	Serial mode register	SMR12	8	8	2, 3 PCLKB	2, 3 ICLK	SCIc, SCId
0008 B301h	SCI12	Bit rate register	BRR12	8	8	2, 3 PCLKB	2, 3 ICLK	
0008 B302h	SCI12	Serial control register	SCR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B303h	SCI12	Transmit data register	TDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B304h	SCI12	Serial status register	SSR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B305h	SCI12	Receive data register	RDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B306h	SCI12	Smart card mode register	SCMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B307h	SCI12	Serial extended mode register	SEMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B308h	SCI12	Noise filter setting register	SNFR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B309h	SCI12	I^2C mode register 1	SIMR112	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ah	SCI12	I^2C mode register 2	SIMR212	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Bh	SCI12	I^2C mode register 3	SIMR312	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ch	SCI12	I^2C status register	SIS12	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Dh	SCI12	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B320h	SCI12	Extended serial module enable register	ESMER	8	8	2, 3 PCLKB	2 ICLK	
0008 B321h	SCI12	Control register 0	CR0	8	8	2, 3 PCLKB	2 ICLK	
0008 B322h	SCI12	Control register 1	CR1	8	8	2, 3 PCLKB	2 ICLK	
0008 B323h	SCI12	Control register 2	CR2	8	8	2, 3 PCLKB	2 ICLK	
0008 B324h	SCI12	Control register 3	CR3	8	8	2, 3 PCLKB	2 ICLK	
0008 B325h	SCI12	Port control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B326h	SCI12	Interrupt control register	ICR	8	8	2, 3 PCLKB	2 ICLK	
0008 B327h	SCI12	Status register	STR	8	8	2, 3 PCLKB	2 ICLK	
0008 B328h	SCI12	Status clear register	STCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B329h	SCI12	Control field 0 data register	CF0DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Ah	SCI12	Control field 0 compare enable register	CF0CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Bh	SCI12	Control field 0 receive data register	CF0RR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Ch	SCI12	Primary control field 1 data register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Dh	SCI12	Secondary control field 1 data register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Eh	SCI12	Control field 1 compare enable register	CF1CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Fh	SCI12	Control field 1 receive data register	CF1RR	8	8	2, 3 PCLKB	2 ICLK	
0008 B330h	SCI12	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B331h	SCI12	Timer mode register	TMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B332h	SCI12	Timer prescaler register	TPRE	8	8	2, 3 PCLKB	2 ICLK	
0008 B333h	SCI12	Timer count register	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C007h	PORT7	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C009h	PORT9	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Dh	PORTD	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C027h	PORT7	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C029h	PORT9	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (13/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Dh	PORTD	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C040h	PORT0	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C041h	PORT1	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C042h	PORT2	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C043h	PORT3	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C044h	PORT4	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C047h	PORT7	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C049h	PORT9	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Dh	PORTD	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C060h	PORT0	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C061h	PORT1	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C067h	PORT7	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C069h	PORT9	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C093h	PORT9	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C11Fh	MPC	Write-protect register	PWPR	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C140h	MPC	P00 pin function control register	P00PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C141h	MPC	P01 pin function control register	P01PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C148h	MPC	P10 pin function control register	P10PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C149h	MPC	P11 pin function control register	P11PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C152h	MPC	P22 pin function control register	P22PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C153h	MPC	P23 pin function control register	P23PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C154h	MPC	P24 pin function control register	P24PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C158h	MPC	P30 pin function control register	P30PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C159h	MPC	P31 pin function control register	P31PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C15Ah	MPC	P32 pin function control register	P32PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C15Bh	MPC	P33 pin function control register	P33PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C160h	MPC	P40 pin function control register	P40PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C161h	MPC	P41 pin function control register	P41PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C162h	MPC	P42 pin function control register	P42PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C163h	MPC	P43 pin function control register	P43PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C164h	MPC	P44 pin function control register	P44PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C165h	MPC	P45 pin function control register	P45PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C166h	MPC	P46 pin function control register	P46PFS	8	8	2, 3 PCLKB	2 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (14/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C167h	MPC	P47 pin function control register	P47PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C178h	MPC	P70 pin function control register	P70PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C179h	MPC	P71 pin function control register	P71PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Ah	MPC	P72 pin function control register	P72PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Bh	MPC	P73 pin function control register	P73PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Ch	MPC	P74 pin function control register	P74PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Dh	MPC	P75 pin function control register	P75PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Eh	MPC	P76 pin function control register	P76PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C189h	MPC	P91 pin function control register	P91PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C18Ah	MPC	P92 pin function control register	P92PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C18Bh	MPC	P93 pin function control register	P93PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C18Ch	MPC	P94 pin function select register	P94PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ABh	MPC	PD3 pin function control register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ACh	MPC	PD4 pin function control register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ADh	MPC	PD5 pin function control register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AEh	MPC	PD6 pin function control register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AFh	MPC	PD7 pin function control register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B2h	MPC	PE2 pin function control register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM
0008 C297h	SYSTEM	Voltage monitoring circuit control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption

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Table 4.1 List of I/O Registers (Address Order) (15/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C330h	ICU	Group 12 interrupt source register	GRP12	32	32	1, 2 PCLKB	2 ICLK	ICUb
0008 C370h	ICU	Group 12 interrupt enable register	GEN12	32	32	1, 2 PCLKB	2 ICLK	
0008 C4C0h	POE	Input level control/status register 1	ICSR1	16	8,16	2, 3 PCLKB	2 ICLK	POE3
0008 C4C2h	POE	Output level control/status register 1	OCSR1	16	8,16	2, 3 PCLKB	2 ICLK	
0008 C4C8h	POE	Input level control/status register 3	ICSR3	16	8,16	2, 3 PCLKB	2 ICLK	
0008 C4CAh	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK	
0008 C4CBh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C4CCh	POE	Port output enable control register 2	POECR2	16	16	2, 3 PCLKB	2 ICLK	
0008 C4CEh	POE	Port output enable control register 3	POECR3	16	16	2, 3 PCLKB	2 ICLK	
0008 C4D0h	POE	Port output enable control register 4	POECR4	16	16	2, 3 PCLKB	2 ICLK	
0008 C4D2h	POE	Port output enable control register 5	POECR5	16	16	2, 3 PCLKB	2 ICLK	
0008 C4D4h	POE	Port output enable control register 6	POECR6	16	16	2, 3 PCLKB	2 ICLK	
0008 C4D6h	POE	Input level control/status register 4	ICSR4	16	8, 16	2, 3 PCLKB	2 ICLK	
0008 C4D8h	POE	Input level control/status register 5	ICSR5	16	8, 16	2, 3 PCLKB	2 ICLK	
0008 C4DAh	POE	Active level register 1	ALR1	16	8, 16	2, 3 PCLKB	2 ICLK	
0008 C4DCh	POE	Input level control/status register 6	ICSR6	16	16	2, 3 PCLKB	2 ICLK	
000C 1200h	MTU3	Timer control register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3
000C 1201h	MTU4	Timer control register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1202h	MTU3	Timer mode register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1203h	MTU4	Timer mode register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1204h	MTU3	Timer I/O control register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1205h	MTU3	Timer I/O control register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1206h	MTU4	Timer I/O control register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1207h	MTU4	Timer I/O control register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1208h	MTU3	Timer interrupt enable register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1209h	MTU4	Timer interrupt enable register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 120Ah	MTU	Timer output master enable register A	TOERA	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 120Dh	MTU	Timer gate control register A	TGCRA	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 120Eh	MTU	Timer output control register 1A	TOCR1A	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 120Fh	MTU	Timer output control register 2A	TOCR2A	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1210h	MTU3	Timer counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1212h	MTU4	Timer counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1214h	MTU	Timer cycle data register A	TCDRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1216h	MTU	Timer dead time data register A	TDDRA	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1218h	MTU3	Timer general register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 121Ah	MTU3	Timer general register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 121Ch	MTU4	Timer general register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 121Eh	MTU4	Timer general register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1220h	MTU	Timer subcounter A	TCNTSA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1222h	MTU	Timer cycle buffer register A	TCBRA	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1224h	MTU3	Timer general register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1226h	MTU3	Timer general register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1228h	MTU4	Timer general register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 122Ah	MTU4	Timer general register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 122Ch	MTU3	Timer status register	TSR	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 122Dh	MTU4	Timer status register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1230h	MTU	Timer interrupt skipping set register 1A	TITCR1A	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1231h	MTU	Timer interrupt skipping counter 1A	TITCNT1A	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1232h	MTU	Timer buffer transfer set register A	TBTERA	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1234h	MTU	Timer dead time enable register A	TDERA	8	8	4, 5 PCLKA	2, 3 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (16/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1236h	MTU	Timer output level buffer register A	TOLBRA	8	8	4, 5 PCLKA	2, 3 ICLK	MTU3
000C 1238h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1239h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 123Ah	MTU	Timer interrupt skipping mode register A	TITMRA	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 123Bh	MTU	Timer interrupt skipping set register 2A	TITCR2A	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 123Ch	MTU	Timer interrupt skipping counter 2A	TITCNT2A	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1240h	MTU4	Timer A/D converter start request control register	TADCR	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1244h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1246h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1248h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 124Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1260h	MTU	Timer waveform control register A	TWCA	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1270h	MTU*1	Timer mode register 2A	TMDR2A	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1272h	MTU3	Timer general register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1274h	MTU4	Timer general register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1276h	MTU4	Timer general register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1280h	MTU	Timer start register A	TSTRA	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1281h	MTU	Timer synchronous register A	TSYRA	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1282h	MTU	Timer counter synchronous start register	TCSYSTR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1284h	MTU	Timer read/write enable register A	TRWERA	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1300h	MTU0	Timer control register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1301h	MTU0	Timer mode register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1302h	MTU0	Timer I/O control register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1303h	MTU0	Timer I/O control register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1304h	MTU0	Timer interrupt enable register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1305h	MTU0	Timer status register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1306h	MTU0	Timer counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1308h	MTU0	Timer general register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 130Ah	MTU0	Timer general register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 130Ch	MTU0	Timer general register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 130Eh	MTU0	Timer general register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1320h	MTU0	Timer general register E	TGRE	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1322h	MTU0	Timer general register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1324h	MTU0	Timer interrupt enable register 2	TIER2	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1325h	MTU0	Timer status register 2	TSR2	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1326h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1380h	MTU1	Timer control register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1381h	MTU1	Timer mode register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1382h	MTU1	Timer I/O control register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1384h	MTU1	Timer interrupt enable register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1385h	MTU1	Timer status register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1386h	MTU1	Timer counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1388h	MTU1	Timer general register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 138Ah	MTU1	Timer general register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1390h	MTU1	Timer input capture control register	TICCR	8	8	4, 5 PCLKA	2, 3 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (17/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1400h	MTU2	Timer control register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK	MTU3
000C 1401h	MTU2	Timer mode register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1402h	MTU2	Timer I/O control register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1404h	MTU2	Timer interrupt enable register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1405h	MTU2	Timer status register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1406h	MTU2	Timer counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1408h	MTU2	Timer general register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 140Ah	MTU2	Timer general register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A00h	MTU6	Timer control register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A01h	MTU7	Timer control register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A02h	MTU6	Timer mode register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1A03h	MTU7	Timer mode register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A04h	MTU6	Timer I/O control register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A05h	MTU6	Timer I/O control register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A06h	MTU7	Timer I/O control register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1A07h	MTU7	Timer I/O control register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A08h	MTU6	Timer interrupt enable register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1A09h	MTU7	Timer interrupt enable register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A0Ah	MTU	Timer output master enable register B	TOERB	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A0Eh	MTU	Timer output control register 1B	TOCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1A0Fh	MTU	Timer output control register 2B	TOCR2B	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A10h	MTU6	Timer counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A12h	MTU7	Timer counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A14h	MTU	Timer cycle data register B	TCDRB	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A16h	MTU	Timer dead time data register B	TDDRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A18h	MTU6	Timer general register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A1Ah	MTU6	Timer general register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A1Ch	MTU7	Timer general register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A1Eh	MTU7	Timer general register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A20h	MTU	Timer subcounter B	TCNTSB	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A22h	MTU	Timer cycle buffer register B	TCBRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A24h	MTU6	Timer general register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A26h	MTU6	Timer general register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A28h	MTU7	Timer general register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A2Ah	MTU7	Timer general register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A2Ch	MTU6	Timer status register	TSR	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1A2Dh	MTU7	Timer status register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A30h	MTU	Timer interrupt skipping set register 1B	TITCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1A31h	MTU	Timer interrupt skipping counter 1B	TITCNT1B	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A32h	MTU	Timer buffer transfer set register B	TBTERB	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A34h	MTU	Timer dead time enable register B	TDERB	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A36h	MTU	Timer output level buffer register B	TOLBRB	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A38h	MTU6	Timer buffer operation transfer mode register	TBTM	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1A39h	MTU7	Timer buffer operation transfer mode register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A3Ah	MTU	Timer interrupt skipping mode register B	TITMRB	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A3Bh	MTU	Timer interrupt skipping set register 2B	TITCR2B	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A3Ch	MTU	Timer interrupt skipping counter 2B	TITCNT2B	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A40h	MTU7	Timer A/D converter start request control register	TADCR	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A44h	MTU7	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (18/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1A46h	MTU7	Timer A/D converter start request cycle set register B	TADCORB	16	16	4, 5 PCLKA	2, 3 ICLK	MTU3
000C 1A48h	MTU7	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1A4Ah	MTU7	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A50h	MTU6	Timer synchronous clear register	TSYCR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A60h	MTU	Timer waveform control register B	TWCRB	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A70h	MTU	Timer mode register 2B	TMDR2B	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A72h	MTU6	Timer general register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A74h	MTU7	Timer general register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A76h	MTU7	Timer general register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1A80h	MTU	Timer start register B	TSTRB	8	8, 16	4, 5 PCLKA	2, 3 ICLK	
000C 1A81h	MTU	Timer synchronous register B	TSYRB	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1A84h	MTU	Timer read/write enable register B	TRWERB	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1C80h	MTU5	Timer counter U	TCNTU	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1C82h	MTU5	Timer general register U	TGRU	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1C84h	MTU5	Timer control register U	TCRU	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1C86h	MTU5	Timer I/O control register U	TIORU	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1C90h	MTU5	Timer counter V	TCNTV	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1C92h	MTU5	Timer general register V	TGRV	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1C94h	MTU5	Timer control register V	TCRV	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1C96h	MTU5	Timer I/O control register V	TIORV	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1CA0h	MTU5	Timer counter W	TCNTW	16	16, 32	4, 5 PCLKA	2, 3 ICLK	
000C 1CA2h	MTU5	Timer general register W	TGRW	16	16	4, 5 PCLKA	2, 3 ICLK	
000C 1CA4h	MTU5	Timer control register W	TCRW	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1CA6h	MTU5	Timer I/O control register W	TIORW	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1CB0h	MTU5	Timer status register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1CB2h	MTU5	Timer interrupt enable register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1CB4h	MTU5	Timer start register	TSTR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 1CB6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	4, 5 PCLKA	2, 3 ICLK	
000C 2000h	GPT	General PWM timer software start register	GTSTR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	GPT
000C 2004h	GPT	General PWM timer hardware source start control register	GTHSCR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2006h	GPT	General PWM timer hardware source clear control register	GTHCCR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2008h	GPT	General PWM timer hardware start source select register	GTHSSR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 200Ah	GPT	General PWM timer hardware stop/clear source select register	GTHPSR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 200Ch	GPT	General PWM timer write-protection register	GTWP	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 200Eh	GPT	General PWM timer sync register	GTSYNC	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2010h	GPT	General PWM timer external trigger input interrupt register	GTETINT	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2014h	GPT	General PWM timer buffer operation disable register	GTBDR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2018h	GPT	General PWM timer start write-protection register	GTSWP	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2080h	GPT	LOCO count control register	LCCR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2082h	GPT	LOCO count status register	LCST	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2084h	GPT	LOCO count value register	LCNT	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2086h	GPT	LOCO count result average register	LCNTA	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2088h	GPT	LOCO count result register 0	LCNT00	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 208Ah	GPT	LOCO count result register 1	LCNT01	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (19/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
000C 208Ch	GPT	LOCO count result register 2	LCNT02	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	GPT
000C 208Eh	GPT	LOCO count result register 3	LCNT03	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2090h	GPT	LOCO count result register 4	LCNT04	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2092h	GPT	LOCO count result register 5	LCNT05	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2094h	GPT	LOCO count result register 6	LCNT06	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2096h	GPT	LOCO count result register 7	LCNT07	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
'000C 2098h	GPT	LOCO count result register 8	LCNT08	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 209Ah	GPT	LOCO count result register 9	LCNT09	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 209Ch	GPT	LOCO count result register 10	LCNT10	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 209Eh	GPT	LOCO count result register 11	LCNT11	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 20A0h	GPT	LOCO count result register 12	LCNT12	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 20A2h	GPT	LOCO count result register 13	LCNT13	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 20A4h	GPT	LOCO count result register 14	LCNT14	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 20A6h	GPT	LOCO count result register 15	LCNT15	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 20A8h	GPT	LOCO count upper permissible deviation register	LCNTDU	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 20AAh	GPT	LOCO count lower permissible deviation register	LCNTDL	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2100h	GPT0	General PWM timer I/O control register	GTIOR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2102h	GPT0	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2104h	GPT0	General PWM timer control register	GTCR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2106h	GPT0	General PWM timer buffer enable register	GTBER	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2108h	GPT0	General PWM timer count direction register	GTUDC	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 210Ah	GPT0	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 210Ch	GPT0	General PWM timer status register	GTST	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 210Eh	GPT0	General PWM timer counter	GTCNT	16	16	2, 5 PCLKA	2, 3 ICLK	
000C 2110h	GPT0	General PWM timer compare capture register A	GTCCRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2112h	GPT0	General PWM timer compare capture register B	GTCCRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2114h	GPT0	General PWM timer compare capture register C	GTCCRC	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2116h	GPT0	General PWM timer compare capture register D	GTCCRD	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2118h	GPT0	General PWM timer compare capture register E	GTCCRE	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 211Ah	GPT0	General PWM timer compare capture register F	GTCCRF	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 211Ch	GPT0	General PWM timer cycle setting register	GTPR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 211Eh	GPT0	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2120h	GPT0	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2124h	GPT0	A/D converter start request timing register A	GTADTRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2126h	GPT0	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2128h	GPT0	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 212Ch	GPT0	A/D converter start request timing register B	GTADTRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 212Eh	GPT0	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2130h	GPT0	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (20/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
000C 2134h	GPT0	General PWM timer output negate control register	GTONCR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	GPT
000C 2136h	GPT0	General PWM timer dead time control register	GTDTCR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2138h	GPT0	General PWM timer dead time value register U	GTDVU	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 213Ah	GPT0	General PWM timer dead time value register D	GTDVD	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 213Ch	GPT0	General PWM timer dead time buffer register U	GTDBU	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 213Eh	GPT0	General PWM timer dead time buffer register D	GTDBD	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2140h	GPT0	General PWM timer output protection function status register	GTSOS	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2142h	GPT0	General PWM timer output protection function temporary release register	GTSOTR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2180h	GPT1	General PWM timer I/O control register	GTIOR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2182h	GPT1	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2184h	GPT1	General PWM timer control register	GTCR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2186h	GPT1	General PWM timer buffer enable register	GTBER	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2188h	GPT1	General PWM timer count direction register	GTUDC	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 218Ah	GPT1	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 218Ch	GPT1	General PWM timer status register	GTST	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 218Eh	GPT1	General PWM timer counter	GTCNT	16	16	2, 5 PCLKA	2, 3 ICLK	
000C 2190h	GPT1	General PWM timer compare capture register A	GTCCRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2192h	GPT1	General PWM timer compare capture register B	GTCCRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2194h	GPT1	General PWM timer compare capture register C	GTCCRC	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2196h	GPT1	General PWM timer compare capture register D	GTCCRD	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2198h	GPT1	General PWM timer compare capture register E	GTCCRE	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 219Ah	GPT1	General PWM timer compare capture register F	GTCCRF	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 219Ch	GPT1	General PWM timer cycle setting register	GTPR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 219Eh	GPT1	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21A0h	GPT1	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21A4h	GPT1	A/D converter start request timing register A	GTADTRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21A6h	GPT1	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21A8h	GPT1	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21ACh	GPT1	A/D converter start request timing register B	GTADTRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21AEh	GPT1	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21B0h	GPT1	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21B4h	GPT1	General PWM timer output negate control register	GTONCR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21B6h	GPT1	General PWM timer dead time control register	GTDTCR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21B8h	GPT1	General PWM timer dead time value register U	GTDVU	16	16, 32	2, 5 PCLKA	2, 3 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (21/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
000C 21BAh	GPT1	General PWM timer dead time value register D	GTDVD	16	16, 32	2, 5 PCLKA	2, 3 ICLK	GPT
000C 21BCh	GPT1	General PWM timer dead time buffer register U	GTDBU	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21BEh	GPT1	General PWM timer dead time buffer register D	GTDBD	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21C0h	GPT1	General PWM timer output protection function status register	GTSOS	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 21C2h	GPT1	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2200h	GPT2	General PWM timer I/O control register	GTIOR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2202h	GPT2	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2204h	GPT2	General PWM timer control register	GTCR	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2206h	GPT2	General PWM timer buffer enable register	GTBER	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2208h	GPT2	General PWM timer count direction register	GTUDC	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 220Ah	GPT2	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 220Ch	GPT2	General PWM timer status register	GTST	16	8, 16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 220Eh	GPT2	General PWM timer counter	GTCNT	16	16	2, 5 PCLKA	2, 3 ICLK	
000C 2210h	GPT2	General PWM timer compare capture register A	GTCCRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2212h	GPT2	General PWM timer compare capture register B	GTCCRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2214h	GPT2	General PWM timer compare capture register C	GTCCRC	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2216h	GPT2	General PWM timer compare capture register D	GTCCRD	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2218h	GPT2	General PWM timer compare capture register E	GTCCRE	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 221Ah	GPT2	General PWM timer compare capture register F	GTCCRF	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 221Ch	GPT2	General PWM timer cycle setting register	GTPR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 221Eh	GPT2	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2220h	GPT2	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2224h	GPT2	A/D converter start request timing register A	GTADTRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2226h	GPT2	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2228h	GPT2	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 222Ch	GPT2	A/D converter start request timing register B	GTADTRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 222Eh	GPT2	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2230h	GPT2	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
000C 2234h	GPT2	General PWM timer output negate control register	GTONCR	16	16, 32	2, 5 PCLKA	2, 3 ICLK	
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 FCLK	2, 3 ICLK	ROM, E2 DataFlash Memory
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 FCLK	2, 3 ICLK	
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 FCLK	2, 3 ICLK	
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 FCLK	2, 3 ICLK	ROM
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory
007F C450h	FLASH	E^2 DataFlash programming/erasure enable register 0	DFLWE0	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 FCLK	2, 3 ICLK	ROM
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 FCLK	2, 3 ICLK	

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Table 4.1 List of I/O Registers (Address Order) (22/22)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name
						ICLK ≥ PCLK	ICLK < PCLK	
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 FCLK	2, 3 ICLK	ROM, E2 DataFlash Memory
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2, 3 FCLK	2, 3 ICLK	ROM
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFCAh	FLASH	E2 DataFlash blank check control register	DFLBCCNT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 FCLK	2, 3 ICLK	ROM
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 FCLK	2, 3 ICLK	ROM

○: Available, ×: Not available

Note 1. MTUA indicates registers shared by the MTU3 and MTU4.
Note 2. MTU indicates registers shared by the MTU0 to MTU7.
Note 3. MTUB indicates registers shared by the MTU6 and MTU7.

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5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant and port 4) *1	Vin	–0.3 to VCC+0.3	V
Input voltage (port 4)	Vin	–0.3 to AVCC0+0.3	V
Input voltage (ports for 5 V tolerant)*1	Vin	–0.3 to +5.8	V
Analog power supply voltage	AVCC0*2	–0.3 to +4.6	V
Reference power supply voltage	VREFH0*2	–0.3 to AVCC0+0.3	V
Analog input voltage (port 4)	V_{AN}	–0.3 to AVCC0+0.3	V
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, D, and E are 5 V tolerant.

Note 2. When the A/D converter is not in use, do not leave the AVCC0, VREFH0, VREFL0, and AVSS0 pins open. Connect the AVCC0 and VREFH0 pins to VCC, and the AVSS0 and VREFL0 pins to VSS, respectively.

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5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin GPT input pin RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (IICBus operating)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Port 4 (also used as an analog port)	V_{IH}	AVCC0 × 0.8	—	AVCC0 + 0.3		
		V_{IL}	–0.3	—	AVCC0×0.2		
	Ports for 5 V tolerant*1	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3		
	EXTAL, TCK, RSPI input pin		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus operating)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, TCK, RSPI input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus operating)		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Ports 4 and PE2	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0V, V_{in} = VCC
Three-state leakage current (off state)	Ports for 5V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0V, V_{in} = 5.5 V
			—	—	5.0		
Input capacitance	All input pins (except for ports PB1 and PB2)	C_{in}	—	—	15	pF	V_{in} = 0V, f = 1 MHz, T_a = 25ºC
	Ports PB1 and PB2		—	—	30		

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, D, and E are 5 V tolerant.

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Table 5.3 DC Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	During operation	Max. *2	I_{CC}*3	—	—	60	mA	ICLK = 100MHz PCLKA = 100MHz PCLKB = 50MHz PCLKD = 50MHz FCLK = 50MHz
		Normal *4		—	25	—		
		Increased by BGO operation*5		—	15	—		
	Sleep mode				25	35		
	All-module-clock-stop mode*6				14	25		
	During standby	Software standby mode		—	0.2	6	mA	
		Deep software standby mode		—	16	40	µA	
Analog power supply current	During 12-bit A/D conversion (sample & hold circuit in use)		AI_{CC0}	—	3	4	mA	
	During 12-bit A/D conversion (sample & hold circuit not in use)			—	2	3	mA	
	Window comparator (1-channel operation)				0.4	1	mA	
	Window comparator (6-channel operation)			—	0.5	1	mA	
	Waiting for 12-bit AD conversion			—	25	32	µA	
Reference power supply current	During 12-bit A/D conversion		AI_{REFH0}	—	0.6	0.7	mA	
	Waiting for 12-bit A/D conversion			—	0.6	0.7	mA	
VCC rising gradient			SrVcc	—	—	20000	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max = 0.87 × f + 13 (Max)
ICC typ = 0.35 × f + 5 (Normal)
ICC max = 0.48 × f + 12 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.
Note 6. The values are for reference.

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Table 5.4 Permissible Output Currents

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	I_{OL}	—	—	2.0*1	mA
Permissible output low current (max. value per pin)	I_{OL}	—	—	4.0*1	mA
Permissible output low current (total)	ΣI_{OL}	—	—	32	mA
Permissible output high current (average value per pin)	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (max. value per pin)	$-I_{OH}$	—	—	4.0	mA
Permissible output high current (total)	$\Sigma-I_{OH}$	—	—	32	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.
Note 1. RIIC pin: IOL = 6 mA (max.)

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5.3 AC Characteristics

Table 5.5 Operation Frequency Value

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock PCLK		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	Flash clock (FCLK)		—*1	—	50	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

5.3.1 Clock Timing

Table 5.6 Clock Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 5.1
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f_{MAIN}	4	—	16	MHz	
Main clock oscillation stabilization time (crystal)		$t_{MAINOSC}$	10	—	—	ms	Figure 5.2
Main clock oscillation stabilization wait time (crystal)		$t_{MAINOSCWT}$	20	—	—	ms	
LOCO clock cycle time		t_{cyc}	6.96	8	9.4	µs	
Low-speed clock oscillator oscillation frequency		f_{LOCO}	106.25	125	143.75	kHz	
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.2
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.4
PLL clock oscillation stabilization wait time		t_{PLLWT1}	1.5	—	—	ms	
PLL clock oscillation stabilization time PLL	PLL operation started before main clock oscillation has settled	t_{PLL2}	10	—	—	ms	Figure 5.5
PLL clock oscillation stabilization wait time		t_{PLLWT2}	11	—	—	ms	

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).

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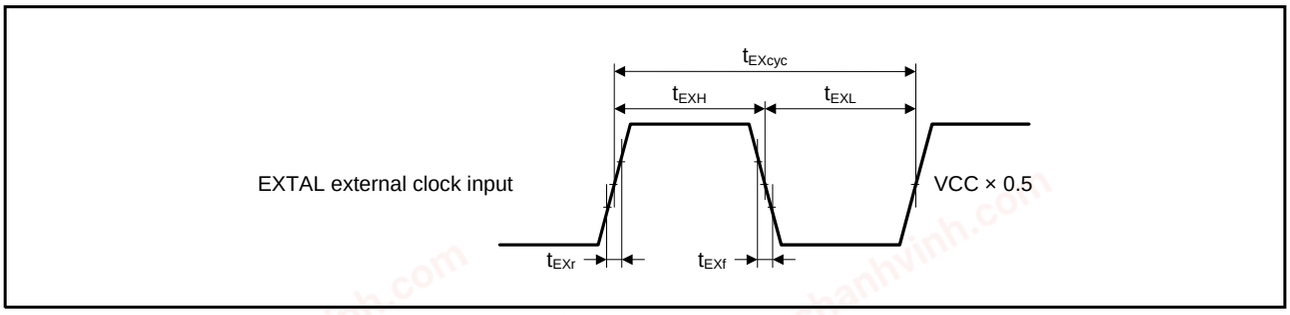


Figure 5.1 EXTAL External Clock Input Timing

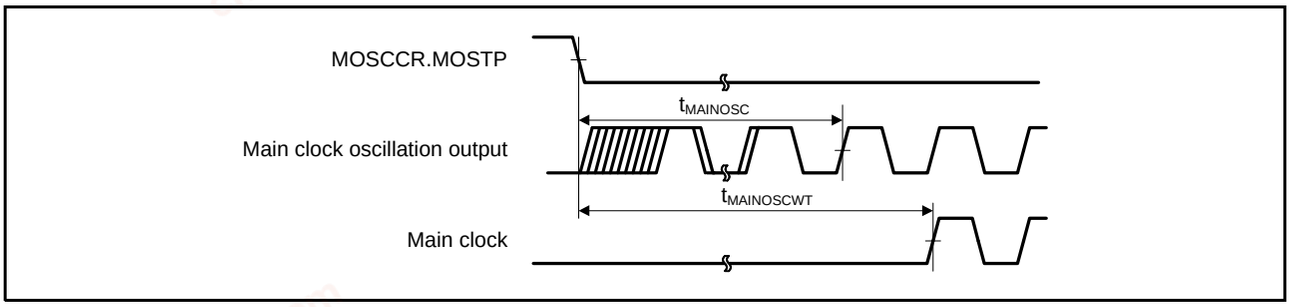


Figure 5.2 Main Clock Oscillation Start Timing

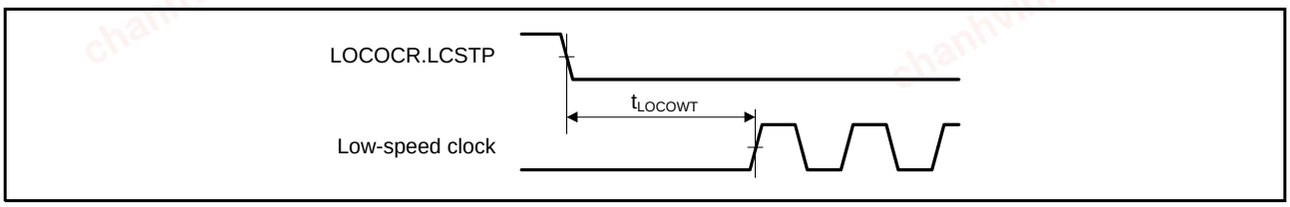


Figure 5.3 LOCO Clock Oscillation Start Timing

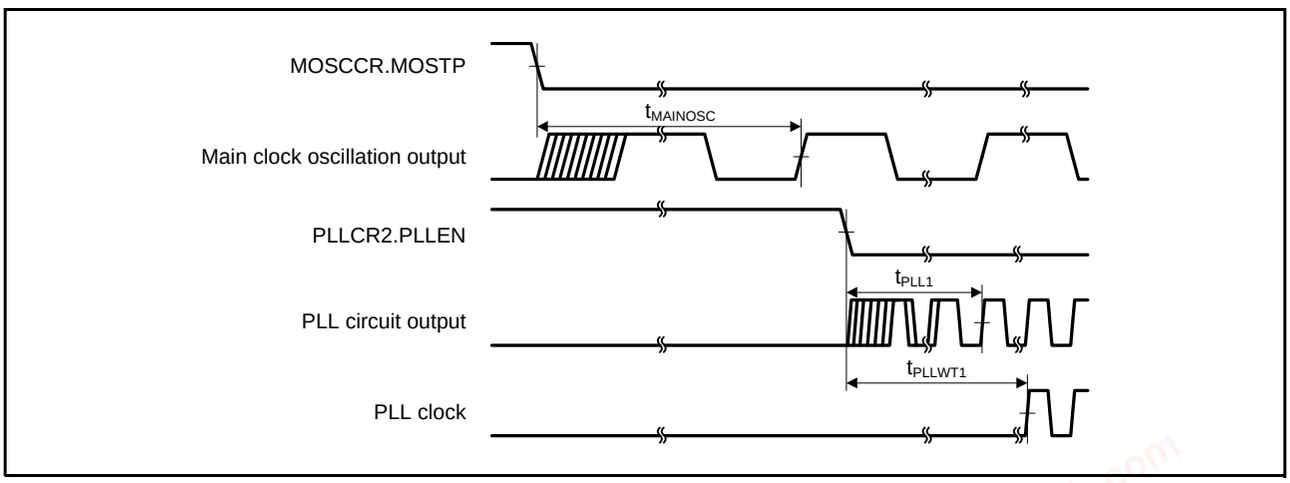


Figure 5.4 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

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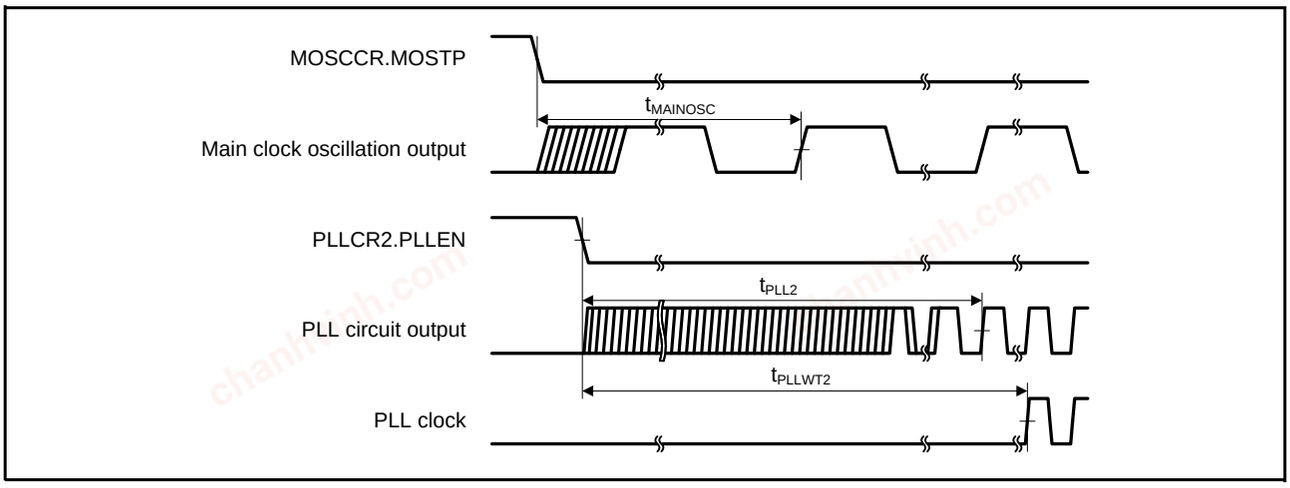


Figure 5.5 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

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5.3.2 Reset Timing

Table 5.7 Reset Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2	—	—	ms	Figure 5.6
	Deep software standby mode	t_{RESWD}	1	—	—	ms	Figure 5.7
	Software standby mode	t_{RESWS}	1	—	—	ms	
	Other than above (except for programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory)	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	59	—	60	t_{cyc}	
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	112	—	120	t_{cyc}	

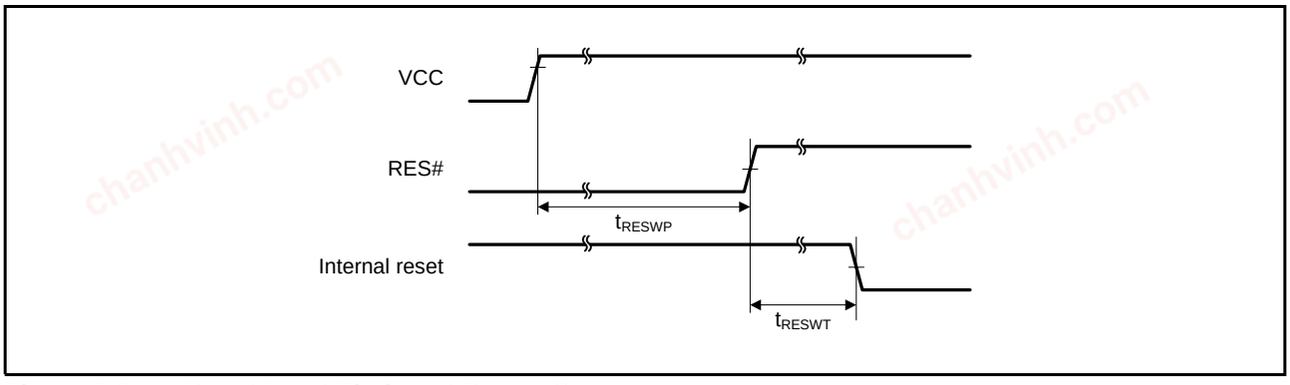


Figure 5.6 Reset Input Timing at Power-On

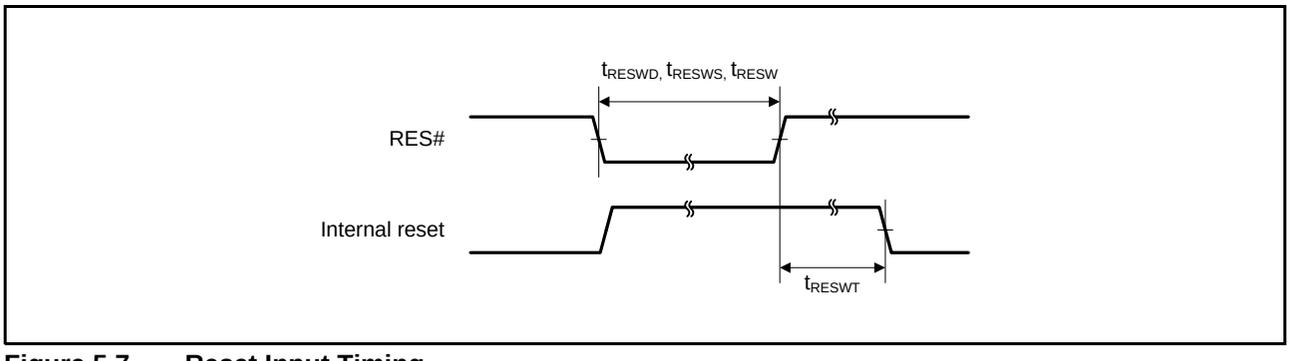


Figure 5.7 Reset Input Timing

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5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.8 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 5.8
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Low-speed clock oscillator or IWDT-specific low-speed clock oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1	ms	Figure 5.9
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

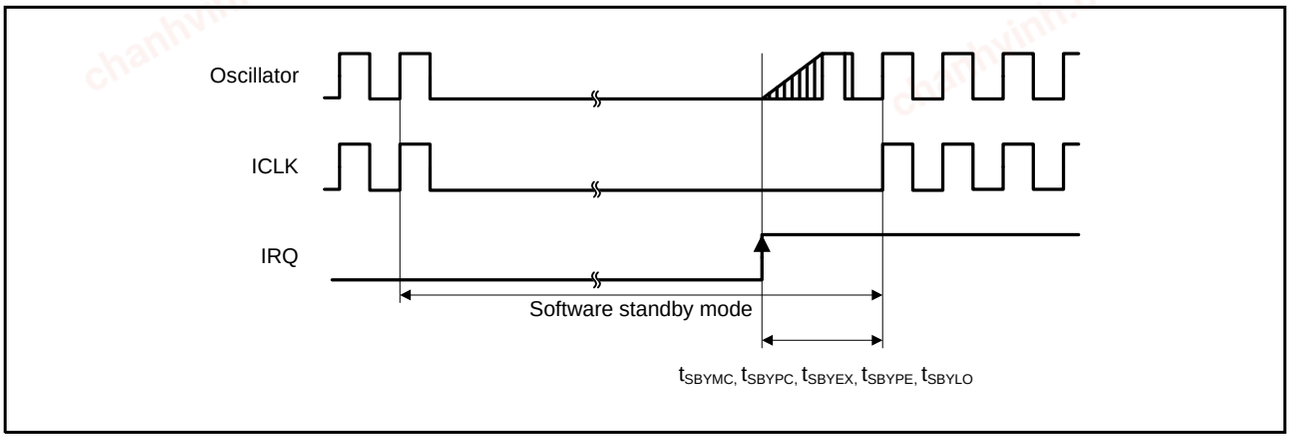


Figure 5.8 Software Standby Mode Cancellation Timing

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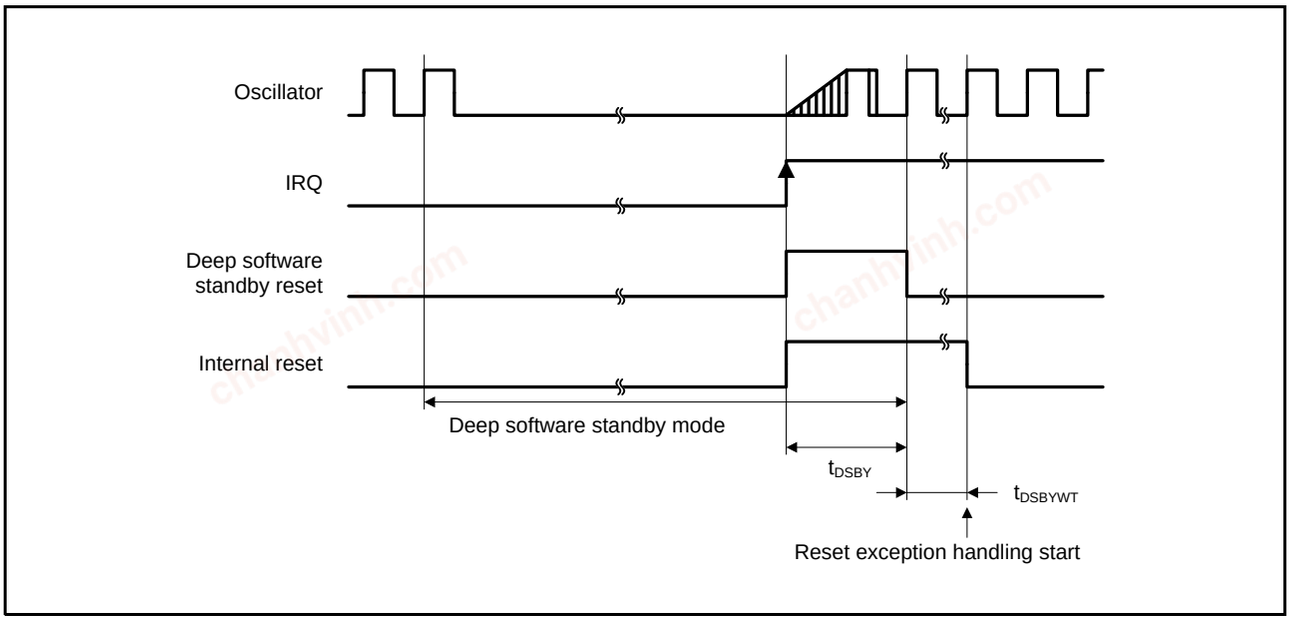


Figure 5.9 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.9 Control Signal Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 5.10
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 5.10
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 5.11
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 5.11

Note 1. t_{Pcyc}: PCLK cycle

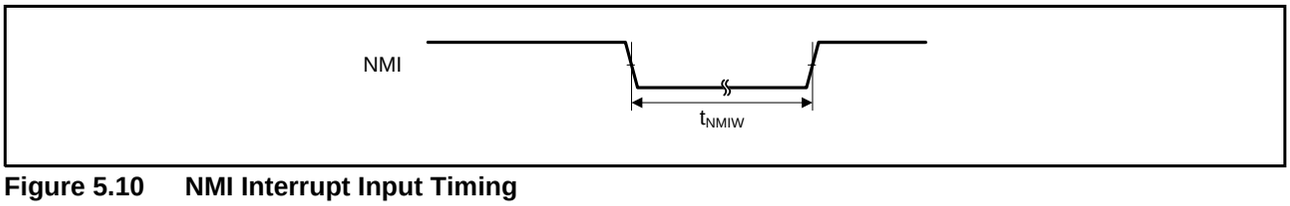


Figure 5.10 NMI Interrupt Input Timing

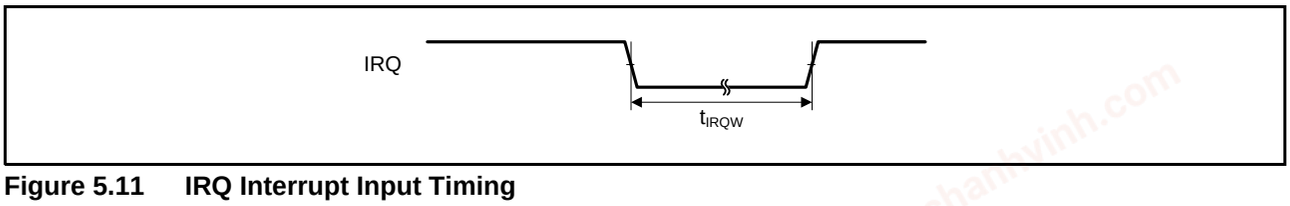


Figure 5.11 IRQ Interrupt Input Timing

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5.3.5 Timing of On-Chip Peripheral Modules

Table 5.10 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.12
MTU3	Input capture input pulse width	Single-edge setting	t_{TICW}	3	—	t_{PAcyc}	Figure 5.13
		Both-edge setting		5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	3	—	t_{PAcyc}	Figure 5.14
		Both-edge setting		5	—		
		Phase counting mode		5	—		
POE3	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.16
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	3	—	t_{PAcyc}	Figure 5.15
		Both-edge setting		5	—		
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.17
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	Figure 5.18
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
A/D converter	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.19

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcye}: ACLKA cycle

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Table 5.11 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 5.20
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output	t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input		—	1	µs	
	Data input setup time	Master	t_{SU}	15	—	ns	Figure 5.21 to Figure 5.24
				20	—		
		Slave		$20 - t_{Pcyc}$	—		
	Data input hold time	Master	t_H	0	—	ns	
		Slave		$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	—	18	ns	
		Slave		—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$	—		
	MOSI rise/fall time	Output	t_{MODR}, t_{MODF}	—	5	ns	
		Input		—	1	µs	
	MISO rise/fall time	Output	t_{MODR}, t_{MODF}	—	5	ns	
		Input		—	1	µs	
	SSL rise/fall time	Output	t_{SPCKR}, t_{SPCKF}	—	15	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	4	t_{Pcyc}	Figure 5.23 and Figure 5.24
	Slave output release time		t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

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Table 5.12 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.20
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKR}, t_{SPCKF}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	Figure 5.21 to Figure 5.24
	Data input hold time	t_{H}	40	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	10	—	ns	
	Data rise/fall time	t_{DR}, t_{DF}	—	20	ns	
	SS input rise/fall time	t_{SSLR}, t_{SSLF}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 5.23 and Figure 5.24
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

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Table 5.13 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 5.25
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc}: RIIC internal reference clock (IICϕ) Cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

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Table 5.14 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDAinput rise time	t_{Sr}	—	1000	ns	Figure 5.25
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

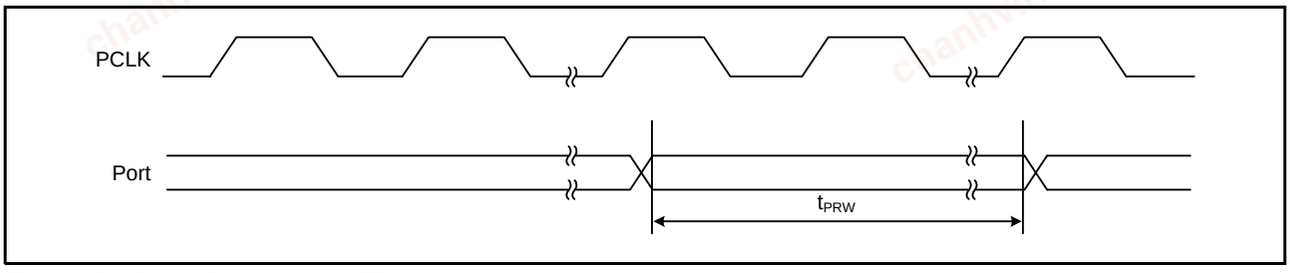


Figure 5.12 I/O port Input Timing

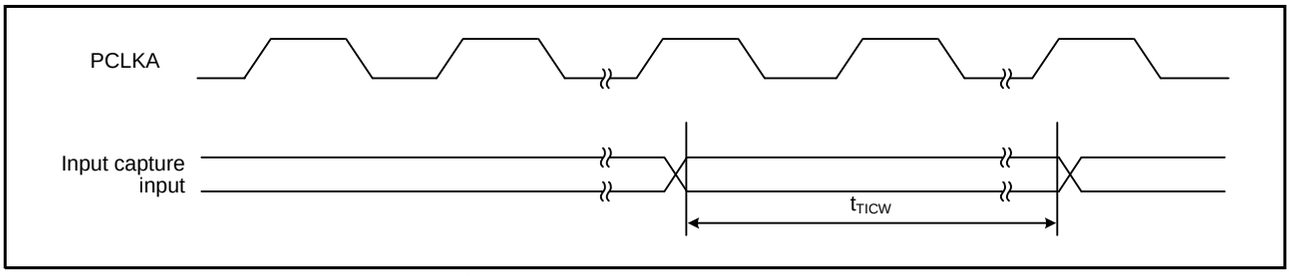


Figure 5.13 MTU Input/Output Timing

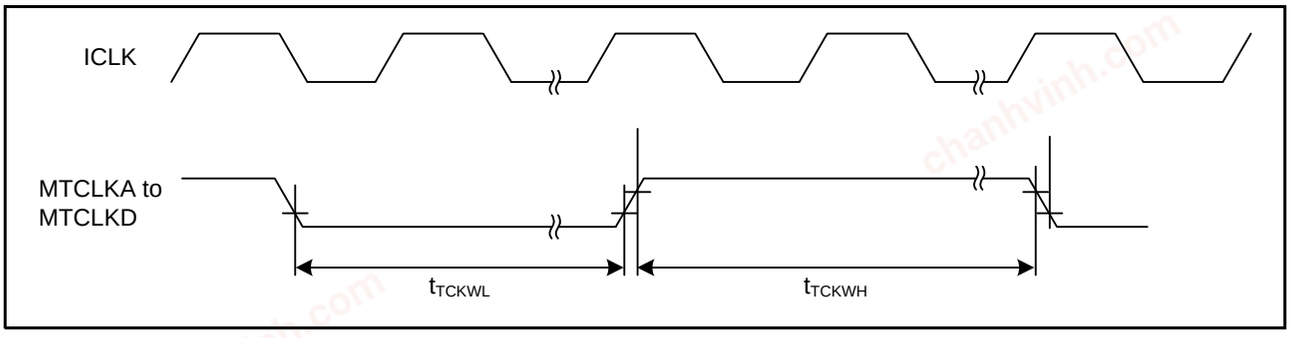


Figure 5.14 MTU Clock Input Timing

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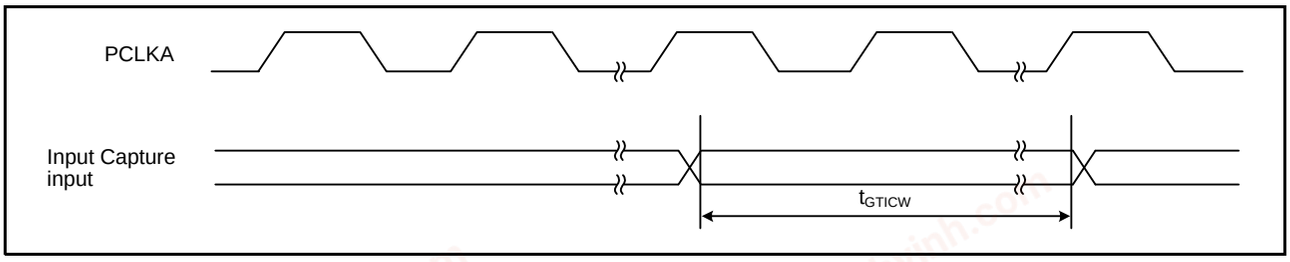


Figure 5.15 GPT Input/Output Timing

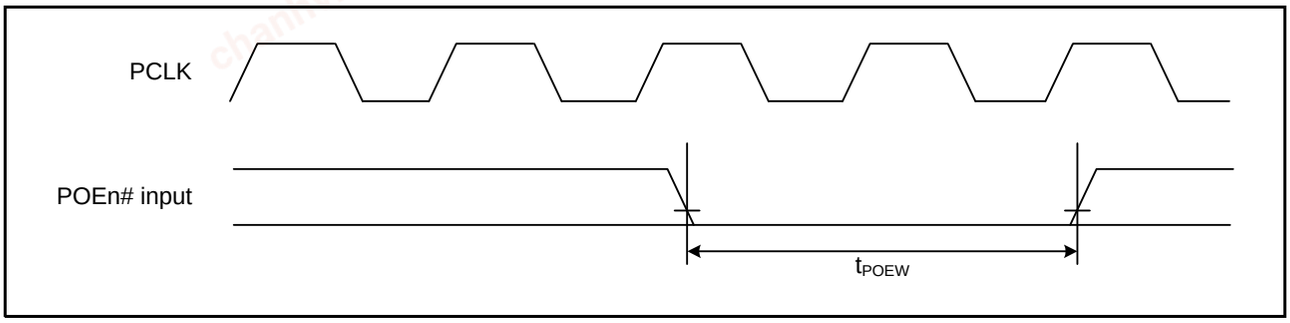


Figure 5.16 POE3# Input Timing

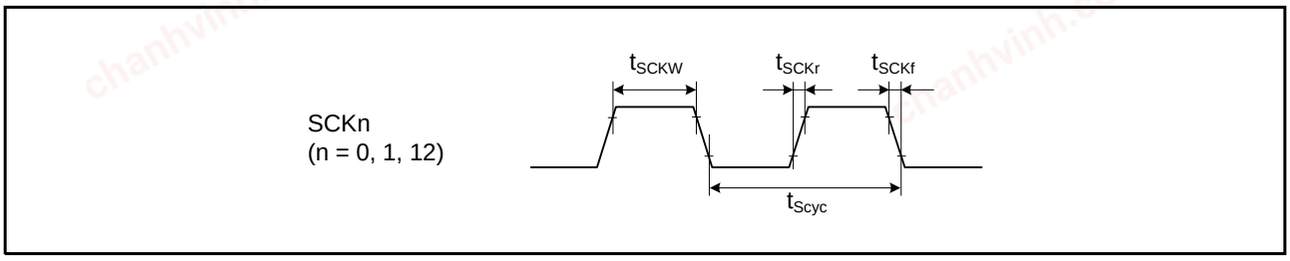


Figure 5.17 SCK Clock Input Timing

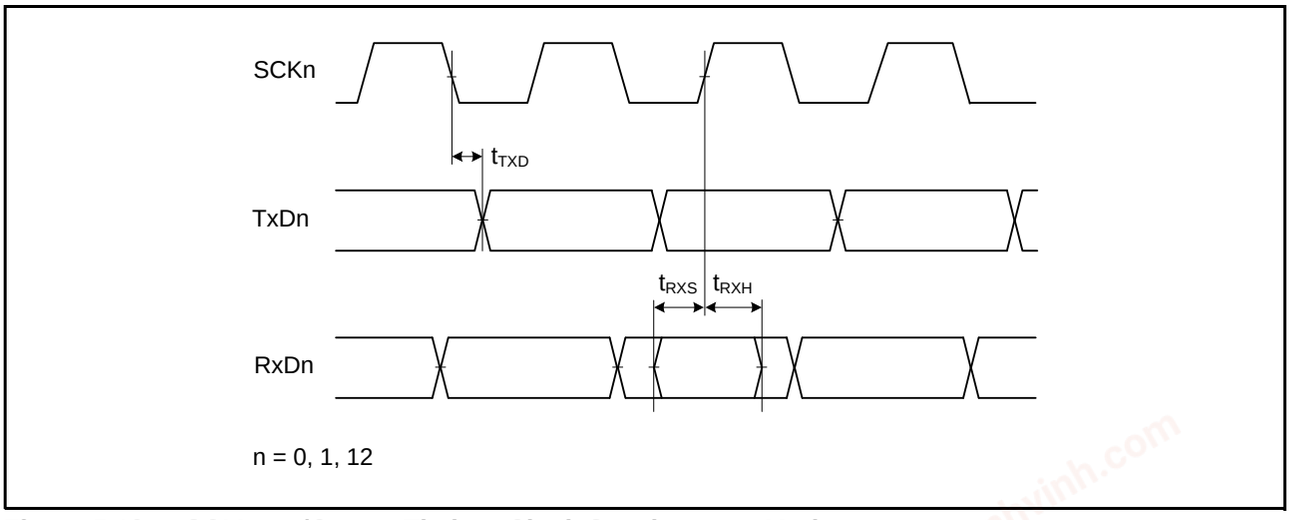


Figure 5.18 SCI Input/Output Timing: Clock Synchronous Mode

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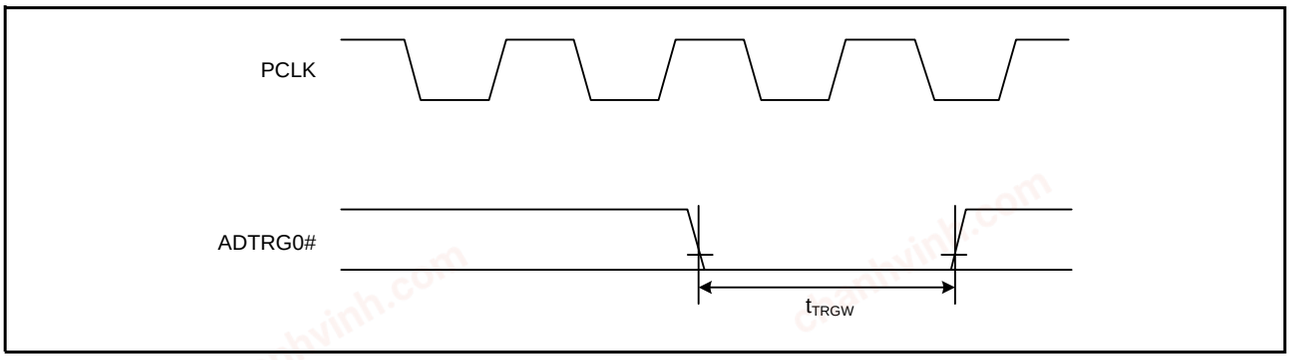


Figure 5.19 AD Converter External Trigger Input Timing

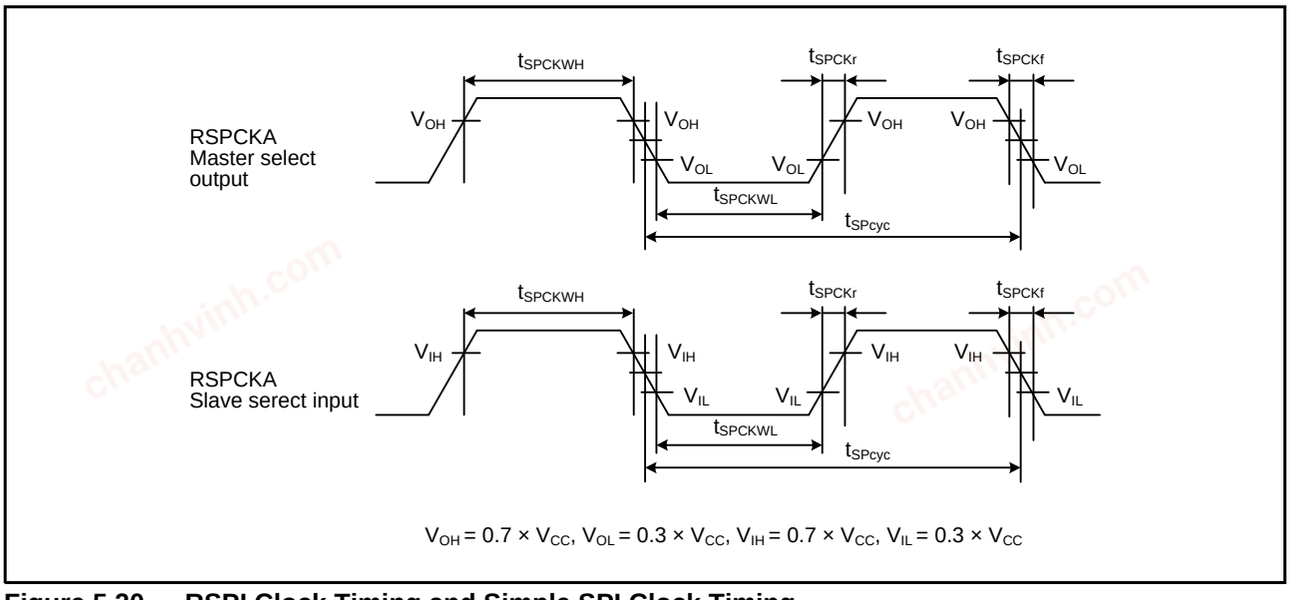


Figure 5.20 RSPI Clock Timing and Simple SPI Clock Timing

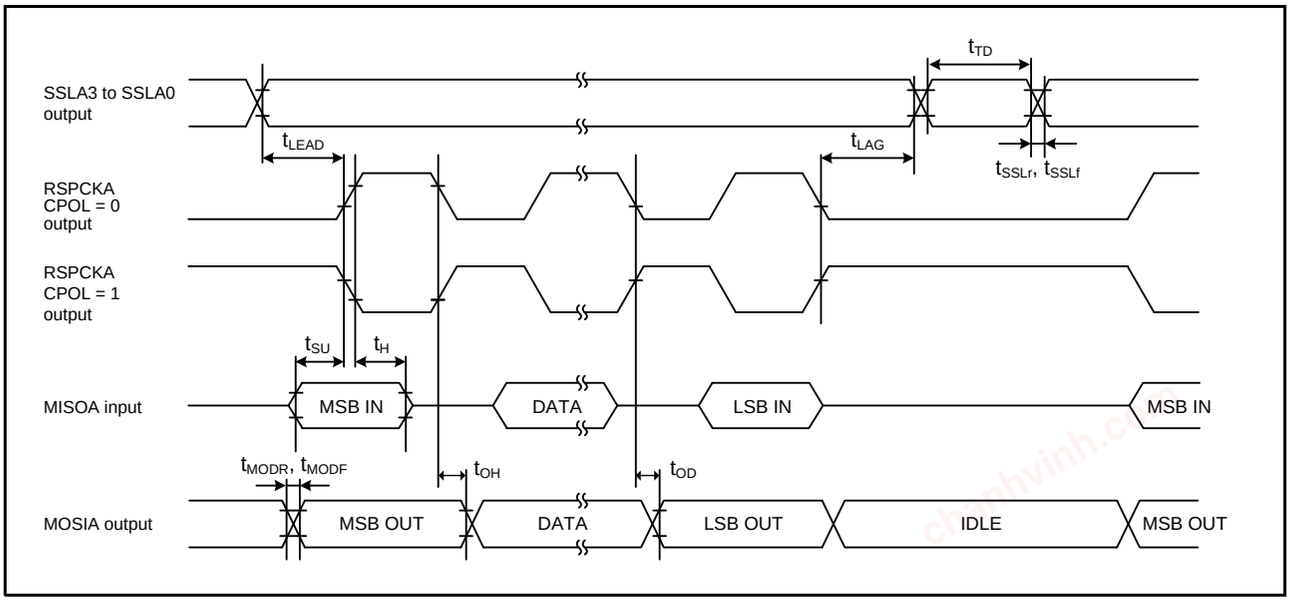


Figure 5.21 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

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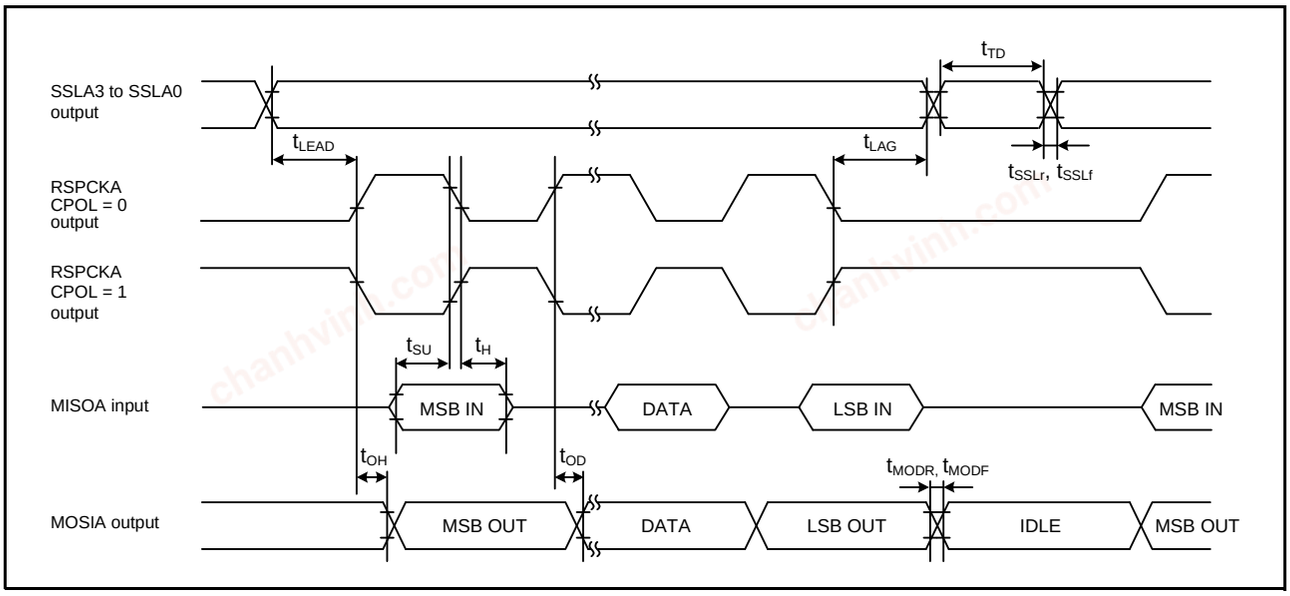


Figure 5.22 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

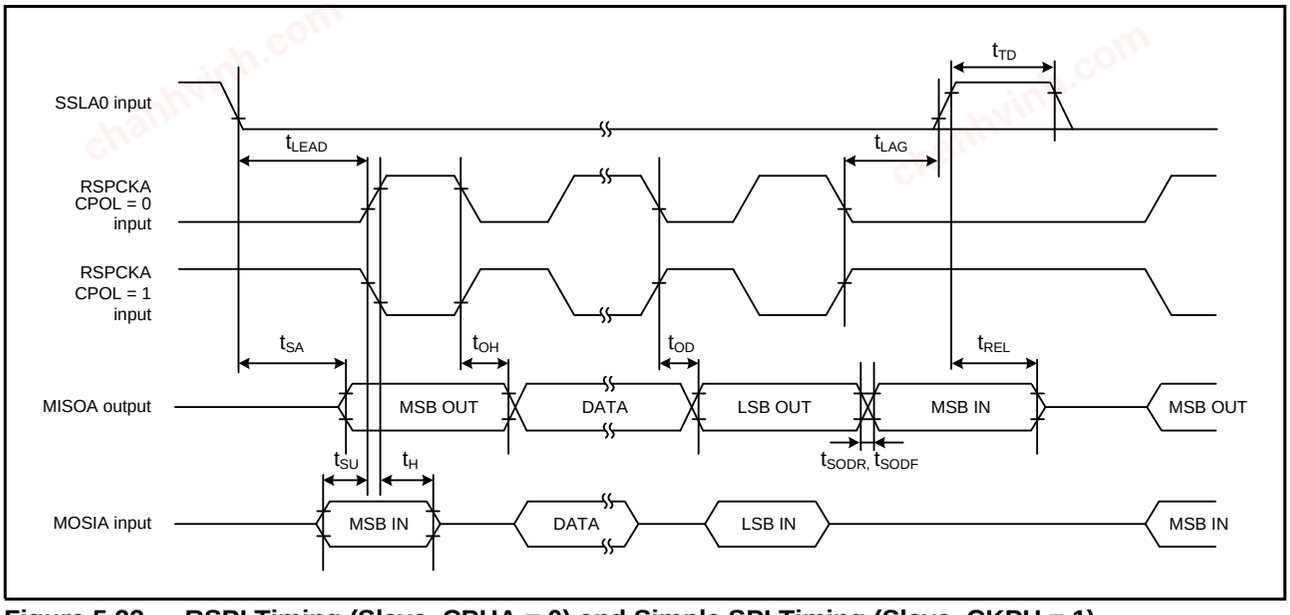


Figure 5.23 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

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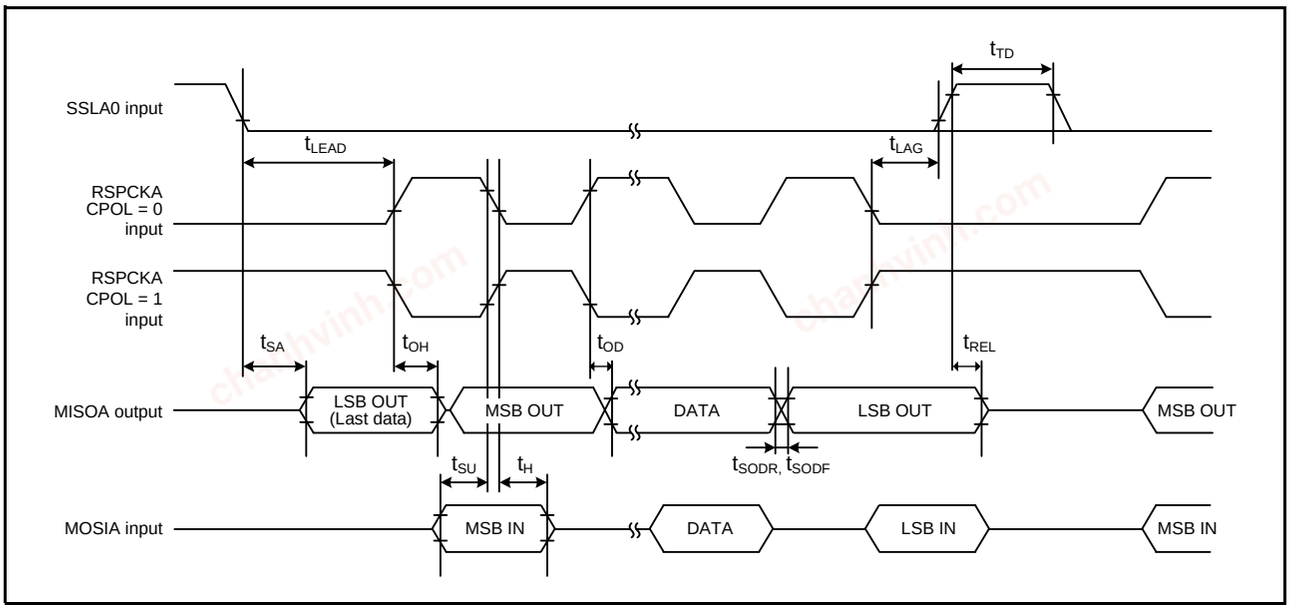
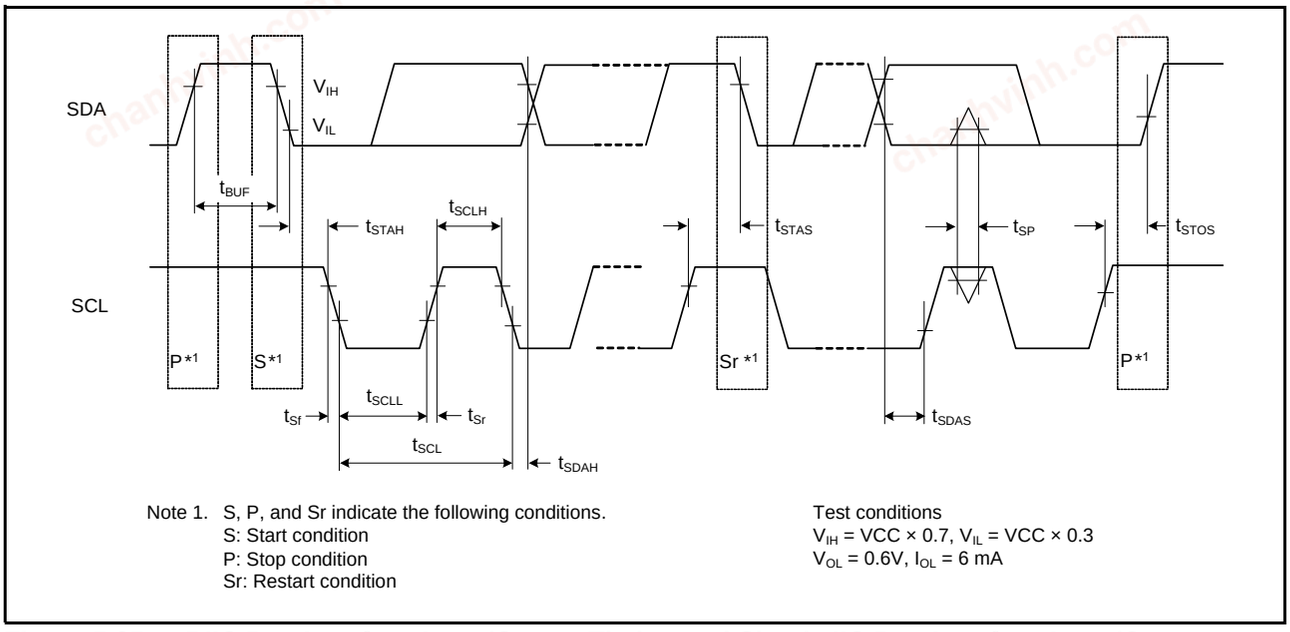


Figure 5.24 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6V, I_{OL} = 6 mA

Figure 5.25 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

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5.4 A/D Conversion Characteristics

Table 5.15 12-Bit A/D Conversion Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		min	typ	max	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time *1 (ADCLK = 50 MHz)	When the sample-and-hold circuit is in use per pin	1.6	—	—	µs	Sampling by the sample-and-hold circuit in 30 states. Sampling by the A/D converter in 20 states.
	When the sample-and-hold circuit is not in use per pin	1.0	—	—	µs	Sampling by the A/D converter in 20 states.
Analog input capacitance		—	—	6	pF	
Integral nonlinearity error		—	—	±4.0	LSB	
Offset error		—	—	±7.5	LSB	
Full-scale error		—	—	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample and hold circuit in use	—	—	±8.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Sample and hold circuit not in use	—	—	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		—	—	3.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.16 Comparator Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min	Typ	Max.	Unit	Test Conditions
Analog input capacitance	Cin	—	—	6	pF	
REFH pin offset voltage	Voff	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	Vin	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	tCR	—	—	0.5	µs	
REFL reply time	tCF	—	—	0.5	µs	

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5.5 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.17 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.5	2.6	2.7	V	Figure 5.26
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.8	2.9		Figure 5.27
	Voltage detection circuit (LVD1)	V_{DER1}	2.80	2.95	3.10		
	Voltage detection circuit (LVD2)	V_{DET2}	2.80	2.95	3.10		
Internal reset time	Power-on reset (POR)	t_{POR}	—	4.6		ms	Figure 5.26
	Voltage detection circuit (LVD0)	t_{LVD0}	—	4.6			Figure 5.27
	Voltage detection circuit (LVD1)	t_{LVD1}	—	0.9			Figure 5.28
	Voltage detection circuit (LVD2)	t_{LVD2}	—	0.9			Figure 5.29
Minimum VCC down time*1		t_{VOFF}	200	—	—	µs	Figure 5.26, Figure 5.27
Response delay time		t_{det}			200	µs	Figure 5.26 to Figure 5.29
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.28 Figure 5.29
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

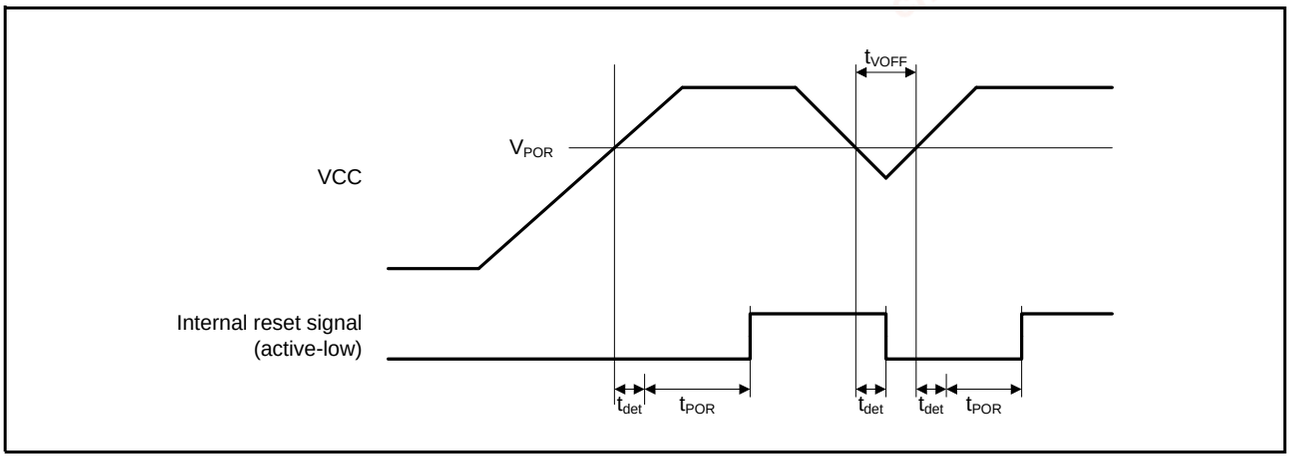


Figure 5.26 Power-on Reset Timing

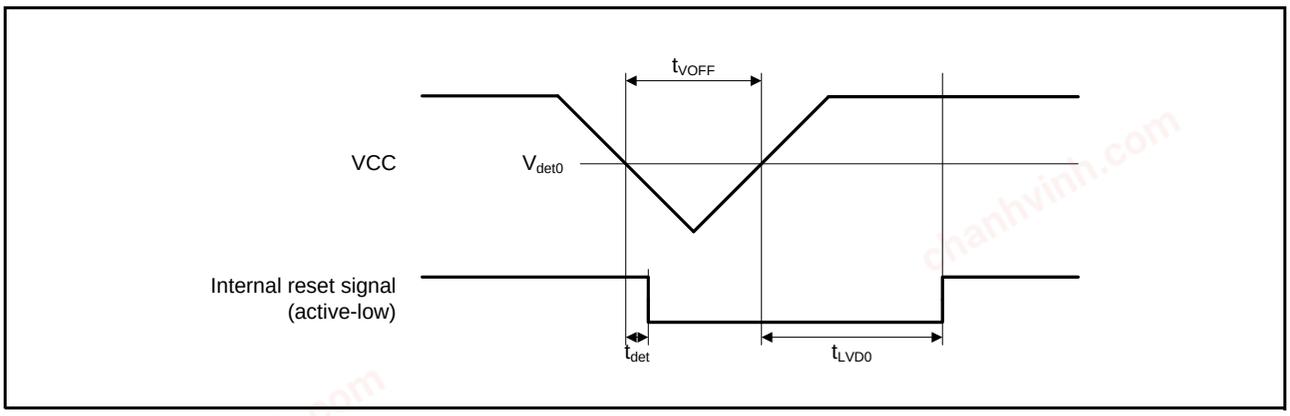


Figure 5.27 Voltage Detection Circuit Timing (V_{det0})

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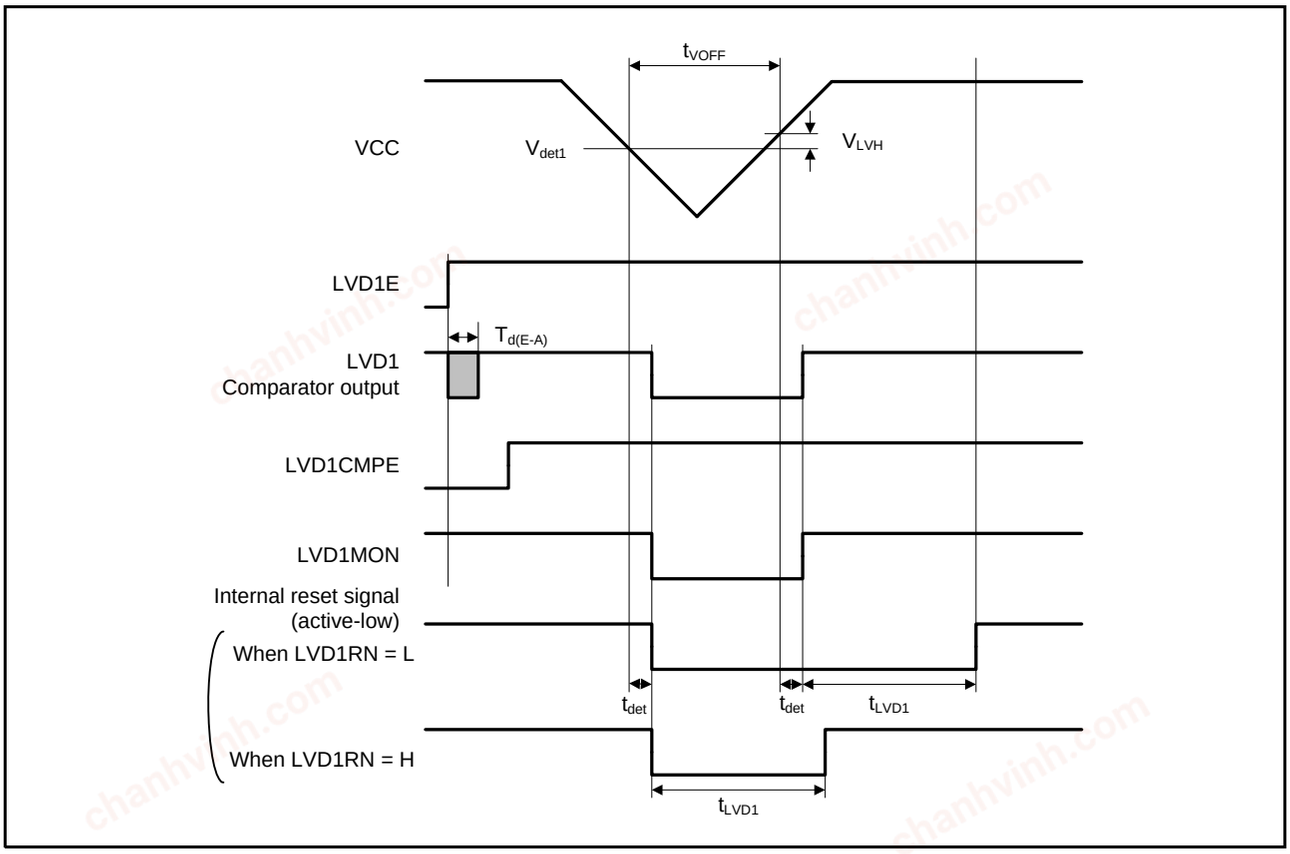


Figure 5.28 Voltage Detection Circuit Timing (V_{det1})

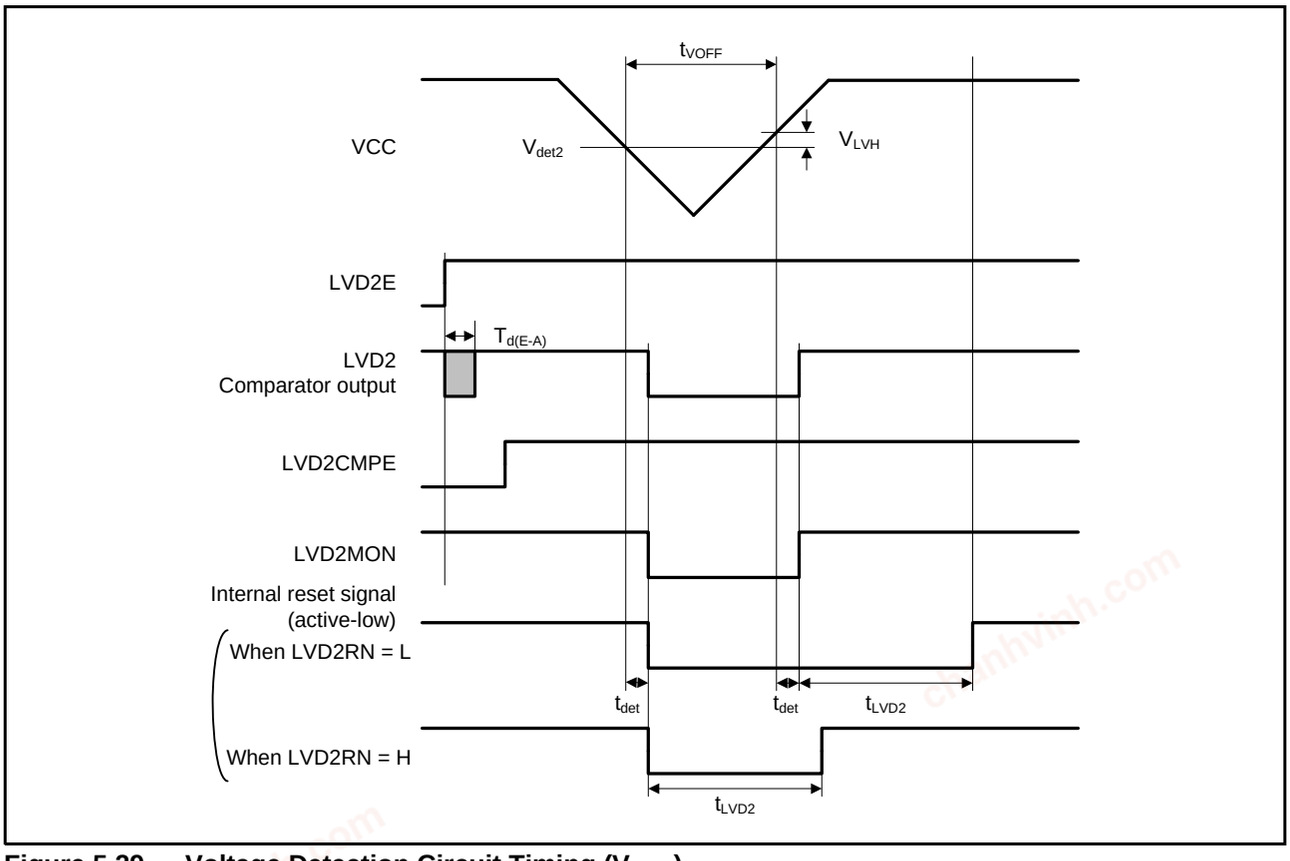


Figure 5.29 Voltage Detection Circuit Timing (V_{det2})

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5.6 Oscillation Stop Detection Timing

Table 5.18 Oscillation Stop Detection Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V, AVCC0 = 3.0 to 3.6 V,
VREFH0 = 3.0 V to AVCC0, Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 5.30

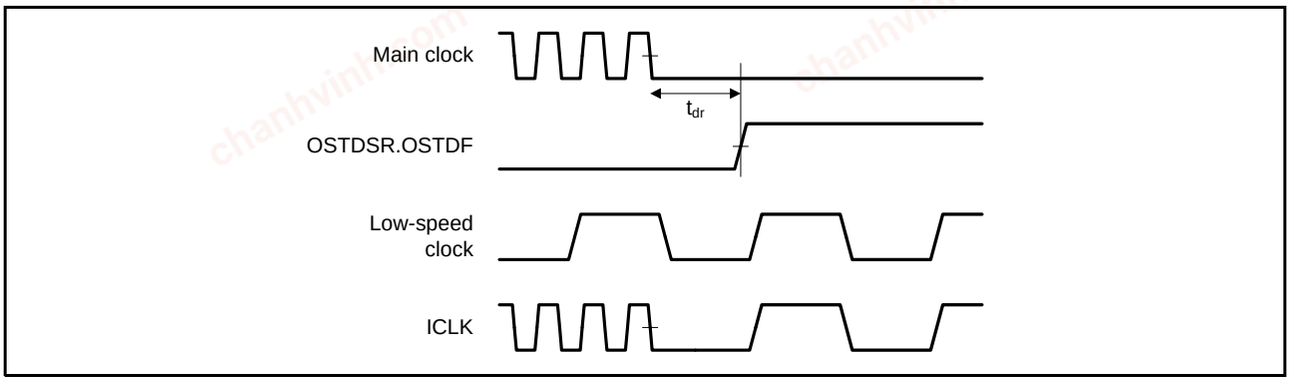


Figure 5.30 Oscillation Stop Detection Timing

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5.7 ROM (Flash Memory for Code Storage) Characteristics

Table 5.19 ROM (Flash Memory for Code Storage) Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	min	typ	max	Unit	Test Conditions
Programming time	128 bytes	t_{P128}	—	1	10	ms	FCLK = 50MHz N_{PEC} ≤ 100
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	128 bytes	t_{P128}	—	1.2	12	ms	FCLK=50MHz N_{PEC} > 100
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	FCLK=50MHz N_{PEC} ≤ 100
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	FCLK=50MHz N_{PEC} > 100
	16 Kbytes	t_{E16K}	—	120	288	ms	
Reprogram/erase cycle *1		N_{PEC}	1000*2	—	—	Times	
Suspend delay time during programming		t_{SPD}	—	—	120	µs	Figure 5.31 FCLK = 50MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	
Data hold time *3		t_{DRP}	10	—	—	Year	
FCU reset time		t_{FCUR}	35	—	—	µs	

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This indicates the minimum number that guarantees the characteristics after reprogramming. (The guaranteed value is in the range from one to the minimum number.)
Note 3. This indicates the characteristic when reprogram is performed within the specification range including the minimum number.

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5.8 E^2 DataFlash Characteristic

Table 5.20 E^2DataFlash (Flash Memory for Data Storage) Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	min	typ	max	Unit	Test Condition
Programming time	2 bytes	t_{DP2}	—	0.25	2	ms	FCLK = 50 MHz
Erasure time	32 bytes	t_{DE32}	—	2	20	ms	FCLK = 50 MHz $N_{PEC} \leq 100$
	32 bytes	t_{DE32}	—	4	20	ms	FCLK = 50 MHz $N_{PEC} > 100$
Blank check time	2 bytes	t_{DBC2}	—	—	30	µs	FCLK = 50 MHz
Reprogram/erase cycle*1		N_{DPEC}	100000*2	—	—	Times	
Suspend delay time during programming		t_{DSPD}	—	—	120	µs	Figure 5.31 PCLKB = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	300	µs	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	µs	
Data hold time *3		t_{DDRP}	10	—	—	Year	

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 2-byte programming is performed 16 times for different addresses in 32-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (over writing is prohibited).
Note 2. This indicates the minimum number that guarantees the characteristics after reprogramming. (The guaranteed value is in the range from one to the minimum number.)
Note 3. This indicates the characteristic when reprogram is performed within the specification range including the minimum number.

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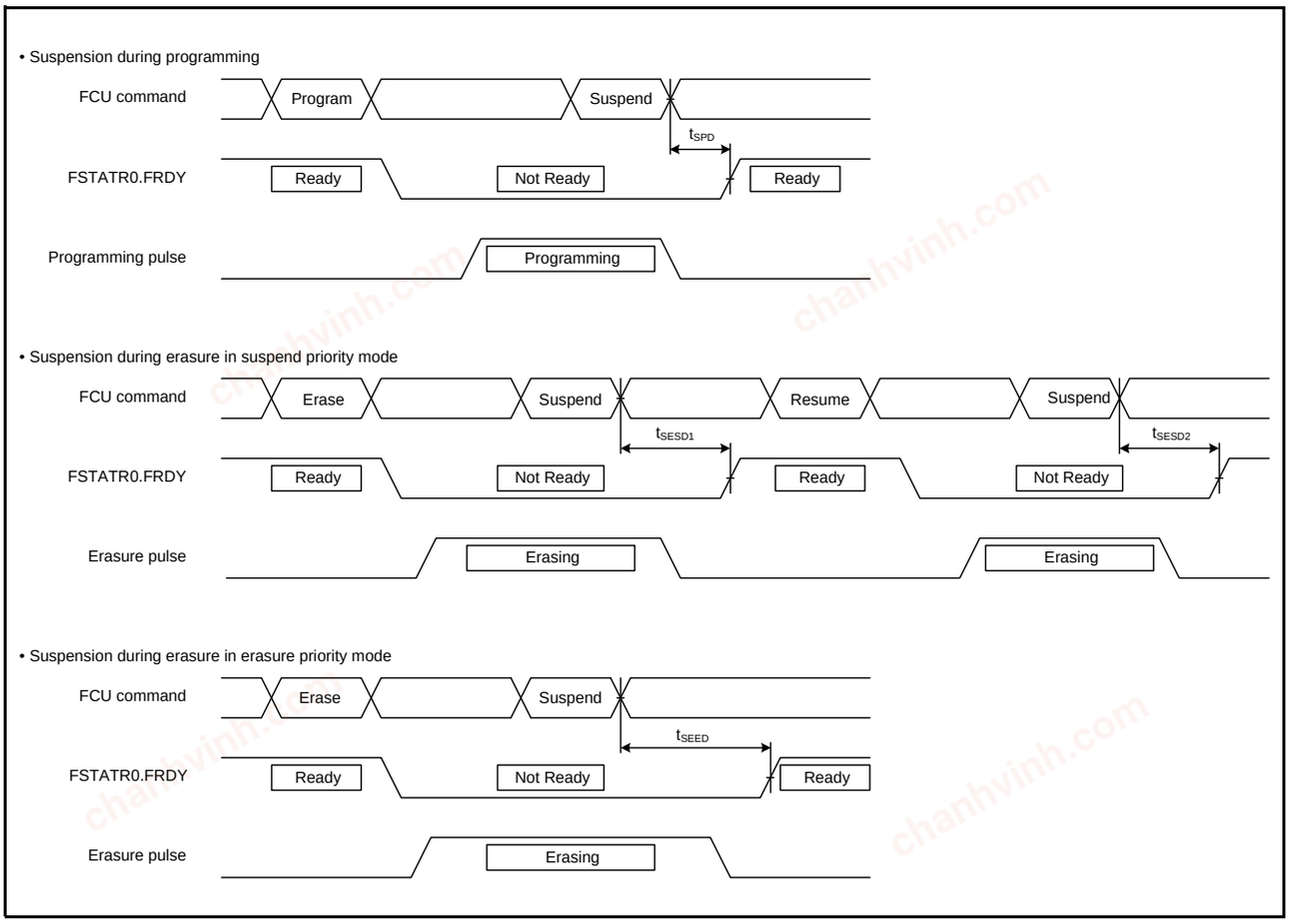


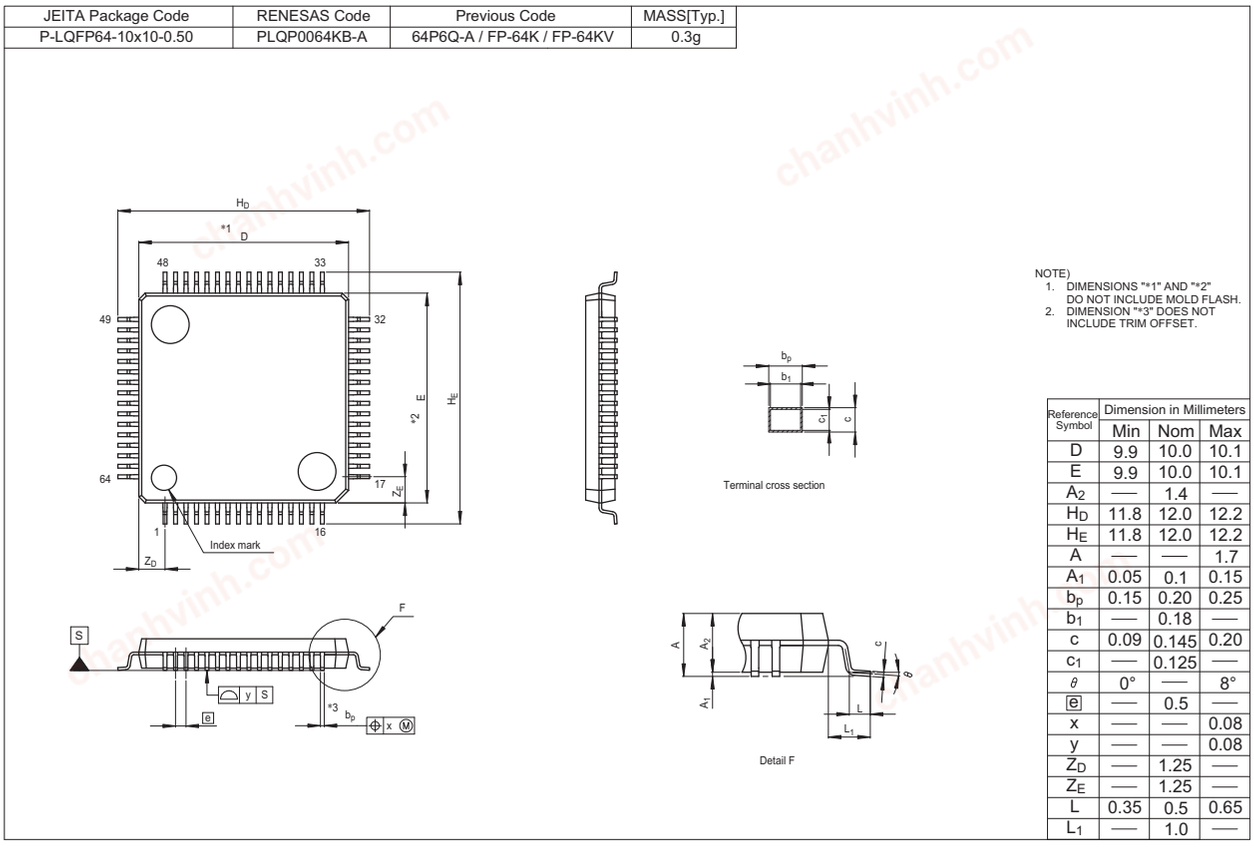
Figure 5.31 Flash Memory Program/Erase Suspend Timing

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Appendix 1.Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation. website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

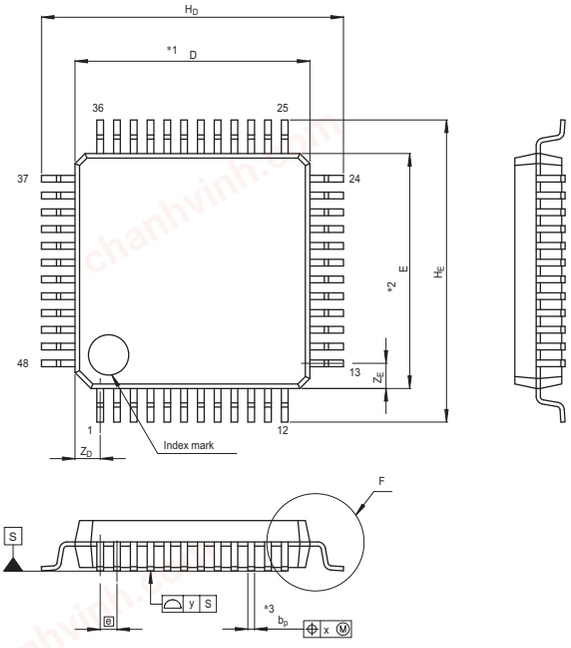


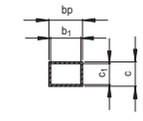
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 64 Pin LQFP (PLQP0064KB-A)

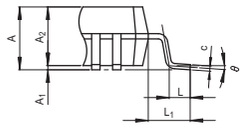
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JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure B 48 Pin LQFP (PLQP0048KB-A)

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REVISION HISTORY	RX63T Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Aug 28, 2012	—	First Edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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