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RL78/G1D

RENESAS MCU

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Rev.1.30
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The RL78/G1D is a microcontroller incorporating the RL78 CPU core and low power consumption RF transceiver supporting the Bluetooth ver.4.2 (Low Energy Single mode) specifications.

1. OUTLINE

1.1 Features

Low Power Technology (3.0V / MCU part: STOP)
- RF transmitter active: 4.3 mA (TYP.)
- RF receiver active: 3.5 mA (TYP.)
- RF sleep (POWER_DOWN mode) operation: 0.3 μA (TYP.)

On-Chip RF Transceiver
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- Bluetooth v4.2 Specification (Low Energy Single mode)
- 2.4 GHz ISM Band, GFSK modulation, TDMA/TDD Frequency Hopping (included AES encryption circuit)
- Adaptivity, exclusively for use in operation as a slave device
- Single ended RF interface

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16-bit RL78-S2 CPU Core
- CISC Architecture (Harvard) with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 μs: @ 32 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5 μs: @ 32.768 kHz operation with subsystem clock)
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- 1-wire on-chip debug function

Main Flash Memory
- 128 KB / 192KB / 256 KB (Block size: 1 KB)
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory
- Data Flash with background operation
- Data flash size: 8 KB size (Erase block size: 1 KB)
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 3.6 V

RAM
- 12 KB / 16KB / 20 KB size
- Supports operands or instructions
- Back-up retention in all modes

On-chip Oscillator
- High accuracy on-chip Oscillator for MCU
- 15kHz low-speed on-chip oscillator for MCU
- 32.768 kHzOn-chip oscillator for the RF slow clock

Data Memory Access (DMA) Controller
- Up to 4 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces
- Simplified I^2C×2
- CSI (7-, 8-bit) ×2,
- UART (7-, 8-, 9-bit) ×2
- I^2C ×1

Supply voltage Management
- Low voltage detection (LVD) with 12 setting options (Notification to Interrupt and/or reset function)
- Power-on reset (POR) monitor/generator

Extended-Function Timers
- Multi-function 16-bit timers: 8 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval Timer: 12-bit, 1 channel
- Watchdog timer: 1 channel (window function)

Rich Analog
- 8/10-bit resolution A/D converter (V_{DD} = 1.6 to 3.6 V)
- Analog input: 8 channels
- Internal voltage reference (1.45 V) and temperature sensor[Note]

Note Can be selected only in HS (high-speed main) mode

Safety Functions
- Comply with the IEC60730 and IEC61508 safety standards

General Purpose I/O
- I/O port: 32 (N-ch open drain I/O [withstand voltage of 6 V]: 2, N-ch open drain I/O [VDD withstand voltage]: 9
- Different potential interface support: Can connect to a 1.8/2.5 V device

Standby function
- MCU part: Low power consumption mode: HALT, STOP
  Power saving mode: SNOOZE
- RF part :Low power saving mode with 6 setting (min. 0.1 μA)

Operating Voltage / Operating Ambient Temperature
1.6 V to 3.6 V / –40 to +85°C

Package Type and Pin Count
48-pin HWQFN (6 × 6) (0.4mm pitch)

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- ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/G1D
128 KB	8 KB	12 KB	R5F11AGG
192 KB	8 KB	16 KB	R5F11AGH
256 KB	8 KB	20 KB[Note]	R5F11AGJ

Note 19 KB when the self-programming function is used.

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1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1D

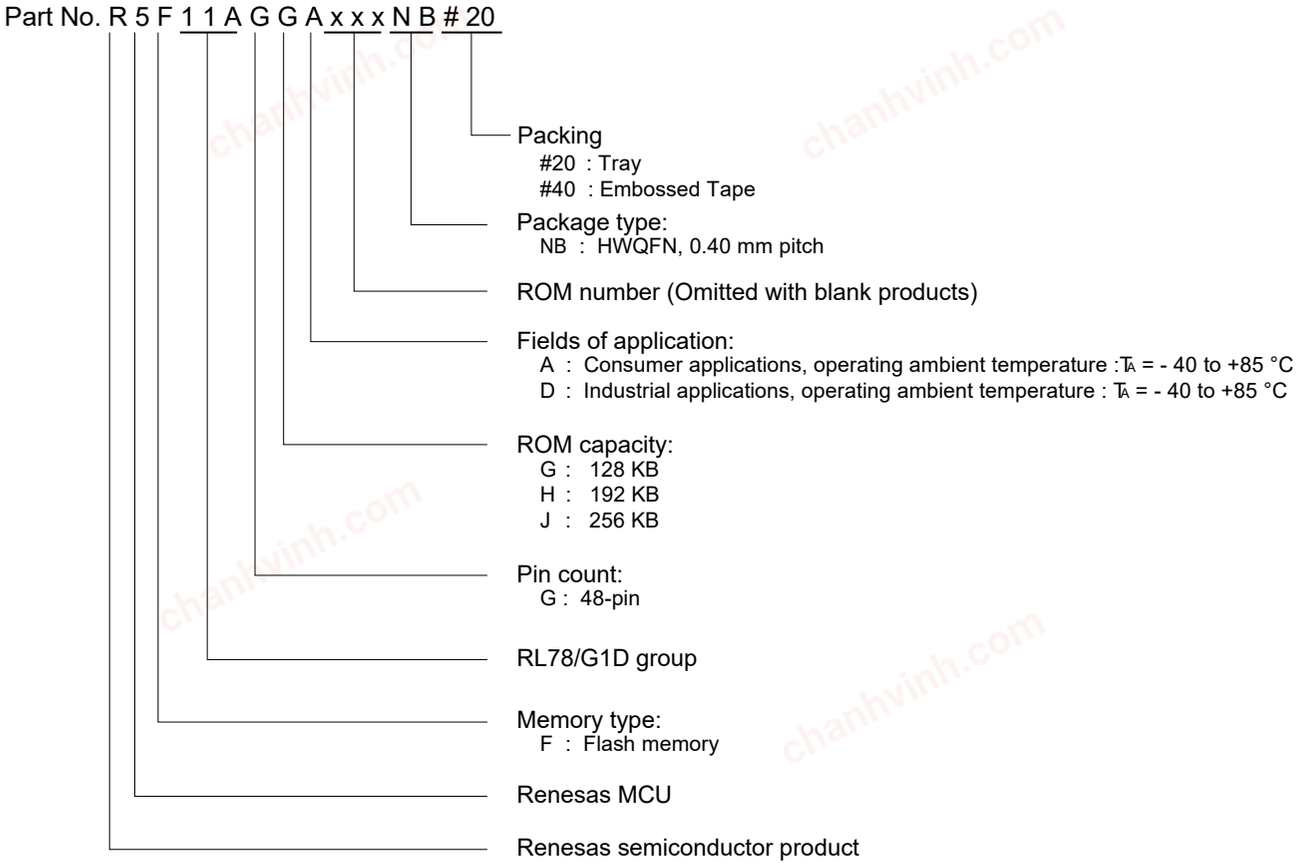


Table 1-1. List of Ordering Part Numbers

Pin count	Package	Fields of Application[Note]	Ordering Part Number	Code Flash Memory	Data Flash Memory
48 pins	Plastic WQFN (6 × 6)	A	R5F11AGGANB#20 R5F11AGGANB#40	128 KB	8 KB
		D	R5F11AGGDNB#20 R5F11AGGDNB#40		
		A	R5F11AGHANB#20 R5F11AGHANB#40	192 KB	8 KB
		D	R5F11AGHDNB#20 R5F11AGHDNB#40		
		A	R5F11AGJANB#20 R5F11AGJANB#40	256 KB	8 KB
		D	R5F11AGJDNB#20 R5F11AGJDNB#40		

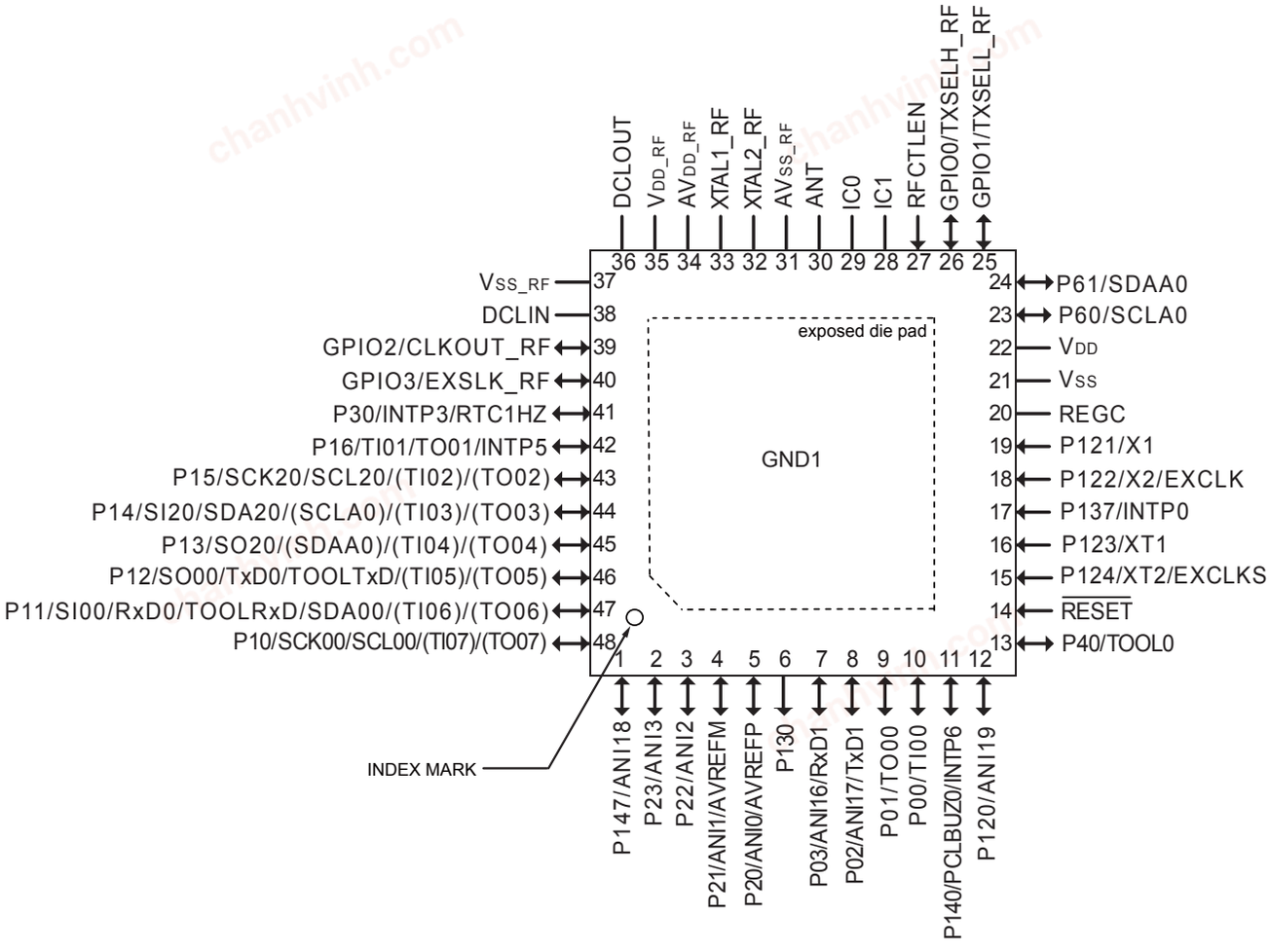
Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1D**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

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1.3 Pin Configuration (Top View)

- 48-pin plastic WQFN (6 × 6 mm, 0.4 mm pitch)



Caution 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).

2. Connect the metal pad (GND1) on the back of the package that has the same potential as AV_{SS_RF}.

Remark 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)..

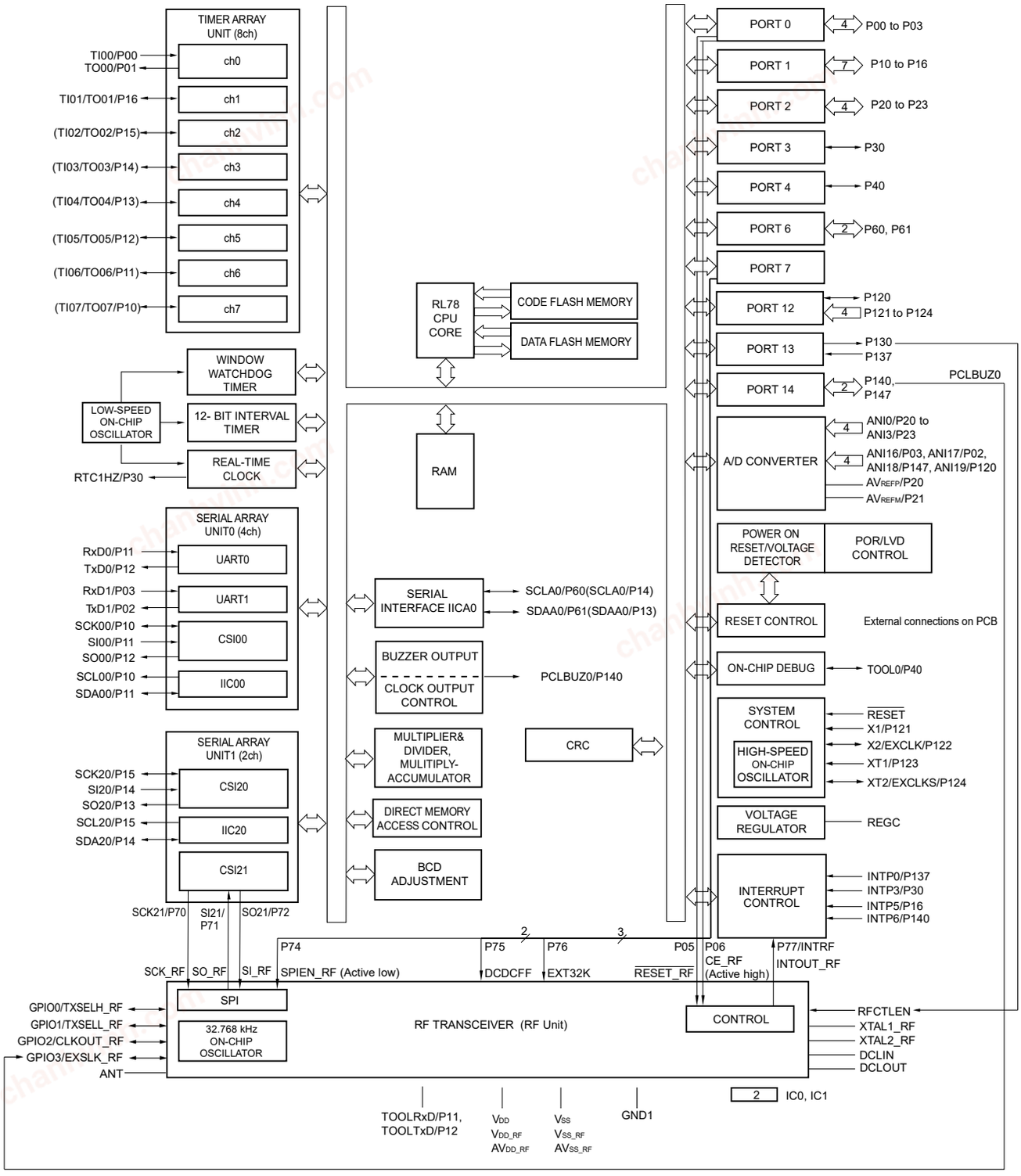
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1.4 Pin Identification

ANI0 to ANI3, ANI16 to ANI19:	Analog input	PCLBUZ0:	Programmable clock output/buzzer output
ANT:	Antenna connection	REGC:	Regulator capacitance
AV_{DD_RF}:	Power supply for RF analog	RFCTLEN:	RF control enable
		RTC1HZ:	Real-time clock correction clock (1 Hz) output
AV_{REFM}:	Analog reference voltage minus	$\overline{RESET}$:	Reset
AV_{REFP}:	Analog reference voltage plus	RxD0, RxD1:	Receive data
		SCLA0:	Serial clock input/output
AV_{SS_RF}:	Ground for RF analog	SCK00, SCK20,	
CLKOUT_RF:	Clock output	SCL00, SCL20:	Serial clock output
DCLIN:	DC-DC converter inductor and DCLOUT capacitor	SDAA0, SDA00, SDA20:	Serial data input/output
		SI00, SI20:	Serial data input
DCLOUT:	DC-DC converter output	SO00, SO20:	Serial data output
EXCLK:	External clock input (Main system clock)	TI00 to TI07:	Timer input
		TO00 to TO07:	Timer output
EXCLKS:	External clock input (Subsystem clock)	TOOL0:	Data input/output for tool
		TOOLRxD, TOOLTxD:	Data input/output for external device
EXSLK_RF:	External slow clock input	TxD0, TxD1:	Transmit data
GND1:	Package exposed die pad	TXSELL_RF,	External PA/LNA control
GPIO0 to GPIO3:	GPIO at RF unit	TXSELH_RF:	
IC0, IC1:	Internal circuit	V_{DD}:	Power supply
INTP0, INTP3,	External interrupt input	V_{DD_RF}:	Power Supply for RF
INTP5, INTP6:		V_{SS}:	Ground
P00 to P03:	Port 0	V_{SS_RF}:	Ground for RF
P10 to P16:	Port 1	X1, X2:	Crystal oscillator (Main system clock)
P20 to P23:	Port 2	XT1, XT2:	Crystal oscillator (Subsystem clock)
P30:	Port 3	XTAL1_RF,	Crystal oscillator (RF clock)
P40:	Port 4	XTAL2_RF:	
P60, P61:	Port 6		
P120 to P124:	Port 12		
P130, P137:	Port 13		
P140, P147:	Port 14		

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<R> 1.5 Block Diagram



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

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1.6 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		R5F11AGG	R5F11AGH	R5F11AGJ
Code flash memory		128 KB	192 KB	256 KB
Data flash memory		8 KB	8 KB	8 KB
RAM		12 KB	16 KB	20 KB[Note 1]
Address space		1 MB		
System clock (RF side)		32 MHz		
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)		
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)		
Subsystem clock		XT1 (Crystal) oscillation, External main system clock input (EXCLKS) 32.768 kHz		
RF slow clock	External input	External clock input for RF block (EXSLK_RF) 32.768 kHz (TYP.)		
	On-chip Oscillator	32.768 kHz (TYP.)		
Low-speed on-chip oscillator		15 kHz (TYP.)		
General-purpose register		(8-bit register × 8) × 4 banks		
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillation clock: f_{IH} = 32 MHz operation)		
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)		
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)		
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.		
I/O port	Total	32[Note 2]		
	CMOS I/O	20[Note 2]		
	CMOS input	5[Note 2]		
	CMOS output	1[Note 2]		
	N-ch O.D. I/O (withstand voltage: 6 V)	2		
	GPIO (RF block)	4		
<R> 2.4 GHz RF transceiver		Supporting Bluetooth v4.2 Specification (Single mode). 2.4 GHz ISM Band, GFSK modulation, TDMA/TDD frequency hopping (Including AES encryption circuit.) Adaptivity (Only in slave operation)		
Timer	16-bit timer	8 channels		
	Watchdog timer	1 channel		
	Real-time clock (RTC)	1 channel		
	12-bit interval timer	1 channel		

(Notes are listed on the next page.)

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Note 1. This is about 19 KB when the self-programming function is used.

2. When RF is used, this count includes the pins that connect the MCU with the RF transceiver by the user externally on the board.

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(2/2)

Item		R5F11AGG	R5F11AGH	R5F11AGJ
Timer	Timer output	8 channels (PWM outputs: 7[Note 1])[Note 2]		
	RTC output	1 channel 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)		
Clock output/buzzer output		1[Note 3]		
		● 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) ● 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)		
	RF unit (Clock output)	● 16 MHz, 8 MHz, 4 MHz		
8/10-bit resolution A/D converter		8 channels		
Serial interface		● CSI/simplified I^2C/UART: 1 channel ● CSI/simplified I^2C: 1 channel ● UART: 1 channel ● CSI: 1 channel (dedicated for internal communications)		
	I^2C bus	1 channel		
Multiplier and divider/multiply-accumulator		Multiplication: 16 bits × 16 bits = 32 bits (Unsigned or signed) Division: 32 bits ÷ 32 bits = 32 bits (Unsigned) Multiply-accumulate: 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)		
DMA controller		4 channels		
Vectored interrupt sources	Internal	29		
	External	4		
Reset		● Reset by RESET pin ● Internal reset by watchdog timer ● Internal reset by power-on-reset ● Internal reset by voltage detector ● Internal reset by illegal instruction execution[Note 4] ● Internal reset by RAM parity error ● Internal reset by illegal-memory access		
Power-on-reset circuit		● Power-on-reset: 1.51 (TYP.) ● Power-down-reset: 1.50 (TYP.)		
Voltage detector		● Rising edge : 1.67 V to 3.13 V (12 stages) ● Falling edge : 1.63 V to 3.06 V (12 stages)		
On-chip debug function		Provided		
Power supply voltage		V_{DD} = 1.6 to 3.6 V (V_{DD} =1.8 to 3.6 V on usage of DC-DC converter)		
Operating ambient temperature		T_A = –40 to +85 °C		
Package		48-pin QFN (6 × 6), (0.4 mm pitch)		

Note 1. The number of outputs varies, depending on the setting of channels in use and the number of the master (see **7.9.3 Operation as multiple PWM output function**).

2. When setting to PIOR0 = 1

3. When RF is used, this count includes the pins that connect the MCU with the RF transceiver by the user externally on the board.

4. The illegal instruction is generated when instruction code FFH is executed. Reset by the illegal instruction execution not issued by emulation with the on-chip debug emulator.

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2. ELECTRICAL SPECIFICATIONS

Caution The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

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2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	–0.5 to +6.5	V
	V_{DDRF1}	V_{DD_RF}	–0.5 to +4.0	V
	V_{DDRF2}	AV_{DD_RF}	–0.5 to +4.0	V
	V_{DDRF3}	DCLIN	–0.5 to +4.0	V
	V_{SSRF}	V_{SS_RF}, AV_{SS_RF}	–0.5 to +0.3	V
Input voltage	V_{I1}	P00, P01, P02, P03, P10, P11, P12, P14, P15, P16, P20, P21, P22, P23, P30, P40, P120, P121, P122, P123, P124, P137, P140, P147, RESET	–0.3 to V_{DD}+0.3 Note 1	V
	V_{I2}	P60, P61	–0.3 to +6.5	V
	V_{IRF1}	GPIO0, GPIO1, GPIO2, GPIO3	–0.3 to V_{DD_RF}+0.3 Note 2	V
	V_{IRF2}	ANT	–0.5 to +1.4	V
Output voltage	V_O	P00, P01, P02, P03, P10, P11, P12, P14, P15, P16, P20, P21, P22, P23, P30, P40, P60, P61, P120, P130, P140, P147	–0.3 to V_{DD}+0.3 Note 1	V
	V_{ORF}	GPIO0, GPIO1, GPIO2, GPIO3, DCLOUT	–0.3 to V_{DD_RF}+0.3 Note 2	V
Analog input voltage	V_{AI}	ANI0, ANI1, ANI2, ANI3, ANI16, ANI17, ANI18, ANI19	–0.3 to V_{DD}+0.3 and –0.3 to $V_{REF(+)}$+0.3 Note 2, 4	V
REGC pin input voltage	V_{IREGC}	REGC	–0.3 to +2.8 and –0.3 to V_{DD}+0.3 Note 3	V
IC pin input voltage	V_{IIC}	IC0, IC1	–0.5 to +0.3	V

Note 1. Must be 6.5 V or lower.

2. Must be 4.0 V or lower.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

4. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. Reference voltage is V_{SS}.

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Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	(This is applicable to all pins listed below.)	–40	mA
		Total of all pins –170mA	P00, P01, P02, P03, P40, P120, P130, P140	–70	mA
			P10, P11, P12, P13, P14, P15, P16, P30, P147	–100	mA
	I_{OH2}	Per pin	(This is applicable to all pins listed below.)	–0.5	mA
		Total of all pins	P20, P21, P22, P23	–2	mA
	I_{OHMRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3	–17	mA
Output current, low	I_{OL1}	Per pin	(This is applicable to all pins listed below.)	40	mA
		Total of all pins 170mA	P00, P01, P02, P03, P40, P120, P130, P140	70	mA
			P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147	100	mA
	I_{OL2}	Per pin	(This is applicable to all pins listed below.)	1	mA
		Total of all pins	P20, P21, P22, P23	5	mA
	I_{OLRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3	17	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		In flash memory programming mode		–40 to +85	°C
Storage temperature	Tstg			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. Reference voltage is V_{SS}.

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2.2 Operating Voltage

(T_A = –40 to +85°C, V_{DD} = V_{DD_RF} = AV_{DD_RF}, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Clock generator		Flash operation mode	Operation voltage	CPU operation clocks (f_{CLK})[Note 1]
Main system clock (f_{MAIN})	High-speed on-chip oscillator (f_{IH})	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 32 MHz
			2.4 V ≤ V_{DD} < 2.7 V	1 MHz to 16 MHz
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 8 MHz
		LV (low-voltage main) mode [Note 2]	1.6 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 4 MHz
	X1 clock oscillator (f_X)	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 20 MHz
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 8 MHz
		LV (low-voltage main) mode [Note 2]	1.6 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 4 MHz
	External main system clock (f_{EX})	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 20 MHz
			2.4 V ≤ V_{DD} < 2.7 V	1 MHz to 16 MHz
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 8 MHz
		LV (low-voltage main) mode[Note 2]	1.6 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 4 MHz
Subsystem clock (f_{SUB})	XT1 clock oscillator (f_{XT})	–	1.6 V ≤ V_{DD} ≤ 3.6 V	32.768 kHz
	External subsystem clock (f_{EXT})	–	1.6 V ≤ V_{DD} ≤ 3.6 V	32.768 kHz

Note 1. Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time.Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

2. This mode is prohibited to use in case of using DC-DC converter.

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2.3 Oscillator Characteristics

2.3.1 X1, XT1, XRF oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency Note 1	Ceramic resonator Crystal resonator	f_X	2.7 V ≤ V_{DD} ≤ 3.6 V	1		20	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1		8	MHz
			1.6 V ≤ V_{DD} ≤ 1.8 V	1		4	MHz
XT1 clock oscillation frequency Note 1		f_{XT}		32	32.768	35	kHz
RF base clock oscillation frequency Note 2		f_{XRF}			32		MHz
RF base clock oscillation frequency accuracy Note 2		f_{XRFP}		-20		+20	ppm

Note 1. Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time.
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

2. This Oscillator characteristics is base clock for RF Transceiver.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user.
Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.3.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Oscillators	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note 1, 2	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy	f_{IHP}	–20 to +85°C	1.8 V ≤ V_{DD} ≤3.6 V	-1.5		+1.5.	%
			1.6 V ≤ V_{DD} <1.8 V	-5.0		+5.0	%
		–40 to –20°C	1.8 V ≤ V_{DD} ≤3.6 V	-2.5		+2.5.	%
			1.6 V ≤ V_{DD} <1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency Note 3	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy	f_{ILP}			–15		+15	%
On-chip oscillator clock frequency for the RF slow clock Note 3	f_{ILRF}				32.768		kHz
On-chip oscillator clock frequency accuracy for the RF slow clock	f_{ILRFP}			-0.025		0.025	%

Note 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for instruction execution time.

3. This indicates the oscillator characteristics only.

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2.4 DC Characteristics

2.4.1 Output current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			–10.0[Note 2]	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			–10.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			–2.5	mA
		P10, P11, P12, P13, P14, P15, P16, P30, P147	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			–19.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			–5.0	mA
		Total of all pins[Note 3]		1.6 V ≤ V_{DD} ≤ 3.6 V			–135.0[Note 4]	mA
	I_{OH2}	P20, P21, P22, P23	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			–0.1[Note 2]	mA
			Total[Note 3]	1.6 V ≤ V_{DD} ≤ 3.6 V			–1.5	mA
	I_{OHRF}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	1.6 V ≤ V_{DD_RF} ≤ 3.6 V			–2.0	mA
Output current, low[Note 1]	I_{OL1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			20.0[Note 2]	mA
		P60, P61	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			15.0[Note 2]	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			15.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			4.5	mA
		P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			35.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			10.0	mA
		Total of all pins[Note 3]		1.6 V ≤ V_{DD} ≤ 3.6 V			150.0	mA
	I_{OL2}	P20, P21, P22, P23	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			0.4[Note 2]	mA
			Total[Note 3]	1.6 V ≤ V_{DD} ≤ 3.6 V			5.0	mA
	I_{OLRF}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	1.6 V ≤ V_{DD_RF} ≤ 3.6 V			2.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OH} = –10.0 mA
Total output current of pins = (–10.0 × 0.7)/(50 × 0.01) = –14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Product for industrial applications (R5F11AGGDNB, R5F11AGHDNB, R5F11AGJDNB) is –100.0 mA.

(**Caution** and **Remark** are listed on the next page.)

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Caution P00, P02, P03, and P10 to P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.2 Input current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Normal mode (I_{THL} = 1)	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P01, P03, P10, P11, P13, P14, P15, P16	TTL mode 3.3 V ≤ V_{DD} ≤ 3.6 V	2.0		V_{DD}	V
			TTL mode 1.6 V ≤ V_{DD} < 3.3V	1.5		V_{DD}	V
	V_{IH3}	P20, P21, P22, P23		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60, P61		0.7V_{DD}		6.0	V
	V_{IH5}	P121, P122, P123, P124, P137, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IHRF}	GPIO0, GPIO1, GPIO2, GPIO3		0.85V_{DD_RF}		V_{DD_RF}	V
Input voltage, low	V_{IL1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147	Normal mode (I_{THL} = 1)	0		0.2V_{DD}	V
	V_{IL2}	P01, P03, P10, P11, P13, P14, P15, P16	TTL mode 3.3 V ≤ V_{DD} ≤ 3.6 V	0		0.5	V
			TTL mode 1.6 V ≤ V_{DD} < 3.3V	0		0.32	V
	V_{IL3}	P20, P21, P22, P23		0		0.3V_{DD}	V
	V_{IL4}	P60, P61		0		0.3V_{DD}	V
	V_{IL5}	P121, P122, P123, P124, P137, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{ILRF}	GPIO0, GPIO1, GPIO2, GPIO3		0		0.1V_{DD_RF}	V

Caution The maximum value of V_{IH} of pins P00, P02, P03, and P10 to P15 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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2.4.3 Output voltage

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = –2.0 mA	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} – 0.6			V
		I_{OH} = –1.5 mA		1.8 V ≤ V_{DD} ≤ 3.6 V	V_{DD} – 0.5			V
		I_{OH} = –1.0 mA		1.6 V ≤ V_{DD} ≤ 3.6 V	V_{DD} – 0.5			V
		I_{OH} = –10 μA	P130		V_{DD} – 0.3			V
	V_{OH2}	I_{OH} = –100 μA	P20, P21, P22, P23		V_{DD} – 0.5			V
	V_{OHRF}	I_{OH} = –2.0 mA	GPIO0, GPIO1, GPIO2, GPIO3	2.7 V ≤ V_{DD_RF} ≤ 3.6 V	V_{DD_RF} – 0.3			V
		I_{OH} = –1.5 mA		1.8 V ≤ V_{DD_RF} ≤ 3.6 V	V_{DD_RF} – 0.3			V
Output voltage, low	V_{OL1}	I_{OL} = 3.0 mA	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	2.7 V ≤ V_{DD} ≤ 3.6 V			0.6	V
		I_{OL} = 1.5 mA					0.4	V
		I_{OL} = 0.6 mA		1.8 V ≤ V_{DD} ≤ 3.6 V			0.4	V
		I_{OL} = 0.3 mA		1.6 V ≤ V_{DD} ≤ 3.6 V			0.4	V
	V_{OL2}	I_{OL} = 400 μA	P20, P21, P22, P23				0.4	V
	V_{OLRF}		GPIO0, GPIO1, GPIO2, GPIO3				0.3	V

Caution P00, P02, P03, and P10 to P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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2.4.4 Input leakage current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	VI = V_{DD}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P60, P61, P120, P140, P147			1	μA
	I_{LIH2}	VI = V_{DD}	P20, P21, P22, P23, P137, $\overline{\text{RESET}}$			1	μA
	I_{LIH3}	VI = V_{DD}	P121, P122, P123, P124 (EXCLK, EXCLKS) (XT1, XT2)	In input port		1	μA
				In external clock input		1	μA
				In resonator connection		10	μA
	I_{LIHRF}	VI = V_{DD_RF}	GPIO0, GPIO1, GPIO2, GPIO3			10	μA
Input leakage current, low	I_{LIL1}	VI = V_{SS}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P60, P61, P120, P140, P147			-1	μA
	I_{LIL2}	VI = V_{SS}	P20, P21, P22, P23, P137, $\overline{\text{RESET}}$			-1	μA
	I_{LIL3}	VI = V_{SS}	P121, P122, P123, P124 (EXCLK, EXCLKS) (XT1, XT2)	In input port		-1	μA
				In external clock input		-1	μA
				In resonator connection		-10	μA
	I_{LILRF}	VI = V_{SS_RF}	GPIO0, GPIO1, GPIO2, GPIO3			-10	μA

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.5 Resistance

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
On-chip pll-up resistance	R_U	VI = V_{SS}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147 In input mode	10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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2.5 Current Consumption

The Current Consumption by the RL78/G1D is the total current including that for the MCU (current flowing into the V_{DD} pin) and that for the RF unit (current flowing into the V_{DD_RF}, AV_{DD_RF} pins).

The characteristics of the MCU (current flowing into the V_{DD} pin) are given in 2.5.1 and the characteristics of the RF unit (current flowing into the V_{DD_RF}/AV_{DD_RF} pins) are given in 2.5.2

2.5.1 MCU

(1) Operating current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Operating current Note 1	I_{DD1}	HS (high-speed main) mode Note 5	Basic operation	f_{IH} = 32 MHz Note 2	V_{DD} = 3.0 V		2.3		mA
			Normal operation	f_{IH} = 32 MHz Note 2	V_{DD} = 3.0 V		5.2	8.5	mA
				f_{IH} = 24 MHz Note 2	V_{DD} = 3.0 V		4.1	6.6	mA
				f_{IH} = 16 MHz Note 2	V_{DD} = 3.0 V		3.0	4.7	mA
		LS(low-speed main) mode Note 5	Normal operation	f_{IH} = 8 MHz Note 2	V_{DD} = 3.0 V		1.3	2.1	mA
					V_{DD} = 2.0 V		1.3	2.1	mA
		LV (low-voltage main) mode Note 5	Normal operation	f_{IH} = 4 MHz Note 2	V_{DD} = 3.0 V		1.3	1.8	mA
					V_{DD} = 2.0 V		1.3	1.8	mA
		HS (high-speed main) mode Note 5	Normal operation	f_{MX} = 20 MHz Note 3	V_{DD} = 3.0 V Note 6		3.4	5.5	mA
							3.6	5.7	mA
				f_{MX} = 10 MHz Note 3	V_{DD} = 3.0 V Note 6		2.1	3.2	mA
							2.1	3.2	mA
		LS (low-speed main) mode Note 5	Normal operation	f_{MX} = 8 MHz Note 3	V_{DD} = 3.0 V Note 6		1.2	2.0	mA
							1.2	2.0	mA
					V_{DD} = 2.0 V Note 6		1.2	2.0	mA
							1.2	2.0	mA
		Subsystem clock operation	Normal operation	f_{SUB} = 32.768 kHz Note 4	T_A = -40°C Note 6		4.8	5.9	µA
							4.9	6.0	µA
					T_A = +25°C Note 6		4.9	5.9	µA
							5.0	6.0	µA
					T_A = +50°C Note 6		5.0	7.6	µA
							5.1	7.7	µA
					T_A = +70°C Note 6		5.2	9.3	µA
							5.3	9.4	µA
					T_A = +85°C Note 6		5.7	13.3	µA
							5.8	13.4	µA

(**Notes** and **Remarks** are listed on the next page.)

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Note 1. Current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed system clock and subsystem clock are stopped.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz

6. The upper value is for square-wave input and the lower is with an oscillator connected.

Remark 1. f_{MX}: High-speed system clock frequency (External main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

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(2) Standby current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
HALT current Note 1, 2	I_{DD2}	HS (high-speed main) mode Note 7	f_{IH} = 32 MHz Note 4	V_{DD} = 3.0 V		0.62	1.86	mA
			f_{IH} = 24 MHz Note 4	V_{DD} = 3.0 V		0.50	1.45	mA
			f_{IH} = 16 MHz Note 4	V_{DD} = 3.0 V		0.44	1.11	mA
		LS (low-speed main) mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		290	620	μA
				V_{DD} = 2.0 V		290	620	μA
		LV (low-voltage main) mode Note 7	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		440	680	μA
				V_{DD} = 2.0 V		440	680	μA
		HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3	V_{DD} = 3.0 V Note 9		0.31	1.08	mA
						0.48	1.28	mA
			f_{MX} = 10 MHz Note 3	V_{DD} = 3.0 V Note 9		0.21	0.63	mA
						0.28	0.71	mA
		LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3	V_{DD} = 3.0 V Note 9		110	360	μA
						160	420	μA
				V_{DD} = 2.0 V Note 9		110	360	μA
						160	420	μA
		Subsystem clock operation	f_{SUB} = 32.768kHz Note 5	T_A = –40°C Note 9		0.28	0.61	μA
						0.47	0.80	μA
				T_A = +25°C Note 9		0.34	0.61	μA
						0.53	0.80	μA
				T_A = +50°C Note 9		0.41	2.30	μA
						0.60	2.49	μA
				T_A = +70°C Note 9		0.64	4.03	μA
						0.83	4.22	μA
				T_A = +85°C Note 9		1.09	8.04	μA
						1.28	8.23	μA
STOP current Note 6, 8	I_{DD3}	T_A = –40°C				0.19	0.52	μA
		T_A = +25°C				0.25	0.52	μA
		T_A = +50°C				0.32	2.21	μA
		T_A = +70°C				0.55	3.94	μA
		T_A = +85°C				1.00	7.95	μA

(**Notes** and **Remarks** are listed on the next page.)

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Note 1. Current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz

8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.

9. The upper value is for square-wave input and the lower is with an oscillator connected.

Remark 1. f_{MX}: High-speed system clock frequency (External main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

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(3) Current for each peripheral circuit

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
Current when PCLBUZ0 and EXSLK_RF are connected together and MCU supplies RF slow clock to RF	I_{PCEX} Note 1				1.0		μA
RTC operating current	I_{RTC} Note 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Note 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Note 1, 2, 5	f_{IL} is 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Note 1, 6	When conversion at maximum speed	AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Thermometer sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVI} Note 1, 7				0.08		μA
Flash self-programming operating current	I_{FSP} Note 1, 9				2.50	12.20	mA
BGO current	I_{BGO} Note 1, 8				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Note 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78 microcontroller is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. Also, add the value of IFIL in case of selecting low-speed on-chip oscillator. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12 bit interval timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1} or I_{DD2} and I_{IT} when f_{CLK} = f_{SUB} when the watchdog timer operates in STOP mode. When using low-speed on-chip oscillator, add I_{FIL}.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The current value of MCU is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The current value of MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit is in operation.

8. Current flowing when operates rewriting to Data flash.

9. Current flowing when operates flash self-programming.

10. Shift time to the SNOOZE mode is referred User's Manual: Hardware.

(**Remarks** are listed on the next page.)

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Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency
2. f_{SUB}: Subsystem clock frequency
3. f_{CLK}: CPU and peripheral hardware clock frequency
4. Temperature condition of the TYP. value is T_A = 25°C

2.5.2 RF unit

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current Note 1, 2	I_{DDRFTX}	Transmission peak current	Transmission output power 0 dBm	RF normal mode	-	4.3	5.7	mA
					-	7.4	9.0	mA
				RF low power mode	-	2.6	4.1	mA
					-	4.4	6.0	mA
				RF high performance mode	-	4.3	5.7	mA
					-	7.4	9.0	mA
	I_{DDRFRX}	Reception peak current		RF normal mode	-	3.5	5.0	mA
					-	6.2	7.5	mA
				RF low power mode	-	3.3	4.8	mA
					-	5.8	7.1	mA
				RF high performance mode	-	3.7	5.2	mA
					-	6.6	7.9	mA
	I_{DDRFST}	STANDBY_RF current			-	0.40	0.9	mA
					-	0.28	0.8	mA
	I_{DDRFSL}	SLEEP_RF current			-	0.50	1.1	mA
					-	0.36	0.8	mA
	I_{DDRFDS}	DEEP_SLEEP current		RF slow clock externally input through EXSLK_RF	-	0.14	3.6	µA
					-	0.14	3.6	µA
				RF slow clock from on-chip oscillator	-	1.8	6.8	µA
					-	1.8	6.8	µA
	I_{DDRFPD}	POWER_DOWN current			-	0.10	3.0	µA
					-	0.10	3.0	µA
	I_{DDRFRS}	RESET_RF current			-	0.10	3.0	µA
					-	0.10	3.0	µA
	I_{DDRFIL}	IDLE_RF current			-	0.50	1.1	mA
					-	0.60	1.1	mA
	I_{DDRFSU}	SETUP_RF current			-	2.5	4.7	mA
					-	3.5	5.0	mA

Note 1. Total current flowing into V_{DD_RF}, and AV_{DD_RF}.
2. For each item, the values in the upper and lower row apply respectively when the DC/DC converter embedded in the RF chip is and is not in use.

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2.6 AC Characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Main system (f_{MAIN}) clock operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (low-voltage main) mode		0.25		1	μs
			LS (low-speed main) mode		0.125		1	μs
		Subsystem clock (f_{SUB}) operation			28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (low-voltage main) mode		0.25		1	μs
			LS (low-speed main) mode		0.125		1	μs
External clock frequency	f_{EX}	EXCLK		2.7 V ≤ V_{DD} ≤ 3.6 V	1		20	MHz
				2.4 V ≤ V_{DD} < 2.7 V	1		16	MHz
				1.8 V ≤ V_{DD} < 2.4 V	1		8	MHz
	f_{EXS}	EXCLKS			32		35	kHz
	f_{EXRF}	EXSLK_RF	When 32.768 kHz input	±500 ppm	32.751616	32.768	32.784384	kHz
			When 16.384 kHz input	±500 ppm	16.375808	16.384	16.392192	kHz
External clock input high-level width, low-level width	t_{EXH}, t_{EXL}	EXCLK		2.7 V ≤ V_{DD} ≤ 3.6 V	24			ns
				2.4 V ≤ V_{DD} < 2.7 V	30			ns
				1.8 V ≤ V_{DD} < 2.4 V	60			ns
	t_{EXHS}, t_{EXLS}	EXCLKS			13.7			μs
	t_{EXHRF}, t_{EXLRF}	EXSLK_RF	When 32.768 kHz input		0.08	15.258	32.69	μs
			When 16.384 kHz input		0.08	8.192	16.304	μs
Timer input high-level width, low-level width	t_{TIH}, t_{TIL}	TI00, TI01, TI02, TI03, TI04, TI05, TI06, TI07			1/f_{MCK}+10			ns
Timer output frequency	t_{TO}	TI00, TI01, TI02, TI03, TI04, TI05, TI06, TI07	HS (high-speed main) mode	2.7 V ≤ V_{DD} < 3.6 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
			LV (low-voltage main) mode				4	MHz
			LS (low-speed main) mode				4	MHz
Clock/buzzer output frequency	t_{PLC}	PCLBUZ0	HS (high-speed main) mode	2.7 V ≤ V_{DD} < 3.6 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
			LV (low-voltage main) mode				4	MHz
			LS (low-speed main) mode				4	MHz
	t_{PCLRF}	CLKOUT_RF					16	MHz

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).
m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

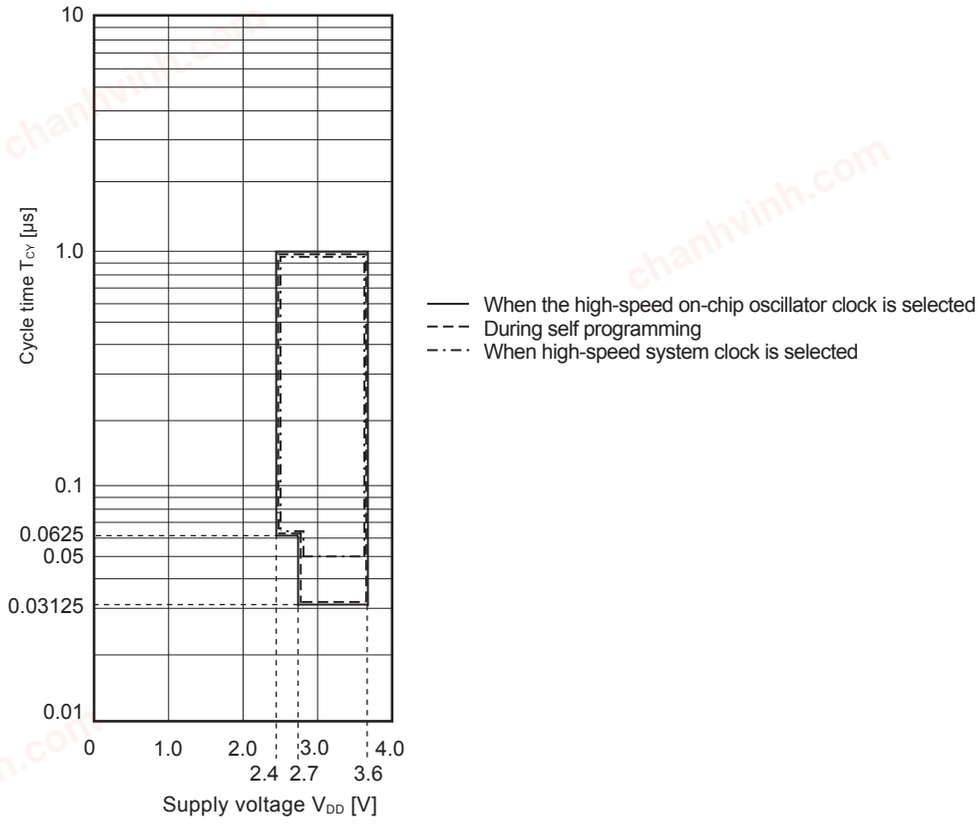
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(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (2/2)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP3, INTP5, INTP6	1			µs
External PA control output High-level width	t_{PAHRF}	TXSELH_RF	283			µs
External PA control output low-level width	t_{PALRF}	TXSELL_RF	283			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	$\overline{\text{RESET}}$	10			µs
$\overline{\text{RESET_RF}}$ internal pin low-level width	t_{RSTLRF}	$\overline{\text{RESET_RF}}$ internal pin	31			µs

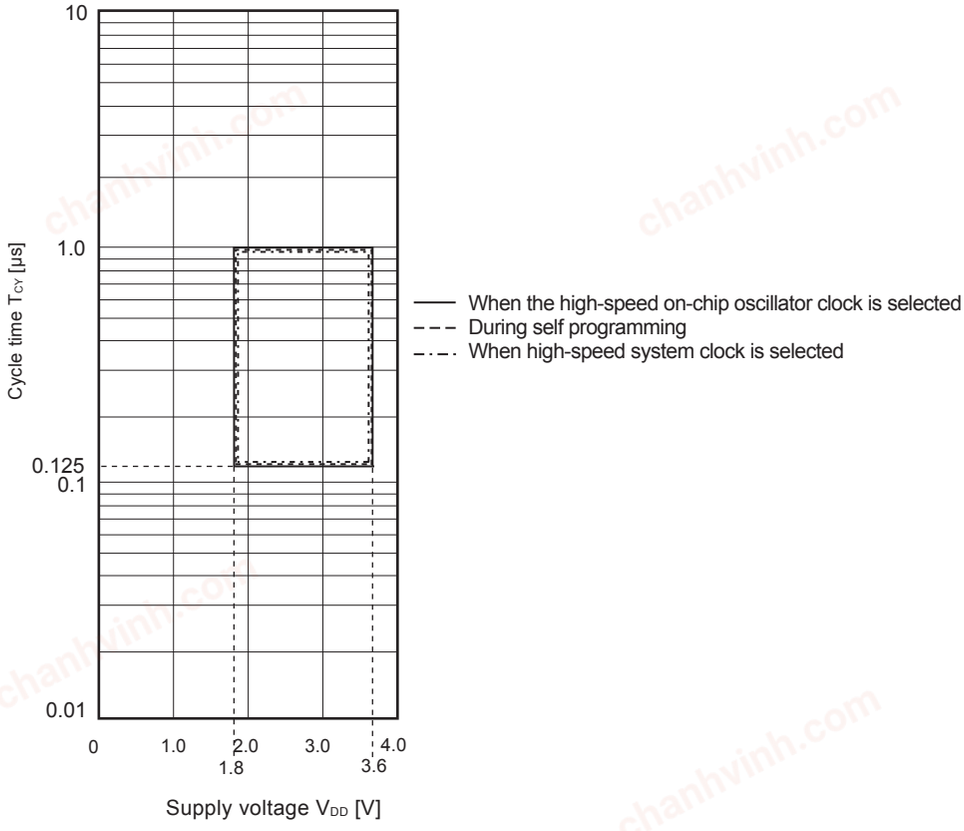
Minimum Instruction Execution Time during Main System Clock Operation

T_{CY} vs V_{DD} (HS (high-speed main) mode)

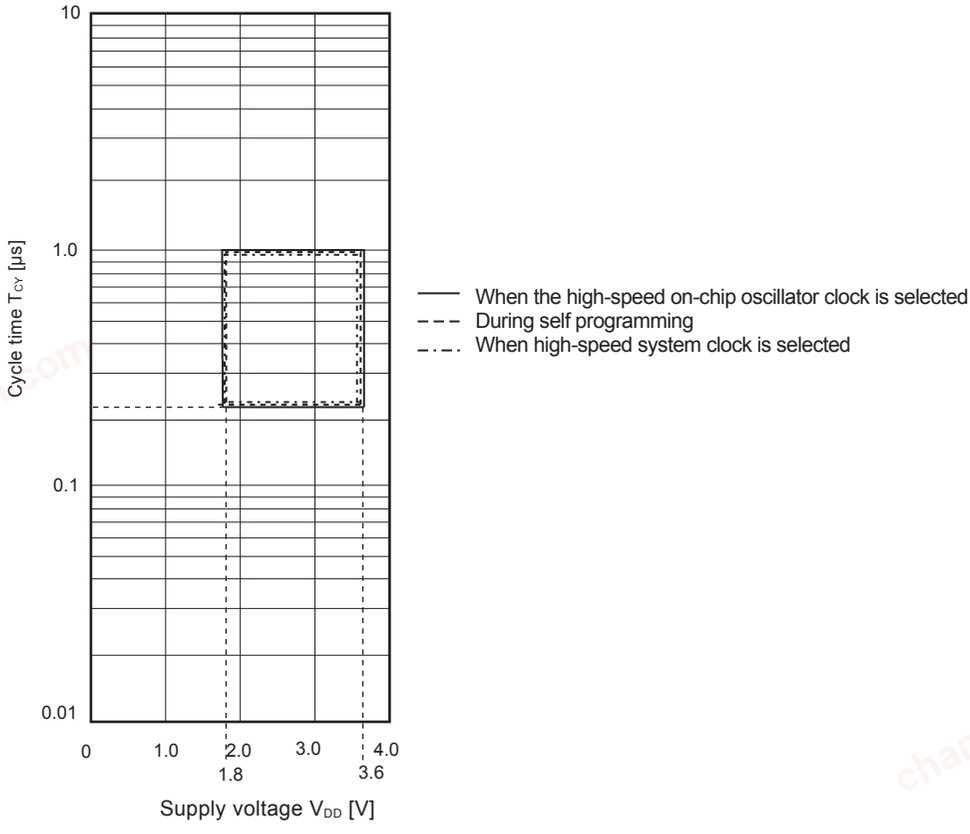


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T_{CY} vs V_{DD} (LS (low-speed main) mode)

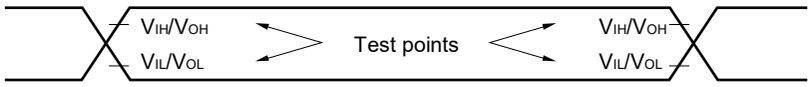


T_{CY} vs V_{DD} (LV (low-voltage main) mode)

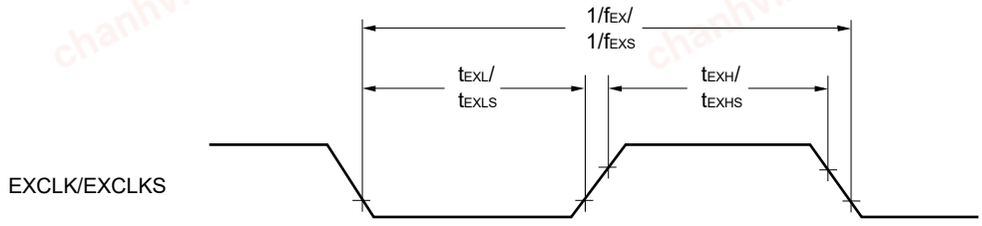


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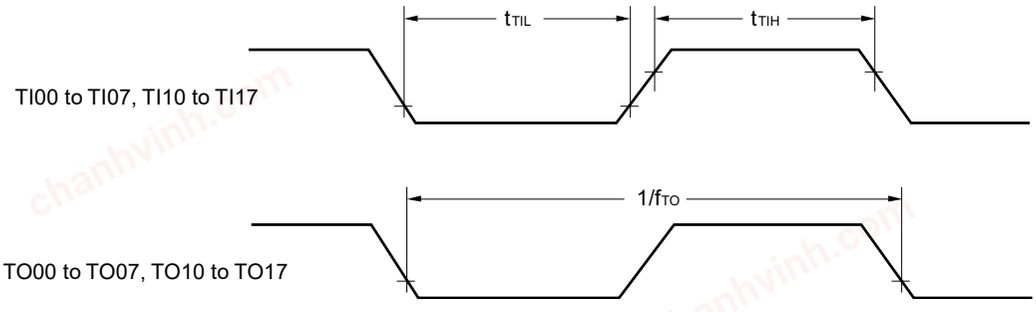
AC Timing Test Points



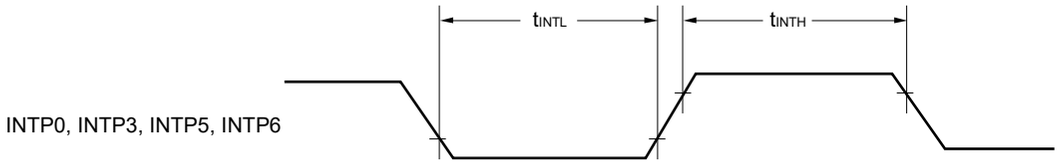
External System Clock Timing



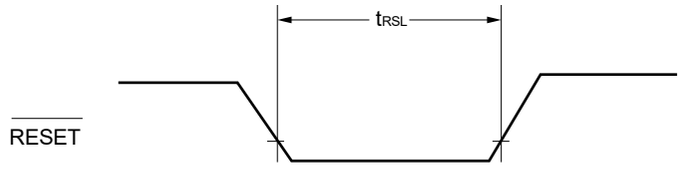
TI/TO Timing



Interrupt Request Input Timing



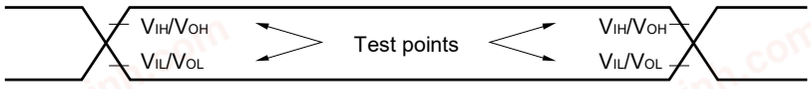
$\overline{\text{RESET}}$ Input Timing



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2.7 Peripheral Functions Characteristics

AC Timing Test Points



2.7.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode	LS (low-speed main) Mode	LV (low-voltage main) Mode	Unit
			MAX.	MAX.	MAX.	
Transfer rate Note 1		2.4 V ≤ V_{DD} ≤ 3.6 V	f_{MCK}/6	f_{MCK}/6	f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2	5.3	1.3	0.6	Mbps
		1.8 V ≤ V_{DD} ≤ 3.6 V	–	f_{MCK}/6	f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2	–	1.3	0.6	Mbps
		1.6 V ≤ V_{DD} ≤ 3.6 V	–	–	f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2	–	–	0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

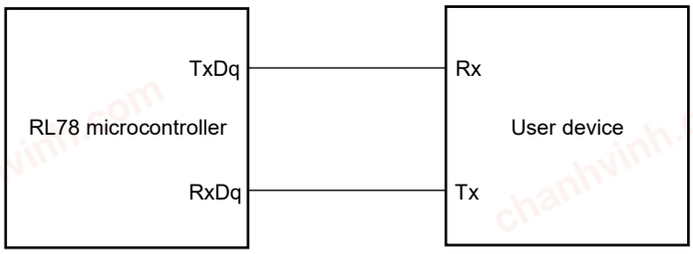
2. Maximum operating frequency of CPU and peripheral hardware clock (f_{CLK}) is following

HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 3.6 V)

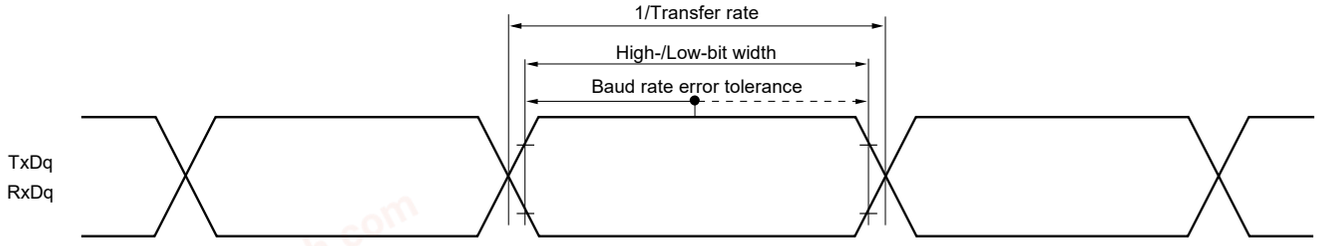
Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

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UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

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(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, supporting CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	83.3		250		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 10$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}		33		110		110		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO1}	C = 20 pF Note 3		10		10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. This specification is valid only when CSI00’s peripheral I/O redirect function is not used.

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

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(3) During communication at same potential (CSI mode) (Internal communication, supporting CSI21 only)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ $2/f_{CLK}$ Note	2.4 V ≤ V_{DD} ≤ 3.6 V	250		250		500		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		250		500		ns
			1.6 V ≤ V_{DD} ≤ 3.6 V	–		–		500		ns

Note Use the f_{CLK} more than 6.5 MHz and lower than 24 MHz.

Remark This specification is for CSI21 only.

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(4) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, supporting CSI00 and CSI20)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/ f_{CLK}	2.7 V ≤ V_{DD} ≤ 3.6 V	125		500		1000		ns
			2.4 V ≤ V_{DD} ≤ 3.6 V	250		500		1000		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		500		1000		ns
			1.6 V ≤ V_{DD} ≤ 3.6 V	–		–		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 – 38		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		t_{KCY1}/2 – 100		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		44		110		110		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		75		110		110		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		110		110		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		220		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V		19		19		19		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		19		19		19		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		19		19		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		19		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO1}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 3.6 V		25		25		25	ns
			2.4 V ≤ V_{DD} ≤ 3.6 V		25		25		25	ns
			1.8 V ≤ V_{DD} ≤ 3.6 V		–		25		25	ns
			1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 11))

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(5) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input, supporting CSI00 and CSI20)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V	f_{MCK} > 16 MHz	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		
		2.4 V ≤ V_{DD} ≤ 3.6 V		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		6/f_{MCK} and 1500		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY2}/2–8		t_{KCY2}/2–8		t_{KCY2}/2–8		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		t_{KCY2}/2–18		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		t_{KCY2}/2 – 66		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		1/f_{MCK} +40		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		1/f_{MCK} +250		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 3.6 V		2/f_{MCK}+ 44		2/f_{MCK}+ 110		2/f_{MCK}+ 110	ns
			2.4 V ≤ V_{DD} ≤ 3.6 V		2/f_{MCK}+ 75		2/f_{MCK}+ 110		2/f_{MCK}+ 110	ns
			1.8 V ≤ V_{DD} ≤ 3.6 V		–		2/f_{MCK}+ 110		2/f_{MCK}+ 110	ns
			1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		2/f_{MCK}+ 220	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SOp output lines.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

(**Caution** and **Remarks** are listed on the next page.)

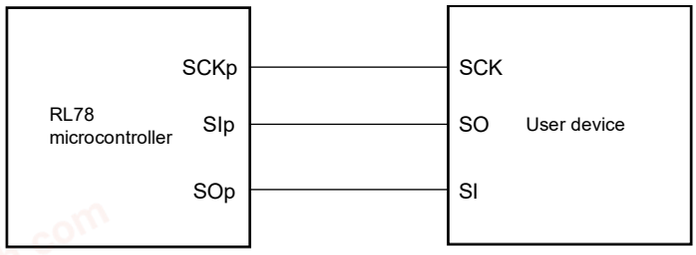
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Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1),
n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

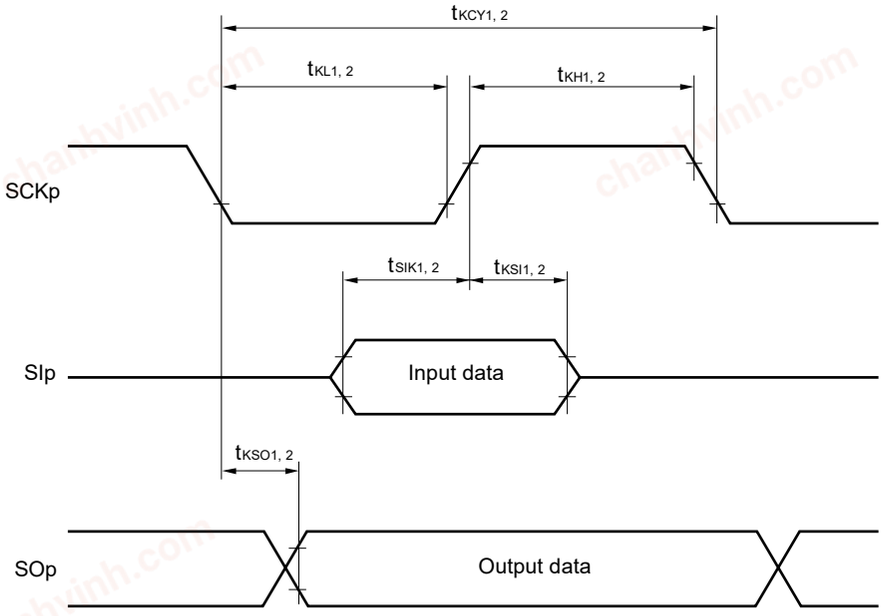
2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 10))

CSI mode connection diagram (during communication at same potential)

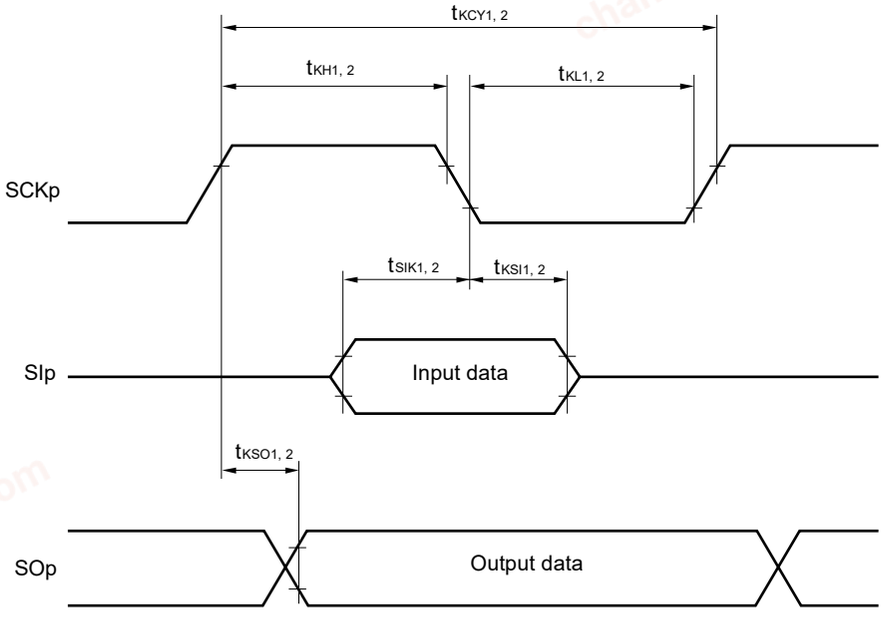


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CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 10, 21)

2. m: Unit number, n: Channel number (mn = 00, 02, 11)

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(6) During communication at same potential (simplified I^2C mode) (1/2)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ		–		400 Note 1		400 Note 1	kHz
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		–		300 Note 1		300 Note 1	kHz
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		–		–		250 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ	–		1150		1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	–		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1850		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ	–		1150		1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	–		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1850		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

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(6) During communication at same potential (simplified I^2C mode) (2/2)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note2		1/f_{MCK} + 145 Note2		1/f_{MCK} + 145 Note2		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note2		1/f_{MCK} + 145 Note2		1/f_{MCK} + 145 Note2		ns
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ	–		1/f_{MCK} + 145 Note2		1/f_{MCK} + 145 Note2		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 Note2		1/f_{MCK} + 230 Note2		1/f_{MCK} + 230 Note2		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	–		1/f_{MCK} + 230 Note2		1/f_{MCK} + 230 Note2		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1/f_{MCK} + 290 Note2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ	–	–	0	355	0	355	ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	–	–	0	405	0	405	ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–	–	–	–	0	405	ns

Note 1. The value must also be f_{MCK}/4 or lower.

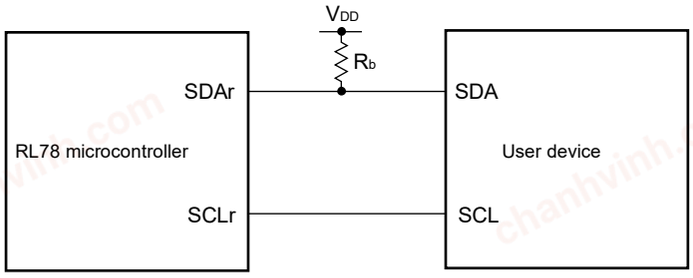
2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

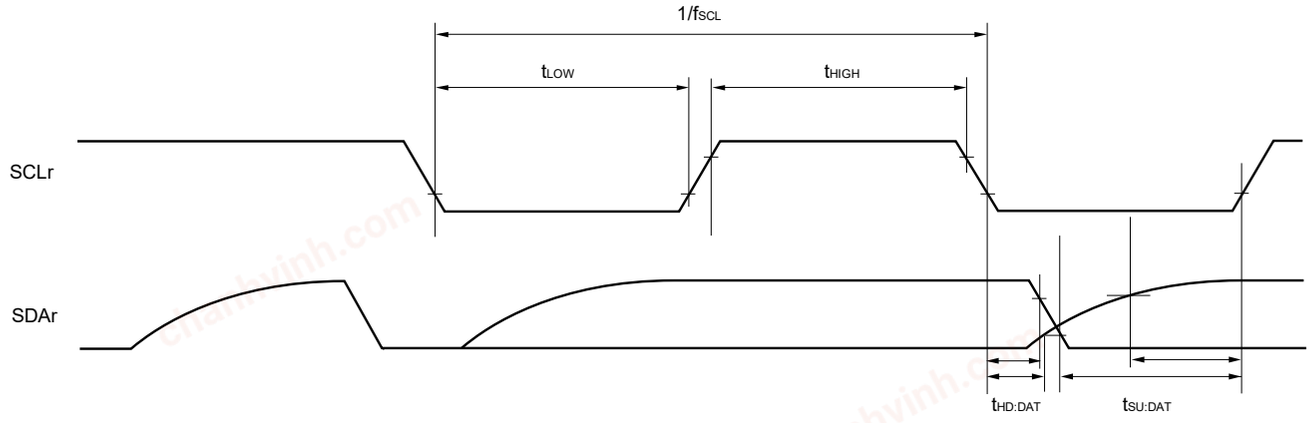
(**Remarks** are listed on the next page.)

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Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. R_b[Ω]:Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 20), g: PIM number (g =1), h: POM number (h = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clockw to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0), mn = 00, 02)

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(7) Communication at different potential (1.8 V, 2.5 V) (UART mode)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode	LS (low-speed main) Mode	LV (low-voltage main) Mode	Unit
				MAX.	MAX.	MAX.	
Transfer rate		Reception	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	5.3	1.3	0.6	Mbps
			2.4 V ≤ V_{DD} ≤ 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	2.6	1.3	0.6	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	–	f_{MCK}/6 Note 1, 2	f_{MCK}/6 Note 1, 2	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	–	1.3	1.3	Mbps
		Transmission	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	**Note 4**	**Note 4**	**Note 4**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V	1.2 Note 5	1.2 Note 5	1.2 Note 5	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	**Note 2, 6**	**Note 2, 6**	**Note 2, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V	0.43	0.43	0.43	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	–	**Note 2, 6**	**Note 2, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V	–	0.43 Note 7	0.43 Note 7	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. Use it with $V_{DD} \geq V_b$.

3. Maximum operating frequency of CPU and peripheral hardware clock (f_{CLK}) is following

HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)
LV (low-voltage main) mode: 4 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)

4. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} ≤ 3.6 V and 2.3 V ≤ Vb ≤ 2.7 V
Maximum transfer rate = 1/{-Cb × Rb × ln (1 - 2.0/Vb)} × 3 [bps]
Baud rate error (theoretical value) =
(1/transfer rate × 2 - {-Cb × Rb × ln (1 - 2.0/Vb)} / (1/transfer rate) × number of transferred bits)
* This value is the theoretical value of the relative difference between the transmission and reception sides.

5. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8V ≤ V_{DD} < 3.3 V and 1.6 V ≤ Vb ≤ 2.0 V

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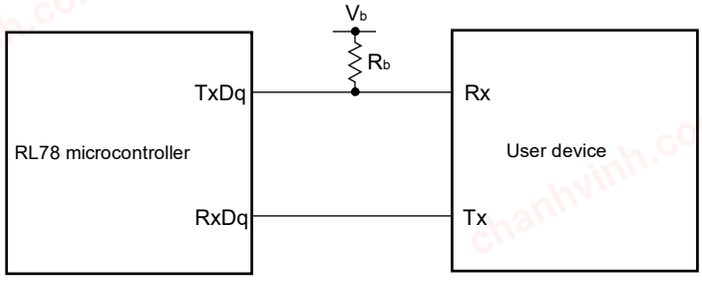
Maximum transfer rate = 1/{-Cb × Rb × ln (1 - 1.5/Vb)} × 3 [bps]
Baud rate error (theoretical value) =
(1/transfer rate × 2 - {-Cb × Rb × ln (1 - 1.5/Vb)} / (1/transfer rate) × number of transferred bits)

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

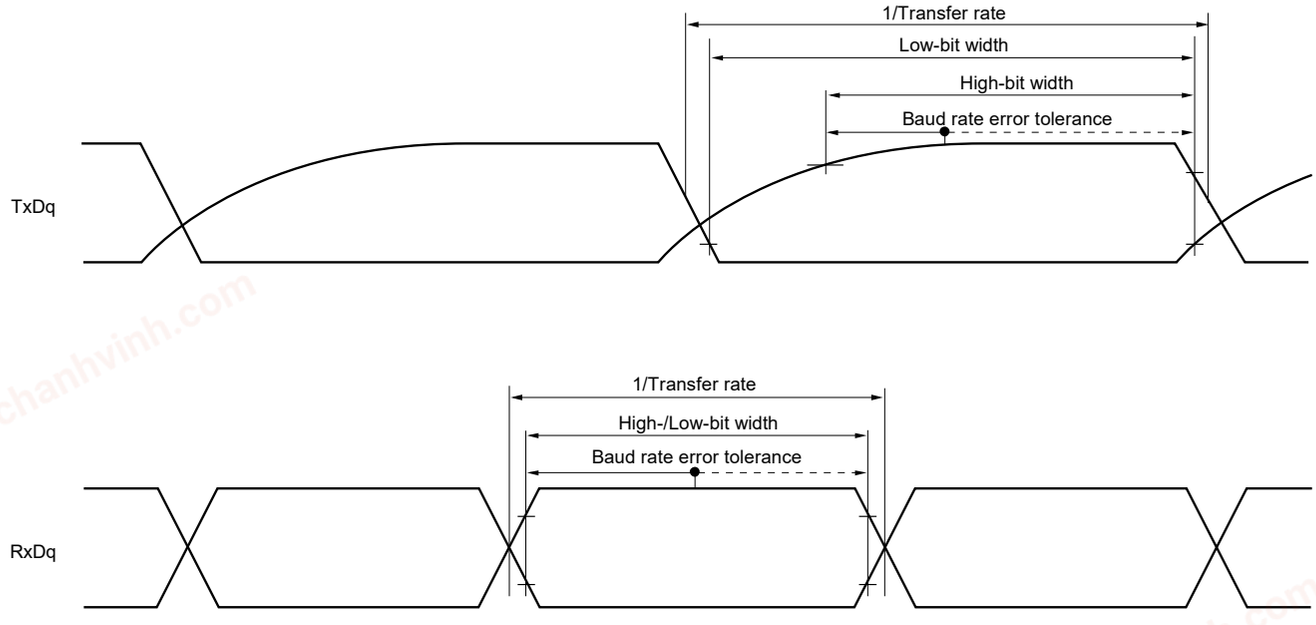
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. R_b[Ω]:Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage
2. q: UART number (q = 0, 1), g: PIM and POM numbers (g = 0, 1)
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage
2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

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(8) Communication at different potential (2.5 V) (CSI mode) (master mode: SCKp... internal clock output, supporting CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 2/f_{CLK} 2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 10		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	121		479		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ		130		130		130	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	33		110		110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ		10		10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

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(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode: master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
			2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
			1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 3 C_b = 30 pF, R_b = 5.5 kΩ	–		1150		1150		ns
SCKp high-level width Note 1	t_{KH1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2-170		t_{KCY1}/2-170		t_{KCY1}/2-170		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2-458		t_{KCY1}/2-458		t_{KCY1}/2-458		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3 C_b = 30 pF, R_b = 5.5 kΩ		–		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
SCKp low-level width Note 1	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3 C_b = 30 pF, R_b = 5.5 kΩ		–		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1, 2	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		177		479		479		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		479		479		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3 C_b = 30 pF, R_b = 5.5 kΩ		–		479		479		ns
SIp hold time (from SCKp↑) Note 1, 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		19		19		19		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3 C_b = 30 pF, R_b = 5.5 kΩ		–		19		19		ns

Note 1. Supporting CSI00 and CSI20.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

3. Use it with V_{DD} ≥ V_b.

(**Caution** is listed on the next page.)

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(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↓ to SOp output Note 1, 3	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ		–		483		483	ns
SIp setup time (to SCKp↓) Note 2, 4	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ	–		110		110		ns
SIp hold time (from SCKp↓) Note 2, 4	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ	–		19		19		ns
Delay time from SCKp↑ to SOp output Note 2, 4	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ		–		25		25	ns

Note 1. Supporting CSI00 and CSI20.

2. Supporting CSI00 only.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

4. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

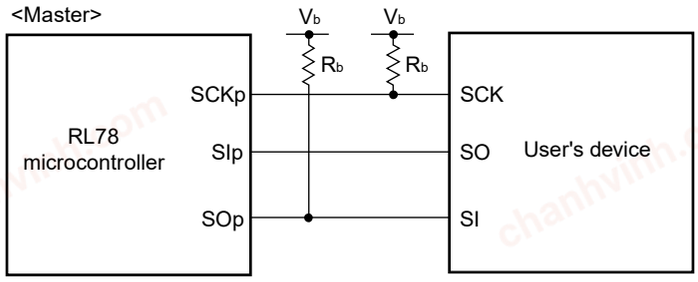
5. Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

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CSI mode connection diagram (during communication at different potential)



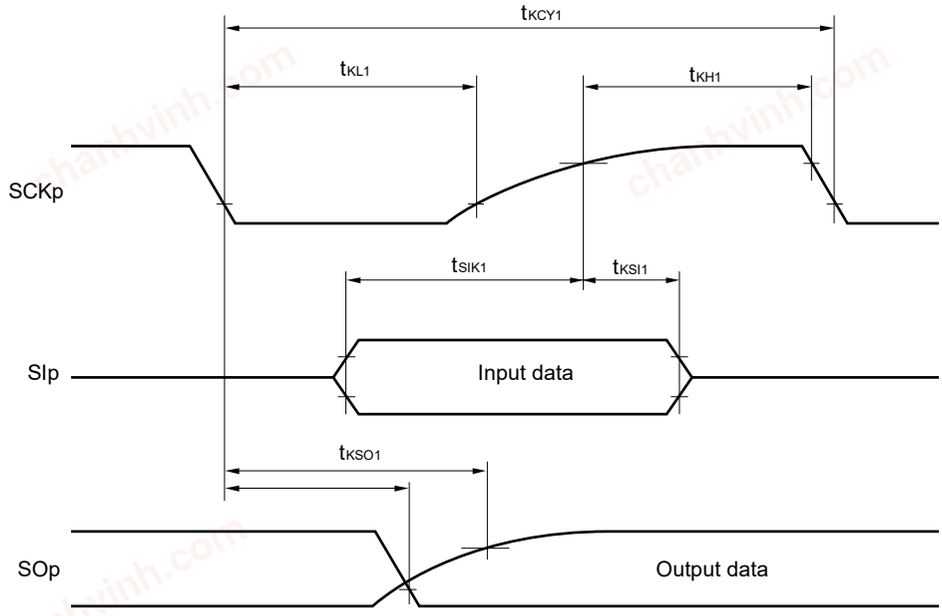
Remark 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

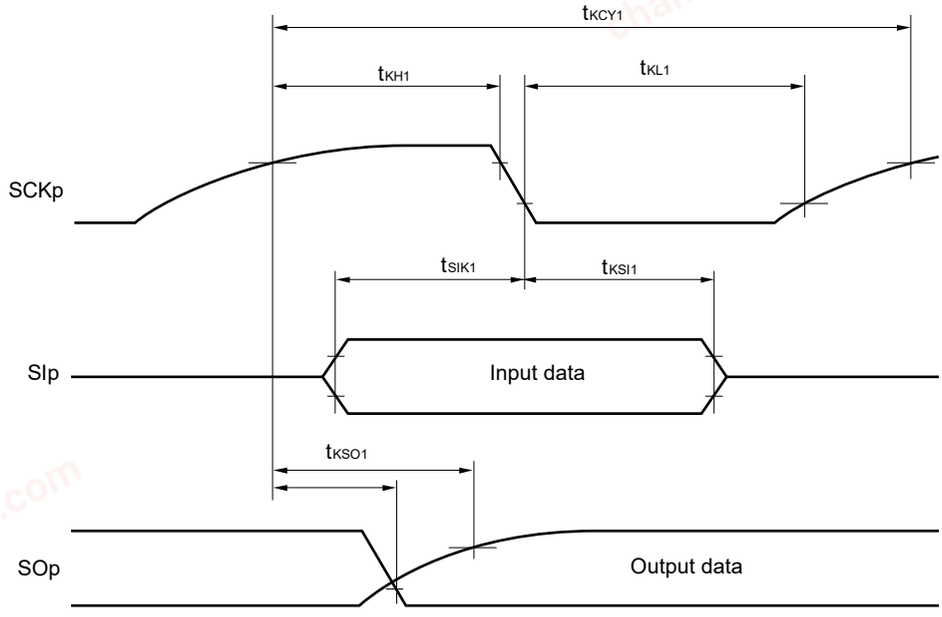
3. f_{MCK} : Operation clock frequency of the serial array unit
(Operation clock to be set by the CKSmn bit of the serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

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CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

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(10) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/ f_{MCK}		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/ f_{MCK}		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/ f_{MCK}		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/ f_{MCK}		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/ f_{MCK}		–		ns
			f_{MCK} ≤ 4MHz	6/f_{MCK}		10/ f_{MCK}		10/ f_{MCK}		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V	24 MHz < f_{MCK}	48/ f_{MCK}		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/ f_{MCK}		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/ f_{MCK}		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/ f_{MCK}		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/ f_{MCK}		16/ f_{MCK}		–		ns
			f_{MCK} ≤ 4MHz	10/ f_{MCK}		10/ f_{MCK}		10/ f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2	24 MHz < f_{MCK}	–		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	–		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	–		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	–		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	–		16/ f_{MCK}		–		ns
			f_{MCK} ≤ 4MHz	–		10/ f_{MCK}		10/ f_{MCK}		ns

(**Notes** and **Caution** are listed on the next page.)

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(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V	t_{KCY2}/2 – 18		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V	t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		1.8 V ≤ V_{DD}<3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2	–		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V	1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD}<3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2	–		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI2}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V	1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V ≤ V_{DD}<3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2	–		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO2}	2.7 V ≤ V_{DD} < 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ V_{DD}< 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 30 pF, R_b = 5.5 kΩ		–		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Note 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. Use it with V_{DD} ≥ V_b.

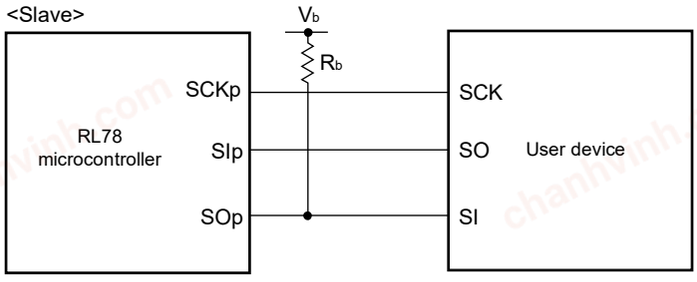
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

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CSI mode connection diagram (during communication at different potential)



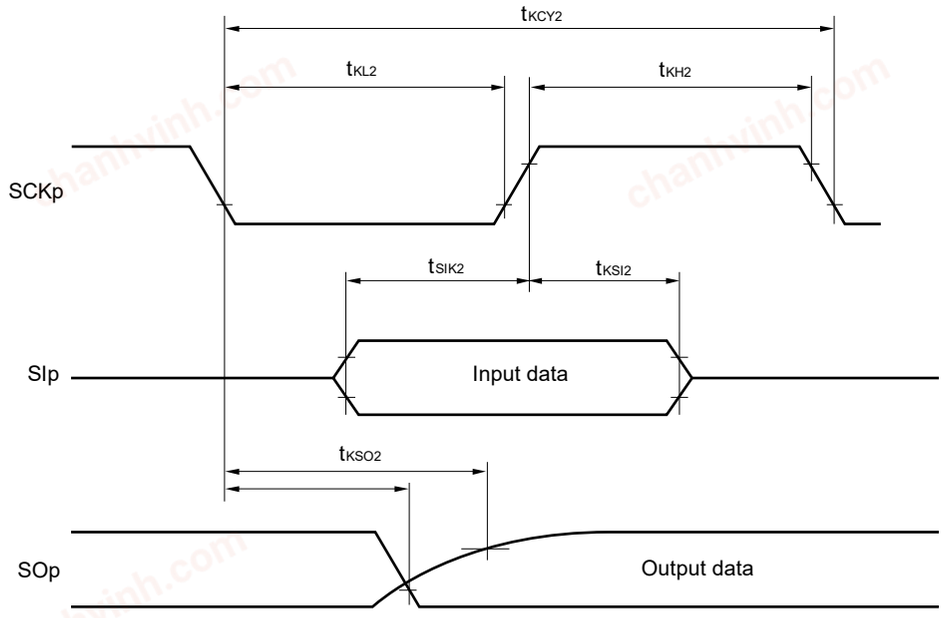
Remark 1. R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number, n: Channel number (mn = 00, 10), g: PIM and POM number (g = 0, 1)

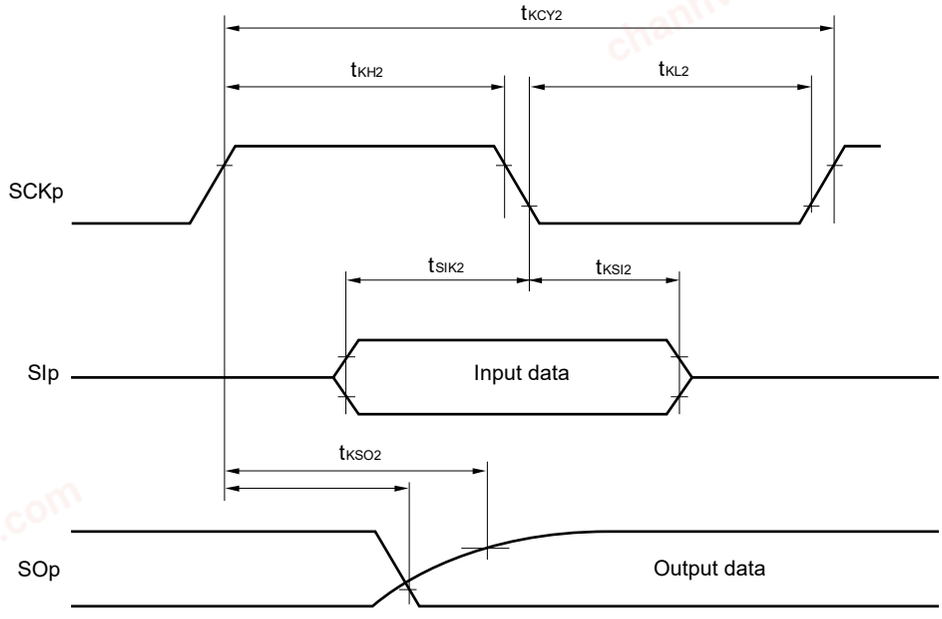
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 10))

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CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

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(11) Communication at different potential (1.8 V, 2.5 V) (simplified I^2C mode)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		300 Note 5		300 Note 5	kHz
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1		300 Note 5		300 Note 5	kHz
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ		–		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	1150		1550		1550		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	1150		1550		1550		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–		1550		1550		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	200		610		610		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	600		610		610		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	610		610		610		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–		610		610		ns

(**Note, Caution** and **Remarks** are listed on the next page.)

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(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	0 Note 4	305	0 Note 4	305	0 Note 4	305	ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	0 Note 4	355	0 Note 4	355	0 Note 4	355	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	0 Note 4	405	0 Note 4	405	0 Note 4	405	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–	–	0 Note 4	405	0 Note 4	405	ns

Note 1. The value must also be f_{MCK}/4 or lower.

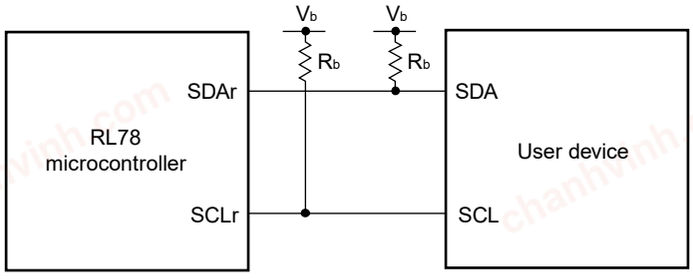
2. Use it with V_{DD} ≥ V_b.

3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

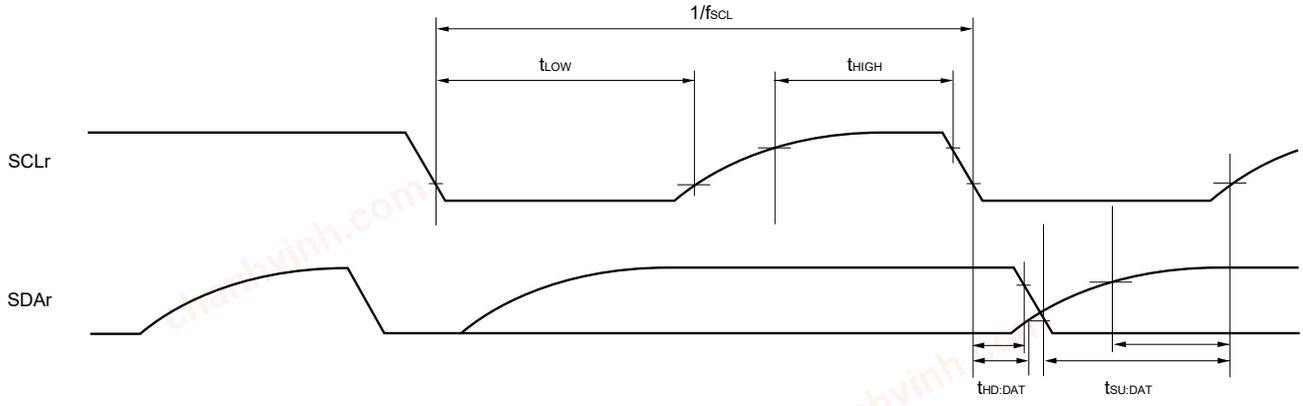
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

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Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

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2.7.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	100	0	100	0	100	kHz
			2.4 V ≤ V_{DD} ≤ 3.6 V	0	100	0	100	0	100	kHz
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		0	100	0	100	kHz
			1.6 V ≤ V_{DD} ≤ 3.6 V	–		–		0	100	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		4.7		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		4.7		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		4.7		4.7		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		4.7		µs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		4.0		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		4.0		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		4.0		4.0		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		4.0		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		4.7		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		4.7		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		4.7		4.7		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		4.7		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		4.0		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		4.0		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		4.0		4.0		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		4.0		µs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		250		250		250		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		250		250		250		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		250		250		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		250		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	3.45	0	3.45	0	3.45	µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0	3.45	0	3.45	0	3.45	µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0	3.45	0	3.45	µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		0	3.45	µs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		4.0		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		4.0		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		4.0		4.0		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		4.0		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		4.7		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		4.7		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		4.7		4.7		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		4.7		µs

(**Notes**, **Caution** and **Remark** are listed on the next page.)

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Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

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(2) I^2C fast mode

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	0	400	kHz
			2.4 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	0	400	kHz
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		0	400	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0.6		0.6		µs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0.6		0.6		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		1.3		1.3		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0.6		0.6		µs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		100		100		100		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		100		100		100		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		100		100		µs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	0.9	0	0.9	0	0.9	µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0	0.9	0	0.9	0	0.9	µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0	0.9	0	0.9	µs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0.6		0.6		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		µs
		2.4 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		1.3		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

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(3) I^2C fast mode plus

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz, 2.7 V ≤ V_{DD} ≤ 3.6 V	0	1000	–		–		kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V	0.26		–		–		µs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V	0.26		–		–		µs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V	0.5		–		–		µs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V	0.26		–		–		µs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V	50		–		–		µs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V	0	0.45	–		–		µs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V	0.26		–		–		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V	0.5		–		–		µs

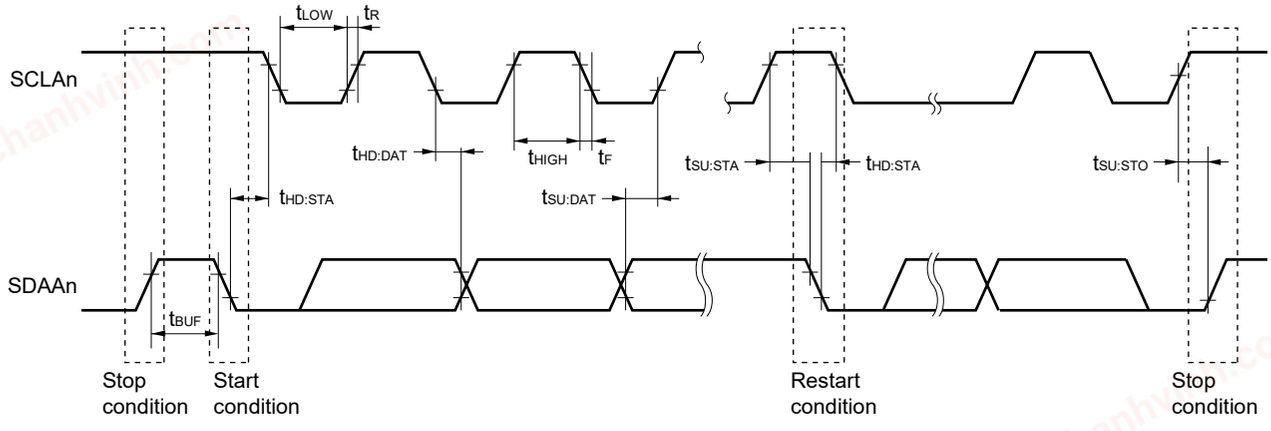
Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0

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2.8 Analog Characteristics

2.8.1 A/D converter characteristics

A/D convertor characteristics category

Reference voltage / Input channel	Ref. voltage(+) = AV_{REFP} Ref. voltage(–) = AV_{REFM}	Ref. voltage(+) = V_{DD} Ref. voltage(–) = V_{SS}	Ref. voltage(+) = V_{BGR} Ref. voltage(–) = AV_{REFM}
ANI0	-	Refer to **2.8.1 (3)**	Refer to **2.8.1 (4)**
ANI1			-
ANI2, ANI3	Refer to **2.8.1 (1)**		Refer to **2.8.1 (4)**
ANI16 to ANI19	Refer to **2.8.1 (2)**		
Internal reference voltage, Temperature sensor output voltage	Refer to **2.8.1 (1)**		-

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), conversion target : ANI2, ANI3, Internal reference voltage, Temperature sensor output voltage

(T_A = –40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V		1.2	±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4		1.2	±7.0	LSB
Conversion time	t_{conv}	10-bit resolution	2.7 V ≤ AV_{REFP} ≤ 3.6 V	3.1875		39	µs
			1.8 V ≤ AV_{REFP} ≤ 3.6 V	17		39	µs
			1.6 V ≤ AV_{REFP} ≤ 3.6 V	57		95	µs
Zero-scale error Note 1, 2	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±0.50	%FSR
Full-scale error Note 1, 2	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±0.50	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±2.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±5.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±1.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±2.0	LSB
Analog input voltage	V_{AIN}	ANI2, ANI3		0		AV_{REFP}	V
		Select internal reference voltage 2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode		V_{BGR} Note 5			V
		Select temperature sensor output voltage 2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode		V_{TMPS25} Note 5			V

Note 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, MAX. value is following.

Overall error: ±1 LSB is added to the MAX. value of AV_{REFP} = V_{DD}.

Zero-scale error / Full-scale error: ±0.05 %FSR is added to the MAX. value of AV_{REFP} = V_{DD}.

Integral linearity error / Differential linearity error: ±0.5 LSB is added to the MAX. value of AV_{REFP} = V_{DD}.

4. When the the conversion time is set to 57 µs (min.) and 95 µs (max.).

5. Refer to **2.8.2 Temperature sensor and internal reference voltage characteristics**.

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(2) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), conversion target : ANI16 to ANI19

(T_A = –40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V		1.2	±5.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4		1.2	±8.5	LSB
Conversion time	T_{conv}	10-bit resolution	2.7 V ≤ V_{DD} ≤ 3.6 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
			1.6 V ≤ AV_{REFP} ≤ 3.6 V	57		95	µs
Zero-scale error Note 1, 2	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±0.60	%FSR
Full-scale error Note 1, 2	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±2.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±2.5	LSB
Analog input voltage	V_{AIN}			0		AV_{REFP} and V_{DD}	V

Note 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, MAX. value is following.

Overall error: ±4 LSB is added to the MAX. value of AV_{REFP} = V_{DD}.

Zero-scale error / Full-scale error: ±0.2 %FSR is added to the MAX. value of AV_{REFP} = V_{DD}.

Integral linearity error / Differential linearity error: ±2 LSB is added to the MAX. value n of AV_{REFP} = V_{DD}.

4. When the the conversion time is set to 57 µs (min.) and 95 µs (max.).

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(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), conversion target : ANI0 to ANI3, ANI16 to ANI19, Internal reference voltage, Temperature sensor output voltage

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3		1.2	±10.5	LSB
Conversion time	T_{cony}	10-bit resolution conversion target : ANI0 to ANI3, ANI16 to ANI19	2.7 V ≤ V_{DD} ≤ 3.6 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
			1.6 V ≤ V_{DD} ≤ 3.6 V	57		95	µs
		10-bit resolution conversion target : Internal reference voltage, Temperature sensor output voltage (HS (high-speed main) Mode)	2.7 V ≤ V_{DD} ≤ 3.6 V	3.5635		39	µs
			2.7 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
Zero-scale error Note 1, 2	E_{ZS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±0.85	%FSR
Full-scale error Note 1, 2	E_{FS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±0.85	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±4.0	LSB
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±6.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±2.0	LSB
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±2.5	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI3, ANI16 to ANI19		0		V_{DD}	V
		Select internal reference voltage 2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode		V_{BGR} Note 4			V
		Select temperature sensor output voltage 2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode		V_{TMPS25} Note 4			V

Note 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the the conversion time is set to 57 µs (min.) and 95 µs (max.).

4. Refer to **2.8.2 Temperature sensor and internal reference voltage characteristics**

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(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), conversion target : ANI0 to ANI3, ANI16 to ANI19

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	T_{cony}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
Zero-scale error Note 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 2**.8.2 Temperature sensor and internal reference voltage characteristics.**

4. When reference voltage (-) = V_{SS}, MAX. value is following.

Zero-scale error: ±0.35 %FSR is added to the MAX. value of reference voltage (–) = AV_{REFM}.

Integral linearity error: ±0.5 LSB is added to the MAX. value of reference voltage (–) = AV_{REFM}.

Differential linearity error: ±0.2 LSB is added to the MAX. value of reference voltage (–) = AV_{REFM}.

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2.8.2 Temperature sensor and internal reference voltage characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, HS (high-speed main) mode)

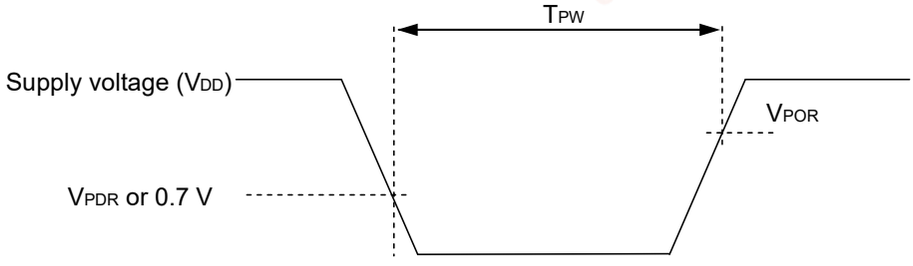
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

2.8.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Rise time	1.47	1.51	1.55	V
	V_{PDR}	Fall time	1.46	1.50	1.54	V
Minimum pulse width[Note]	T_{PW}	Other than STOP/SUB_RUN/SUB_HALT	300			μs

Note This is the time required for the POR circuit to execute a reset operation when V_{DD} falls below V_{PDR}. When the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC) or when the microcontroller enters STOP mode, this is the time required for the POR circuit to execute a reset operation between when V_{DD} falls below 0.7 V and when V_{DD} rises to V_{POR} or higher.



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2.8.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode
(T_A = –40 to +85°C, $V_{PDR} \le V_{DD} = V_{DD_RF} = AV_{DD_RF} \le 3.6$ V, $V_{SS} = V_{SS_RF} = AV_{SS_RF}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage	V_{LVI2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3	3.06	3.12	V
		V_{LVI3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.9	2.96	3.02	V
		V_{LVI4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.8	2.86	2.91	V
		V_{LVI5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.7	2.75	2.81	V
		V_{LVI6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.6	2.65	2.7	V
		V_{LVI7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.5	2.55	2.6	V
		V_{LVI8}	Power supply rise time	2.45	2.5	2.55	V
			Power supply fall time	2.4	2.45	2.5	V
		V_{LVI9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2	2.04	2.08	V
		V_{LVI10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.9	1.94	1.98	V
		V_{LVI11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.8	1.84	1.87	V
		V_{LVI12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.7	1.73	1.77	V
		V_{LVI13}	Power supply rise time	1.64	1.67	1.7	V
			Power supply fall time	1.6	1.63	1.66	V
Minimum pulse width		T_{LW}		300			μs
Detection delay time						300	μs

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LVD Detection Voltage of Interrupt & Reset Mode
(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDA0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V_{LVDA1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.8	1.84	1.87	V
	V_{LVDA3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V_{LVDB1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V

2.8.5 Supply voltage rise time

(T_A = –40 to +85°C, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} rise slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.6 AC Characteristics.

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2.9 RF Transceiver Characteristics

2.9.1 RF transmission characteristics

Unless specified otherwise, the measurement is performed by our evaluation board.

(T_A = +25°C, V_{DD} = V_{DD_RF} = AV_{DD_RF} = 3.0 V, f = 2440 MHz, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RF frequency range	RF_{CF}			2402		2480	MHz
Data rate	RF_{DATA}				1		Mbps
Maximum transmitted output power	RF_{POWER}	RF output pin	RF low power mode	-18	-15	-12	dBm
			RF normal mode	-3	0	3	dBm
			RF high performance mode	-3	0	3	dBm
Transmitted output power setting	RF_{TXPOW}	0, -1, -2, -7, -10, -15 dBm		-15		0	dBm
Spurious radiation	RF_{TXSP}	30 to 88 MHz			-76	-55	dBm
		88 to 216 MHz			-76	-52	dBm
		216 to 960 MHz			-74	-49	dBm
		960 to 1000 MHz			-74	-30	dBm
		1 to 12.75 GHz			-42	-41	dBm
		1.8 to 1.9 GHz			-73	-47	dBm
		5.15 to 5.3 GHz			-71	-47	dBm
Harmonics	RF_{TXHC1}	2nd Harmonics			-52	-41	dBm
	RF_{TXHC2}	3rd Harmonics			-51	-41	dBm
Frequency tolerance	RF_{TXFERR}			-30		+30	ppm
Impedance	RF_{Z1}				50+j0		Ω

Caution Install EMI countermeasures as required to prevent EMI effects of the RF transmission characteristics.

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2.9.2 RF reception characteristics

Unless specified otherwise, the measurement is performed by our evaluation board.

(T_A = +25°C, V_{DD} = V_{DD_RF} = AV_{DD_RF} = 3.0 V, f = 2440 MHz, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

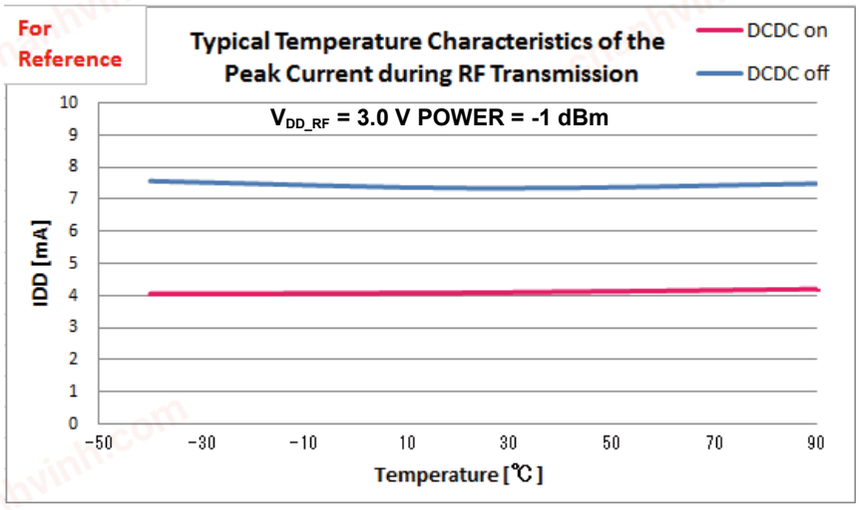
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RF input frequency	RF_{RXFRIN}			2402		2480	MHz
Maximum input level	RF_{LEVL}	PER ≤ 30.8% RF input pin	RF low power mode	-10	0	-	dBm
			RF normal mode	-10	1	-	dBm
			RF high performance mode	-10	1	-	dBm
Receiver sensitivity	RF_{STY}	PER ≤ 30.8%	RF low power mode	-	-60	-50	dBm
			RF normal mode	-	-90	-70	dBm
			RF high performance mode	-	-92	-70	dBm
Secondary radiation	RF_{RXSP}		30 MHz to 1 GHz	-	-72	-57	dBm/ 100 kHz
			1 GHz to 12 GHz	-	-57	-54	dBm/ 100 kHz
Common channel rejection ratio	RF_{CCR}	PER ≤ 30.8%, Prf = –67dBm		-21	-12	-	dB
Adjacent channel rejection ratio	RF_{ADCR}	PER ≤ 30.8% Prf = –67 dBm	±1 MHz	-15	-5	-	dB
			±2 MHz	17	29	-	dB
			±3 MHz	27	34	-	dB
Blocking	RF_{BLK}	PER ≤ 30.8% Prf = –67 dBm	30 MHz - 2000 MHz	-30	-13	-	dB
			2000 MHz to 2399 MHz	-35	-30	-	dBm
			2484 MHz to 3000 MHz	-35	-30	-	dBm
			> 3000 MHz	-30	-17	-	dBm
Frequency tolerance	RF_{RXFERR}	PER ≤ 30.8%		-250		+250	kHz
RSSI accuracy	RF_{RSSIS}	T_A = +25°C, –70 dBm ≤ Prf ≤ –10 dBm		-4	0	4	dB

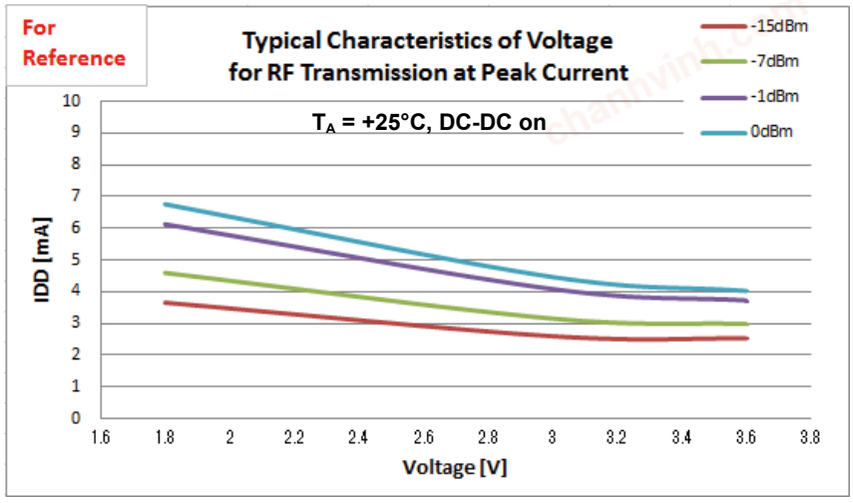
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2.9.3 Performance mapping for typical RF (Reference)

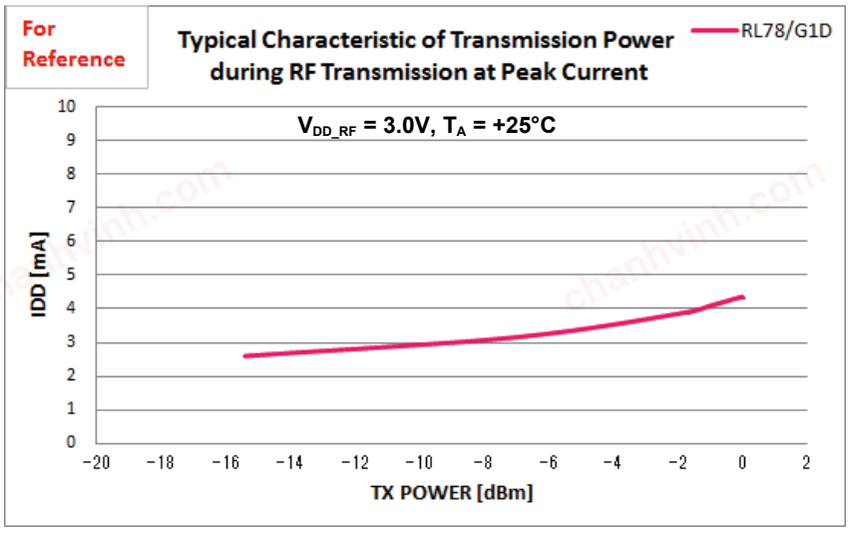
(1) Peak Current during RF Transmission

Unless specified otherwise, the measurement is performed by our evaluation board.
Current consumption is not including MCU unit.





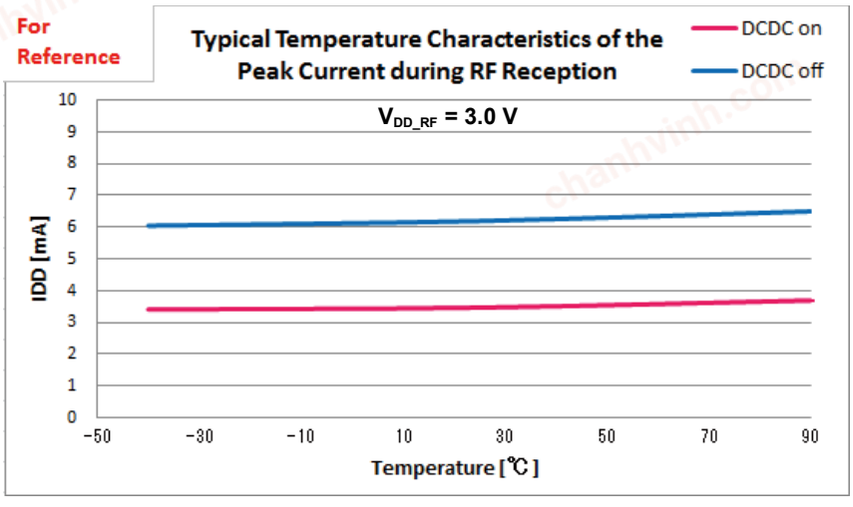
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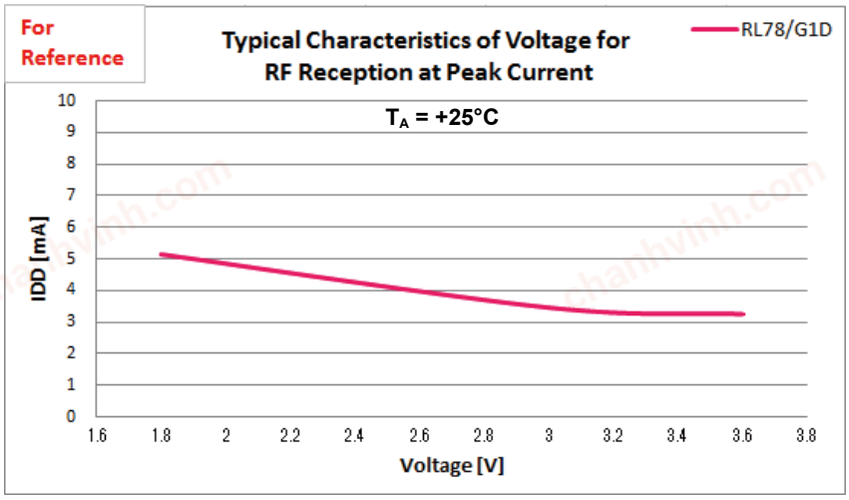
(2) Peak Current during RF Reception

Unless specified otherwise, the measurement is performed by our evaluation board.

Current consumption is not including MCU unit.

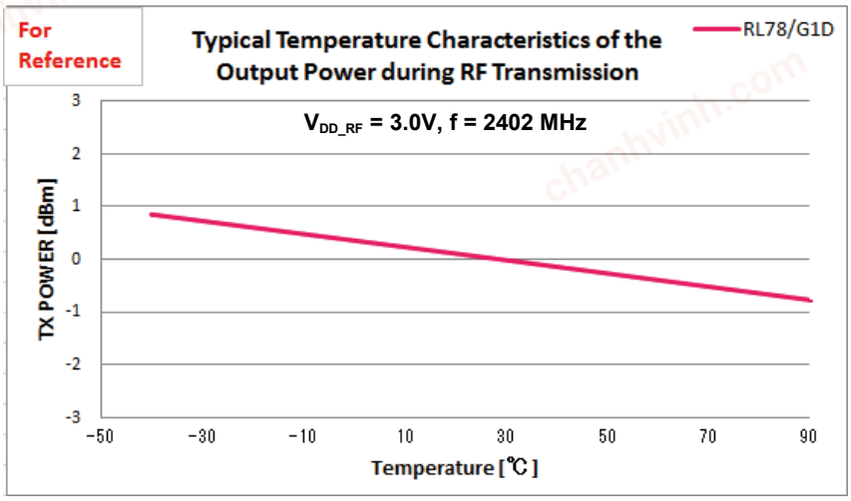


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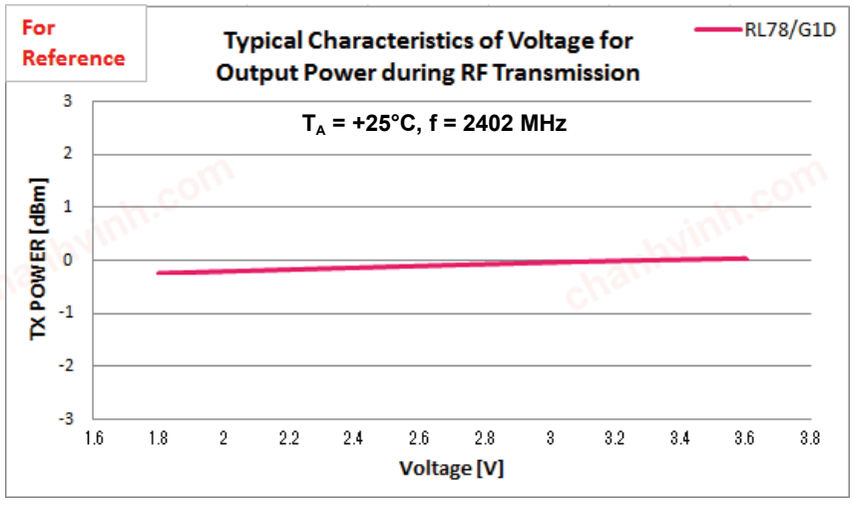


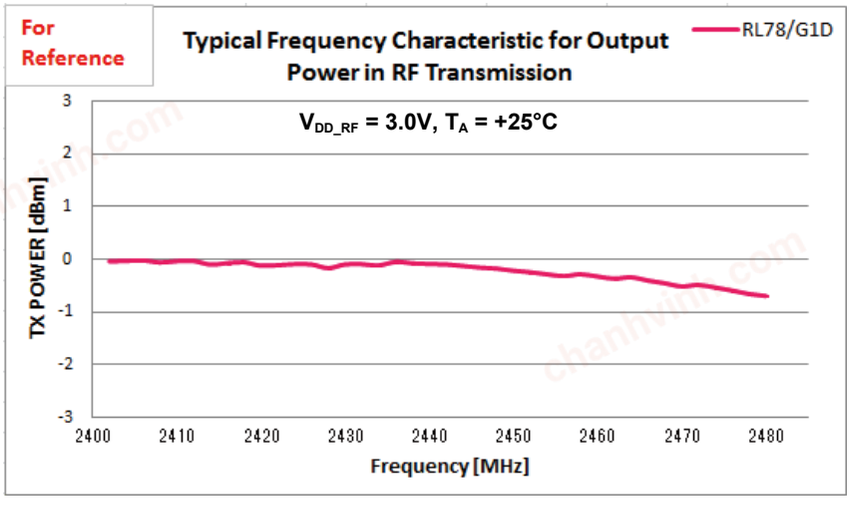
(3) RF Output Power during Transmission

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Current consumption is not including MCU unit.



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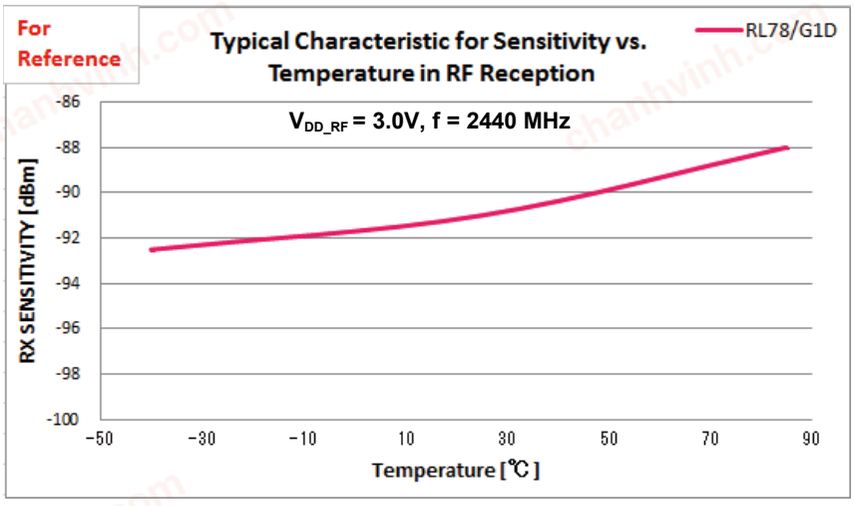


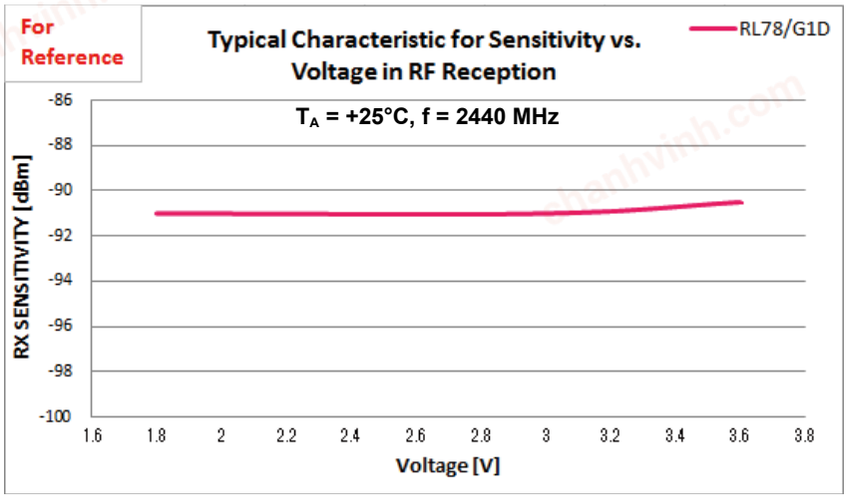
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(4) RF Reception Sensitivity

Unless specified otherwise, the measurement is performed by our evaluation board.

Current consumption is not including MCU unit.





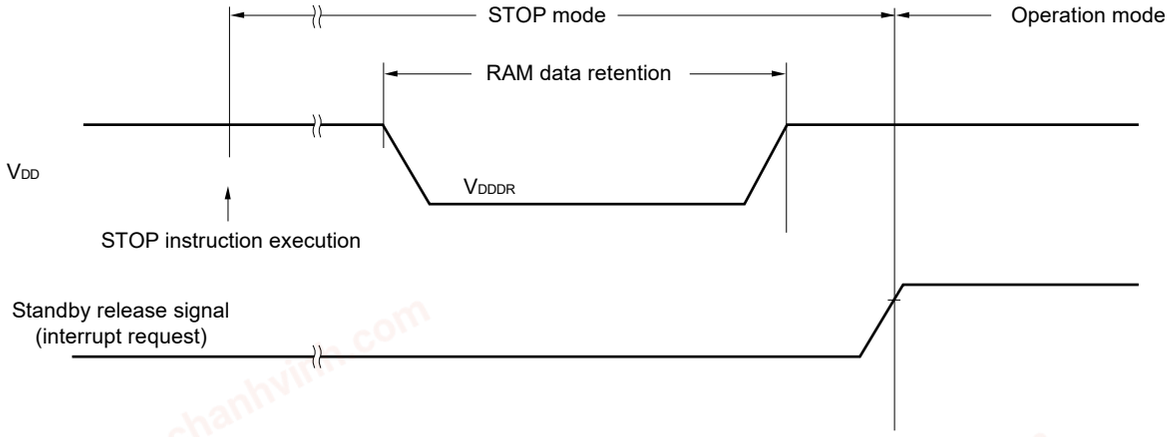
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2.10 RAM Data Retention Characteristics

(T_A = -40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.11 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 3.6 V	1		32	MHz
Number of code flash rewrites Note 1, 2, 3	C_{erwr}	Retained for 20 years, T_A = 85°C	1,000			Times
Number of data flash rewrites Note 1, 2, 3		Retained for 1 year, T_A = 25°C		1,000,000		Times
		Retained for 5 years, T_A = 85°C	100,000			Times
		Retained for 20 years, T_A = 85°C	10,000			Times

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This shows the flash memory characteristics. This is a result obtained from Renesas Electronics reliability test.

2.12 Special Flash Memory Programming Communication (UART)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

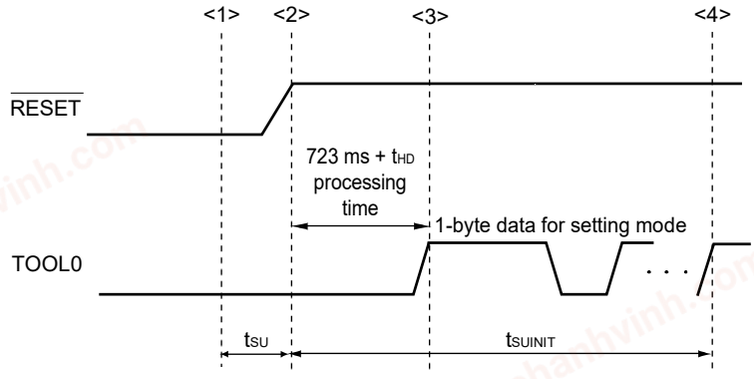
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		When programming of flash memory	115,200		1,000,000	bps

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2.13 Timing of Entry to Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.		100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10		μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1		ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

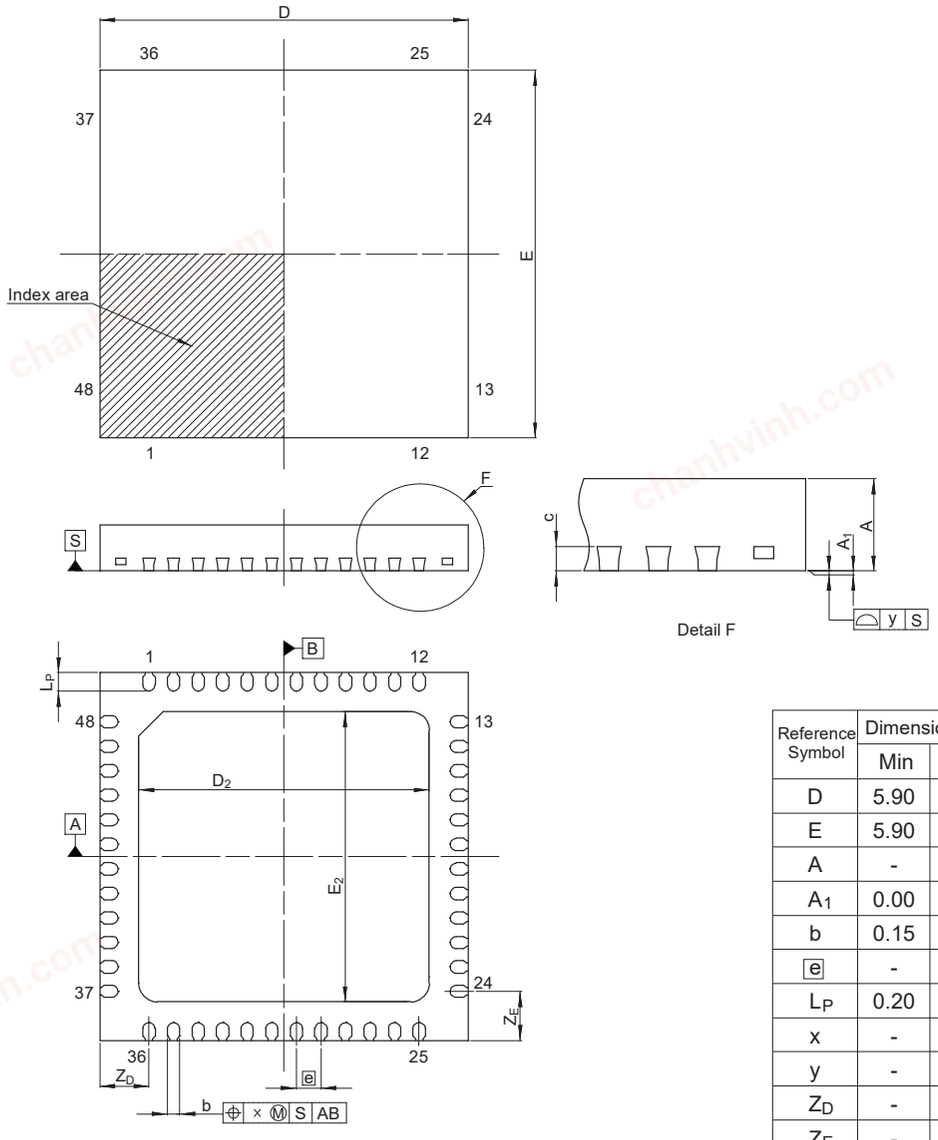
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3. PACKAGE DRAWINGS

3.1 48-pin plastic WQFN (6 × 6)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HWQFN48-6x6-0.40	PWQN0048LB-A	-	0.07

Unit: mm



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	5.90	6.00	6.10
E	5.90	6.00	6.10
A	-	-	0.80
A_1	0.00	-	-
b	0.15	0.20	0.25
e	-	0.40	-
L_P	0.20	0.30	0.40
x	-	-	0.05
y	-	-	0.05
Z_D	-	0.80	-
Z_E	-	0.80	-
c	-	0.20	-
D_2	-	4.73	-
E_2	-	4.73	-

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Revision History — RL78/G1D Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 24, 2015	-	First Edition issued
1.10	Sep 25, 2015	p.1	Change of description in 1.1 Features
		p.7, 9	Change of 1.6 Outline of Functions
		p.14	Change of description in 2.3.2 On-chip oscillator characteristics
		p.19	Change of description in 2.5. Current Consumption
		p.23	Addition of specification to 2.5.1(3) Current for each peripheral circuit
		p.65	Change of description in 2.9.1 RF transmission characteristics
		p.66	Change of description in 2.9.2 RF reception characteristics
		p.67 to 71	Change of description in 30.9.3 Performance mapping for typical RF (Reference)
1.20	Dec 16, 2016	p.4	Change of pin name in 1.3 Pin Configuration (Top View)
		p.58	Change of pin names in 2.8 Analog Characteristics (1)
		p.60	Change of pin name in 2.8 Analog Characteristics (3)
1.30	Feb 23, 2018	p.1, 7	Change of Bluetooth version
		p.1	Identification of CPU core subcode
		p.6	Change of 1.5 Block Diagram
		p.55 to 57	Change of Note 2

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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