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RL78/G1M, G1N
RENESAS MCU

R01DS0378EJ0100
Rev.1.00
May 29, 2020

1. OUTLINE

1.1 Features

Ultra-low power consumption technology

- V_{DD} = single power supply voltage of 2.0 to 5.5 V (Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage (V_{SPOR}) of the selectable power-on-reset (SPOR) circuit should also be considered.)
- HALT mode
- STOP mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.05 µs: @ 20 MHz operation with high-speed on-chip oscillator) to low speed (1.0 µs: @ 1 MHz operation)
- Address space: 1 MB
- General-purpose registers: 8-bit register × 8
- On-chip RAM: 512 B to 1 KB

Code flash memory

- Code flash memory: 4 KB to 8 KB
- On-chip debug function

High-speed on-chip oscillator

- Select from 20 MHz, 10 MHz, 5 MHz, 2.5 MHz, and 1.25 MHz
- High accuracy: ±2.0% (V_{DD} = 2.0 to 5.5 V, T_A = –20 to +85°C)

Operating ambient temperature

- T_A = –40 to +85°C

Power management and reset function

- On-chip selectable power-on-reset (SPOR) circuit

Serial interface

- CSI: 1 channel
- UART: 1 channel

Timer

- 8-/16-bit timer: 4 channels
- 12-bit interval timer: 1 channel
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)
- Real-time output function: 8 channels (RL78/G1M only)

A/D converter

- 8/10-bit resolution A/D converter (V_{DD} = 2.4 to 5.5 V)
- Analog input: 8 channels

I/O port

- I/O port: 18 (N-ch open drain output [V_{DD} withstand voltage]: 14)
  (P-ch open drain output [V_{DD} withstand voltage]: 6)
- High current pin (RL78/G1N only)
- Can be set to N-ch open drain and on-chip pull-up resistor
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

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○ ROM, RAM capacities

Flash ROM	RAM	20 Pins	
		RL78/G1M	RL78/G1N
8 KB	1 KB	R5F11W68ASM R5F11W68DSM	R5F11Y68ASM R5F11Y68DSM
4 KB	512 B	R5F11W67ASM R5F11W67DSM	R5F11Y67ASM R5F11Y67DSM

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

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1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1M, G1N

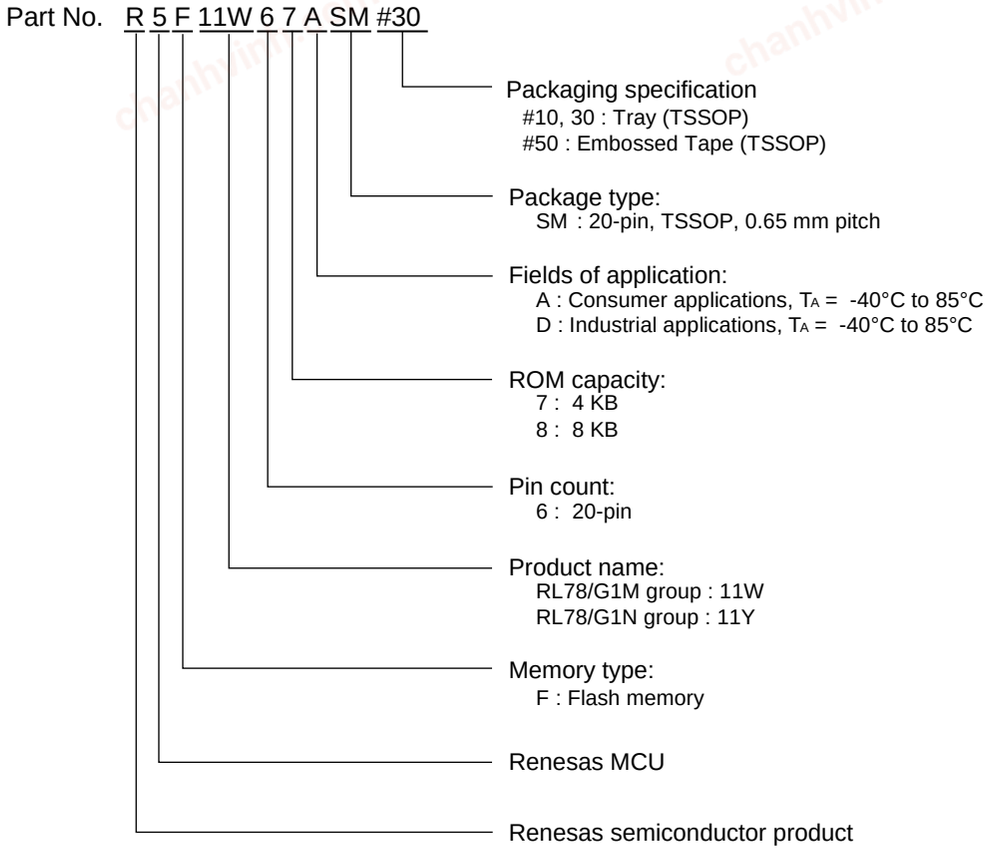


Table 1-1. List of Ordering Part Numbers

Pin Count	Package	Fields of Application[Note]	Part Number	RENESAS Code
20 pins	20-pin plastic TSSOP (4.4 × 6.5 mm, 0.65 mm pitch)	A	R5F11W67ASM#10, R5F11W68ASM#10 R5F11W67ASM#30, R5F11W68ASM#30 R5F11W67ASM#50, R5F11W68ASM#50 R5F11Y67ASM#10, R5F11Y68ASM#10 R5F11Y67ASM#30, R5F11Y68ASM#30 R5F11Y67ASM#50, R5F11Y68ASM#50	PTSP0020JI-A
		D	R5F11W67DSM#10, R5F11W68DSM#10 R5F11W67DSM#30, R5F11W68DSM#30 R5F11W67DSM#50, R5F11W68DSM#50 R5F11Y67DSM#10, R5F11Y68DSM#10 R5F11Y67DSM#30, R5F11Y68DSM#30 R5F11Y67DSM#50, R5F11Y68DSM#50	

Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1M, G1N**.

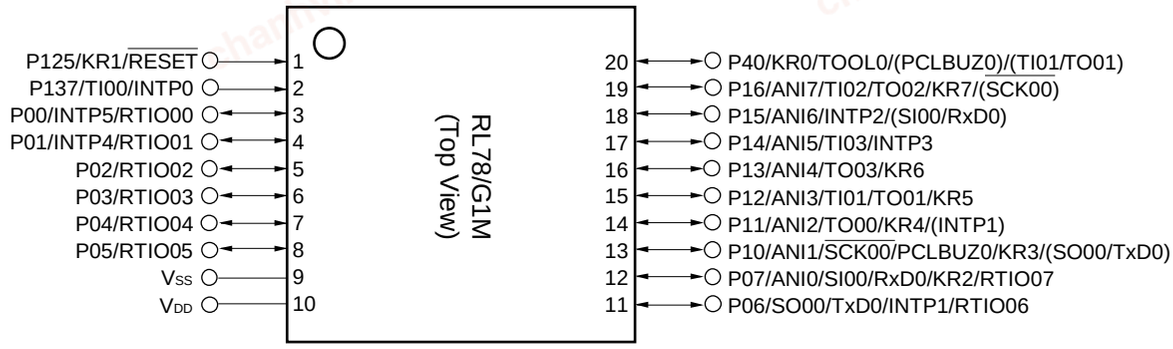
Caution The part number represents the number at the time of publication.
Be sure to review the latest part number through the target product page in the Renesas Electronics Corp. website.

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1.3 Pin Configuration (Top View)

1.3.1 RL78/G1M products

● 20-pin plastic TSSOP (4.4 × 6.5 mm, 0.65 mm pitch)

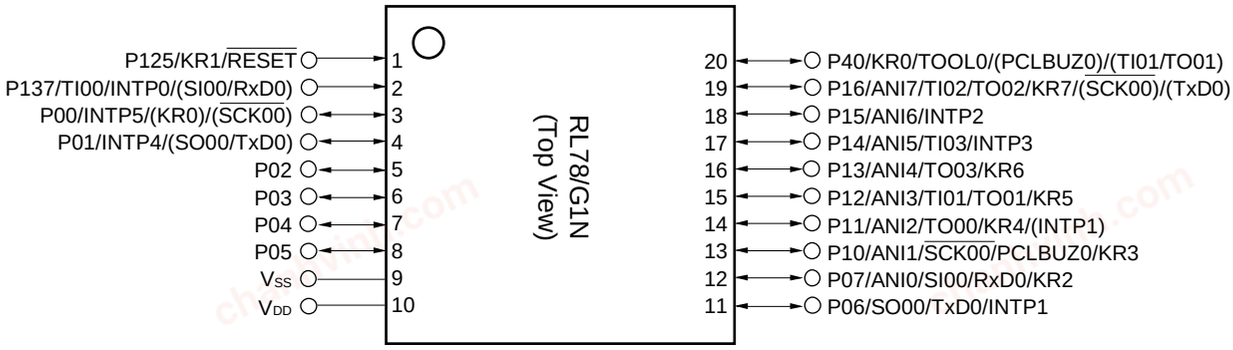


Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-7 Format of Peripheral I/O Redirection Register (PIOR)** in the **RL78/G1M, G1N User's Manual**.

1.3.2 RL78/G1N products

● 20-pin plastic TSSOP (4.4 × 6.5 mm, 0.65 mm pitch)



Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-7 Format of Peripheral I/O Redirection Register (PIOR)** in the **RL78/G1M, G1N User's Manual**.

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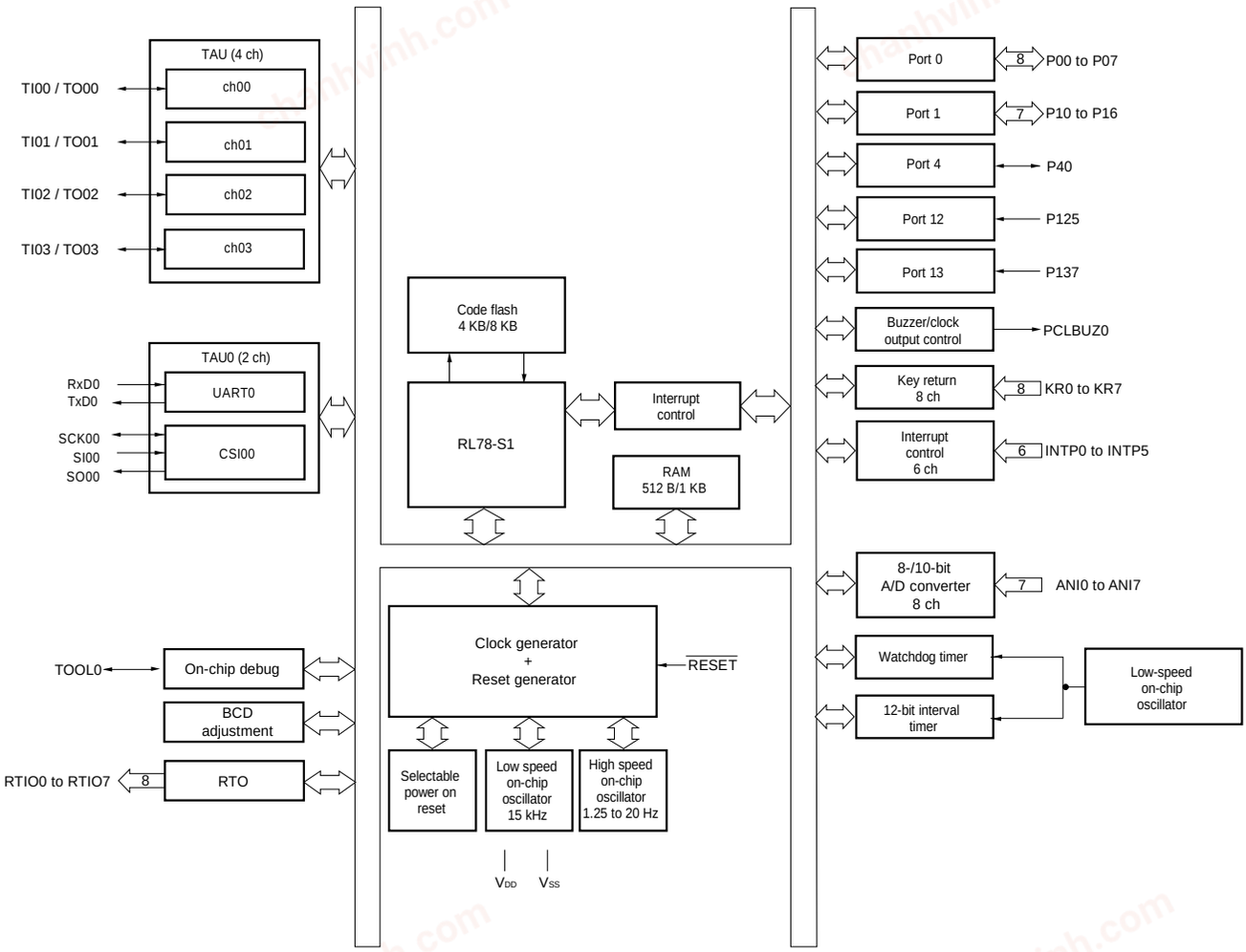
1.4 Pin Identification

ANI0 to ANI7	: Analog input
INTP0 to INTP5	: External interrupt input
KR0 to KR7	: Key return
P00 to P07	: Port 0
P10 to P16	: Port 1
P40	: Port 4
P125	: Port 12
P137	: Port 13
PCLBUZ0	: Programmable clock output/buzzer output
$\overline{\text{RESET}}$	: Reset
RTIO00 to RTIO07	: Real-time output
RxD0	: Receive data
SCK00	: Serial clock input/output
SI00	: Serial data input
SO00	: Serial data output
TI00 to TI03	: Timer input
TO00 to TO03	: Timer output
TOOL0	: Data input/output for tool
TxD0	: Transmit data
ANI0 to ANI7	: Analog input
V_{DD}	: Power supply
V_{SS}	: Ground

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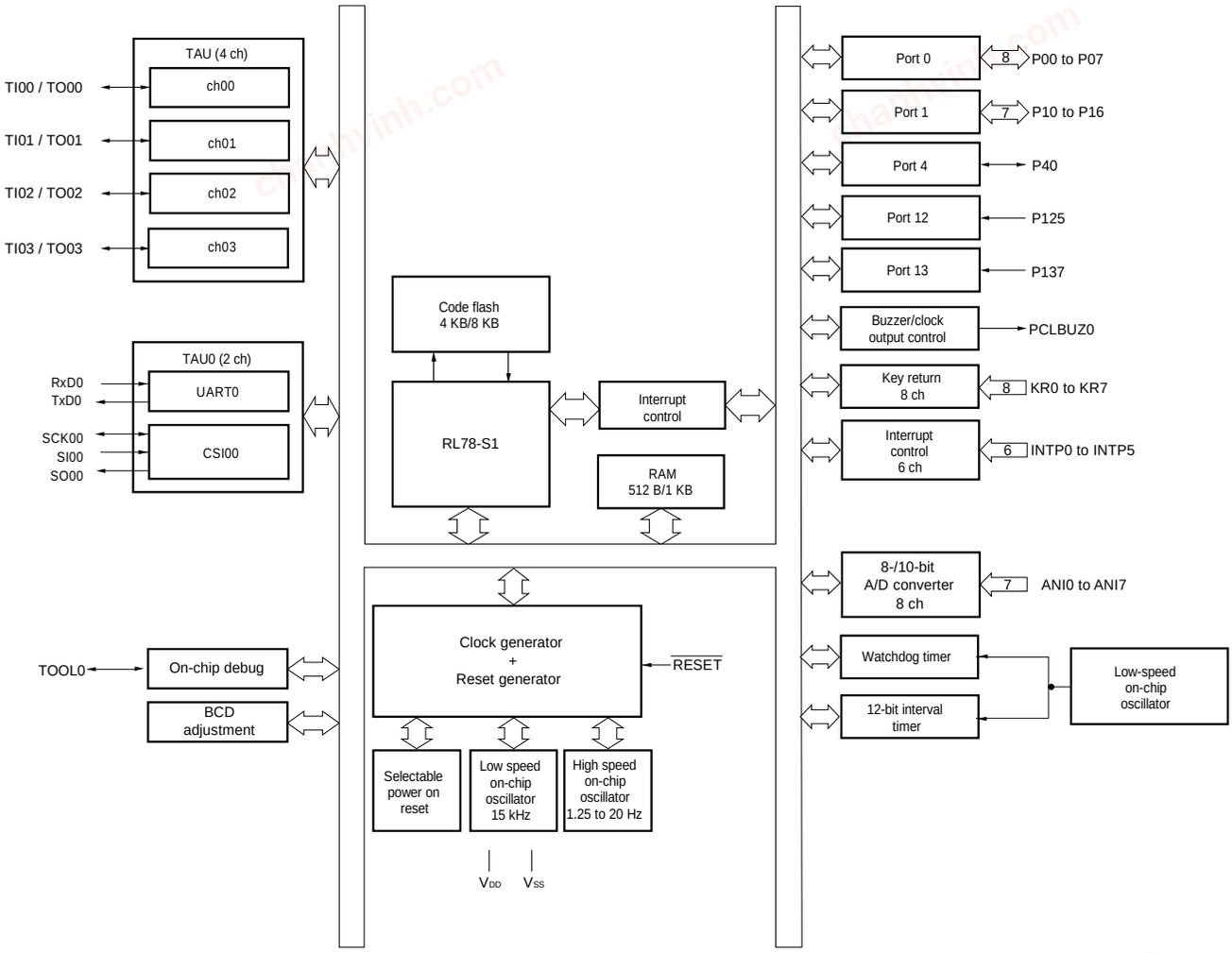
1.5 Block Diagram

1.5.1 RL78/G1M products



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1.5.2 RL78/G1N products



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1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		20-pin			
		RL78/G1M Products		RL78/G1N Products	
		R5F11W67ASM R5F11W67DSM	R5F11W68ASM R5F11W68DSM	R5F11Y67ASM R5F11Y67DSM	R5F11Y68ASM R5F11Y68DSM
Code flash memory		4 KB	8 KB	4 KB	8 KB
RAM		512 B	1 KB	512 B	1 KB
Main system clock	High-speed on-chip oscillator clock	● 1.25 to 20 MHz (V_{DD} = 2.7 to 5.5 V) ● 1.25 to 5 MHz (V_{DD} = 2.0 to 5.5 V[Note 1])			
Low-speed on-chip oscillator clock		15 kHz ±15%			
General-purpose register		8-bit register × 8			
Minimum instruction execution time		0.05 μs (20 MHz operation)			
Instruction set		● Data transfer (8 bits) ● Adder and subtractor/logical operation (8 bits) ● Multiplication (8 bits × 8 bits) ● Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.			
I/O port	Total	18			
	CMOS I/O	16 (N-ch open-drain output (V_{DD} tolerance): 14)			
				P-ch open-drain output (high current pin): 6	
	CMOS input	2			
Timer	16-bit timer	4 channels			
	Watchdog timer	1 channel			
	12-bit interval timer	1 channel			
	Timer output	4 channels (PWM outputs: 3[Note 2])			
Real-time output		8 channels		–	
Clock output/buzzer output		1			
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f_{MAIN} = 20 MHz operation)			
8-/10-bit resolution A/D converter		8 channels			
Serial interface		CSI: 1 channel, UART: 1 channel			
Vectored interrupt sources	Internal	12			
	External	7			
Key interrupt		8			

Notes 1. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage (V_{SPOR}) of the selectable power-on-reset (SPOR) circuit should also be considered.

2. The number of outputs varies, depending on the setting of channels in use and the number of the master (refer to **6.9.4 Operation as multiple PWM output function** in the **RL78/G1M, G1N User's Manual**).

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(2/2)

Item	20-pin			
	RL78/G1M Products		RL78/G1N Products	
	R5F11W67ASM R5F11W67DSM	R5F11W68ASM R5F11W68DSM	R5F11Y67ASM R5F11Y67DSM	R5F11Y68ASM R5F11Y68DSM
Reset	● Reset by RESET pin ● Internal reset by watchdog timer ● Internal reset by selectable power-on-reset ● Internal reset by illegal instruction execution Note 1 ● Internal reset by data retention lower limit voltage			
Selectable power-on-reset circuit	● Detection voltage Rising edge (V_{SPOR}): 2.25 V/2.68 V/3.02 V/4.45 V (max.) Falling edge (V_{SPDR}): 2.20 V/2.62 V/2.96 V/4.37 V (max.)			
On-chip debug function	Provided			
Power supply voltage	V_{DD} = 2.0 to 5.5 V Note 2			
Operating ambient temperature	T_A = -40 to + 85°C			

Notes 1. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the on-chip debug emulator.

2. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage (V_{SPOR}) of the selectable power-on-reset (SPOR) circuit should also be considered.

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2. ELECTRICAL SPECIFICATIONS

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Functions and 2.2 Functions Other than Port Pins in the RL78/G1M, G1N User's Manual.

3. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage (V_{SPOR}) of the selectable power-on-reset (SPOR) circuit should also be considered.

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2.1 Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbols	Conditions			Ratings	Unit
Supply voltage[Note 1]	V_{DD}				–0.5 to +6.5	V
Input voltage[Note 1]	V_{I1}				–0.3 to V_{DD} + 0.3[Note 2]	V
Output voltage[Note 1]	V_{O1}				–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin	P00 to P05	RL78/G1M	–40	mA
				RL78/G1N	–130	mA
			P06, P07, P10 to P16, P40		–40	mA
		Total of all pins	P00 to P05	RL78/G1M	–70	mA
				RL78/G1N	–160	mA
			P06, P07, P10 to P16, P40	RL78/G1M	–100	mA
				RL78/G1N	–100	mA
Output current, low	I_{OL1}	Per pin			40	mA
		Total of all pins	P00 to P05	RL78/G1M	70	mA
				RL78/G1N	90	mA
			P06, P07, P10 to P16, P40	RL78/G1M	100	mA
				RL78/G1N	170	mA
Operating ambient temperature	T_A				–40 to +85	°C
Storage temperature	T_{stg}				–65 to +150	°C

Notes 1. V_{SS} is used as the reference potential.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. The reference voltage is V_{SS}.

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2.2 Oscillator Characteristics

2.2.1 On-chip oscillator characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation frequency Notes 1, 2	f_{IH}		1.25		20	MHz
High-speed on-chip oscillator oscillation frequency accuracy		T_A = –40 to –20°C	–3		+3	%
		T_A = –20 to +85°C	–2		+2	%
Low-speed on-chip oscillator oscillation frequency Note 3	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (000C2H).

2. This only indicates the oscillator characteristics. See **AC Characteristics** for instruction execution time.

3. This only indicates the oscillator characteristics.

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2.3 DC Characteristics

2.3.1 Pin characteristics of RL78/G1M

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P07, P10 to P16, P40				–10[Note 2]	mA
		Total of P00 to P05 (When duty ≤ 70%)[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			–50	mA
			2.7 V ≤ V_{DD} < 4.0 V			–10	mA
			2.0 V ≤ V_{DD} < 2.7 V			–7.5	mA
		Total of P06, P07, P10 to P16, P40 (When duty ≤ 70%)[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			–80	mA
			2.7 V ≤ V_{DD} < 4.0 V			–16	mA
			2.0 V ≤ V_{DD} < 2.7 V			–12	mA
		Total of all pins (When duty ≤ 70%)[Note 3]				–130	mA
Output current, low	I_{OL1}	Per pin for P00 to P07, P10 to P16, P40				20[Note 2]	mA
		Total of P00 to P05 (When duty ≤ 70%)[Note 4]	4.0 V ≤ V_{DD} ≤ 5.5 V			60	mA
			2.7 V ≤ V_{DD} < 4.0 V			9	mA
			2.0 V ≤ V_{DD} < 2.7 V			1.8	mA
		Total of P06, P07, P10 to P16, P40 (When duty ≤ 70%)[Note 4]	4.0 V ≤ V_{DD} ≤ 5.5 V			100	mA
			2.7 V ≤ V_{DD} < 4.0 V			15	mA
			2.0 V ≤ V_{DD} < 2.7 V			3	mA
		Total of all pins (When duty ≤ 70%)[Note 4]				160	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P06 and P10 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

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2.3.2 Pin characteristics of RL78/G1N

(T_A = –40 to +85°C, 4.5 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Total of all pins (When duty ≤ 70%)[Note 3]	4.5 V ≤ V_{DD} ≤ 5.5 V			–160	mA
		Total of P00 to P05 (When duty ≤ 70%)[Note 3]	4.5 V ≤ V_{DD} ≤ 5.5 V			–140	mA
		Total of P06, P07, P10 to P16, P40 (When duty ≤ 70%)[Note 3]	4.5 V ≤ V_{DD} ≤ 5.5 V			–80	mA
		Per pin (COM) for P00 to P05[Note 5]	4.5 V ≤ V_{DD} ≤ 5.5 V			–120[Note 2]	mA
		Per pin (SEG, other) for P06, P07, P10 to P16, P40	4.5 V ≤ V_{DD} ≤ 5.5 V			–10[Note 2]	mA
Output current, low	I_{OL1}	Total of all pins (When duty ≤ 70%)[Note 4]	4.5 V ≤ V_{DD} ≤ 5.5 V			160	mA
		Total of P00 to P05 (When duty ≤ 70%)[Note 4]	4.5 V ≤ V_{DD} ≤ 5.5 V			80	mA
		Total of P06, P07, P10 to P16, P40 (When duty ≤ 70%)[Note 4]	4.5 V ≤ V_{DD} ≤ 5.5 V			150	mA
		Per pin (SEG) for P06, P07, P10 to P15[Note 6]	4.5 V ≤ V_{DD} ≤ 5.5 V			15	mA
		Per pin (COM, other) for P00 to P05, P16, P40	4.5 V ≤ V_{DD} ≤ 5.5 V			20[Note 2]	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

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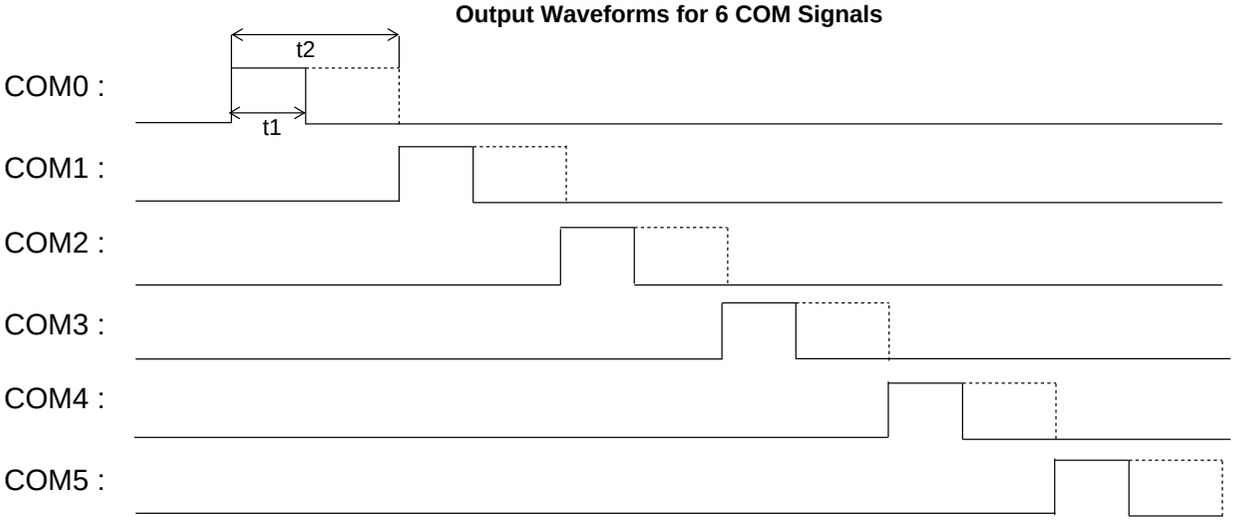
Notes 5. Specification under conditions where (t1/t2*100%) ≤ 25%.
The output current when the condition changes to a value in the range of (t1/t2*100%) > 25% can be calculated from the following expression (after replacing (t1/t2*100%) with n%).

- Total output current of pins = (I_{OH} × 0.25)/(n × 0.01)

<Example> Where n = 60% and I_{OH} = -120.0 mA
Total output current of pins = (-120.0 × 0.25)/(60 × 0.01) = -50 mA

However, the current does not depend on the number of COM signals. A current higher than the absolute maximum rating must not flow into one pin.
The waveforms for 6 COM signals are shown below.

Output Waveforms for 6 COM Signals



Notes 6. Specification under conditions where (t1/t2*100%) ≤ 25%.
The output current when the condition changes to a value in the range of (t1/t2*100%) > 25% can be calculated from the following expression (after replacing (t1/t2*100%) with n%).

- Total output current of pins = (I_{OL} × 0.25)/(n × 0.01)

<Example> Where n = 60% and I_{OL} = 15.0 mA
Total output current of pins = (15.0 × 0.25)/(60 × 0.01) = 6.25 mA

However, the current does not depend on the number of COM signals. A current higher than the absolute maximum rating must not flow into one pin.

Caution P06, P07, P10 to P15 do not output high level in N-ch open-drain mode.
Set P-ch open drain of P00 to P05 to off state (high impedance) during A/D conversion (RL78/G1N).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

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2.3.3 Common items

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}				0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}				0		0.2 V_{DD}	V
Output voltage, high[Note 1]	V_{OH1}	P00 to P05	I_{OH} = –10 mA	4.0 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 1.5		V_{DD}	V
			I_{OH} = –3 mA	4.0 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.7		V_{DD}	V
			I_{OH} = –2 mA	2.7 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.6		V_{DD}	V
			I_{OH} = –1.5 mA	2.0 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.5		V_{DD}	V
			I_{OH} = –120 mA[Note 3]	4.5 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 1.0		V_{DD}	V
	V_{OH2}	P06, P07, P10 to P16, P40	I_{OH} = –10 mA	4.0 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 1.5		V_{DD}	V
			I_{OH} = –3 mA	4.0 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.7		V_{DD}	V
			I_{OH} = –2 mA	2.7 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.6		V_{DD}	V
			I_{OH} = –1.5 mA	2.0 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.5		V_{DD}	V
Output voltage, low[Note 2]	V_{OL1}	P00 to P05, P16, P40	I_{OL} = 20 mA	4.0 V ≤ V_{DD} ≤ 5.5 V	0		1.5	V
			I_{OL} = 1.5 mA	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.4	V
			I_{OL} = 0.6 mA	2.0 V ≤ V_{DD} ≤ 5.5 V	0		0.4	V
	V_{OL2}	P06, P07, P10 to P15	I_{OL} = 20 mA	4.0 V ≤ V_{DD} ≤ 5.5 V	0		1.5	V
			I_{OL} = 1.5 mA	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.4	V
			I_{OL} = 0.6 mA	2.0 V ≤ V_{DD} ≤ 5.5 V	0		0.4	V
			I_{OL} = 15 mA[Note 4]	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.6	V
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P16, P40, P41, P125, P137 V_I = V_{DD}					1	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P16, P40, P41, P125, P137 V_I = V_{SS}					–1	μA
On-chip pull-up resistance	R_U	V_I = V_{SS}			10	20	100	kΩ
On-chip pull-down resistance[Note 5]	R_O	V_I = V_{DD}			100	200		kΩ

Notes 1. The value under the condition which satisfies the high-level output current (I_{OH1}).
2. The value under the condition which satisfies the low-level output current (I_{OL1}).
3. P-ch open-drain (RL78/G1N only)
4. N-ch open-drain
5. RL78/G1N only.

Caution The maximum value of V_{IH} is V_{DD} even in N-ch open-drain mode.
Do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

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2.3.4 Supply current characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	Basic operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		1.05		mA
			Normal operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		2.19	2.95	
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		1.13	1.56	
	I_{DD2}[Note 2]	HALT mode		f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		390	980	µA
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		300	640	
	I_{DD3}[Note 3]	STOP mode[Note 4]		V_{DD} = 3.0 V			0.61[Note 5]	2.35	µA
12-bit interval timer operating current	I_{TMKA}[Notes 6, 7]						0.31		µA
Watchdog timer operating current	I_{WDT}[Notes 6, 7]						0.31		µA
A/D converter operating current	I_{ADC}[Note 6]	When conversion at maximum speed		V_{DD} = 5.0 V			1.30	1.90	mA
				V_{DD} = 3.0 V			0.50		mA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. When watchdog timer and A/D converter are stopped. The values below the MAX. column include the leakage current.

4. Condition applies at any temperature.

5. Value at V_{DD} = 3 V, T_A = 25°C.

6. Current flowing into V_{DD}.

7. Excluding the operating current of the low-speed on-chip oscillator (f_{IL}).

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. Temperature condition of the typical value is T_A = 25°C

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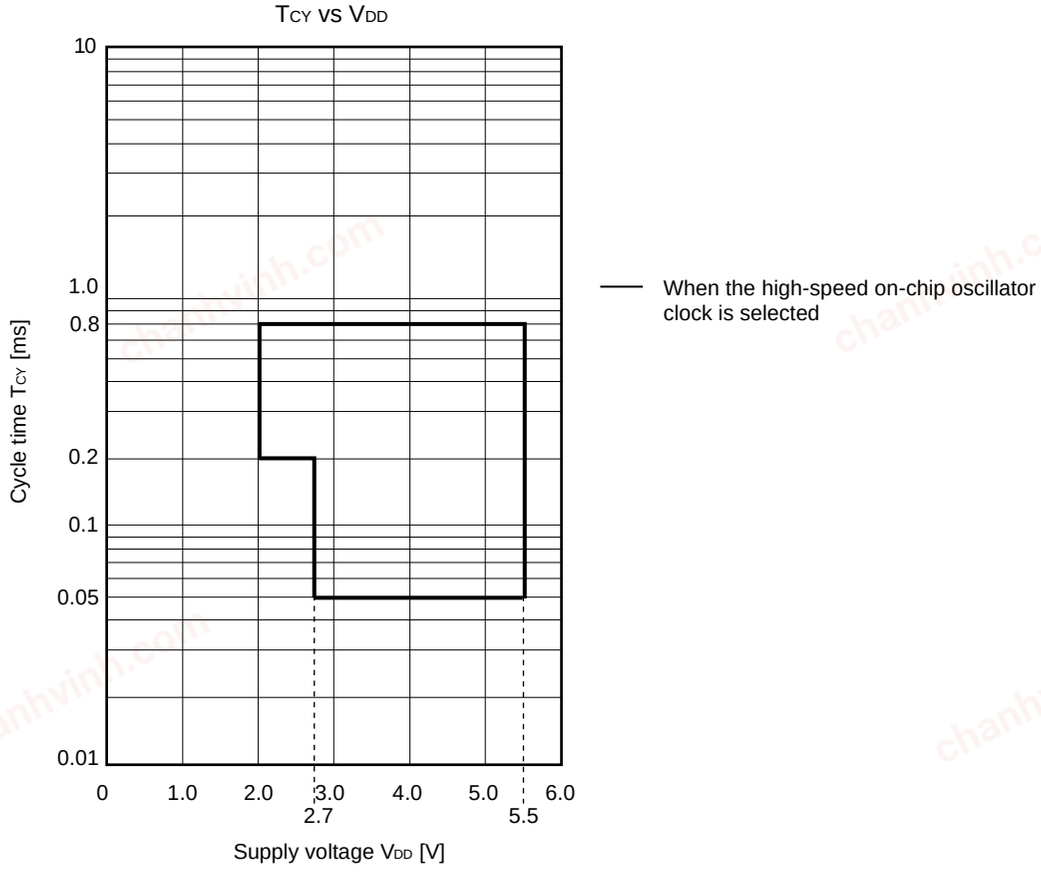
2.4 AC Characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		0.8	µs
			2.0 V ≤ V_{DD} ≤ 5.5 V	0.2		0.8	µs
TI00 to TI03 input high-level width, low-level width	t_{TIH}, t_{TIL}	Noise filter is not used		1/f_{MCK}+10			ns
TO00 to TO03 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
PCLBUZ0 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs

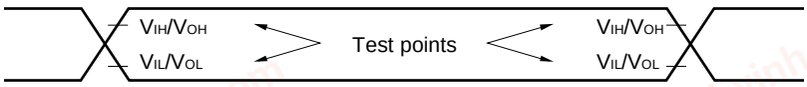
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n1 bit of timer mode register 0nH (TMR0nH). n: Channel number (n = 0 to 3))

Minimum Instruction Execution Time during Main System Clock Operation

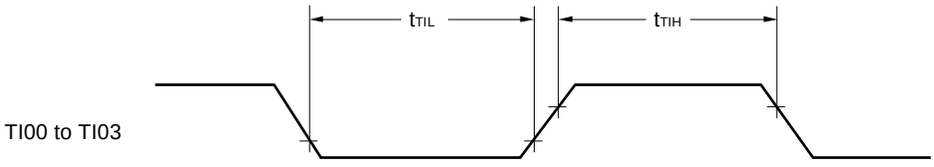


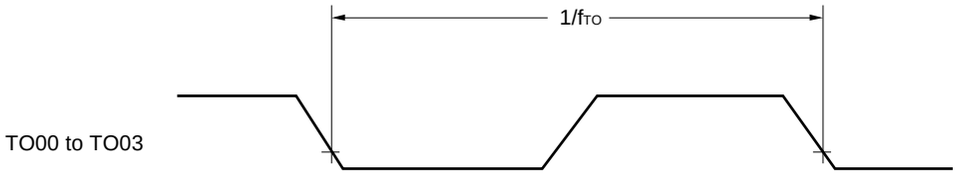
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AC Timing Test Points

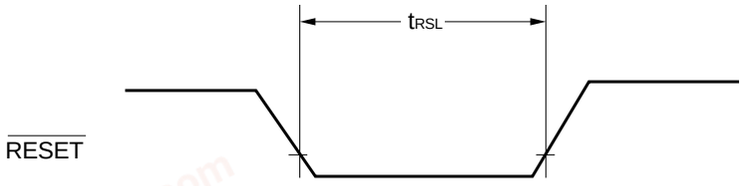


TI/TO Timing





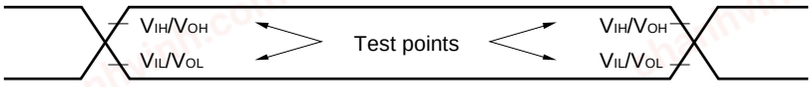
$\overline{\text{RESET}}$ Input Timing



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2.5 Serial Interface Characteristics

AC Timing Test Points



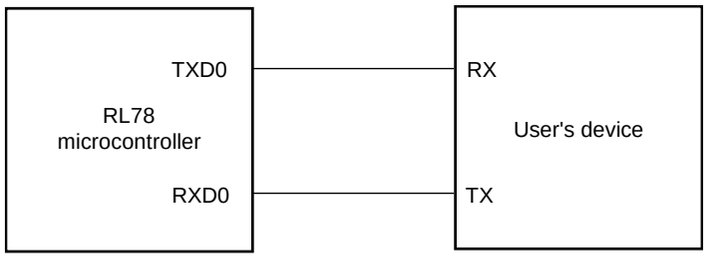
2.5.1 Serial array unit

(1) UART mode (dedicated baud rate generator output)

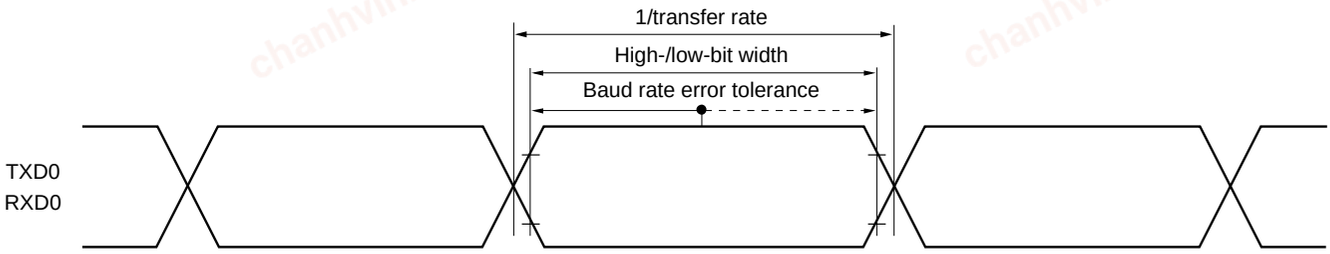
(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 20 MHz			3.3	Mbps

UART mode connection diagram



UART mode bit width (reference)



Remark f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0, 1))

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(2) CSI mode (master mode, SCKp...internal clock output)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 – 18			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 – 50			ns
SIp setup time (to SCKp↑)Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		47			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		110			ns
SIp hold time (from SCKp↑)Note 1	t_{KSI1}			19			ns
Delay time from SCKp↓ to SOp outputNote 2	t_{KSO1}	C = 30 pFNote 3				25	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes “to SCKp↓” and SIp hold time becomes “from SCKp↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes “from SCKp↑” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Remark p: CSI number (p = 00), n: Channel number (n = 0)

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(3) CSI mode (slave mode, SCKp…external clock input)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 16 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY}/2			ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK}+20			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK}+30			ns
SIp hold time (from SCKp↑)[Note 1]	t_{KSI2}	2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK}+31			ns
Delay time from SCKp↓ to SOp output[Note 2]	t_{KSO2}	C = 30 pF[Note 3]	2.7 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK}+50	ns
			2.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK}+110	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes “to SCKp↓” and the SIp hold time becomes “from SCKp↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes “from SCKp↑” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

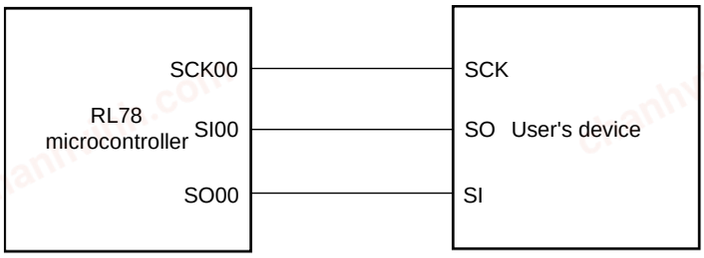
3. C is the load capacitance of the SOp output lines.

Remarks 1. p: CSI number (p = 00), n: Channel number (n = 0)

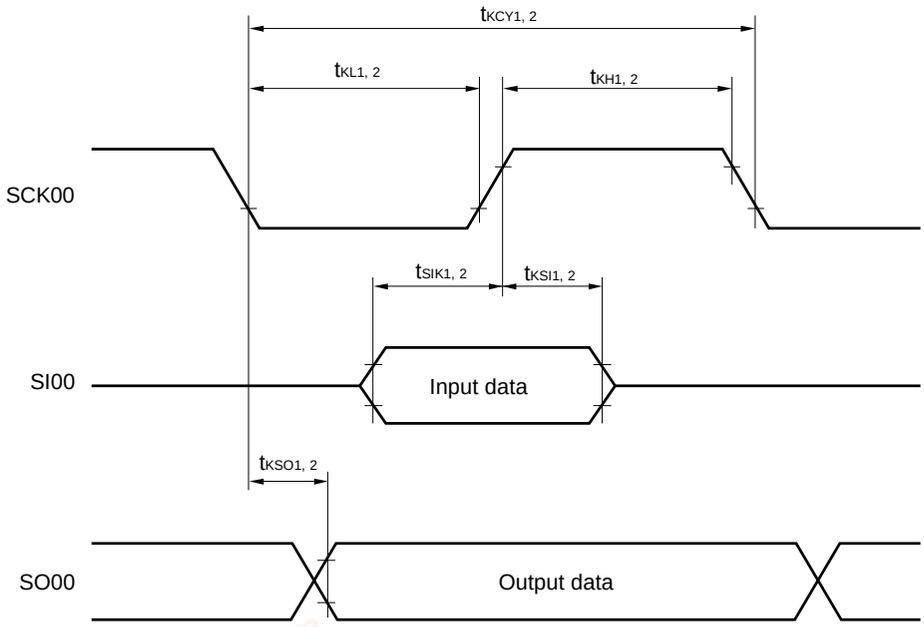
2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0))

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CSI mode connection diagram



CSI mode serial transfer timing
(When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1.)



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2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(Target ANI pin: ANI0 to ANI7)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Notes 1, 2, 3]	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1	LSB
			V_{DD} = 3 V		±2.3	±4.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI7	2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		18.4	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V[Note 5]	4.6		18.4	
Zero-scale error[Notes 1, 2, 3, 4]	E_{ZS}	10-bit resolution	V_{DD} = 5 V			±0.19	%FSR
			V_{DD} = 3 V			±0.39	%FSR
Full-scale error[Notes 1, 2, 3, 4]	E_{FS}	10-bit resolution	V_{DD} = 5 V			±0.29	%FSR
			V_{DD} = 3 V			±0.42	%FSR
Integral linearity error[Notes 1, 2, 3]	ILE	10-bit resolution	V_{DD} = 5 V			±1.8	LSB
			V_{DD} = 3 V			±1.7	LSB
Differential linearity error[Notes 1, 2, 3]	DLE	10-bit resolution	V_{DD} = 5 V			±1.4	LSB
			V_{DD} = 3 V			±1.5	LSB
Analog input voltage	V_{AIN}	Target pin: ANI0 to ANI7		0		V_{DD}	V

Notes 1. TYP. Value is the average value at T_A = 25°C. MAX. value is the average value ±3σ at normal distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

4. This value is indicated as a ratio (%FSR) to the full-scale value.

5. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when conversion is done in the operating voltage range of 2.4 V ≤ V_{DD} < 2.7 V.

Cautions 1. Arrange wiring and insert the capacitor so that no noise appears on the power supply/ground line.

2. Do not allow any pulses that rapidly change such as digital signals to be input/output to/from the pins adjacent to the conversion pin during A/D conversion.

3. Set P-ch open drain of P00 to P05 to off state (high impedance) during A/D conversion (RL78/G1N).

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2.6.2 SPOR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V_{SPOR0}	Power supply rise time	4.08	4.28	4.45	V
		Power supply fall time	4.00	4.20	4.37	V
	V_{SPOR1}	Power supply rise time	2.76	2.90	3.02	V
		Power supply fall time	2.70	2.84	2.96	V
	V_{SPOR2}	Power supply rise time	2.44	2.57	2.68	V
		Power supply fall time	2.40	2.52	2.62	V
	V_{SPOR3}	Power supply rise time	2.05	2.16	2.25	V
		Power supply fall time	2.00	2.11	2.20	V
Minimum pulse width[Note]	T_{SPW}		300			μs

Note Time required for the reset operation by the SPOR when V_{DD} becomes under V_{SPOR}.

Caution Set the detection voltage (V_{SPOR}) in the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H). The operating voltage range is as follows:
When the CPU operating frequency is from 1.25 MHz to 20 MHz: V_{DD} = 2.7 to 5.5 V
When the CPU operating frequency is from 1.25 MHz to 5 MHz: V_{DD} = 2.0 to 5.5 V

2.6.3 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

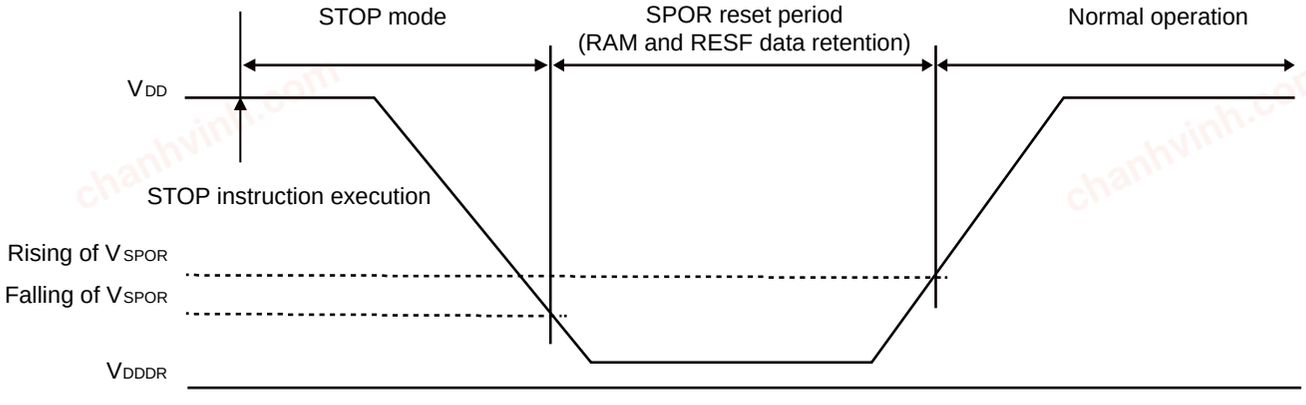
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

2.6.4 RAM data retention characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.9		5.5	V

Caution Data in RAM are retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}). Note that data in the RESF register might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}).



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2.7 Flash Memory Programming Characteristics

(T_A = 0 to +40°C, 4.5 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Code flash memory rewritable times Notes 1, 2, 3	C_{erwr}	Retained for 20 years (T_A = 85°C)	1000			Times

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer.

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.8 Dedicated Flash Memory Programmer Communication (UART)

(T_A = 0 to +40°C, 4.5 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

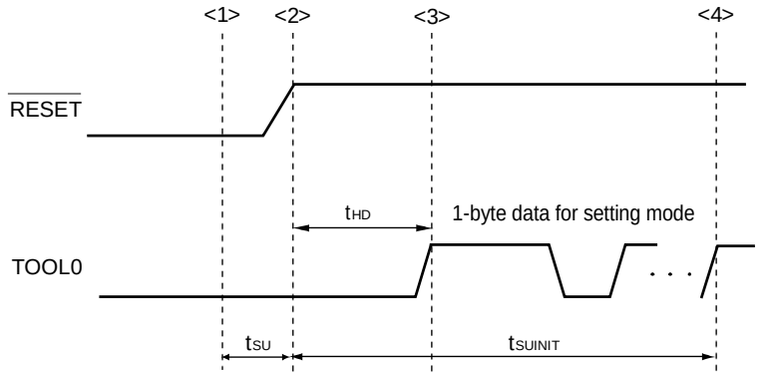
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate				115,200		bps

Remark The transfer rate during flash memory programming is fixed to 115,200 bps.

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2.9 Timing of Entry to Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	SPOR reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	SPOR reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released	t_{HD}	SPOR reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (SPOR reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of entry to the flash memory programming mode by UART reception.

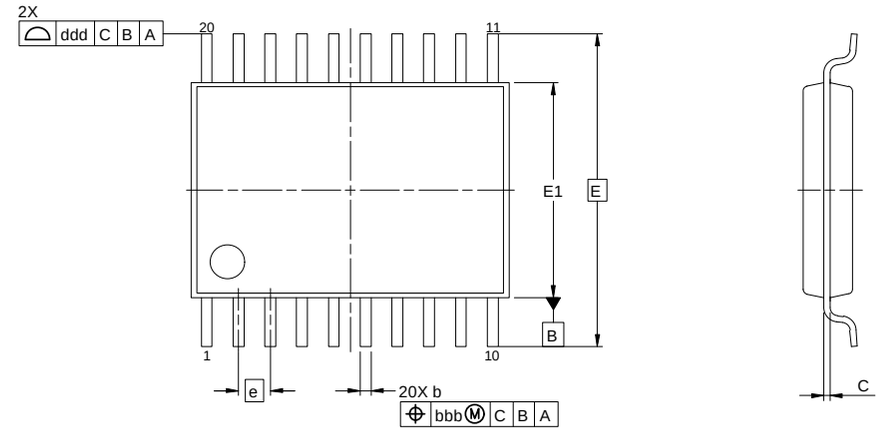
Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms (68 ms at T_A = –40 to +85°C) after the external reset is released during this period.
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released

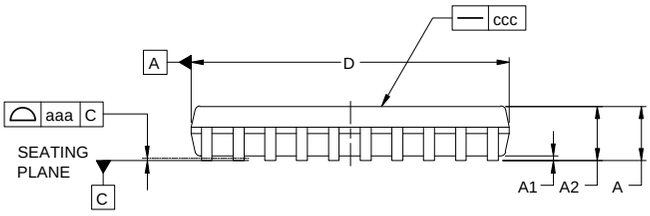
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3. PACKAGE DRAWINGS

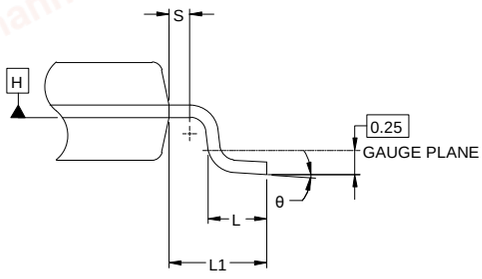
3.1 20-Pin Products

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TSSOP20-4.40x6.50-0.65	PTSP0020JI-A	0.08





Detail of Lead End



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
C	0.09	0.127	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		

NOTES:
1.DIMENSION 'D' AND 'E1' DOES NOT INCLUDE MOLD FLASH.
2.DIMENSION 'b' DOES NOT INCLUDE TRIM OFFSET.
3.DIMENSION 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.

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Revision History	RL78/G1M, G1N Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	May 29, 2020	–	First Edition issued.

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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