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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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R1RW0408D Series

4M High Speed SRAM (512-kword × 8-bit)

REJ03C0111-0200
Rev. 2.00
Dec.1.2008

Description

The R1RW0408D is a 4-Mbit high speed static RAM organized 512-kword × 8-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The R1RW0408D is packaged in 400-mil 36-pin SOJ for high density surface mounting.

Features

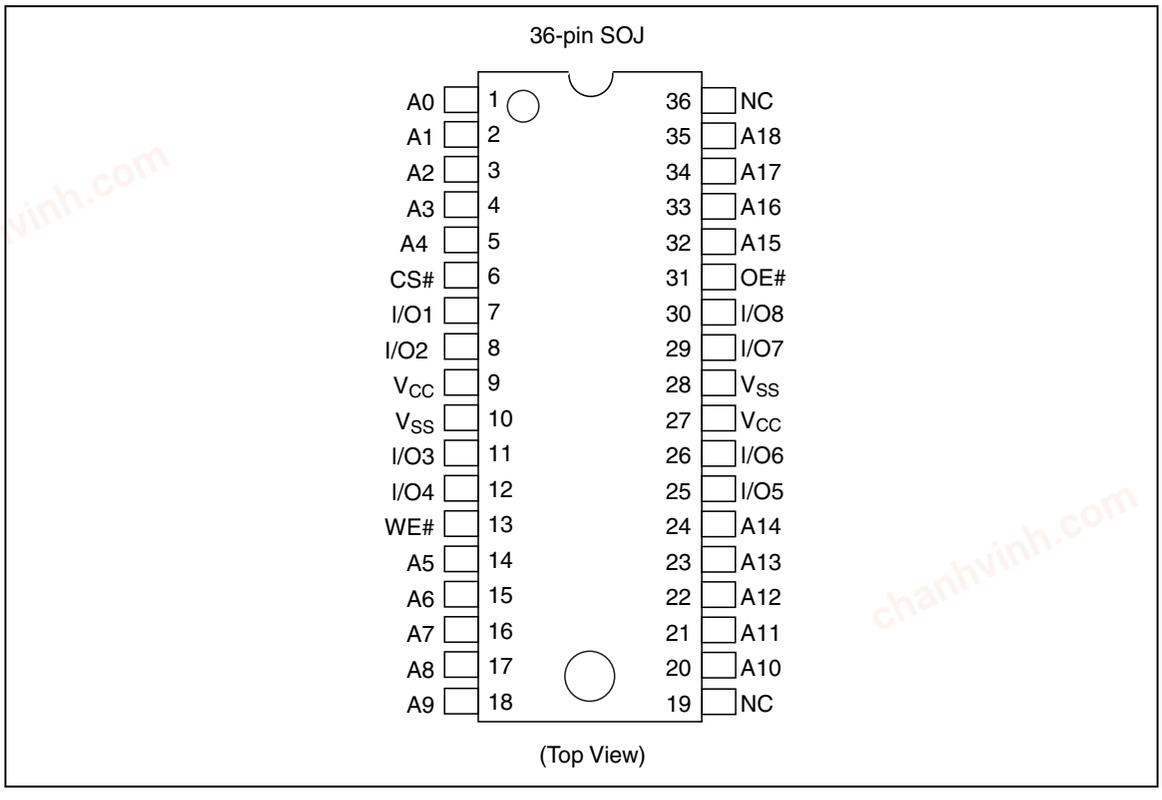
- Single supply: 3.3 V ± 0.3 V
- Access time: 10 ns /12 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - — All inputs and outputs
- Operating current: 115mA/ 100mA (max)
- TTL standby current: 40 mA (max)
- CMOS standby current: 5 mA (max)
  : 0.8 mA (max) (L-version)
- Data retention current: 0.4 mA (max) (L-version)
- Data retention voltage: 2 V (min) (L-version)
- Center V_{CC} and V_{SS} type pin out

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Ordering Information

Type No.	Access time	Package
R1RW0408DGE-0PR	10 ns	400-mil 36-pin plastic SOJ (36P0K)
R1RW0408DGE-2PR	12 ns	
R1RW0408DGE-2LR	12 ns	

Pin Arrangement



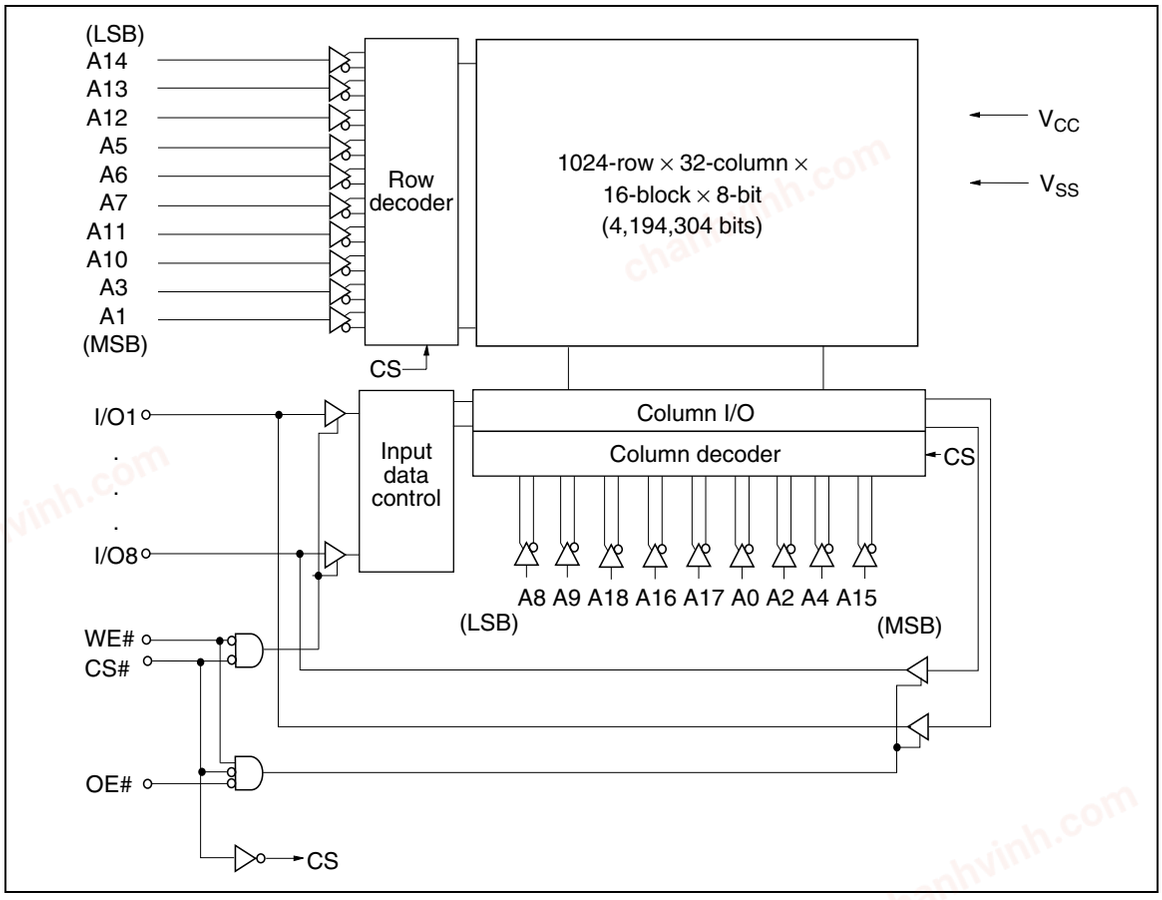
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Pin Description

Pin name	Function
A0 to A18	Address input
I/O1 to I/O8	Data input/output
CS#	Chip select
OE#	Output enable
WE#	Write enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

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Block Diagram



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Operation Table

CS#	OE#	WE#	Mode	V_{CC} current	I/O	Ref. cycle
H	×	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	Output disable	I_{CC}	High-Z	—
L	L	H	Read	I_{CC}	D_{OUT}	Read cycle (1) to (3)
L	H	L	Write	I_{CC}	D_{IN}	Write cycle (1)
L	L	L	Write	I_{CC}	D_{IN}	Write cycle (2)

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.5*[2]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Notes: 1. V_T (min) = –2.0 V for pulse width (under shoot) ≤ 6 ns.
2. V_T (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 6 ns.

Recommended DC Operating Conditions

(Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}*[3]	3.0	3.3	3.6	V
	V_{SS}*[4]	0	0	0	V
Input voltage	V_{IH}	2.0	—	V_{CC} + 0.5*[2]	V
	V_{IL}	–0.5*[1]	—	0.8	V

Notes: 1. V_{IL} (min) = –2.0 V for pulse width (under shoot) ≤ 6 ns.
2. V_{IH} (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 6 ns.
3. The supply voltage with all V_{CC} pins must be on the same level.
4. The supply voltage with all V_{SS} pins must be on the same level.

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DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter		Symbol	Min	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	2	µA	V_{IN} = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	2	µA	V_{IN} = V_{SS} to V_{CC}
Operation power supply current	10ns cycle	I_{CC}	—	115	mA	Min cycle CS# = V_{IL}, I_{OUT} = 0 mA Other inputs = V_{IH}/V_{IL}
	12ns cycle	I_{CC}	—	100	mA	
Standby power supply current		I_{SB}	—	40	mA	Min cycle CS# = V_{IH}, Other inputs = V_{IH}/V_{IL}
		I_{SB1}	—	5	mA	f = 0 MHz V_{CC} ≥ CS# ≥ V_{CC} – 0.2 V, (1) 0 V ≤ V_{IN} ≤ 0.2 V or (2) V_{CC} ≥ V_{IN} ≥ V_{CC} – 0.2 V
			—*[1]	0.8*[1]	mA	
Output voltage		V_{OL}	—	0.4	V	I_{OL} = 8 mA
		V_{OH}	2.4	—	V	I_{OH} = –4 mA

Note: 1. This characteristics is guaranteed only for L-version.

Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance*[1]	C_{IN}	—	6	pF	V_{IN} = 0 V
Input/output capacitance*[1]	$C_{I/O}$	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

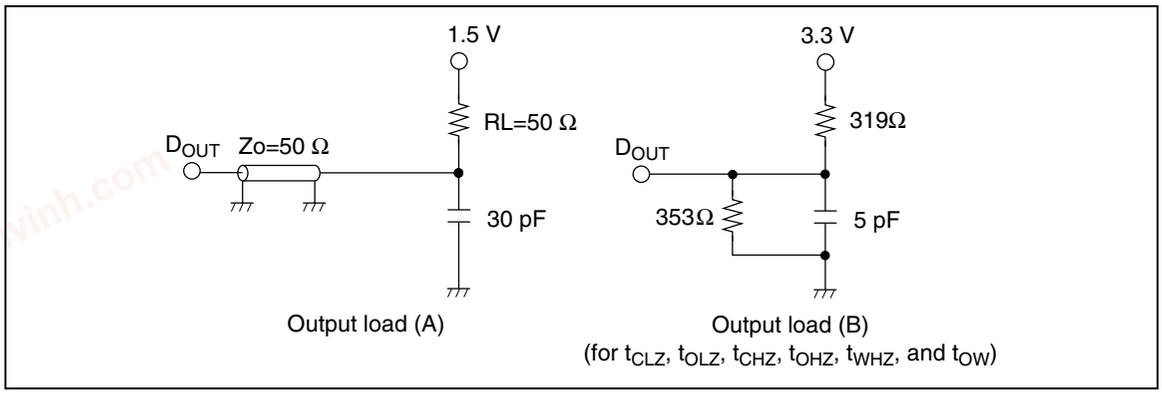
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AC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

		R1RW0408D					
		10ns Version		12ns Version			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	10	—	12	—	ns	
Address access time	t_{AA}	—	10	—	12	ns	
Chip select access time	t_{ACS}	—	10	—	12	ns	
Output enable to output valid	t_{OE}	—	5	—	6	ns	
Output hold from address change	t_{OH}	3	—	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	5	—	6	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	—	6	ns	1

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Write Cycle

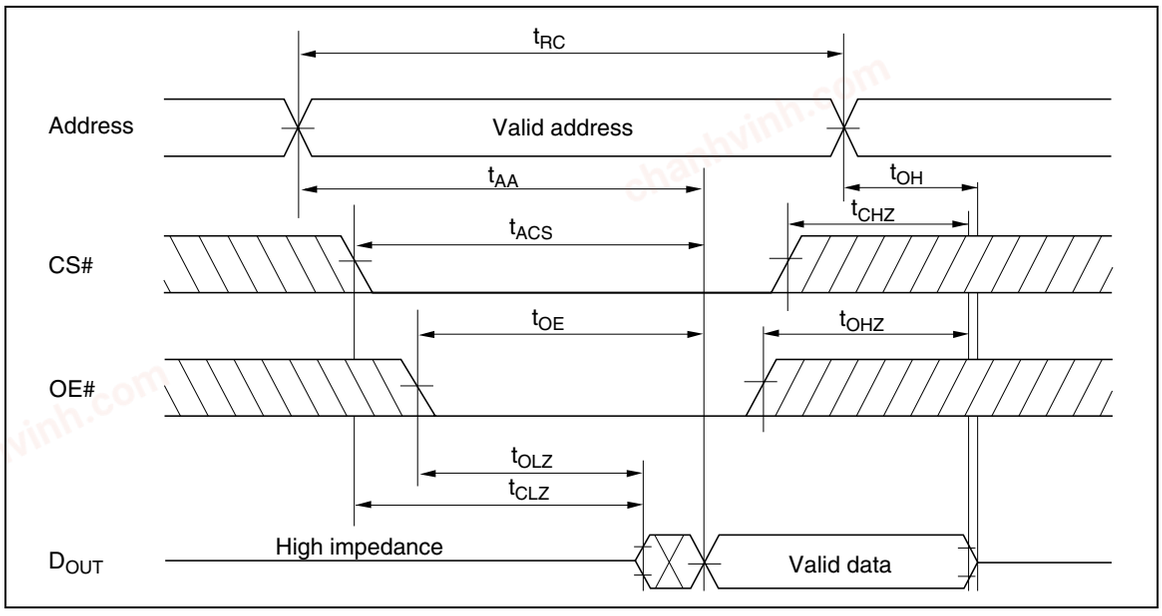
		R1RW0408D					
		10ns Version		12ns Version			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	10	—	12	—	ns	
Address valid to end of write	t_{AW}	7	—	8	—	ns	
Chip select to end of write	t_{CW}	7	—	8	—	ns	9
Write pulse width	t_{WP}	7	—	8	—	ns	8
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	5	—	6	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	—	6	ns	1
Write enable to output in high-Z	t_{WHZ}	—	5	—	6	ns	1

Notes:
1. Transition is measured ±200 mV from steady voltage with output load (B). This parameter is sampled and not 100% tested.
2. Address should be valid prior to or coincident with CS# transition low.
3. WE# and/or CS# must be high during address transition time.
4. If CS# and OE# are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
5. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, output remains a high impedance state.
6. t_{AS} is measured from the latest address transition to the later of CS# or WE# going low.
7. t_{WR} is measured from the earlier of CS# or WE# going high to the first address transition.
8. A write occurs during the overlap of a low CS# and a low WE#. A write begins at the latest transition among CS# going low and WE# going low. A write ends at the earliest transition among CS# going high and WE# going high. t_{WP} is measured from the beginning of write to the end of write.
9. t_{CW} is measured from the later of CS# going low to the end of write.

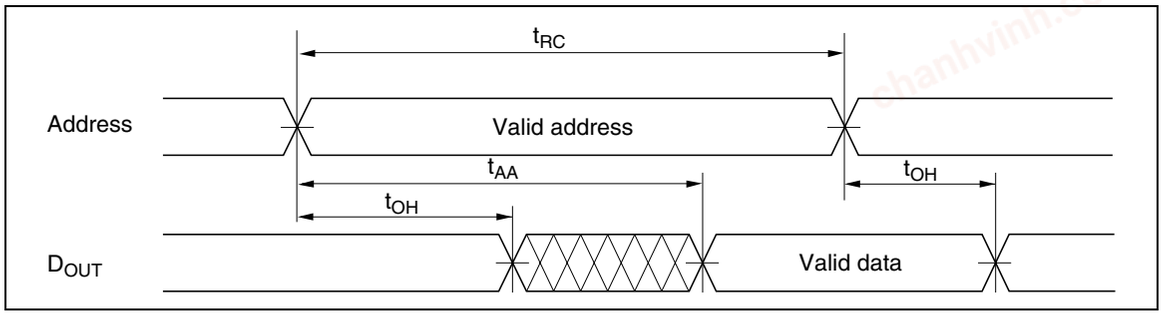
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Timing Waveforms

Read Timing Waveform (1) (WE# = V_{IH})

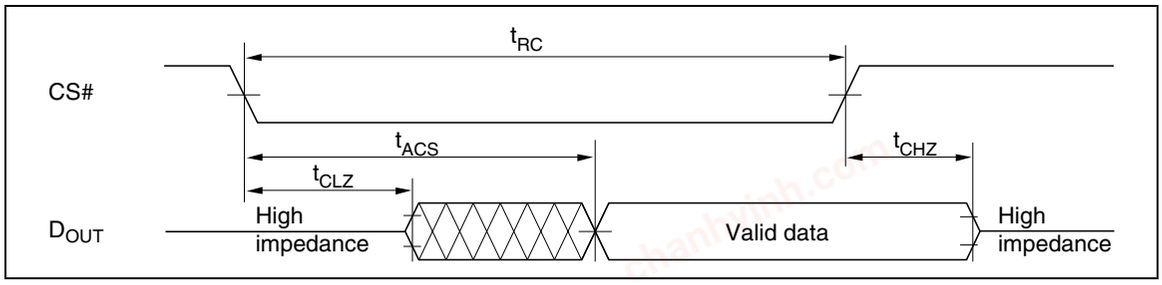


Read Timing Waveform (2) (WE# = V_{IH}, CS# = V_{IL}, OE# = V_{IL})

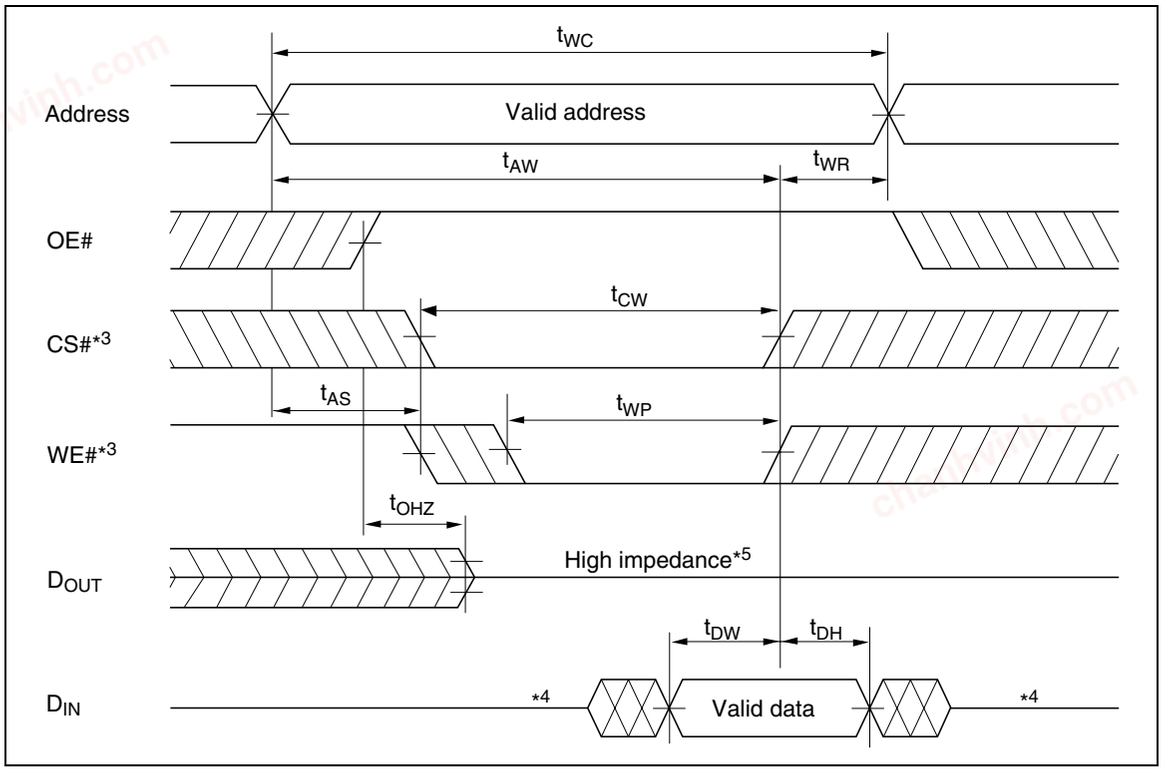


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Read Timing Waveform (3) (WE# = V_{IH}, CS# = V_{IL}, OE# = V_{IL})*2

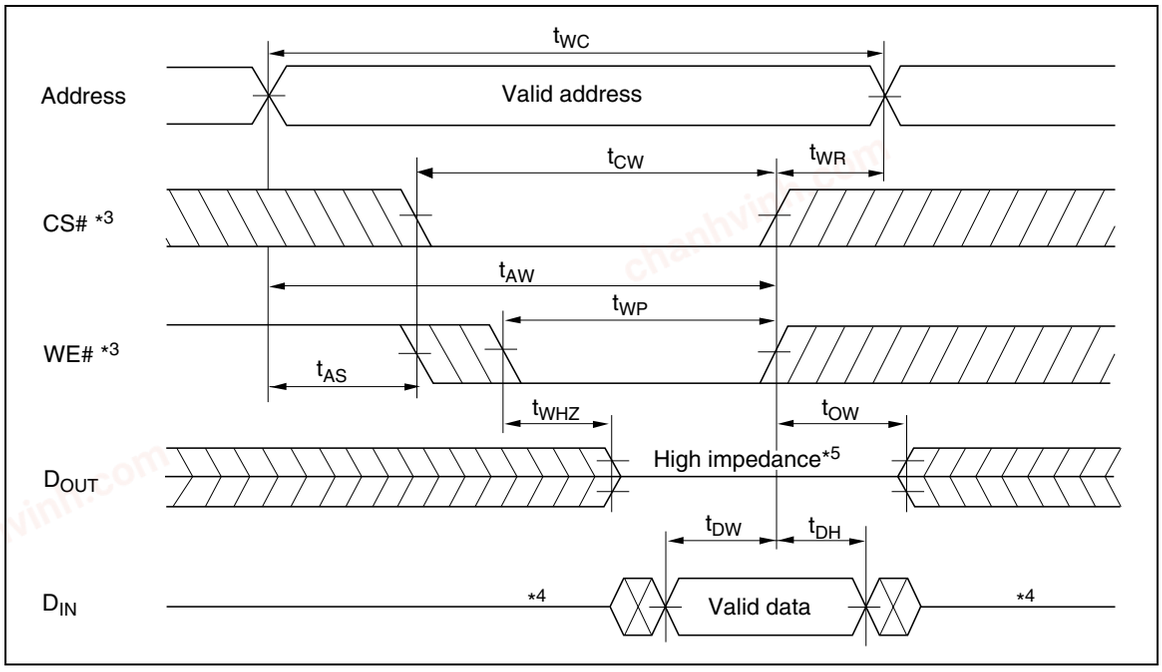


Write Timing Waveform (1) (WE# Controlled)



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Write Timing Waveform (2) (CS# Controlled)



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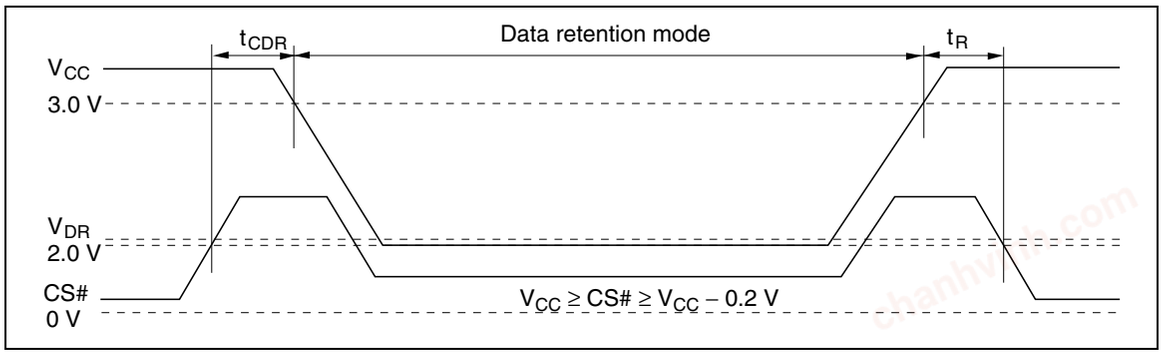
Low V_{CC} Data Retention Characteristics

(Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	V	$V_{CC} \geq CS\# \geq V_{CC} - 0.2$ V (1) 0 V ≤ V_{IN} ≤ 0.2 V or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR}	—	400	µA	V_{CC} = 3 V, $V_{CC} \geq CS\# \geq V_{CC} - 0.2$ V (1) 0 V ≤ V_{IN} ≤ 0.2 V or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	ns	See retention waveform
Operation recovery time	t_R	5	—	ms	

Low V_{CC} Data Retention Timing Waveform



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Revision History R1RW0408D Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Sep. 30, 2003	—	Initial issue
1.00	Mar.12.2004	—	Deletion of Preliminary
2.00	Dec.01.2008	—	Part Number 10ns Version Adding
		P1	Features Access time 10ns and operating current 115mA adding
		P2	Order Information Type No R1RW0408DGE-0PRAdding
			DC Characteristics Operating power supply current 10ns parameter adding
		P7	AC Characteristics Read ,Write parameter 10ns parameter adding
		P8/P9	

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