chanhvinh.com

To our customers,

# Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

chanhvinh.com

chanhvinh.com

# Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

chanhvinh.com

# R1RP0416D Series

## 4M High Speed SRAM (256-kword × 16-bit)

REJ03C0108-0100Z
Rev. 1.00
Mar.12.2004

### Description

The R1RP0416D Series is a 4-Mbit high speed static RAM organized 256-k word × 16-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 400-mil 44-pin plastic SOJ and 400-mil 44-pin plastic TSOPII.

### Features

- Single 5.0 V supply: 5.0 V ± 10%
- Access time: 12 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - — All inputs and outputs
- Operating current: 160 mA (max)
- TTL standby current: 40 mA (max)
- CMOS standby current: 5 mA (max)
  : 1.0 mA (max) (L-version)
- Data retention current: 0.5 mA (max) (L-version)
- Data retention voltage: 2 V (min) (L-version)
- Center $V_{CC}$ and $V_{SS}$ type pin out

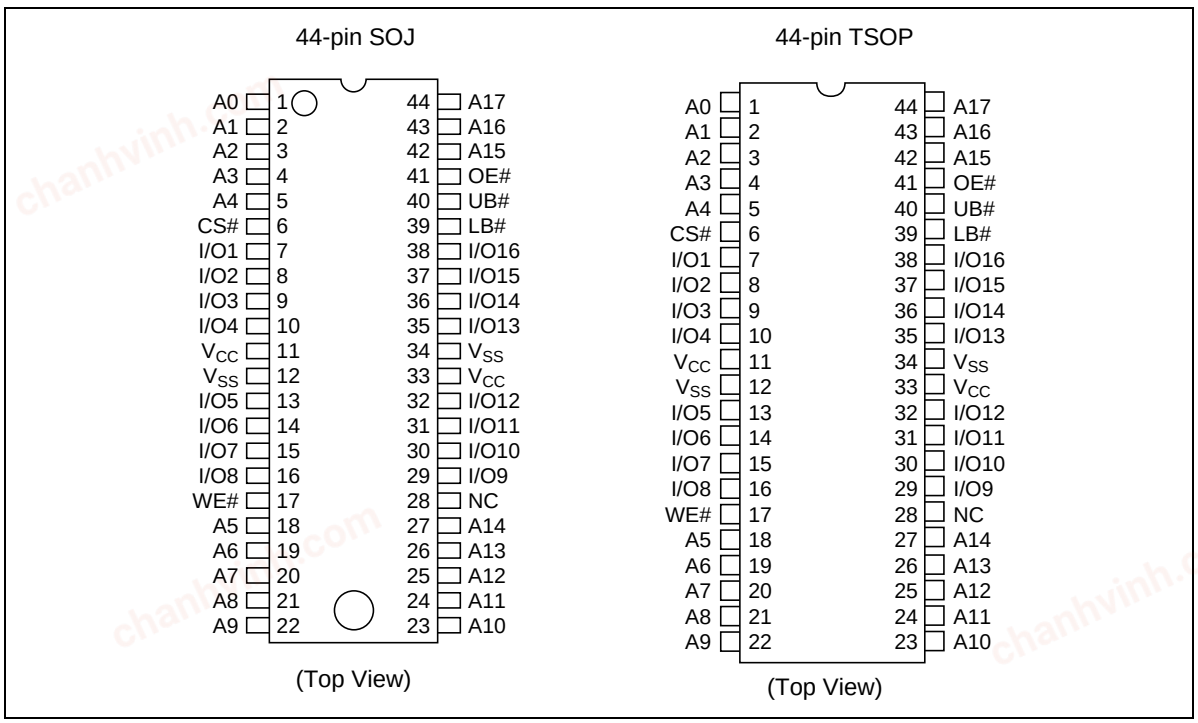
### Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| R1RP0416DGE-2PR | 12 ns | 400-mil 44-pin plastic SOJ (44P0K) |
| R1RP0416DGE-2LR | 12 ns | |
| R1RP0416DSB-2PR | 12 ns | 400-mil 44-pin plastic TSOPII (44P3W-H) |
| R1RP0416DSB-2LR | 12 ns | |

chanhvinh.com



## Pin Arrangement



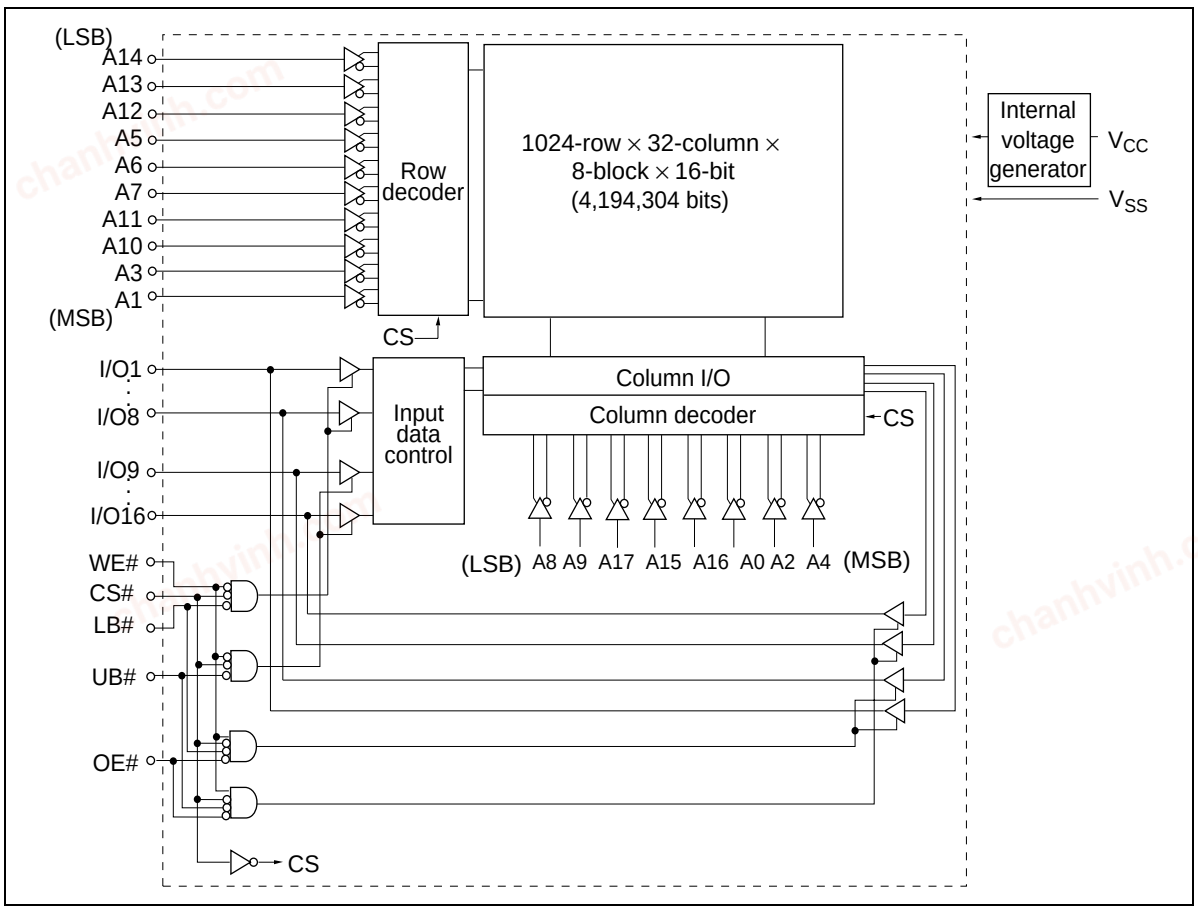

## Pin Description

| Pin name | Function |
|---|---|
| A0 to A17 | Address input |
| I/O1 to I/O16 | Data input/output |
| CS# | Chip select |
| OE# | Output enable |
| WE# | Write enable |
| UB# | Upper byte select |
| LB# | Lower byte select |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No connection |

chanhvinh.com



## Block Diagram



chanhvinh.com



## Operation Table

| CS# | OE# | WE# | LB# | UB# | Mode | $V_{CC}$ current | I/O1–I/O8 | I/O9–I/O16 | Ref. cycle |
|---|---|---|---|---|---|---|---|---|---|
| H | × | × | × | × | Standby | $I_{SB}$, $I_{SB1}$ | High-Z | High-Z | — |
| L | H | H | × | × | Output disable | $I_{CC}$ | High-Z | High-Z | — |
| L | L | H | L | L | Read | $I_{CC}$ | Output | Output | Read cycle |
| L | L | H | L | H | Lower byte read | $I_{CC}$ | Output | High-Z | Read cycle |
| L | L | H | H | L | Upper byte read | $I_{CC}$ | High-Z | Output | Read cycle |
| L | L | H | H | H | — | $I_{CC}$ | High-Z | High-Z | — |
| L | × | L | L | L | Write | $I_{CC}$ | Input | Input | Write cycle |
| L | × | L | L | H | Lower byte write | $I_{CC}$ | Input | High-Z | Write cycle |
| L | × | L | H | L | Upper byte write | $I_{CC}$ | High-Z | Input | Write cycle |
| L | × | L | H | H | — | $I_{CC}$ | High-Z | High-Z | — |

Note: H: $V_{IH}$, L: $V_{IL}$, ×: $V_{IH}$ or $V_{IL}$

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +7.0 | V |
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5*[1] to $V_{CC}$ + 0.5*[2] | V |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |
| Storage temperature under bias | Tbias | –10 to +85 | °C |

Notes: 1. $V_T$ (min) = –2.0 V for pulse width (under shoot) ≤ 6 ns.
2. $V_T$ (max) = $V_{CC}$ + 2.0 V for pulse width (over shoot) ≤ 6 ns.

## Recommended DC Operating Conditions

(Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$*[3] | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$*[4] | 0 | 0 | 0 | V |
| Input voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 0.5*[2] | V |
| | $V_{IL}$ | –0.5*[1] | — | 0.8 | V |

Notes: 1. $V_{IL}$ (min) = –2.0 V for pulse width (under shoot) ≤ 6 ns.
2. $V_{IH}$ (max) = $V_{CC}$ + 2.0 V for pulse width (over shoot) ≤ 6 ns.
3. The supply voltage with all $V_{CC}$ pins must be on the same level.
4. The supply voltage with all $V_{SS}$ pins must be on the same level.

chanhvinh.com



## DC Characteristics

(Ta = 0 to +70°C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V)

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Input leakage current | $\|I_{LI}\|$ | — | 2 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ |
| Output leakage current | $\|I_{LO}\|$ | — | 2 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ |
| Operation power supply current | $I_{CC}$ | — | 160 | mA | Min cycle<br>CS# = $V_{IL}$, $I_{OUT}$ = 0 mA<br>Other inputs = $V_{IH}$/$V_{IL}$ |
| Standby power supply current | $I_{SB}$ | — | 40 | mA | Min cycle, CS# = $V_{IH}$,<br>Other inputs = $V_{IH}$/$V_{IL}$ |
| | $I_{SB1}$ | — | 5 | mA | f = 0 MHz<br>$V_{CC}$ ≥ CS# ≥ $V_{CC}$ – 0.2 V,<br>(1) 0 V ≤ $V_{IN}$ ≤ 0.2 V or<br>(2) $V_{CC}$ ≥ $V_{IN}$ ≥ $V_{CC}$ – 0.2 V |
| | | —*[1] | 1.0*[1] | | |
| Output voltage | $V_{OL}$ | — | 0.4 | V | $I_{OL}$ = 8 mA |
| | $V_{OH}$ | 2.4 | — | V | $I_{OH}$ = –4 mA |

Note: 1. This characteristics is guaranteed only for L-version.

## Capacitance

(Ta = +25°C, f = 1.0 MHz)

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Input capacitance*[1] | $C_{IN}$ | — | 6 | pF | $V_{IN}$ = 0 V |
| Input/output capacitance*[1] | $C_{I/O}$ | — | 8 | pF | $V_{I/O}$ = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

chanhvinh.com

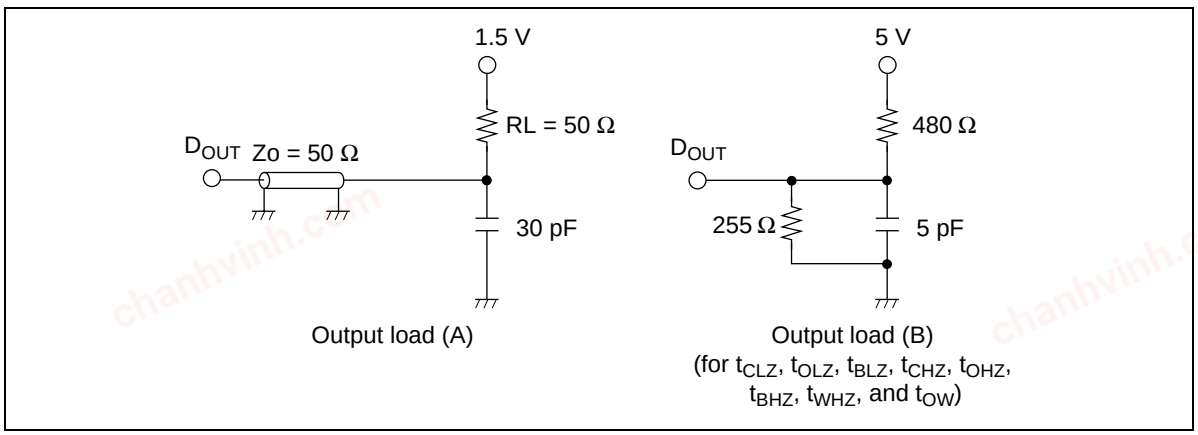


## AC Characteristics

(Ta = 0 to +70°C, $V_{CC}$ = 5.0 V ± 10%, unless otherwise noted.)

### Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)




### Read Cycle

| | | R1RP0416D | | | |
|---|---|---|---|---|---|
| | | -2 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** | **Notes** |
| Read cycle time | $t_{RC}$ | 12 | — | ns | |
| Address access time | $t_{AA}$ | — | 12 | ns | |
| Chip select access time | $t_{ACS}$ | — | 12 | ns | |
| Output enable to output valid | $t_{OE}$ | — | 6 | ns | |
| Byte select to output valid | $t_{BA}$ | — | 6 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | — | ns | |
| Chip select to output in low-Z | $t_{CLZ}$ | 3 | — | ns | 1 |
| Output enable to output in low-Z | $t_{OLZ}$ | 0 | — | ns | 1 |
| Byte select to output in low-Z | $t_{BLZ}$ | 0 | — | ns | 1 |
| Chip deselect to output in high-Z | $t_{CHZ}$ | — | 6 | ns | 1 |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 6 | ns | 1 |
| Byte deselect to output in high-Z | $t_{BHZ}$ | — | 6 | ns | 1 |

chanhvinh.com



## Write Cycle

| | | R1RP0416D | | | |
|---|---|---|---|---|---|
| | | -2 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** | **Notes** |
| Write cycle time | $t_{WC}$ | 12 | — | ns | |
| Address valid to end of write | $t_{AW}$ | 8 | — | ns | |
| Chip select to end of write | $t_{CW}$ | 8 | — | ns | 8 |
| Write pulse width | $t_{WP}$ | 8 | — | ns | 7 |
| Byte select to end of write | $t_{BW}$ | 8 | — | ns | |
| Address setup time | $t_{AS}$ | 0 | — | ns | 5 |
| Write recovery time | $t_{WR}$ | 0 | — | ns | 6 |
| Data to write time overlap | $t_{DW}$ | 6 | — | ns | |
| Data hold from write time | $t_{DH}$ | 0 | — | ns | |
| Write disable to output in low-Z | $t_{OW}$ | 3 | — | ns | 1 |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 6 | ns | 1 |
| Write enable to output in high-Z | $t_{WHZ}$ | — | 6 | ns | 1 |

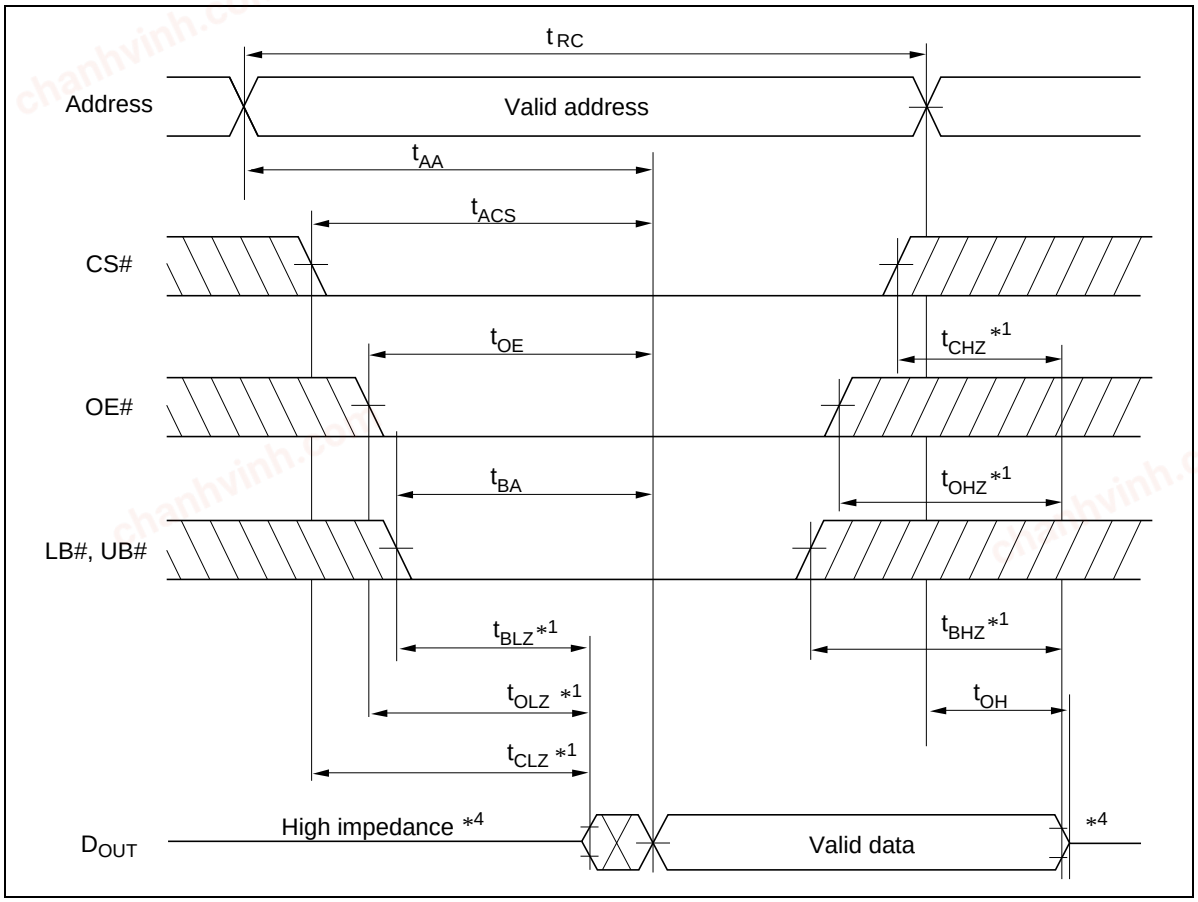
Notes:
1. Transition is measured ±200 mV from steady voltage with output load (B). This parameter is sampled and not 100% tested.
2. If the CS# or LB# or UB# low transition occurs simultaneously with the WE# low transition or after the WE# transition, output remains a high impedance state.
3. WE# and/or CS# must be high during address transition time.
4. If CS#, OE#, LB# and UB# are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
5. $t_{AS}$ is measured from the latest address transition to the latest of CS#, WE#, LB# or UB# going low.
6. $t_{WR}$ is measured from the earliest of CS#, WE#, LB# or UB# going high to the first address transition.
7. A write occurs during the overlap of a low CS#, a low WE# and a low LB# or a low UB# ($t_{WP}$). A write begins at the latest transition among CS# going low, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS# going high, WE# going high and LB# going high or UB# going high.
8. $t_{CW}$ is measured from the later of CS# going low to the end of write.

chanhvinh.com



## Timing Waveforms

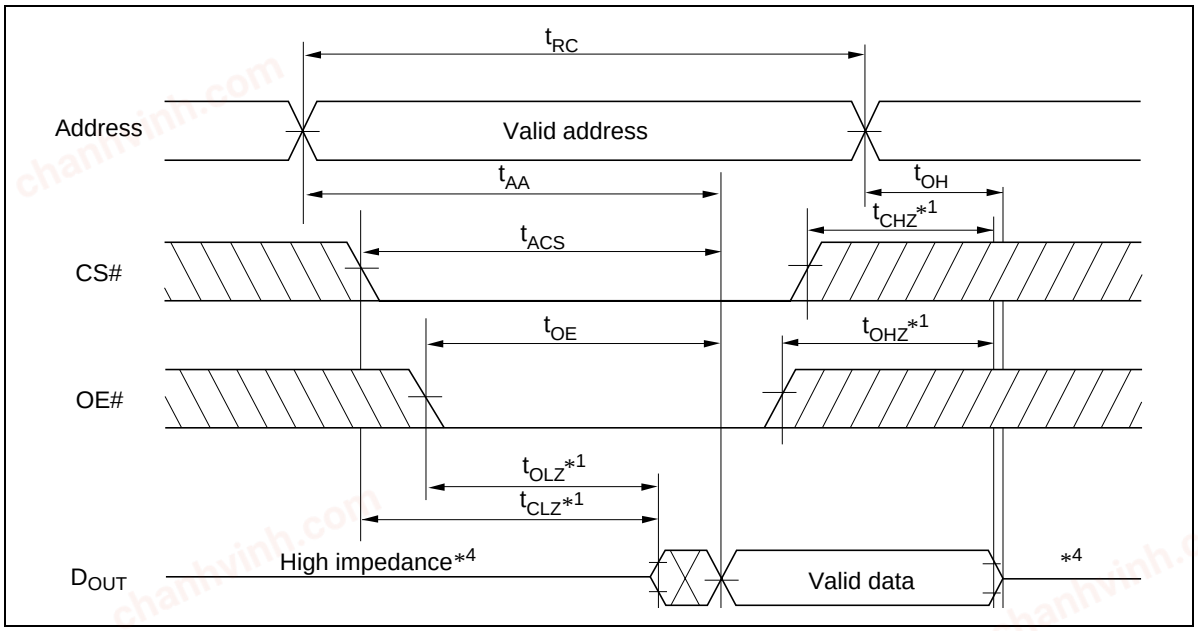
**Read Timing Waveform (1)** ($WE\# = V_{IH}$)



chanhvinh.com



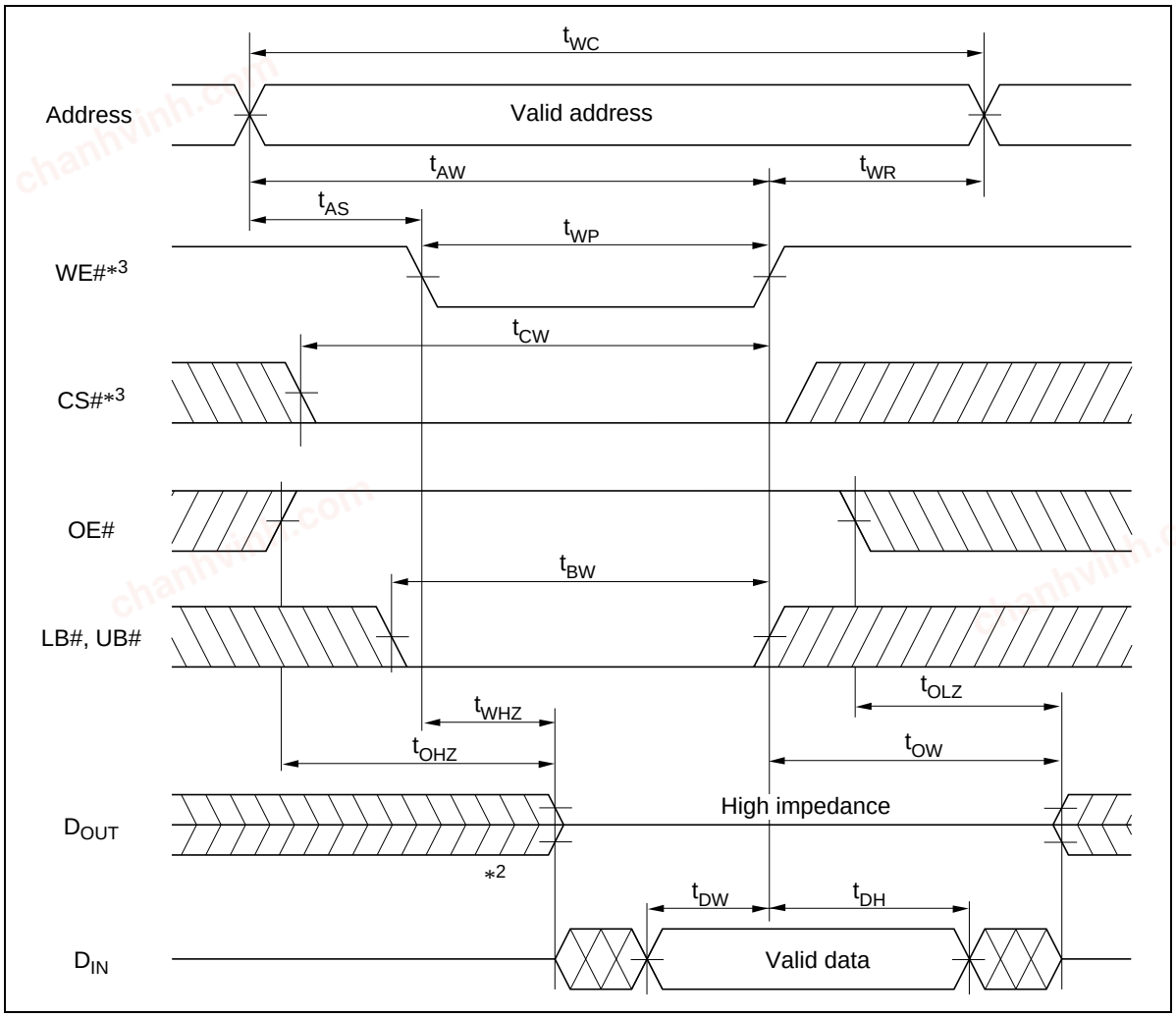
**Read Timing Waveform (2)** (WE# = $V_{IH}$, LB# = $V_{IL}$, UB# = $V_{IL}$)



chanhvinh.com



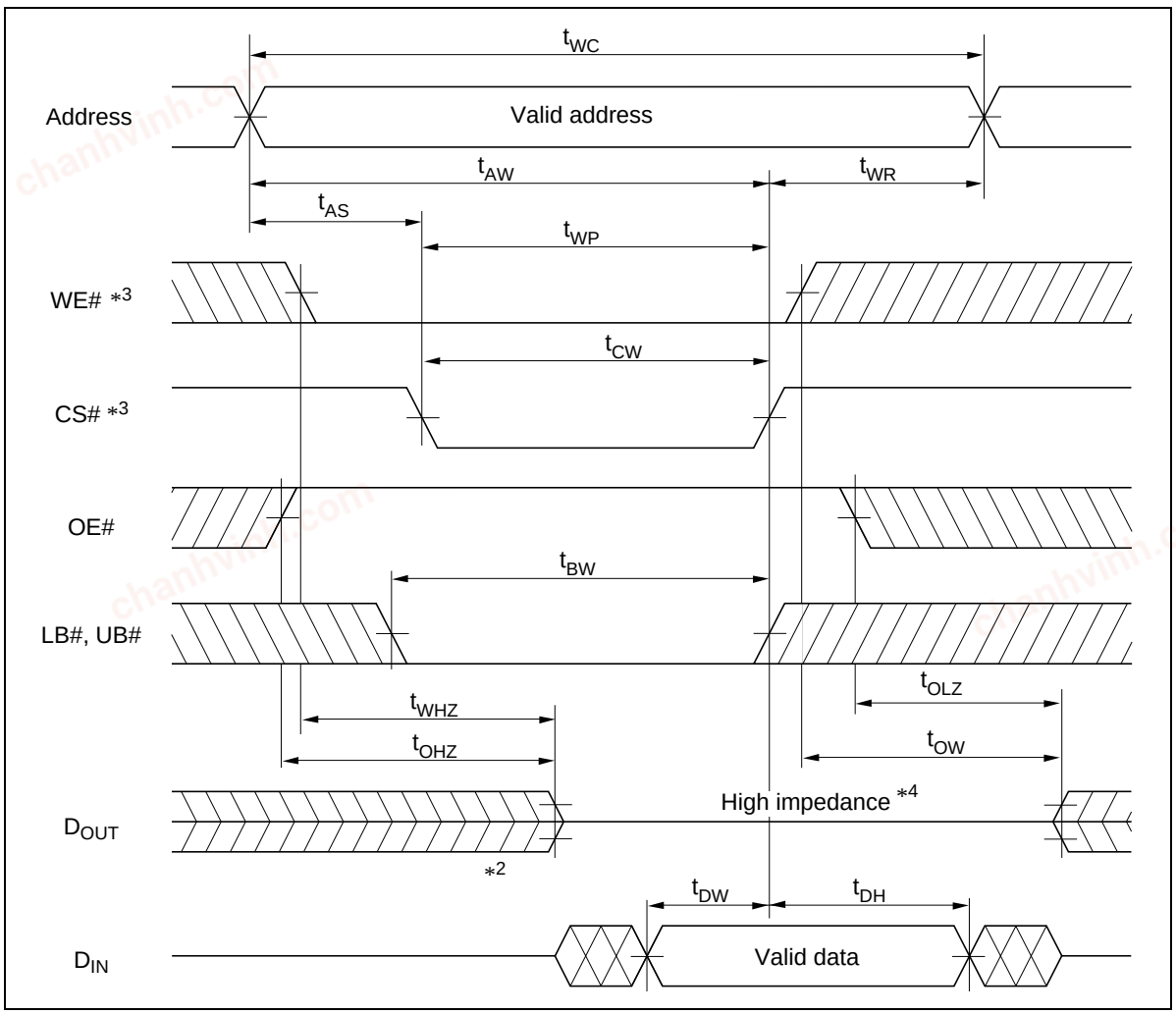
**Write Timing Waveform (1)** (WE# Controlled)



chanhvinh.com



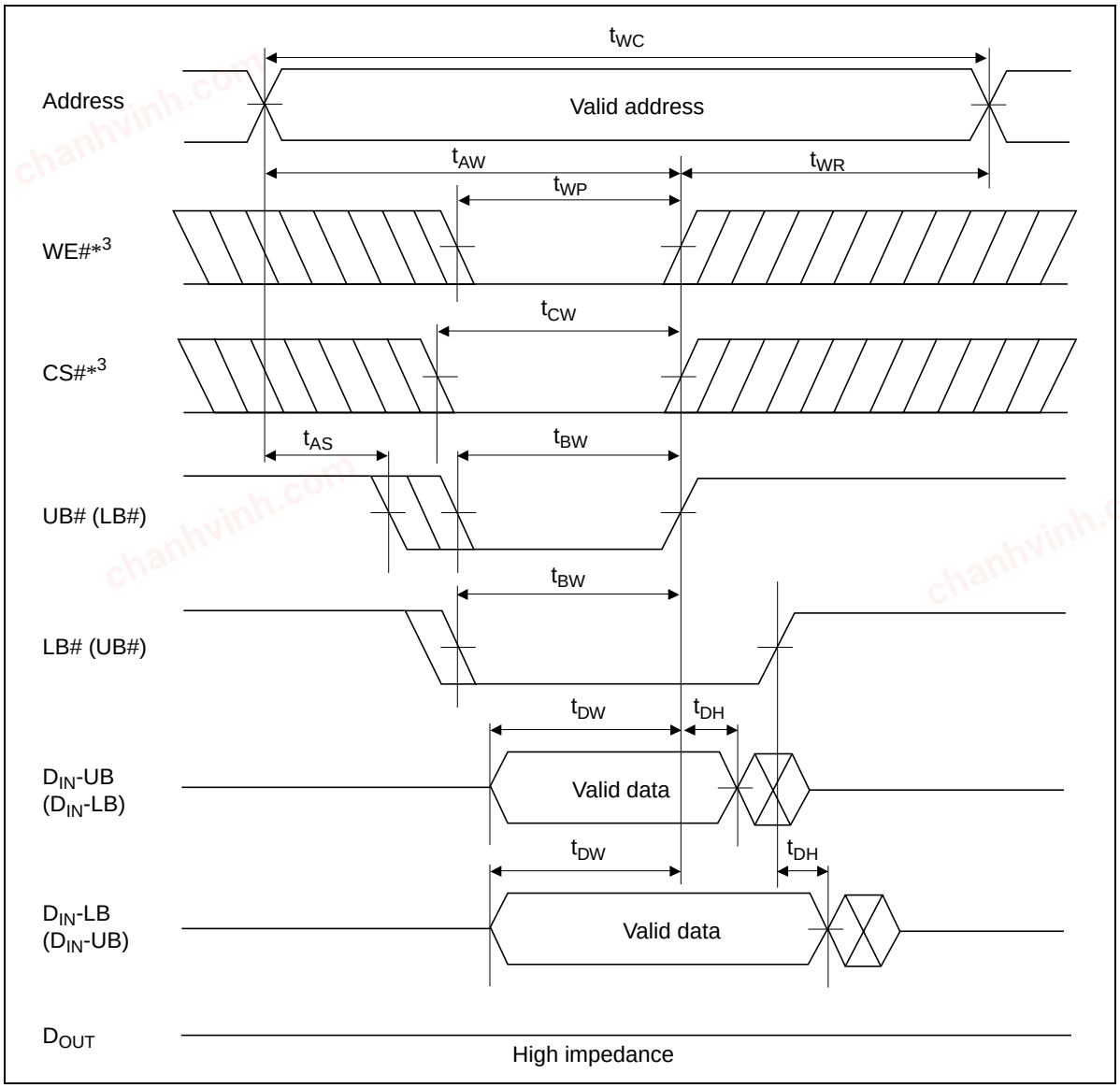
**Write Timing Waveform (2)** (CS# Controlled)



chanhvinh.com



**Write Timing Waveform (3)** (LB#, UB# Controlled, OE# = $V_{IH}$)



chanhvinh.com



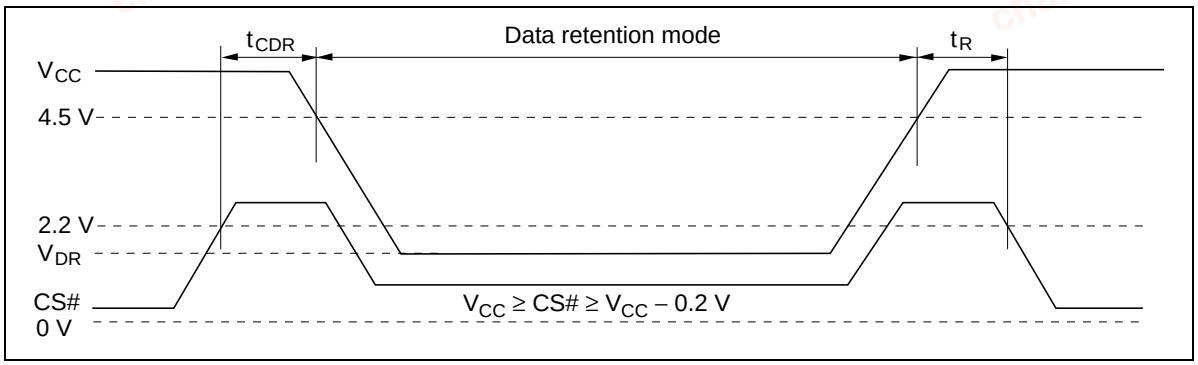
## Low $V_{CC}$ Data Retention Characteristics

(Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | 2.0 | — | V | $V_{CC} \geq CS\# \geq V_{CC} - 0.2$ V,<br>(1) 0 V ≤ $V_{IN}$ ≤ 0.2 V or<br>(2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2$ V |
| Data retention current | $I_{CCDR}$ | — | 500 | µA | $V_{CC}$ = 3 V<br>$V_{CC} \geq CS\# \geq V_{CC} - 0.2$ V,<br>(1) 0 V ≤ $V_{IN}$ ≤ 0.2 V or<br>(2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2$ V |
| Chip deselect to data retention time | $t_{CDR}$ | 0 | — | ns | See retention waveform |
| Operation recovery time | $t_R$ | 5 | — | ms | |

### Low $V_{CC}$ Data Retention Timing Waveform



chanhvinh.com

## Revision History R1RP0416D Series Data Sheet

| Rev. | Date | Contents of Modification | |
|---|---|---|---|
| | | Page | Description |
| 0.01 | Sep. 30, 2003 | — | Initial issue |
| 1.00 | Mar.12.2004 | — | Deletion of Preliminary |

chanhvinh.com

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.

## RENESAS SALES OFFICES

http://www.renesas.com

**Renesas Technology America, Inc.**
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited.**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

**Renesas Technology Europe GmbH**
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

**Renesas Technology Hong Kong Ltd.**
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

**Renesas Technology Taiwan Co., Ltd.**
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology (Shanghai) Co., Ltd.**
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

**Renesas Technology Singapore Pte. Ltd.**
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

© 2003, 2004. Renesas Technology Corp., All rights reserved. Printed in Japan.

Colophon .1.0