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R1LV0108E Series

1Mb Advanced LPSRAM (128k word x 8bit)

R10DS0049EJ0200
Rev.2.00
2011.01.14

Description

The R1LV0108E Series is a family of low voltage 1-Mbit static RAMs organized as 131,072-word by 8-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies. The R1LV0108E Series has realized higher density, higher performance and low power consumption. The R1LV0108E Series is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives. It has been packaged in 32-pin SOP,32-pin TSOP and 32-pin sTSOP.

Features

- Single 2.7~3.6V power supply
- Small stand-by current: 1µA (3.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS1# and CS2
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

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Ordering Information

Orderable Part Name	Access time	Temperature Range	Package	Shipping Container	Quantity
R1LV0108ESP-5SR#B0	55 ns	0 ~ +70°C	525-mil 32-pin plastic SOP PRSP0032DA-A (32P2M-A)	Tube	Max. 25pcs/Tube Max. 225pcs/Inner Bag Max. 900pcs/Inner Box
R1LV0108ESP-5SI#B0		-40 ~ +85°C			
R1LV0108ESP-7SR#B0	70 ns	0 ~ +70°C			
R1LV0108ESP-7SI#B0		-40 ~ +85°C			
R1LV0108ESP-5SR#S0	55 ns	0 ~ +70°C		Embossed tape	1000pcs/Reel
R1LV0108ESP-5SI#S0		-40 ~ +85°C			
R1LV0108ESP-7SR#S0	70 ns	0 ~ +70°C			
R1LV0108ESP-7SI#S0		-40 ~ +85°C			
R1LV0108ESA-5SR#B0	55 ns	0 ~ +70°C	8mm×13.4mm 32-pin plastic sTSOP (normal-bend type) PTSA0032KB-A (32P3K-B)	Tray	Max. 234pcs/Tray Max. 1872pcs/Inner Box
R1LV0108ESA-5SI#B0		-40 ~ +85°C			
R1LV0108ESA-7SR#B0	70 ns	0 ~ +70°C			
R1LV0108ESA-7SI#B0		-40 ~ +85°C			
R1LV0108ESA-5SR#S0	55 ns	0 ~ +70°C		Embossed tape	1000pcs/Reel
R1LV0108ESA-5SI#S0		-40 ~ +85°C			
R1LV0108ESA-7SR#S0	70 ns	0 ~ +70°C			
R1LV0108ESA-7SI#S0		-40 ~ +85°C			
R1LV0108ESF-5SR#B0	55 ns	0 ~ +70°C	8mm×20mm 32-pin plastic TSOP (normal-bend type) PTSA0032KA-A (32P3H-E)	Tray	Max. 156pcs/Tray Max. 1248pcs/Inner Box
R1LV0108ESF-5SI#B0		-40 ~ +85°C			
R1LV0108ESF-7SR#B0	70 ns	0 ~ +70°C			
R1LV0108ESF-7SI#B0		-40 ~ +85°C			
R1LV0108ESF-5SR#S0	55 ns	0 ~ +70°C		Embossed tape	1000pcs/Reel
R1LV0108ESF-5SI#S0		-40 ~ +85°C			
R1LV0108ESF-7SR#S0	70 ns	0 ~ +70°C			
R1LV0108ESF-7SI#S0		-40 ~ +85°C			

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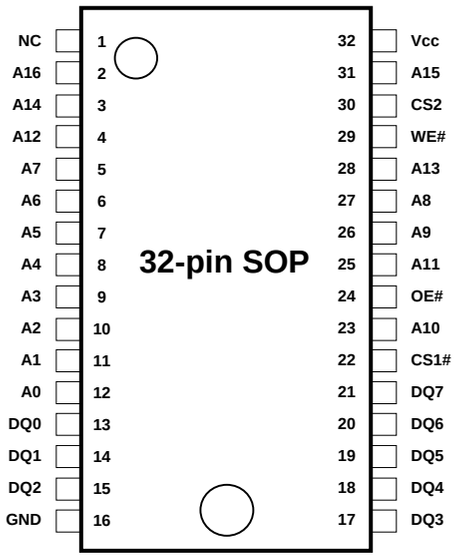
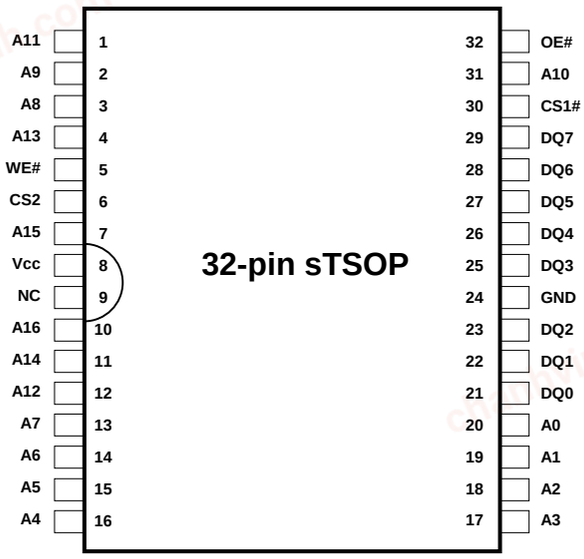
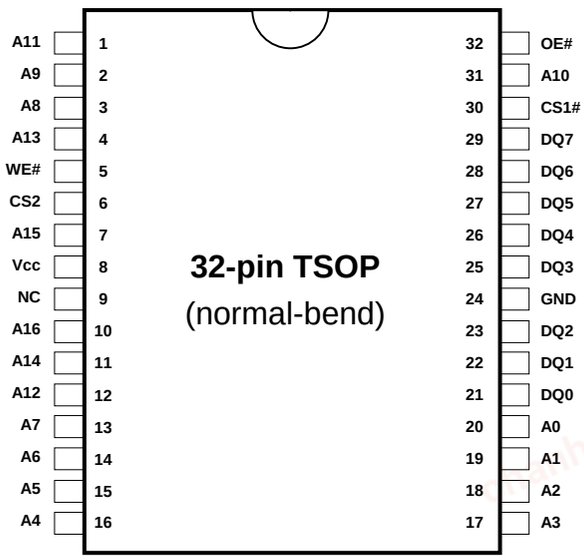
Pin Arrangement







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Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A16	Address input
DQ0 to DQ7	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
WE#	Write enable
OE#	Output enable
NC	Non connection

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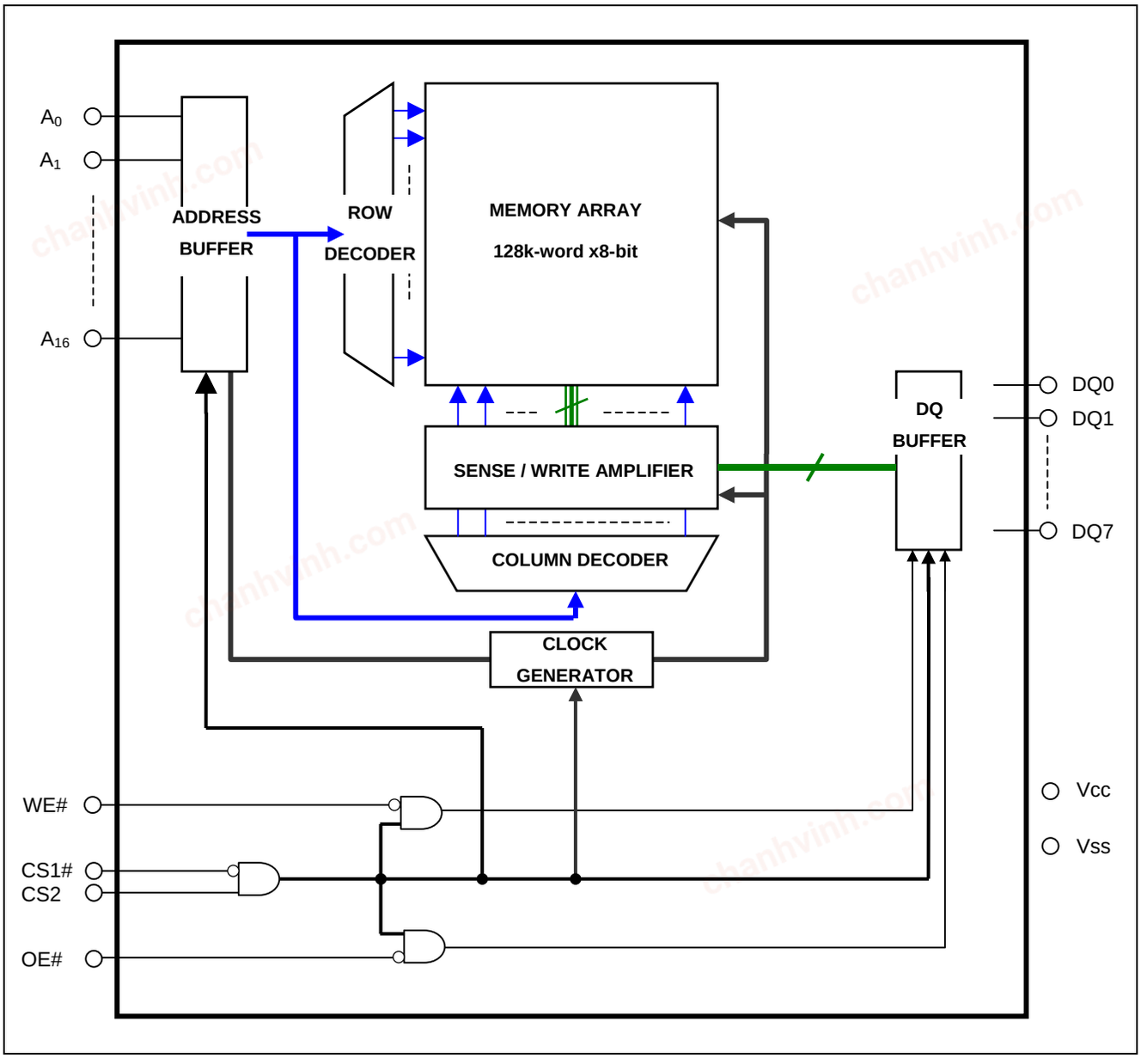
Block Diagram



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Operation Table

CS1#	CS2	WE#	OE#	DQ0~7	Operation
X	L	X	X	High-Z	Stand-by
H	X	X	X	High-Z	Stand-by
L	H	L	X	Din	Write
L	H	H	L	Dout	Read
L	H	H	H	High-Z	Output disable

Note 1. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum

Parameter	Symbol	Value		unit
Power supply voltage relative to Vss	Vcc	-0.3 to +4.6		V
Terminal voltage on any pin relative to Vss	V_T	-0.3[*1] to Vcc+0.3[*2]		V
Power dissipation	P_T	0.7		W
Operation temperature	Topr[*3]	R Ver.	0 to +70	°C
		I Ver.	-40 to +85	
Storage temperature range	Tstg	-65 to 150		°C
Storage temperature range under bias	Tbias[*3]	R Ver.	0 to +70	°C
		I Ver.	-40 to +85	

Note 1. –3.0V for pulse ≤ 30ns (full width at half maximum)
2. Maximum voltage is +4.6V.
3. Ambient temperature range depends on R/I-version. Please see table on page 1.

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DC Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage		Vcc	2.7	3.0	3.6	V	
		Vss	0	0	0	V	
Input high voltage		V_{IH}	2.0	-	Vcc+0.3	V	
Input low voltage		V_{IL}	-0.3	-	0.6	V	1
Ambient temperature range	R Ver.	Ta	0	-	+70	°C	2
	I Ver.		-40	-	+85	°C	2

Note 1. –3.0V for pulse ≤ 30ns (full width at half maximum)
2. Ambient temperature range depends on R/I-version. Please see table on page 1.

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	$\lvert I_{LI} \rvert$	-	-	1	µA	Vin = Vss to Vcc	
Output leakage current	$\lvert I_{LO} \rvert$	-	-	1	µA	CS1# =V_{IH} or CS2 =V_{IL} or OE# =V_{IH}, VI/O =Vss to Vcc	
Average operating current	I_{CC1}	-	15	25	mA	Min. cycle, duty =100%, II/O = 0mA CS1# =V_{IL}, CS2 =V_{IH}, Others = V_{IH}/V_{IL}	
	I_{CC2}	-	2	5	mA	Cycle =1µs, duty =100%, II/O = 0mA CS1# ≤ 0.2V, CS2 ≥ Vcc-0.2V, V_{IH} ≥ Vcc-0.2V, V_{IL} ≤ 0.2V	
Standby current	I_{SB}	-	-	0.33	mA	"CS2 =V_{IL}" or "CS2 = V_{IH} and CS1# =V_{IH}", Others = Vss to Vcc	
Standby current	I_{SB1}	-	1*1	2	µA	~+25°C	Vin = Vss to Vcc (1) CS2 ≤ 0.2 or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V
		-	-	3	µA	~+40°C	
		-	-	8	µA	~+70°C	
		-	-	10	µA	~+85°C	
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -0.5mA	
	V_{OH2}	Vcc - 0.5	-	-	V	I_{OH} = -0.05mA	
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA	

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25ºC), and not 100% tested.

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Capacitance

(Vcc = 2.7V ~ 3.6V, f = 1MHz, Ta = 0 ~ +70°C / -40 ~ +85°C[*2])

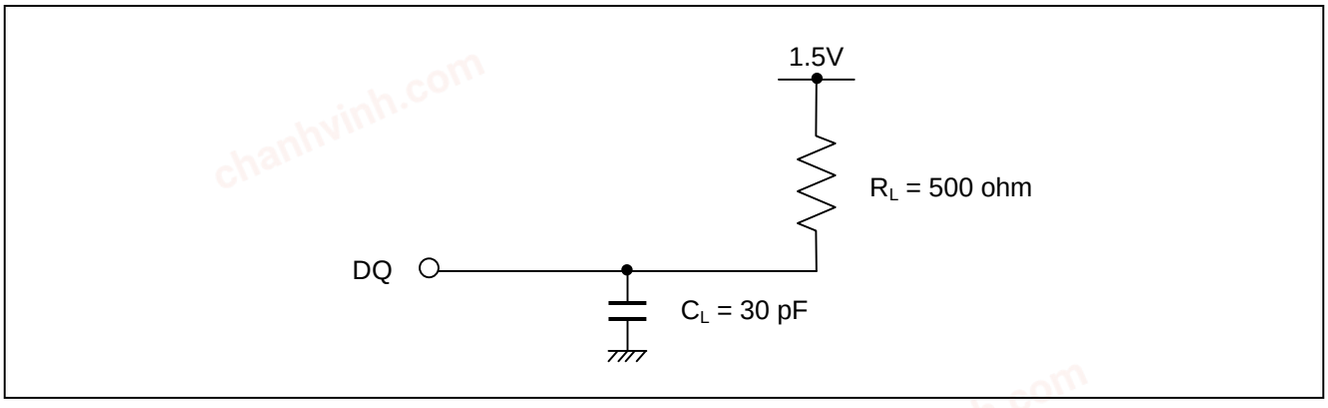
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	-	-	8	pF	Vin =0V	1
Input / output capacitance	$C_{I/O}$	-	-	10	pF	VI/O =0V	1

Note 1. This parameter is sampled and not 100% tested.
2. Ambient temperature range depends on R/I-version. Please see table on page 1.

AC Characteristics

Test Conditions (Vcc = 2.7V ~ 3.6V, Ta = 0 ~ +70°C / -40 ~ +85°C[*1])

- Input pulse levels: VIL = 0.4V, VIH = 2.2V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



Note 1. Ambient temperature range depends on R/I-version. Please see table on page 1.

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Read Cycle

Parameter	Symbol	R1LV0108E**-5S*		R1LV0108E**-7S*		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	55	-	70	-	ns	
Address access time	t_{AA}	-	55	-	70	ns	
Chip select access time	t_{ACS1}	-	55	-	70	ns	
	t_{ACS2}	-	55	-	70	ns	
Output enable to output valid	t_{OE}	-	30	-	35	ns	
Output hold from address change	t_{OH}	5	-	10	-	ns	
Chip select to output in low-Z	t_{CLZ1}	5	-	10	-	ns	2,3
	t_{CLZ2}	5	-	10	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	25	ns	1,2,3
	t_{CHZ2}	0	20	0	25	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1,2,3

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Write Cycle

Parameter	Symbol	R1LV0108E**-5S*		R1LV0108E**-7S*		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	55	-	70	-	ns	
Address valid to end of write	t_{AW}	50	-	55	-	ns	
Chip select to end of write	t_{CW}	50	-	55	-	ns	5
Write pulse width	t_{WP}	45	-	50	-	ns	4
Address setup time	t_{AS}	0	-	0	-	ns	6
Write recovery time	t_{WR}	0	-	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	30	-	ns	
Data hold from write time	t_{DH}	0	-	0	-	ns	
Output enable from end of write	t_{OW}	5	-	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	0	25	ns	1,2

Note
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE#.
   A write begins at the latest transition among CS1# going low, CS2 going high and WE# going low.
   A write ends at the earliest transition among CS1# going high, CS2 going low and WE# going high.
   t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS1# going low or CS2 going high to end of write.
6. t_{AS} is measured the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.
8. Don't apply inverted phase signal externally when DQ pin is output mode.

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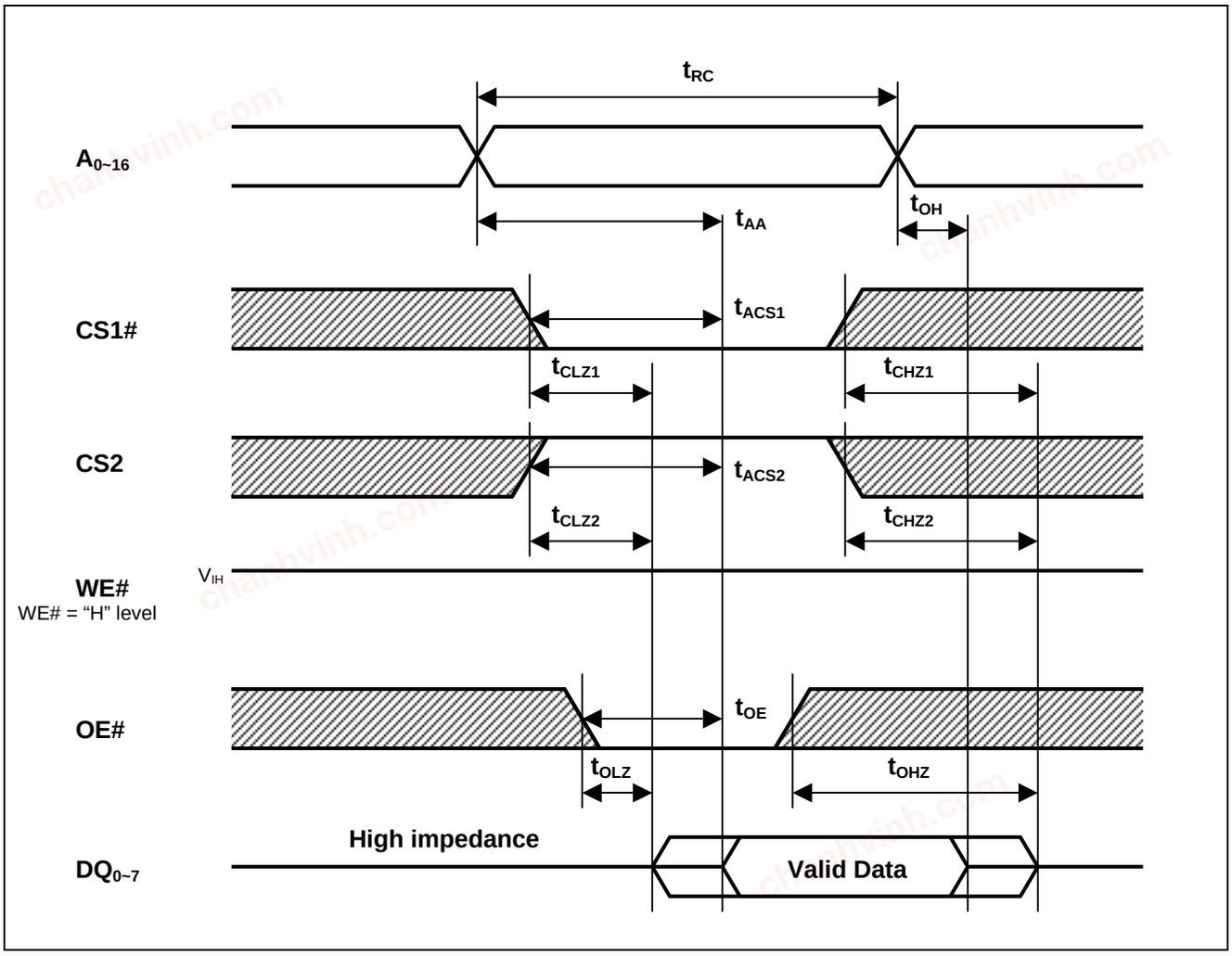
Timing Waveforms

Read Cycle



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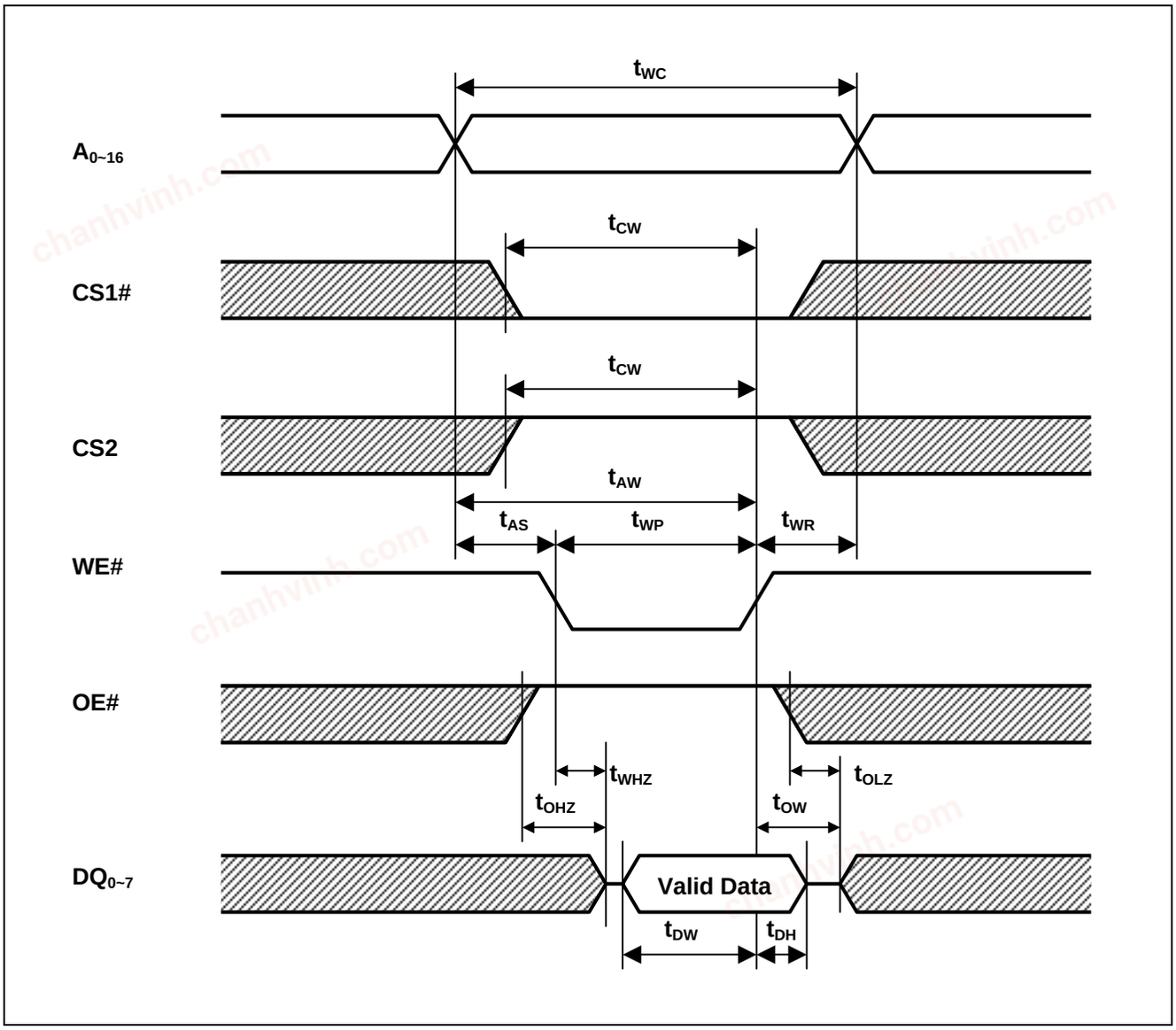
Write Cycle (1) (WE# CLOCK)



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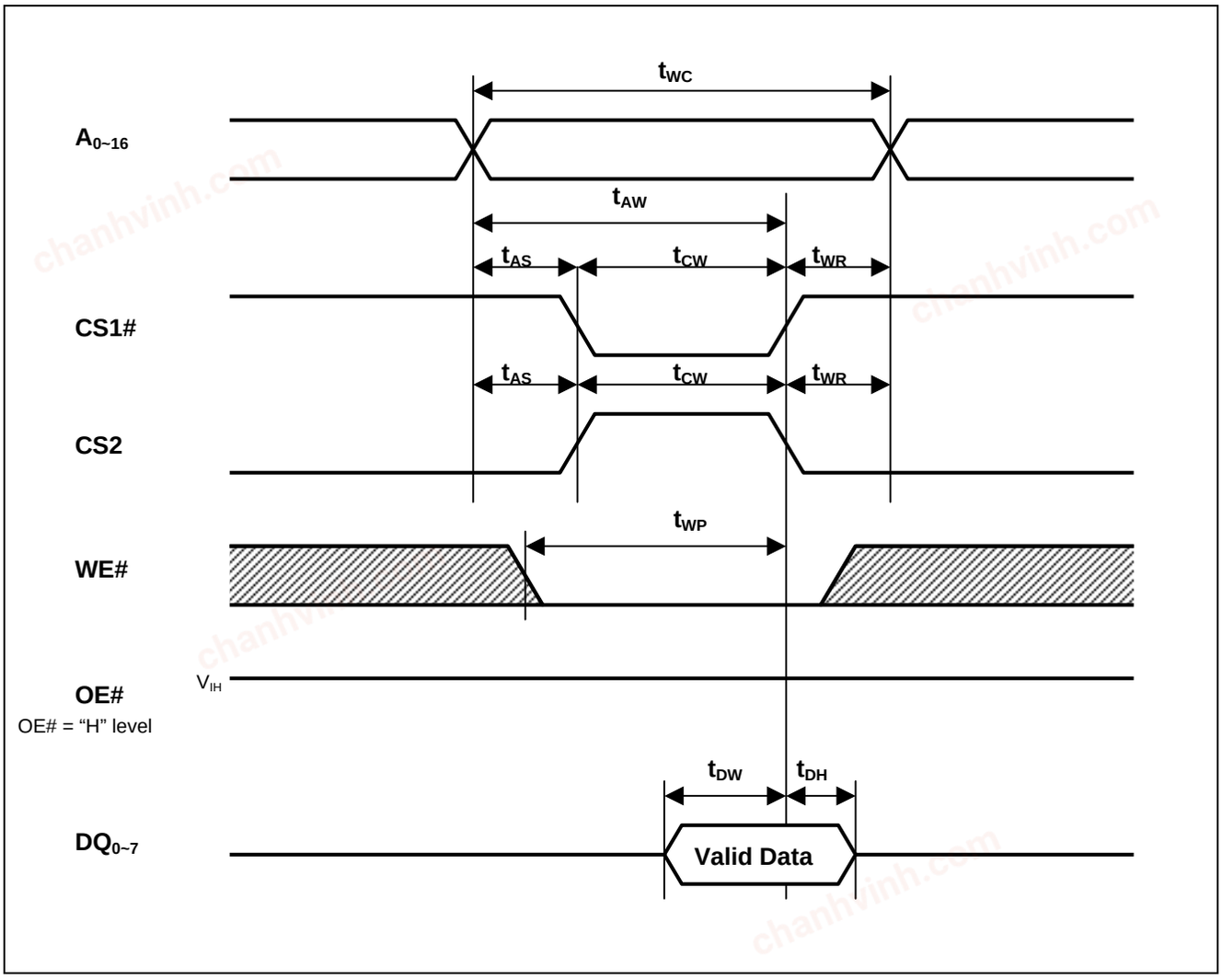
Write Cycle (2) (CS1#, CS2 CLOCK)



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Low Vcc Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[*2]	
V_{CC} for data retention	V_{DR}	2.0	-	3.6	V	Vin ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V	
Data retention current	I_{CCDR}	-	1[*1]	2	µA	~+25°C	Vcc=3.0V, Vin ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V
		-	-	3	µA	~+40°C	
		-	-	8	µA	~+70°C	
		-	-	10	µA	~+85°C	
Chip deselect to data retention time	t_{CDR}	0	-	-	ns	See retention waveform.	
Operation recovery time	t_R	5	-	-	ms		

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25ºC), and not 100% tested.

2. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE#, CS1#, OE#, DQ) can be in the high impedance state.
   If CS1# controls data retention mode, CS2 must be CS2 ≥ Vcc-0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, WE# ,OE#, DQ) can be in the high impedance state.

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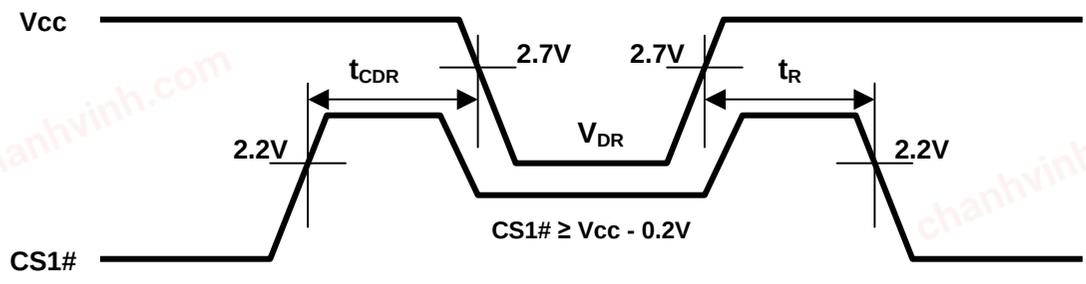
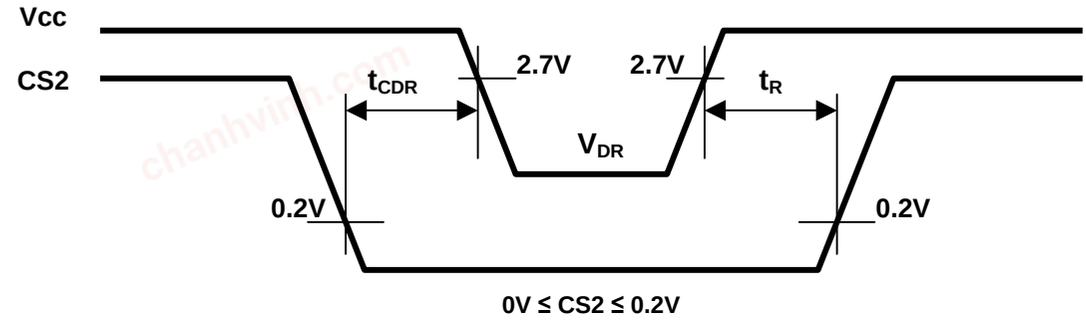
Low Vcc Data Retention Timing Waveforms

(1) CS1# Controlled



(2) CS2 Controlled



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Revision History	R1LV0108E Series Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	2010.12.27	-	First Edition issued
2.00	2011.01.14	2	Ordering Information is revised

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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