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# R1LP0408D Series

## 4Mb Advanced LPSRAM (512-kword × 8-bit)

R10DS0104EJ0200
Rev.2.00
2012.5.30

## Description

The R1LP0408D Series is a family of 4-Mbit static RAMs organized 512-kword × 8-bit, fabricated by Renesas's high-performance CMOS and TFT technologies. The R1LP0408D Series has realized higher density, higher performance and low power consumption. The R1LP0408D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 32-pin SOP and 32-pin TSOP.

## Features

- Single 5V supply: 4.5V to 5.5V
- Access time: 55/70ns (max)
- Power dissipation:
  — Standby: 4µW (typ)
- Equal access and cycle times
- Common data input and output
  — Three state output
- Directly TTL compatible
  — All inputs and outputs
- Battery backup operation

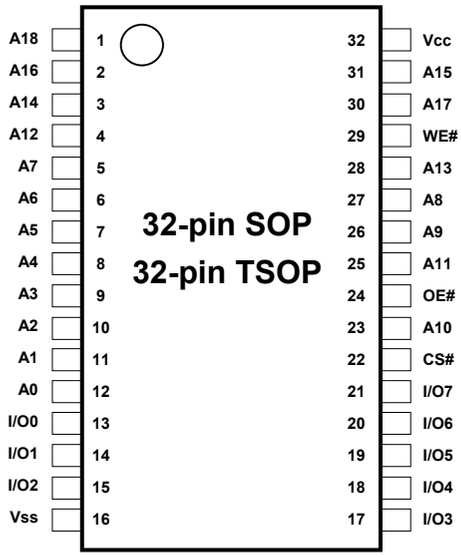
## Part Name Information

| Part Name | Access time | Temperature Range | Package | Shipping Container | Quantity |
|---|---|---|---|---|---|
| R1LP0408DSP-5SR#B* | 55 ns | 0 ~ +70°C | 525-mil 32-pin plastic SOP<br>PRSP0032DF-A<br>(032P2S-A) | Tube | Max. 25pcs/Tube<br>Max. 225pcs/Inner Bag<br>Max. 900pcs/Inner Box |
| R1LP0408DSP-5SI#B* | | -40 ~ +85°C | | | |
| R1LP0408DSP-7SR#B* | 70 ns | 0 ~ +70°C | | | |
| R1LP0408DSP-7SI#B* | | -40 ~ +85°C | | | |
| R1LP0408DSP-5SR#S* | 55 ns | 0 ~ +70°C | | Embossed tape | 1000pcs/Reel |
| R1LP0408DSP-5SI#S* | | -40 ~ +85°C | | | |
| R1LP0408DSP-7SR#S* | 70 ns | 0 ~ +70°C | | | |
| R1LP0408DSP-7SI#S* | | -40 ~ +85°C | | | |
| R1LP0408DSB-5SR#B* | 55 ns | 0 ~ +70°C | 400-mil 32-pin plastic TSOP(II)<br>PTSB0032DC-A<br>(032PTY-A) | Tray | Max. 117pcs/Tray<br>Max. 936pcs/Inner Box |
| R1LP0408DSB-5SI#B* | | -40 ~ +85°C | | | |
| R1LP0408DSB-7SR#B* | 70 ns | 0 ~ +70°C | | | |
| R1LP0408DSB-7SI#B* | | -40 ~ +85°C | | | |
| R1LP0408DSB-5SR#S* | 55 ns | 0 ~ +70°C | | Embossed tape | 1000pcs/Reel |
| R1LP0408DSB-5SI#S* | | -40 ~ +85°C | | | |
| R1LP0408DSB-7SR#S* | 70 ns | 0 ~ +70°C | | | |
| R1LP0408DSB-7SI#S* | | -40 ~ +85°C | | | |

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**Pin Arrangement**



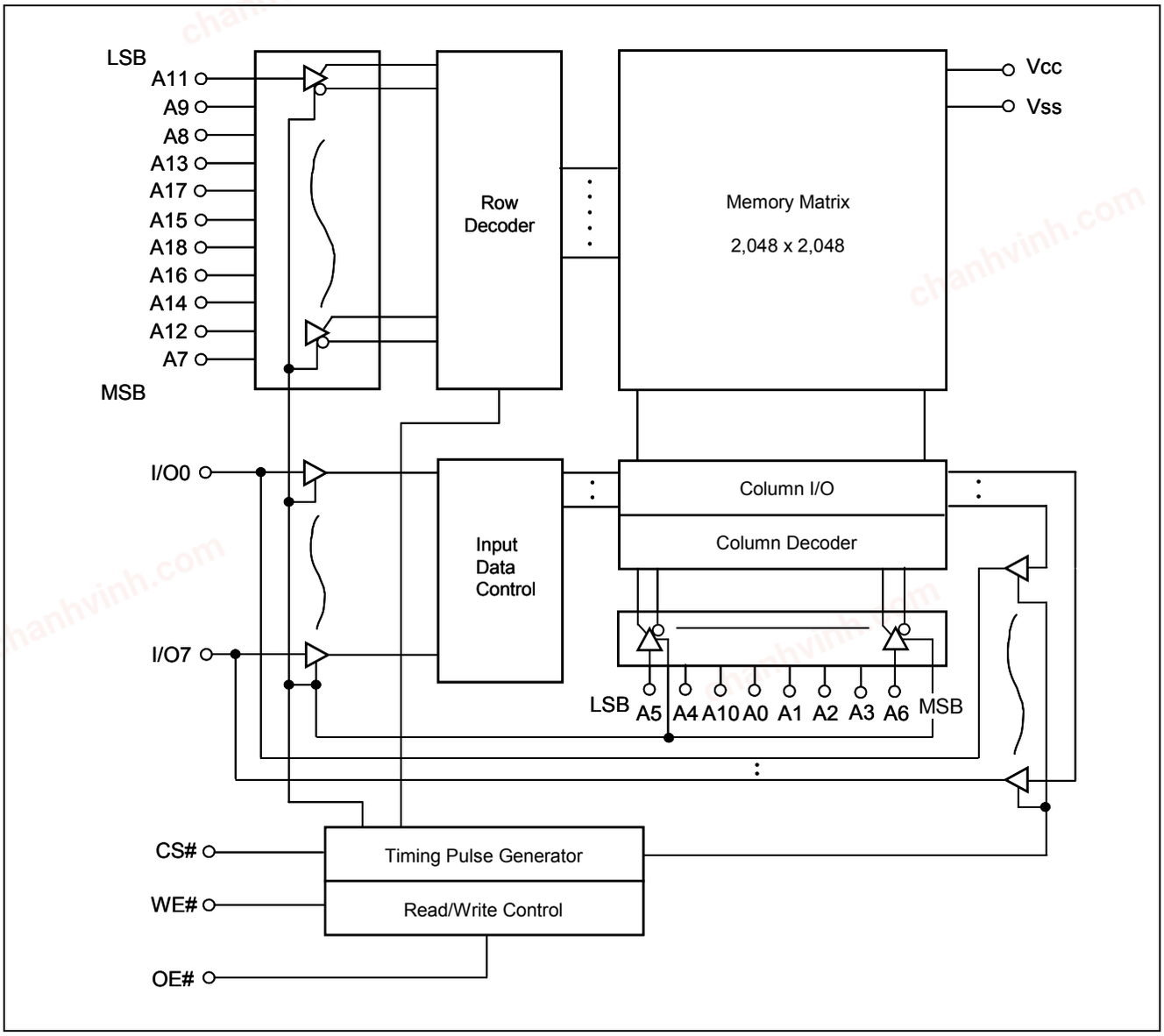

## Pin Description

| Pin name | Function |
|---|---|
| Vcc | Power supply |
| Vss | Ground |
| A0 to A18 | Address input |
| I/O0 to I/O7 | Data input/output |
| CS# | Chip select |
| WE# | Write enable |
| OE# | Output enable |

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## Block Diagram



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## Operation Table

| WE# | CS# | OE# | Mode | Vcc current | I/O0 to I/O7 | Ref. cycle |
|---|---|---|---|---|---|---|
| × | H | × | Not selected | $I_{SB}$, $I_{SB1}$ | High-Z | — |
| H | L | H | Output disable | Icc | High-Z | — |
| H | L | L | Read | Icc | Dout | Read cycle |
| L | L | H | Write | Icc | Din | Write cycle (1) |
| L | L | L | Write | Icc | Din | Write cycle (2) |

Note 1. H: $V_{IH}$ L:$V_{IL}$ ×: $V_{IH}$ or $V_{IL}$

## Absolute Maximum Ratings

| Parameter | Symbol | Value | | unit |
|---|---|---|---|---|
| Power supply voltage relative to Vss | Vcc | -0.5 to +7.0 | | V |
| Terminal voltage on any pin relative to Vss | $V_T$ | -0.5[*1] to Vcc+0.3[*2] | | V |
| Power dissipation | $P_T$ | 0.7 | | W |
| Operation temperature | Topr[*3] | R Ver. | 0 to +70 | °C |
| | | I Ver. | -40 to +85 | |
| Storage temperature range | Tstg | -65 to 150 | | °C |
| Storage temperature range under bias | Tbias[*3] | R Ver. | 0 to +70 | °C |
| | | I Ver. | -40 to +85 | |

Note 1. -3.0V for pulse ≤ 30ns (full width at half maximum)
2. Maximum voltage is +7.0V.
3. Ambient temperature range depends on R/I-version. Please see table on page 1.

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## DC Operating Conditions

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Supply voltage | | Vcc | 4.5 | 5.0 | 5.5 | V | |
| | | Vss | 0 | 0 | 0 | V | |
| Input high voltage | | $V_{IH}$ | 2.2 | — | Vcc+0.3 | V | |
| Input low voltage | | $V_{IL}$ | -0.3 | — | 0.8 | V | 1 |
| Ambient temperature range | R Ver. | Ta | 0 | — | +70 | °C | 2 |
| | I Ver. | | -40 | — | +85 | °C | 2 |

Note 1. -3.0V for pulse ≤ 30ns (full width at half maximum)
2. Ambient temperature range depends on R/I-version. Please see table on page 1.

## DC Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $\lvert I_{LI} \rvert$ | — | — | 1 | µA | Vin = Vss to Vcc |
| Output leakage current | $\lvert I_{LO} \rvert$ | — | — | 1 | µA | CS# =$V_{IH}$ or OE# =$V_{IH}$,<br>VI/O =Vss to Vcc |
| Operating current | Icc | — | 5*1 | 10 | mA | CS# =$V_{IL}$,<br>Others = $V_{IH}$/$V_{IL}$, II/O = 0mA |
| Average operating current | $I_{CC1}$ | — | 15*1 | 25 | mA | Min. cycle, duty =100%, II/O = 0mA<br>CS# =$V_{IL}$, Others = $V_{IH}$/$V_{IL}$ |
| | $I_{CC2}$ | — | 3*1 | 5 | mA | Cycle =1µs, duty =100%, II/O = 0mA<br>CS# ≤ 0.2V,<br>$V_{IH}$ ≥ Vcc-0.2V, $V_{IL}$ ≤ 0.2V |
| Standby current | $I_{SB}$ | — | 0.1*1 | 0.5 | mA | CS# =$V_{IH}$,<br>Others = Vss to Vcc |
| Standby current | $I_{SB1}$ | — | 0.8*1 | 2.5 | µA | ~+25°C — Vin = Vss to Vcc, CS# ≥ Vcc-0.2V |
| | | — | 1*2 | 3 | µA | ~+40°C |
| | | — | — | 8 | µA | ~+70°C |
| | | — | — | 10 | µA | ~+85°C |
| Output high voltage | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = -1mA |
| | $V_{OH2}$ | Vcc-0.5 | — | — | V | $I_{OH}$ = -0.1mA |
| Output low voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 2.1mA |

Note 1. Typical parameter indicates the value for the center of distribution at 5.0V (Ta=25ºC), and not 100% tested.
2. Typical parameter indicates the value for the center of distribution at 5.0V (Ta=40ºC), and not 100% tested.

## Capacitance

(Vcc = 4.5V ~ 5.5V, f = 1MHz, Ta = 0 ~ +70°C / -40 ~ +85°C*2)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions | Note |
|---|---|---|---|---|---|---|---|
| Input capacitance | C in | — | — | 8 | pF | Vin =0V | 1 |
| Input / output capacitance | $C_{I/O}$ | — | — | 10 | pF | VI/O =0V | 1 |

Note 1. This parameter is sampled and not 100% tested.
2. Ambient temperature range depends on R/I-version. Please see table on page 1.

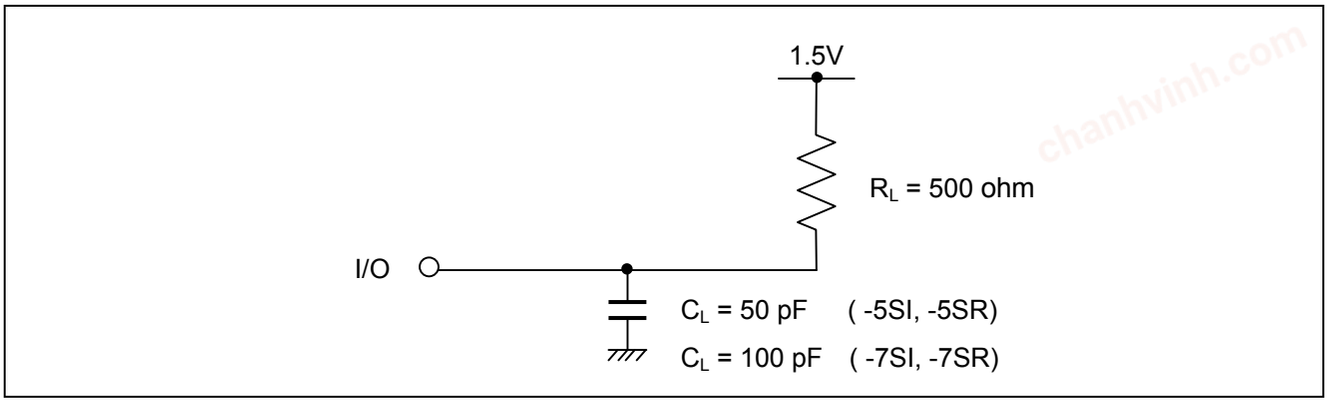
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## AC Characteristics

Test Conditions (Vcc = 4.5V ~ 5.5V, Ta = 0 ~ +70°C / -40 ~ +85°C[*1])

- Input pulse levels: VIL = 0.4V, VIH = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)




Note 1. Ambient temperature range depends on R/I-version. Please see table on page 1.

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### Read Cycle

| Parameter | Symbol | R1LP0408DS*-5S* | | R1LP0408DS*-7S* | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Read cycle time | $t_{RC}$ | 55 | — | 70 | — | ns | |
| Address access time | $t_{AA}$ | — | 55 | — | 70 | ns | |
| Chip select access time | $t_{ACS}$ | — | 55 | — | 70 | ns | |
| Output enable to output valid | $t_{OE}$ | — | 25 | — | 35 | ns | |
| Chip select to output in low-Z | $t_{CLZ}$ | 10 | — | 10 | — | ns | 2 |
| Output enable to output in low-Z | $t_{OLZ}$ | 5 | — | 5 | — | ns | 2 |
| Chip deselect to output in high-Z | $t_{CHZ}$ | 0 | 20 | 0 | 25 | ns | 1,2 |
| Output disable to output in high-Z | $t_{OHZ}$ | 0 | 20 | 0 | 25 | ns | 1,2 |
| Output hold from address change | $t_{OH}$ | 10 | — | 10 | — | ns | |

### Write Cycle

| Parameter | Symbol | R1LP0408DS*-5S* | | R1LP0408DS*-7S* | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Write cycle time | $t_{WC}$ | 55 | — | 70 | — | ns | |
| Chip select to end of write | $t_{CW}$ | 50 | — | 60 | — | ns | 4 |
| Address setup time | $t_{AS}$ | 0 | — | 0 | — | ns | 5 |
| Address valid to end of write | $t_{AW}$ | 50 | — | 60 | — | ns | |
| Write pulse width | $t_{WP}$ | 40 | — | 50 | — | ns | 3,12 |
| Write recovery time | $t_{WR}$ | 0 | — | 0 | — | ns | 6 |
| Write to output in high-Z | $t_{WHZ}$ | 0 | 20 | 0 | 25 | ns | 1,2,7 |
| Data to write time overlap | $t_{DW}$ | 25 | — | 30 | — | ns | |
| Data hold from write time | $t_{DH}$ | 0 | — | 0 | — | ns | |
| Output enable from end of write | $t_{OW}$ | 5 | — | 5 | — | ns | 2 |
| Output disable to output in high-Z | $t_{OHZ}$ | 0 | 20 | 0 | 25 | ns | 1,2,7 |

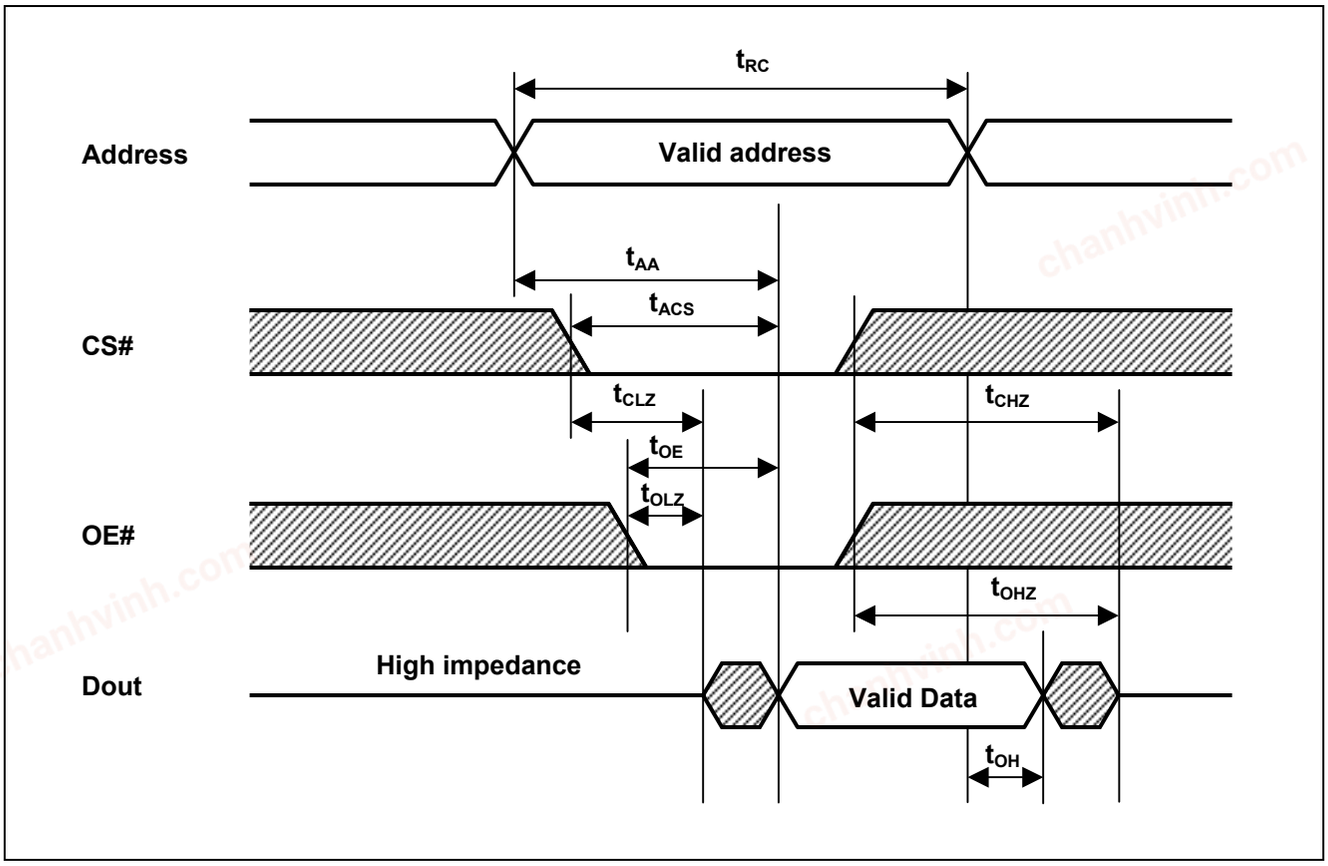
Note
1. $t_{CHZ}$, $t_{OHZ}$ and $t_{WHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap ($t_{WP}$) of a low CS# and a low WE#.
   A write begins at the later transition of CS# going low or WE# going low.
   A write ends at the earlier transition of CS# going high or WE# going high.
   $t_{WP}$ is measured from the beginning of write to the end of write.
4. $t_{CW}$ is measured from CS# going low to end of write.
5. $t_{AS}$ is measured the address valid to the beginning of write.
6. $t_{WR}$ is measured from the earlier of WE# or CS# going high to the end of write cycle.
7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
8. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
9. Dout is the same phase of the write data of this write cycle.
10. Dout is the read data of next address.
11. If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
12. In the write cycle with OE# low fixed, $t_{WP}$ must satisfy the following equation to avoid a problem of data bus contention.
    $t_{WP} \geq t_{DW}$ min + $t_{WHZ}$ max

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## Timing Waveforms

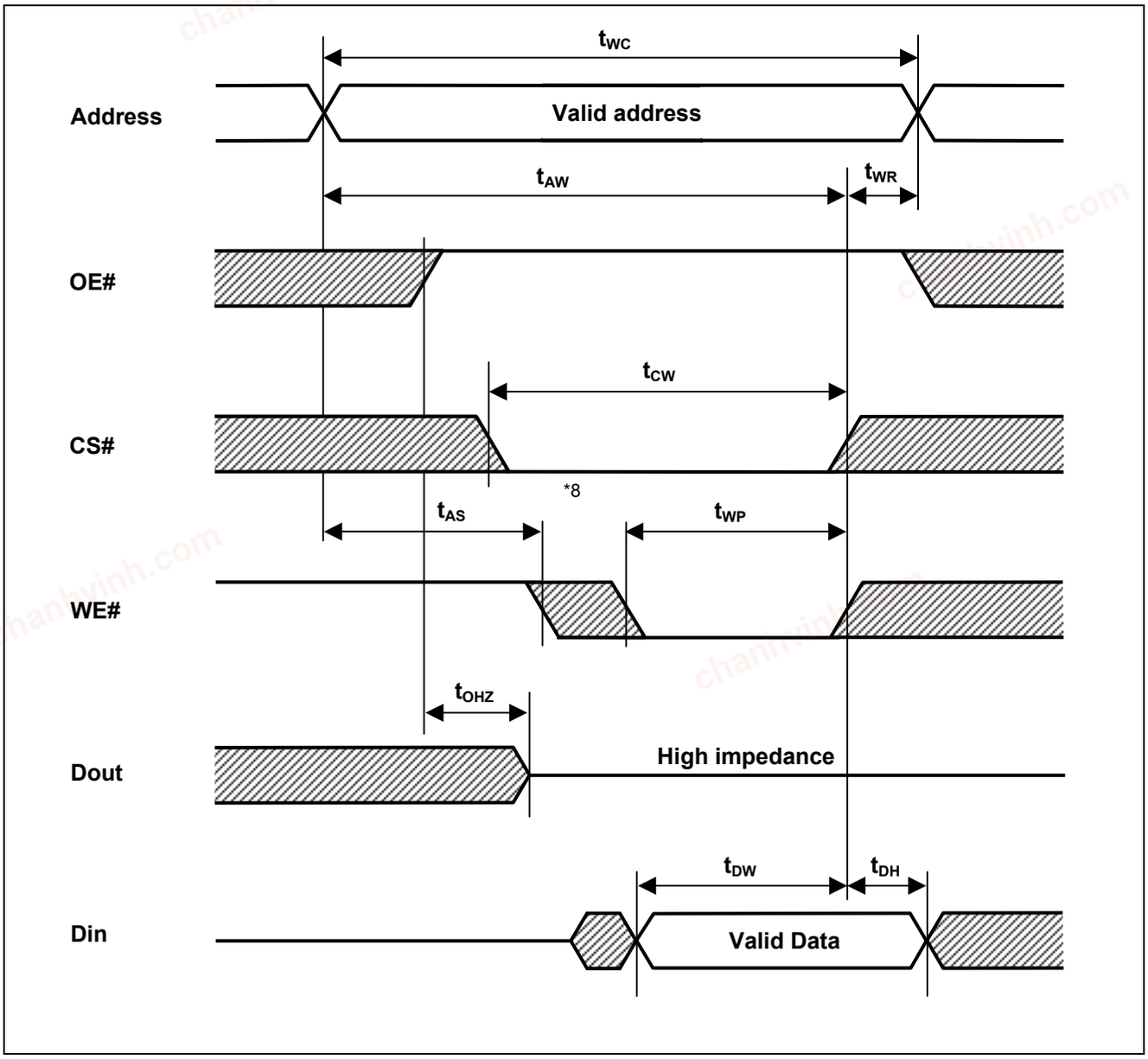
### Read Cycle (WE# = $V_{IH}$ )



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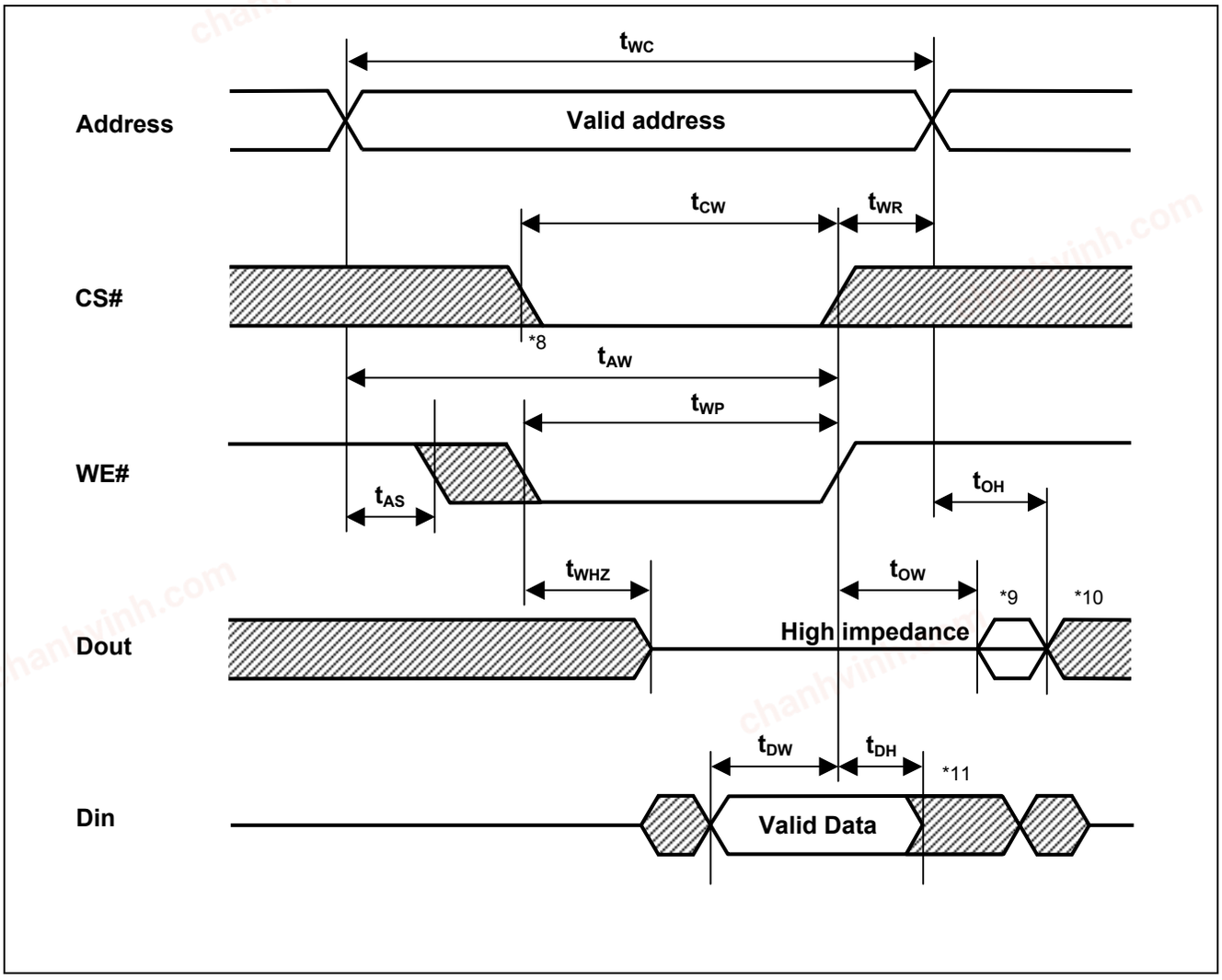
**Write Cycle (1) (OE# CLOCK)**



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**Write Cycle (2) (OE# Low Fixed)**



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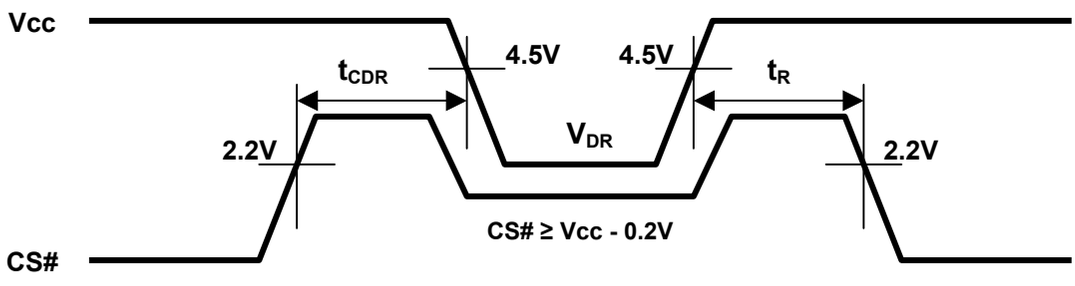
## Low Vcc Data Retention Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions[*3] | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | 2.0 | — | 5.5 | V | Vin ≥ 0V, CS# ≥ Vcc-0.2V | |
| Data retention current | $I_{CCDR}$ | — | 0.8[*1] | 2.5 | µA | ~+25°C | Vcc=3.0V, Vin ≥ 0V, CS# ≥ Vcc-0.2V |
| | | — | 1[*2] | 3 | µA | ~+40°C | |
| | | — | — | 8 | µA | ~+70°C | |
| | | — | — | 10 | µA | ~+85°C | |
| Chip deselect time to data retention | $t_{CDR}$ | 0 | — | — | ns | See retention waveform. | |
| Operation recovery time | $t_R$ | 5 | — | — | ms | | |

Note
1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.
2. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40ºC), and not 100% tested.
3. CS# controls address buffer, WE# buffer, OE# buffer and Din buffer. If data retention mode, Vin levels (address, WE#, OE#, I/O) can be in the high impedance state.

## Low Vcc Data Retention Timing Waveforms

**CS# Controlled**



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| Revision History | R1LP0408D Series Data Sheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | 2012.4.13 | — | First Edition issued (SOP package) |
| 2.00 | 2012.5.30 | P.1 | Add TSOP package to Part Name Information |
| | | | |

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**Renesas Electronics America Inc.**
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

**Renesas Electronics Hong Kong Limited**
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

**Renesas Electronics Taiwan Co., Ltd.**
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

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1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics Korea Co., Ltd.**
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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