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ISL97687

4-Channel LED Driver with Phase Shift Control and 10-Bit Dimming Resolution

FN7714
Rev.4.00
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The ISL97687 is a PWM controlled LED driver that supports four channels of LED current, for Monitor and TV LCD backlight applications. It is capable of driving 160mA per channel from a 9V to 32V input supply, with current sources rated up to 75V absolute maximum.

The ISL97687's current sources achieve typical current matching to ±1%, while dynamically maintaining the minimum required V_{OUT} necessary for regulation. This adaptive scheme compensates for the non-uniformity of forward voltage variance in the LED strings.

The ISL97687 can decode both an incoming PWM signal and an analog input voltage, for DC-to-PWM dimming applications. Modes include direct PWM and several modes where the PWM frequency is synthesized on chip at 10-bit resolution. This can be either free running, or synchronized with the frame rate to give both a frequency and a phase lock, minimizing panel to panel variation and display flicker. Phase shift is supported, reducing flicker and audio noise, as is multiplication of the incoming decoded analog and PWM values.

The ISL97687 has an advanced dynamic headroom control function that monitors the highest LED forward voltage string, and regulates the output to the correct level to minimize power loss. This proprietary regulation scheme also allows for extremely linear PWM dimming from 0.02% to 100%. The LED current can also be switched between two current levels, giving support for 3D applications. The ISL97687 incorporates extensive protections of string open and short-circuit detections, OVP, and OTP.

Features

- 4x160mA, 75V rated channels with integrated channel regulation FETs
- Channels can be ganged for high current
  - 2x350mA
  - 1x700mA
- 9V~32V input voltage
- Dimming modes:
  - Direct PWM dimming from 100Hz~30kHz
  - PWM dimming with adjustable output frequency
    - 10-bit dimming resolution
    - V_{SYNC} function to synchronize PWM signal to frame rate
    - Phase shift
  - Analog to PWM dimming with 8-bit resolution
- 2 selectable current levels for 3D applications
- Current matching of ±1%
- Integrated fault protection features such as string open circuit protection, string short-circuit protection, overvoltage protection, and over-temperature protection
- 28 Ld 5mmx5mm TQFN and 28 Ld 300mil SOIC packages available

Applications

- Monitor/TV LED backlighting
- General/industrial/automotive lighting

Related Literature

For a full list of related documents, visit our website:

- ISL97687 device page

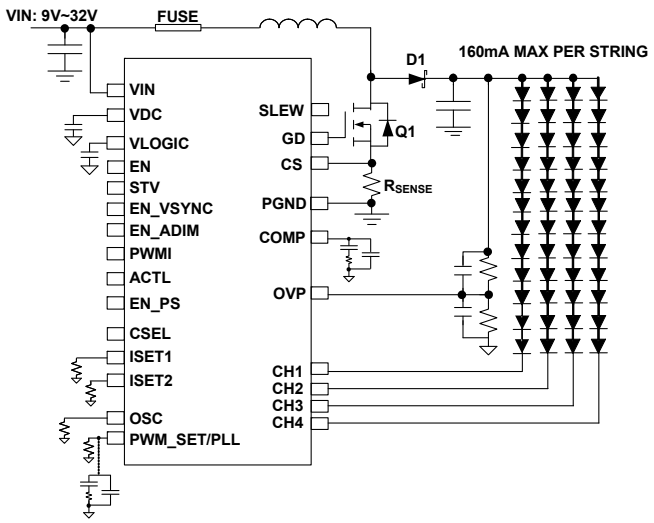


FIGURE 1. ISL97687 APPLICATION DIAGRAM

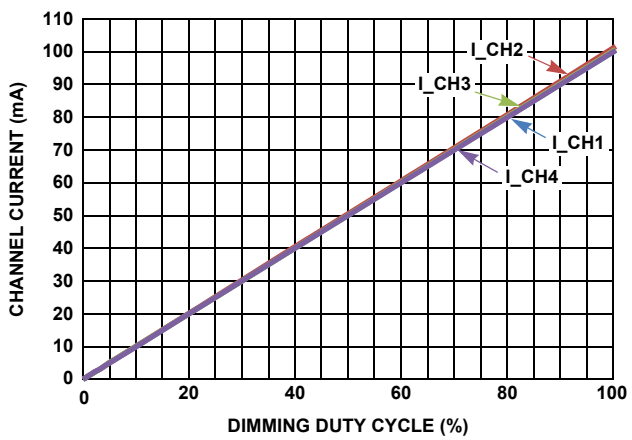


FIGURE 2. PWM DIMMING LINEARITY

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Overview

Block Diagram

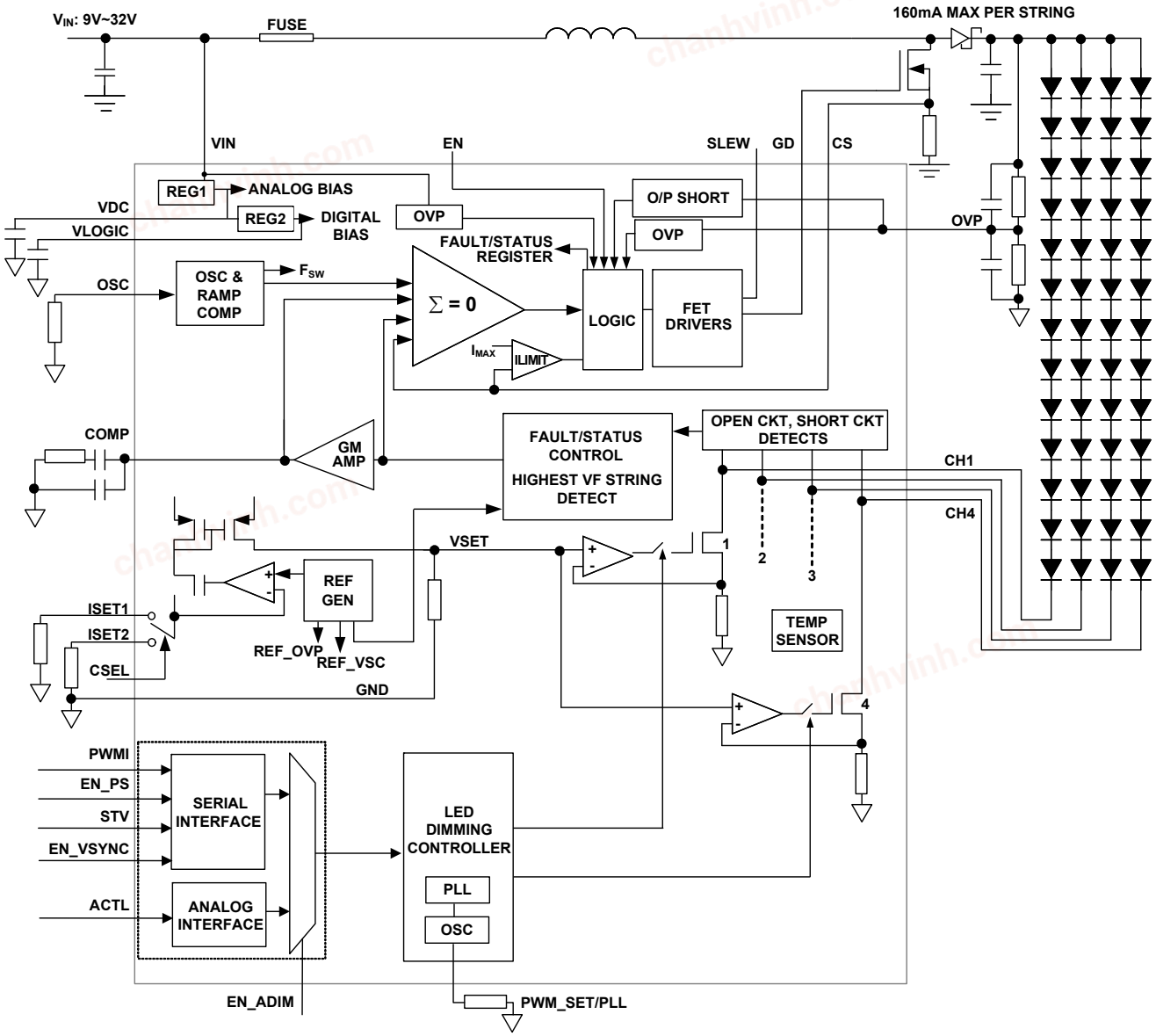


FIGURE 3. ISL97687 BLOCK DIAGRAM

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Ordering Information

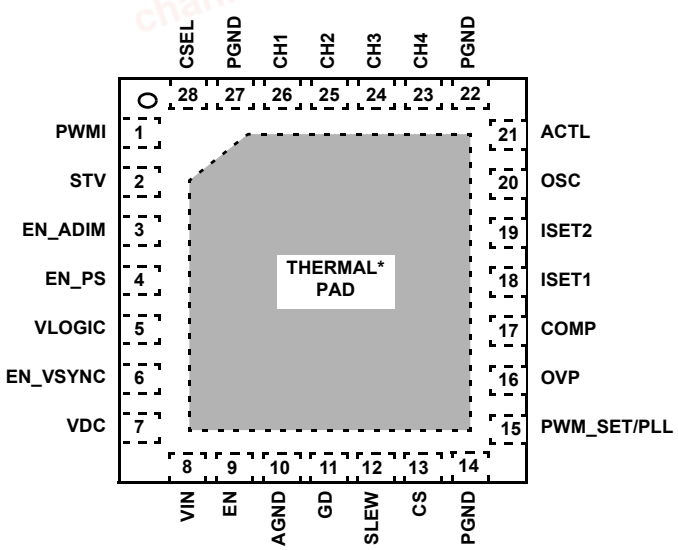
PART NUMBER (Notes 2, 3)	PART MARKING	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL97687IRTZ	ISL9768 7IRTZ	-	28 Ld 5x5 TQFN	L28.5x5B
ISL97687IRTZ-T	ISL9768 7IRTZ	6k	28 Ld 5x5 TQFN	L28.5x5B
ISL976787IBZ	ISL97687IBZ	-	28 Ld SOIC (300mil)	M28.3
ISL976787IBZ-T	ISL97687IBZ	1k	28 Ld SOIC (300mil)	M28.3
ISL97687IRTZ-LEVALZ	Evaluation Board (12 LEDs populated in each channel)			
ISL97687IRTZ-HEVALZ	Evaluation Board (22 LEDs populated in each channel)			

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL97687 device information page. For more information about MSL, see TB363.

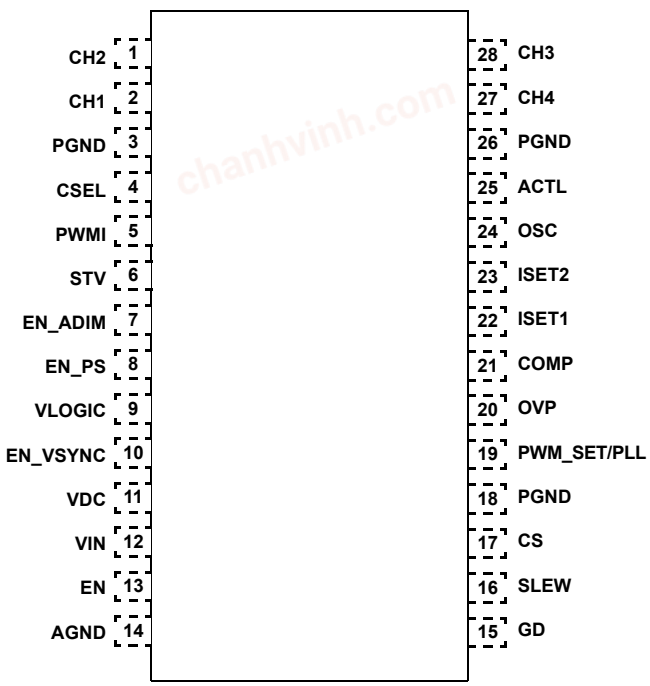
Pin Configurations

28 LD 5x5 TQFN
TOP VIEW



*EXPOSED THERMAL PAD

28 LD SOIC
TOP VIEW



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Pin Descriptions

TQFN	SOIC	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	5	PWMI	I	PWM brightness control input pin
2	6	STV	I	Start vertical frame signal; used in VSYNC mode
3	7	EN_ADIM	I	Enable analog dimming
4	8	EN_PS	I	Enable phase shift
5	9	VLOGIC	S	Internal 2.5V digital bias regulator. Needs decoupling capacitor added to ground.
6	10	EN_VSYNC	I	Frame synchronization enable. Ties high to VDC for enable V_{SYNC} function. PWM_SET/PLL also needs to be configured with an RC network. Pin can be tied to VDC or VLOGIC to enable function.
7	11	VDC	S	Internal 5V analog bias regulator. Needs decoupling capacitor added to ground.
8	12	VIN	S	Main power input. Range: 9V to 32V.
9	13	EN	I	LED driver enable. The whole chip shuts down when low.
10	14	AGND	S	Analog ground
11	15	GD	O	External boost FET gate control
12	16	SLEW	I	Boost regulation switching slew rate control
13	17	CS	I	External boost FET current sense input
14	18	PGND	S	Boost FET gate driver power ground and ground reference for the CS pin.
15	19	PWM_SET/ PLL	I	For direct PWM mode, tie this pin high to VDC. For other non-VSYNC modes, connect to a resistor to set the dimming frequency. If the VSYNC function is enabled, connect this pin to the PLL loop filter network.
16	20	OVP	I	Overvoltage protection input and output voltage feedback pin.
17	21	COMP	I	Boost compensation
18	22	ISET1	I	Resistor connection for setting LED current. 28.7kΩ = 100mA.
19	23	ISET2	I	Resistor connection for setting LED current. 28.7kΩ = 100mA.
20	24	OSC	I	Boost switching frequency adjustment.
21	25	ACTL	I	Analog dimming input (input range is 0.3V to 3V).
22	26	PGND	S	Power Ground return for LED current.
23	27	CH4	I	LED PWM driver
24	28	CH3	I	LED PWM driver
25	1	CH2	I	LED PWM driver
26	2	CH1	I	LED PWM driver
27	3	PGND	S	Power ground return for LED current.
28	4	CSEL	I	ISET resistor selection pin. CSEL = 0 : ISET 1 resistor sets LED current CSEL = 1 : ISET 2 resistor sets LED current

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Absolute Maximum Ratings (T_A = +25°C)

VIN, EN, PWMI, ACTL . . . . . -0.3V to 45V
VDC. . . . . -0.3V to 5.75V
VLOGIC . . . . . -0.3V to 2.75V
COMP, ISET1, ISET2, PWM_SET,
OSC, CS, OVP. . . . . -0.3V to min (VDC+0.3V, 5.75V)
EN_VSYNC, CSEL. . . . . -0.3V to 5.75V
STV, EN_ADIM, EN_PS . . . . . -0.3V to 5.75V
CH1 - CH4 . . . . . -0.3V to 75V
GD, SLEW. . . . . -0.3V to 18V
PGND . . . . . -0.3V to +0.3V
Above voltage ratings are all with respect to AGND pin

ESD Rating
Human Body Model (Tested per JESD22-A114F). 2kV
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (JESD22-C101E) 1kV
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld TQFN (4 layer + vias, Notes 4, 5) . . .	32	4
28 Ld SOIC (4 layer, Notes 6, 7)	54	25
Thermal Characterization (Typical, Note 8)		PSI_{JT} (°C/W)
28 Ld TQFN		1
28 Ld SOIC.		4

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C

Power Dissipation	TQFN (W)	SOIC (W)
T_A < +25°C	3.13	1.85
T_A < +70°C	1.72	1.02
T_A < +85°C	1.25	0.74
T_A < +105°C	0.63	0.37

Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. For θ_{JC}, the "case temp" location is taken at the package top center.
7. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
8. PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings.

Electrical Specifications

All specifications below are characterized at T_A = -40°C to +105°C; V_{IN} = 12V, EN = 5V. **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	CONDITION	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
GENERAL						
Backlight Supply Voltage	V_{IN}	(Note 10)	**9**		**32**	V
V_{IN} Shutdown Current	I_{VIN_STBY}	EN = 0			**5**	µA
Switching	I_{VIN_ACTIVE}	R_{FPWM} = 3.3kΩ, I_{LED} = 100mA, f_{SW} = 600kHz, C_{OUT_SW} = 1nF		10	**13**	mA
Non-Switching				4	**5.5**	mA
Undervoltage Lockout Threshold	V_{UVLO}		**2.9**		**3.3**	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}			300		mV
LINEAR REGULATOR						
5V Analog Bias Regulator	V_{DC}	V_{IN} > 6V	**4.8**	5	**5.1**	V
V_{DC} LDO Load Regulation Tolerance	V_{DC_DROP}	I_{VDC} = 30mA		71	**100**	mV
2.5V Logic Bias Regulator	V_{LOGIC}	V_{IN} > 6V	**2.3**	2.4	**2.5**	V
V_{LOGIC} LDO Load Regulation Tolerance	V_{LOGIC_DROP}	I_{VLOGIC} = 30mA		31	**100**	mV
BOOST SWITCH CONTROLLER						
Soft-Start	t_{SS}			16		ms
Boost FET Current Limit (See Equation 5)	I_{SW_LIMIT}	R_{SENSE} = 50mΩ	**3.1**	3.4	**3.8**	A
Gate Rise Time	t_R	C_{OUT_SW} = 1000pF		20		ns
Gate Falling Time	t_F	C_{OUT_SW} = 1000pF		17.6		ns
Gate Driver Output Voltage	V_{GD}	C_{OUT_SW} = 1000pF		10		V

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Electrical Specifications

All specifications below are characterized at T_A = -40°C to +105°C; V_{IN} = 12V, EN = 5V. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	CONDITION	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Boost Maximum Duty Cycle	D_{MAX}	f_{SW} = 600kHz	**92**			%
Boost Minimum Duty Cycle	D_{MIN}	f_{SW} = 1.2MHz			**26**	%
Boost Switching Frequency (See Equation 4)	f_{SW}	R_{OSC} = 250kΩ	**180**	200	**220**	kHz
		R_{OSC} = 83kΩ	**540**	600	**660**	kHz
		R_{OSC} = 42kΩ	**1.08**	1.2	**1.32**	MHz
Boost Peak Efficiency	EFF_{PEAK}			90		%
REFERENCE						
Channel-to-Channel Current Matching	I_{MATCH}	Channels are in a single IC, I_{LED}: 100mA	**-2**	±1	**2**	%
Absolute Current	I_{ACC}	$R_{ISET1/2}$ = 28.7kΩ	**-3**		**3**	%
FAULT DETECTION						
Channel Short-Circuit Threshold	V_{SC}		**7.2**	8	**8.8**	V
Over-Temperature Threshold	V_{TEMP}			150		°C
Over-Temperature Threshold Accuracy	V_{TEMP_ACC}			5		°C
Overvoltage Limit on OVP Pin	V_{OVP_OUT}		**1.18**	1.22	**1.24**	V
Overvoltage Limit on VIN Pin	V_{OVP_IN}			35		V
DIGITAL I/O LOGIC LEVEL SPECIFICATIONS						
Logic Input Low Voltage - STV, EN_PS, EN_VSYNC, EN_ADIM, PWMI, CSEL, EN	V_{IL}				**0.8**	V
Logic Input High Voltage - STV, EN_PS, EN_VSYNC, EN_ADIM, PWMI, CSEL, EN	V_{IH}		**1.5**		**5.5**	V
Frame Frequency	STV		**30**		**240**	Hz
CURRENT SOURCES						
Dominant Channel Current Source Headroom at CH Pin	$V_{HEADROOM}$	I_{LED} = 160mA, T_A = +25°C		0.75 (Note 11)		V
Dominant Channel Current Sink Headroom Range at CHx Pin	$V_{HEADROOM_RANGE}$	I_{LED} = 20mA, T_A = +25°C		90		mV
Voltage at ISET1 and 2 Pins	$V_{ISET1,2}$		**1.18**	1.21	**1.24**	V
Maximum LED Current per Channel	I_{LED_MAX}		**160**			mA
PWM GENERATOR						
Generated PWM Frequency (See Equation 3)	f_{PWM}	R_{PWM_SET} = 333kΩ	**45**	50	**55**	Hz
		R_{PWM_SET} = 3.3kΩ	**4.5**	5	**5.5**	kHz
PWM Dimming Duty Cycle Limits	Dimming Range	f_{PWM} ≤ 20kHz	**0.1**		**100**	%
PWMI Input Frequency Range	f_{PWMI}		**60**		**20k**	Hz
PWM_SET Voltage	V_{PWM_SET}	R_{PWM_SET} = 3.3kΩ	**1.18**	1.21	**1.25**	V
Analog Dimming Input	V_{ACTL}	0% Dimming	**0.28**	0.3	**0.31**	V
		100% Dimming	**2.95**	3	**3.1**	V
Minimum PWM On-Time in Direct PWM Mode	t_{PWM_MIN}			350		ns

NOTES:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. At maximum V_{IN} of 32V, minimum V_{OUT} is 35V. Minimum V_{OUT} can be lower at lower V_{IN}.
11. Varies within the range specified by $V_{HEADROOM_RANGE}$.

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Typical Performance Curves

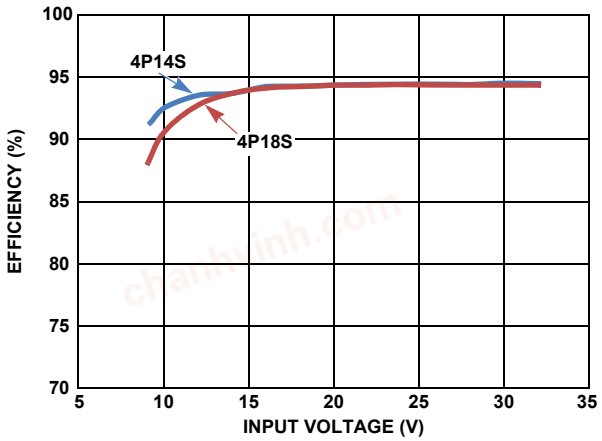


FIGURE 4. EFFICIENCY vs V_{IN} (I_{CH}: 100mA, f_{DIM}: 200Hz, V_{OUT}: 45V FOR 4P14S AND 55V FOR 4P18S)

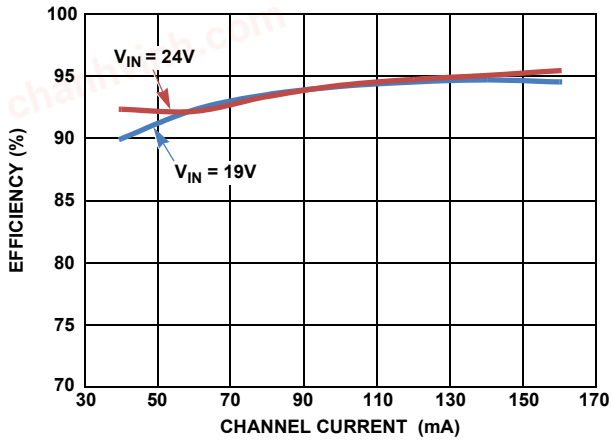


FIGURE 5. EFFICIENCY vs I_{CH} (V_{OUT}: 55V FOR 4P18S, f_{DIM}:200Hz)

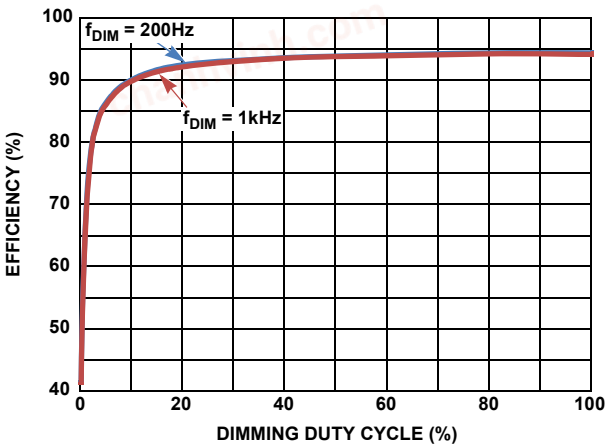


FIGURE 6. EFFICIENCY vs PWM DIMMING (V_{IN}: 24V, V_{OUT}: 55V FOR 4P18S, I_{CH}: 100mA)

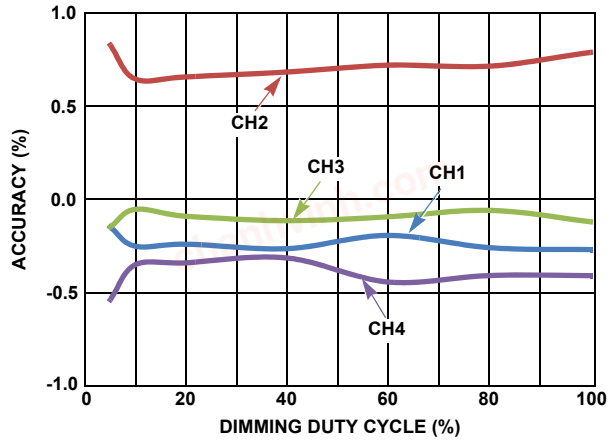


FIGURE 7. ACCURACY vs PWM DIMMING (V_{IN}: 24V, V_{OUT}: 55V FOR 4P18S, I_{CH}: 100mA)

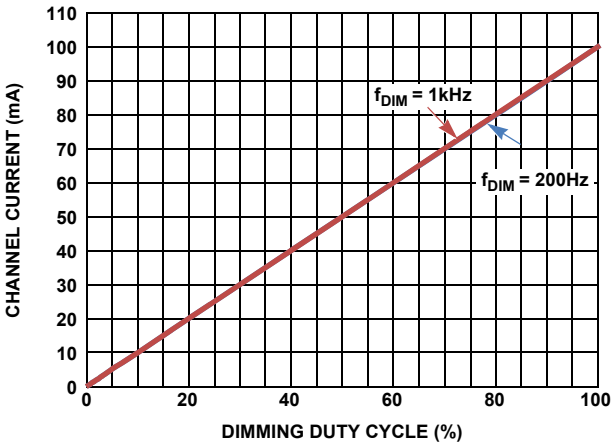


FIGURE 8. PWM DIMMING LINEARITY (V_{IN}: 24V, V_{OUT}: 55V FOR 4P18S)

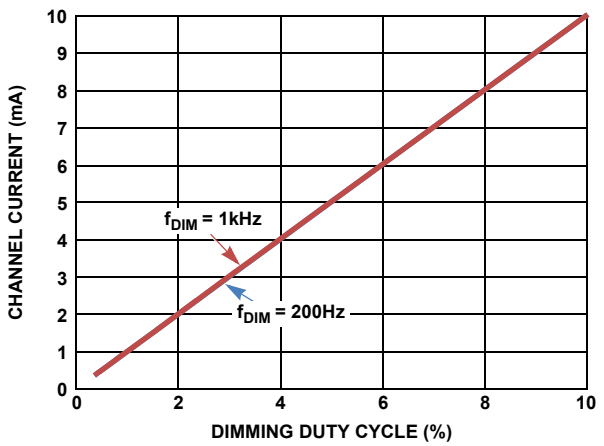


FIGURE 9. PWM DIMMING LINEARITY (V_{IN}: 24V, V_{OUT}: 55V FOR 4P18S)

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Typical Performance Curves (Continued)

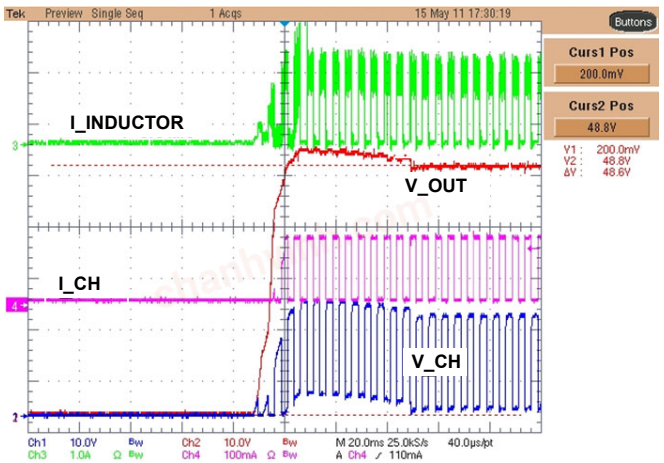


FIGURE 10. START-UP (DIRECT PWM DIMMING, V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

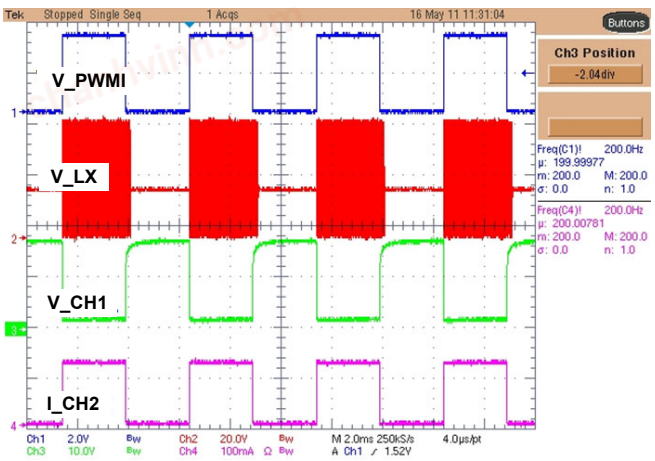


FIGURE 11. DIRECT PWM DIMMING (V_{IN}: 19V, LEDs: 4P18S, f_{DIM}: 200Hz)

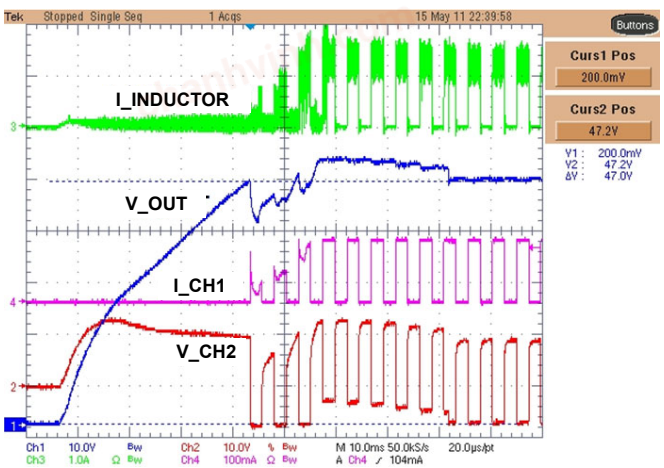


FIGURE 12. START-UP WITHOUT PHASE SHIFT (V_{IN} : 19V, I_{CH}: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

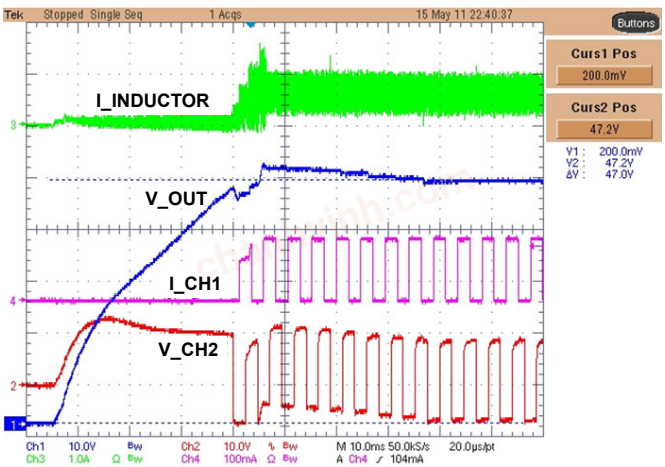


FIGURE 13. START-UP WITH PHASE SHIFT (V_{IN} : 19V, I_{CH}: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

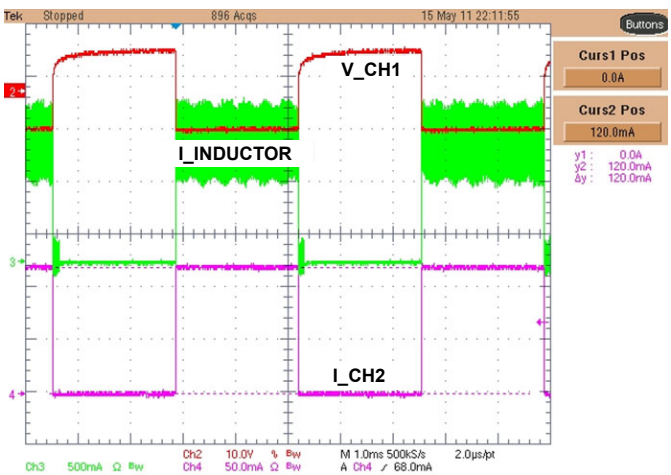


FIGURE 14. PWM DIMMING WITHOUT PHASE SHIFT (V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

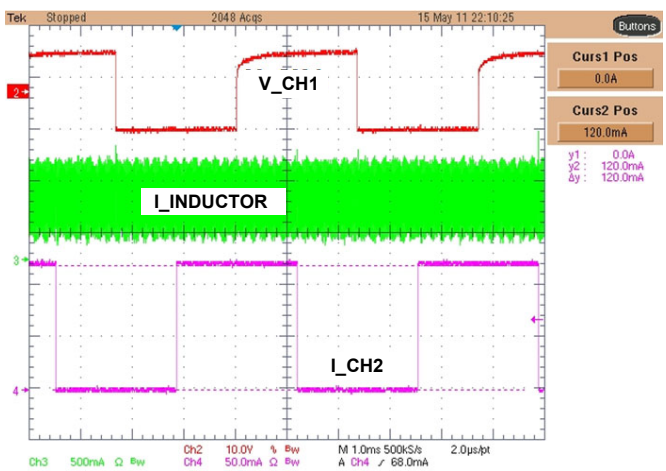


FIGURE 15. PWM DIMMING WITH PHASE SHIFT (V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

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Typical Performance Curves (Continued)

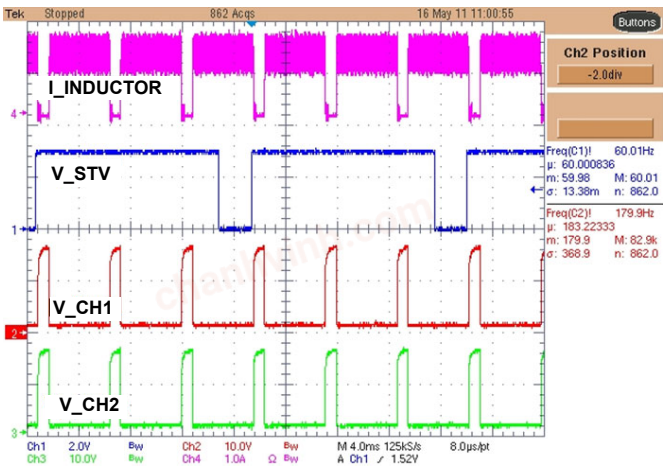


FIGURE 16. V_{SYNC} ENABLED DIMMING WITHOUT PHASE SHIFT (V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, 180Hz OUTPUT PHASE AND FREQUENCY LOCKED TO 60Hz STV)

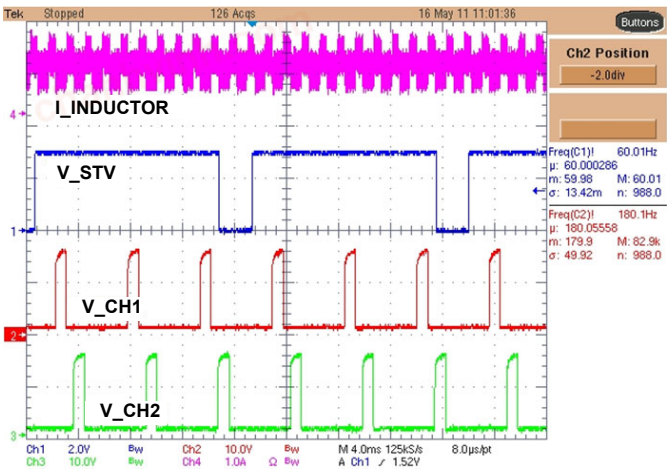


FIGURE 17. V_{SYNC} ENABLED WITH PHASE SHIFT (V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, 180Hz OUTPUT PHASE AND FREQUENCY LOCKED TO 60Hz STV)

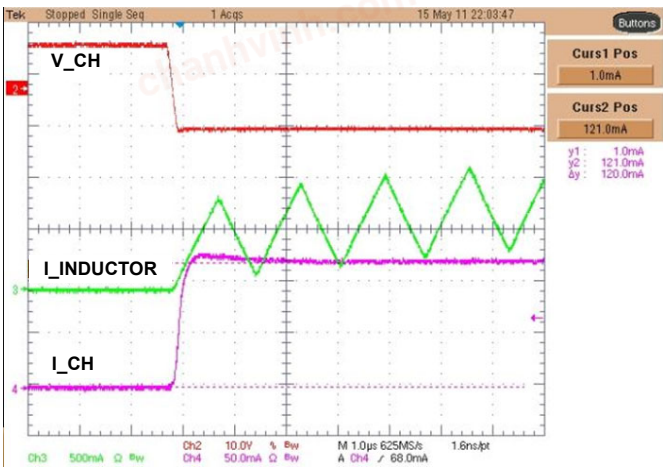


FIGURE 18. PWM SWITCHING AND TRANSIENT RESPONSE OF INDUCTOR CURRENT

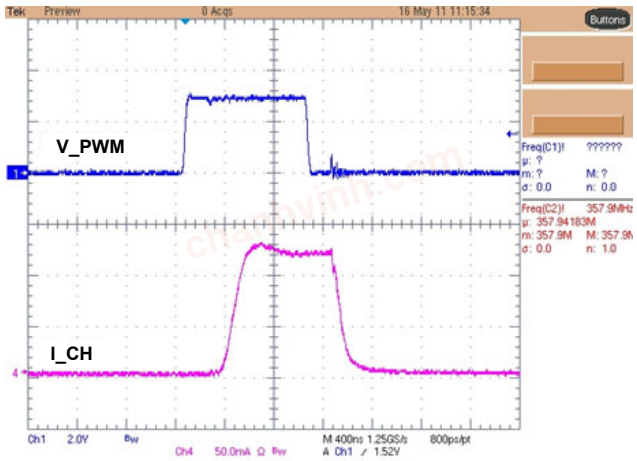


FIGURE 19. MINIMUM DIMMING DUTY CYCLE (0.05%, f_{DIM}: 500Hz, I_{CH} = 120mA, DIRECT PWM MODE)

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Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED string with the highest forward voltage drop to run at the programmed current. The ISL97687 employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. The number of LEDs that can be driven by ISL97687 depends on the type of LED chosen in the application. The ISL97687 is capable of boosting up to greater than 70V and driving 4 Channels of LEDs at a maximum of 160mA per channel.

OVP and VOUT

The Overvoltage Protection (OVP) pin has a function of setting the overvoltage trip level and limiting the V_{OUT} regulation range.

The ISL97687 OVP threshold is set by R_{UPPER} and R_{LOWER} as shown in Equation 1:

$$V_{OUT_OVP} = \frac{1.21(R_{UPPER} + R_{LOWER})}{R_{LOWER}} \quad \text{(EQ. 1)}$$

and V_{OUT} can only regulate between 30% and 100% of the V_{OUT_OVP} such that:

Allowable V_{OUT} = 30% to 100% of V_{OUT_OVP}

For example, a 1MΩ R_{UPPER} and 19kΩ R_{LOWER} sets OVP to 65.9V. The boost can regulate down to 30% of OVP, so it can go as low as 19.5V. If V_{OUT} needs to be lower than this, the OVP level must be reduced. Otherwise, V_{OUT} regulates to 19.5V, and the ISL97687 may overheat. However, it's recommended that the OVP be set to no more than 20% above the nominal operating voltage. This prevents the need for output capacitor voltage ratings and the inductor current rating to be set significantly higher than needed under normal conditions, allowing a smaller and cheaper solution, and keeping the maximum voltages and currents that can be seen in the system during fault conditions at less extreme levels.

Place parallel capacitors across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high value resistors. The ratio of the OVP capacitors should be the inverse of the OVP resistors. For example, if R_{UPPER}/R_{LOWER} = 33/1, C_{UPPER}/C_{LOWER} = 1/33 with C_{UPPER} = 100pF and C_{LOWER} = 3.3nF. These components are not always needed, but it is highly recommended to include placeholders.

Current Matching and Current Accuracy

The LED current in each channel is regulated using an active current source circuit, as shown in Figure 20. The peak LED current is set by translating the R_{ISET} current to the output with a scaling factor of $2919/R_{ISET}$. The drain terminals of the current source MOSFETs are designed to operate within a range of about 750mV to optimize power loss versus accuracy requirements. The sources of channel-to-channel current matching error come from the op amp offsets, reference voltage, and current source sense resistors. These parameters are optimized for current matching and absolute current accuracy. However, the absolute accuracy is additionally determined by the external R_{ISET}. A 0.1% tolerance resistor is therefore recommended.

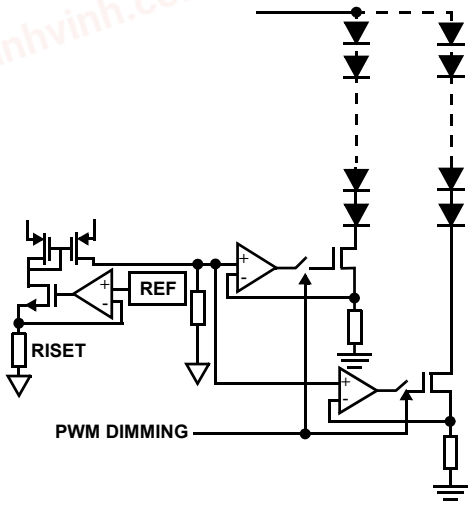


FIGURE 20. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97687 features a proprietary dynamic headroom control circuit that detects the highest forward voltage string, or effectively the lowest voltage from any of the CH pins. The system regulates the output voltage to the correct level to allow the channel with the lowest voltage to have just sufficient headroom to correctly regulate the LED current. Because all LED strings are connected to the same output voltage, the other CH pins have a higher voltage, but the regulated current source circuit on each channel ensures that each channel has the correct current level. The output voltage regulation is dynamic, and is updated as needed, to allow for temperature and aging effects in the LEDs.

Dimming Controls

The ISL97687 provides two basic ways to control the LED current, and therefore, the brightness. These are described in detail in subsequent sub-sections, but can be broadly divided into the following two types of dimming:

- LED DC current adjustment
- PWM chopping of the LED current defined by LED DC current adjustment

LED DC Current Setting

Set the initial brightness by choosing an appropriate value for the resistor on the ISET1/2 pins. This resistor must connect to AGND, and should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{2919}{R_{ISET}} \quad \text{(EQ. 2)}$$

The ISL97687 includes two built-in levels of current, individually set by the resistors on ISET1 and ISET2, according to Equation 2 that can be switched between by using the CSEL pin.

- CSEL = 0: The current setting is based on ISET1
- CSEL = 1: The current setting is based on ISET2

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This is typically used in 3D systems to provide a higher current level in 3D modes, but is not restricted to this application. CSEL can be switched in operation and updates immediately in direct PWM mode, and at the start of the next PWM dimming cycle in other modes. The different current levels need to be close enough so that the change in output voltages (V_{OUT}) are within 2.3% of VOUT_OVP.

LED DC DIMMING

It is possible to control the LED current by applying a DC voltage V_{DIM} to the ISET1/2 pin via a resistor as in Figure 21.

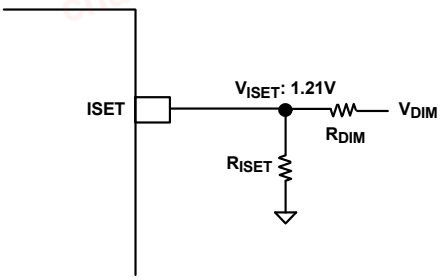


FIGURE 21. LED CURRENT CONTROL WITH V_{DIM}

If the V_{DIM} is above V_{ISET} 1.21V, the brightness reduces, and vice versa. In this configuration, it is important that the control voltage be set to the maximum brightness (minimum voltage) level when the ISL97687 is enabled, even if the LEDs are not lit at this point. This is necessary to allow the chip to calibrate to the maximum current level that needs to be supported. Otherwise, on-chip power dissipation is higher at current levels above the start-up level. Dimming with this technique should be limited to a minimum of 10~20% brightness, as LED current accuracy is increasingly degraded at lower levels.

When dimming with this technique, if the brightness level needs to be changed significantly, V_{DIM} must be adjusted with multiple small dimming steps. Dimming steps should be small enough to ensure the maximum step change in the output voltage (V_{OUT}) does not exceed 2.3% of V_{OUT_OVP}, where V_{OUT_OVP} can be calculated using Equation 1. The output voltage needs to stabilize before doing another change.

LED PWM CONTROL

The ISL97687 provides many different PWM dimming methods. Each of these results in PWM chopping of the current in the LEDs of all four channels, to provide an average LED current and control the brightness. During the on-periods, the LED peak current is defined by the value of the resistor on ISET1 or ISET2, as described in Equation 2.

Dimming can either be “direct PWM” mode, where both the frequency and duty cycle of the LEDs match that of the incoming PWMI signal, or the duty cycle and frequency sources must be selected from the following.

SUPPORTED LED DUTY CYCLE SOURCES

- Decoded PWMI pin duty cycle (PWM input mode)
- Decoded ACTL pin voltage (Analog input mode)
- Analog*PWM input mode (Both PWM and Analog inputs are used)

SUPPORTED LED FREQUENCY SOURCES

- Free running internal oscillator (Internal PWM frequency mode)
- Frequency can be phase and frequency locked to frame rate (V_{SYNC} mode)

Additionally, phase shift mode can be enabled in all configurations except direct PWM, allowing the LED strings to turn on in sequence.

LED PWM DIMMING IN DIRECT PWM MODE

When the PWM_SET/PLL pin is tied to VDC, the PWMI input signal directly controls the LEDs. The dimming frequency and phase of the LEDs are the same as that of PWMI. This mode can get very high effective PWM resolution, as the resolution is effectively determined by the PWMI signal source.

LED PWM DIMMING – DUTY CYCLE CONTROL

In non-direct PWM mode, the ISL97687 can decode the incoming PWMI duty cycle information at 10-bit resolution and the ACTL voltage level at 8-bit resolution and apply these values to the LEDs as a PWM output at a new frequency.

For applications where DC-PWM dimming is required, the analog dimming mode must be enabled (EN_ADIM = high). The analog control input pin (ACTL) must then be fed with a voltage of 0.3V to 3.0V. This is decoded as an 8-bit duty cycle of 0% to 100% respectively. This interface supports backward compatibility with CCFL backlight driving systems, but can also be used in other applications, such as analog ALS interfaces. External circuitry can shift most analog input ranges to the required level. Figure 22 is an example that maps a 0V to 3.5V input to give a 10-100% output range, but this can be tailored to other requirements. The PWM dimming frequency, set by the PWM_SET pin, should be at least 1kHz when EN_ADIM is high.

In Analog mode, the decoded 10-bit PWM duty cycle information from the PWMI pin is also used, multiplied by the 8-bit level decoded from the ACTL pin. For example, if ACTL = 2.3V (74%) and PWMI = 50%, LED dimming is 74% x 50% = 37%. For analog dimming applications where this multiplication is not needed, PWMI should be tied high, giving the ACTL pin full control over the duty cycle range. For applications where analog dimming is not needed, EN_ADIM should be low and PWMI should be driven with the required duty cycle.

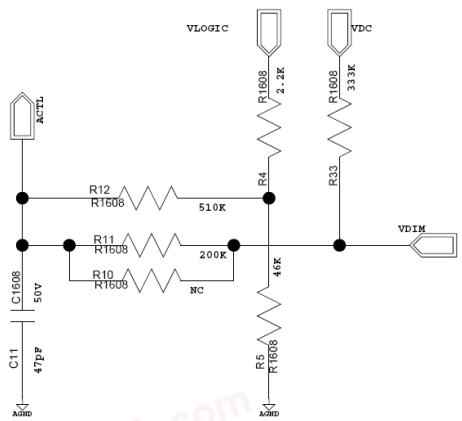


FIGURE 22. EXAMPLE OF ACTL INPUT ADJUSTMENT

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PWM Dimming Frequency Adjustment

The dimming frequencies of serial interface and ACTL modes are set by an external resistor at the PWM_SET pin, as shown in Equation 3:

$$f_{PWM} = \frac{(1.665)\times 10^{7}}{R_{PWMSET}} \quad \text{(EQ. 3)}$$

where f_{PWM} is the desirable PWM dimming frequency and R_{PWMSET} is the setting resistor.

V_{SYNC} FUNCTION

The V_{SYNC} function provides accurate LED dimming frequencies and makes sure that the video data is properly aligned with the frame rate. A Phase Locked Loop (PLL) locks the frequency to a multiple of the frame rate. Additionally, the phase of the PWM output is aligned with the frame rate to provide very predictable video performance. In V_{SYNC} mode, the PWM_SET/PLL pin is used as the PLL loop compensation pin and needs a loop filter connected between it and ground.

Frame rates between 30Hz and 300Hz are supported, and an automatic frequency detection circuit provides the same output frequency at 30, 60, 120, 180, 240, and 300Hz.

Additionally, the PWM dimming frequency can be pre-selected to any of the following values shown in Table 1 (**Note:** For the 60Hz range, the frequencies are scaled by a factor of framerate/60Hz and for the 120Hz range are be scaled by a factor of framerate/120Hz).

TABLE 1. PRE-SELECTED PWM DIMMING FREQUENCY AT V_{SYNC} MODE

DIMMING FREQUENCY			
(Hz)	(kHz)	(kHz)	(kHz)
180	1.26	5.70	13.38
240	1.38	6.18	13.86
300	1.50	6.66	14.34
360	1.62	7.14	14.82
420	1.74	7.62	15.30
480	1.86	8.10	15.78
540	1.98	8.58	16.26
600	2.10	9.06	16.74
660	2.34	9.54	17.22
720	2.58	10.02	17.70
780	2.88	10.50	18.18
840	3.36	10.98	18.66
900	3.78	11.46	19.14
960	4.20	11.94	19.62
1.02k	4.74	12.42	20.10
1.14k	5.22	12.90	20.58

Phase Shift Control

The ISL97687 is capable of delaying the phase of each current source within the PWM cycle. Conventional LED drivers present the worst load transients to the boost converter, by turning on all channels simultaneously, as shown in Figure 23. The ISL97687 can be configured to phase shift each channel by 90°, individually turning them on and off at different points during the PWM dimming period, as shown in Figure 24. At duty cycles below 100%, the load presented to the boost peaks at a lower level and/or spends less time at the peak, when compared to that of a conventional LED driver, as shown in Figure 23. Additionally, load steps are limited to the LED current of one CH pin, one quarter of that of a standard driver. This can help reduce transients on V_{OUT} and also reduces audio noise by limiting the magnitude of changes in magnetic field required in the inductor needed to track the load. Audio noise is also generally improved for PWM frequencies in the audio band, as the effective frequency of the boost load is multiplied by a factor of 4, meaning that, for example, a 5kHz LED frequency offers an effective boost load frequency of 20kHz.

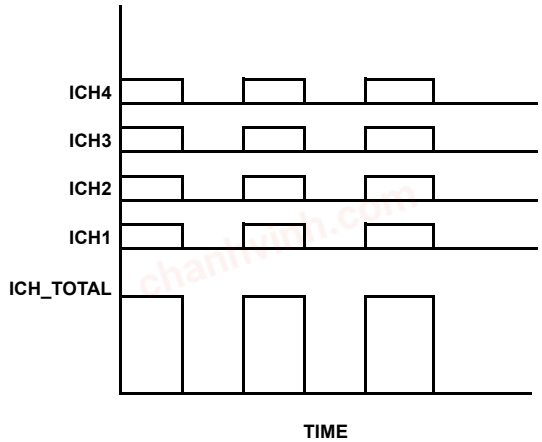


FIGURE 23. NON PHASE SHIFT PWM DIMMING AT 50% DUTY CYCLE

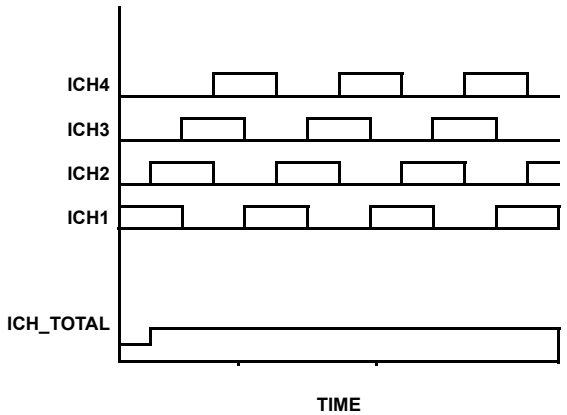


FIGURE 24. PHASE SHIFT PWM DIMMING AT 50% DUTY CYCLE

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V_{OUT} Control when LEDs are Off

When the backlight is enabled but all LEDs are off (such as during the PWM off times), the switching regulator of a typical LED driver stops switching, which can allow the output to begin to discharge.

This is not a problem when the LED off times are short and the duty cycle is running at a high duty cycle, or the output capacitance is large. However, it presents two problems. First, for low duty cycles at low frequencies, V_{OUT} can droop between on-times, resulting in under-regulation of the current when the LEDs are next switched on. Second, at high PWM frequencies or very low duty cycles, LED on-times can be shorter than the minimum number of boost cycles needed to ramp up the inductor current to the required level to support the load. For example, a 1% on-time while running at 20kHz PWM dimming frequency is only 500ns. If the boost switching frequency is set at 500kHz, this only represents a quarter of a switching cycle per LED on-time, which may not be sufficient to ramp the inductor current to the required level.

The ISL97687 incorporates an additional PFM switching mechanism that allows the boost stage to continue to switch at low current levels to replace the energy lost from the output capacitor due to the OVP stack resistance and capacitor self discharge. For very short pulses, this also means that the charge delivered to the LEDs in the on-times is provided entirely by the output capacitor, kept at the correct voltage by the PFM mode in the off-times. This allows the output to always remain very close to the required level, so that when the LEDs are re-enabled, the boost output is already at the correct level. This dramatically improves LED PWM performance, providing industry leading linearity down to sub 1% levels, and reduces the overshoot in the boost inductor current, caused by transient switching when the LEDs are switched on, to a minimum level.

The system continues to maintain V_{OUT} at the target level for 120ms after the last time the LEDs were on. If all LEDs are off for a longer period than this, the converter stops switching and goes into a sleep mode, allowing V_{OUT} to decay to save power during long backlight-off periods.

Switching Frequency

The boost switching frequency can be adjusted by the resistor on the OSC pin, which must be connected to AGND, and follows Equation 4:

$$f_{SW} = \frac{(5 \times 10^{10})}{R_{OSC}} \quad \text{(EQ. 4)}$$

where f_{SW} is the desirable boost switching frequency and R_{OSC} is the setting resistor.

5V and 2.4V Low Dropout Regulators

A 5V LDO regulator provides the low voltage supply needed to drive internal circuits. The output of this LDO is the VDC pin. A decoupling capacitor of 1µF or more is required between this pin and AGND for correct operation. Similarly, a 2.4V LDO regulator is present at the VLOGIC pin, and also requires a 1µF decoupling capacitor. Both pins can be used as a coarse voltage reference, or as a supply for other circuits, but can only support a load of up to ~10mA and should not be used to power noisy circuits that can feed significant noise onto their supply.

Soft-Start and Boost Current Limit

The boost current limit should be set by using a resistor from CS to PGND. The typical current limit can be calculated as:

$$I_{LIMIT} = \frac{0.17}{R_{CS}} \quad \text{(EQ. 5)}$$

The CS resistor should be chosen based on the maximum load that needs to be driven. Typically, a limit of 30~40% more than is required under DC conditions is sufficient to allow for necessary overshoots during load transients. Values of 20~100mΩ are supported.

It is important that PGND pin 14 (QFN)/18 (SOIC) is connected directly to the base of the sense resistor, with no other connection to the ground system, except via this path. This is because this pin is used as a ground reference for the CS pin. Connecting it here gives the maximum noise immunity and the best stability characteristics.

The ISL97687 uses a digital current limit based soft start. The initial limit level is set to one ninth of the full current limit, with eight subsequent steps increasing this by a ninth of the final value every 2ms until it reaches the full limit. In the event that no LEDs have been conducting during the interval since the last step (for example if the LEDs are running at low duty cycle at low PWM frequency), the step is delayed until the LEDs are conducting again.

If the LEDs are off for more than 120ms (making the converter go into sleep mode), soft-start is restarted when the LEDs are re-enabled.

Fault Protection and Monitoring

The ISL97687 features extensive protection functions to cover all perceivable failure conditions. The failure mode of an LED can be either open or short-circuit. The behavior of an open circuit LED can additionally take the form of either infinite or very high resistance or, for some LEDs, a zener diode, which is integrated into the device, in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes) an open circuit LED failure only results in the loss of one LED channel, without affecting other channels. Similarly, a short-circuit condition on a channel that results in that channel being turned off does not affect other channels, unless a similar fault is occurring.

Due to the lag in boost response to any load change at its output, certain transient events (such as significant step changes in LED duty cycle, or a change in LED current caused by CSEL switching) can transiently look like LED fault modes. The ISL97687 uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED strings to fault out. See Figure 26 and Table 2 for more details.

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Short-Circuit Protection (SCP)

The short-circuit detection circuit monitors the voltage on each channel and disables faulty channels that are detected to be more than the short-circuit threshold, 8V above the lowest CH pin, following a timeout period.

Open Circuit Protection (OCP)

When any of the LEDs become open circuit during the operation, that channel is disabled after a timeout period, and the part continues to drive the other channels. The ISL97687 monitors the current in each channel such that any string which reaches the intended output current is considered “good”. Should the current subsequently fall below the target, the channel is considered an “open circuit”. Furthermore, should the boost output of the ISL97687 reach the OVP limit, all channels which are not “good” are timed out.

Unused CH pins should be grounded, which disables them from start-up. This prevents V_{OUT} having to ramp to OVP at start-up, to determine that they are open.

Undervoltage Lockout

If the input voltage falls below the UVLO level of 2.8V, the device stops switching and resets. Operation restarts, with all digital settings returning to their default states, when the input voltage is back in the normal operating range.

Over-Temperature Protection (OTP)

The OTP threshold is set to +150°C. When this is reached, the boost stops switching and the output current sources are switched off and stay off until power or EN is cycled. For the extensive fault protection conditions, see Figure 26 and Table 2.

VIN OVP

If V_{IN} exceeds 35V, the part shuts down until power or EN is cycled. At this point, all digital settings are reset to their default states.

Shutdown

When the EN pin is low the entire chip is shut down to give close to zero shutdown current. The digital interfaces are not active during this time. The EN can be high before VIN.

COMPENSATION

The ISL97687 boost regulator uses a current mode control architecture, with an external compensation network connected to the COMP pin. The component values shown in Figure 25 should be used. The network comprises a 47pF capacitor from COMP to AGND, in parallel with a series RC of 25kΩ and 2.2nF, also from COMP to AGND.

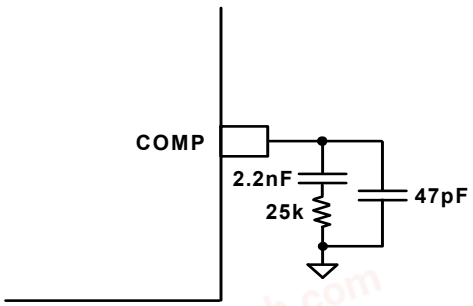


FIGURE 25. COMPENSATION NETWORK

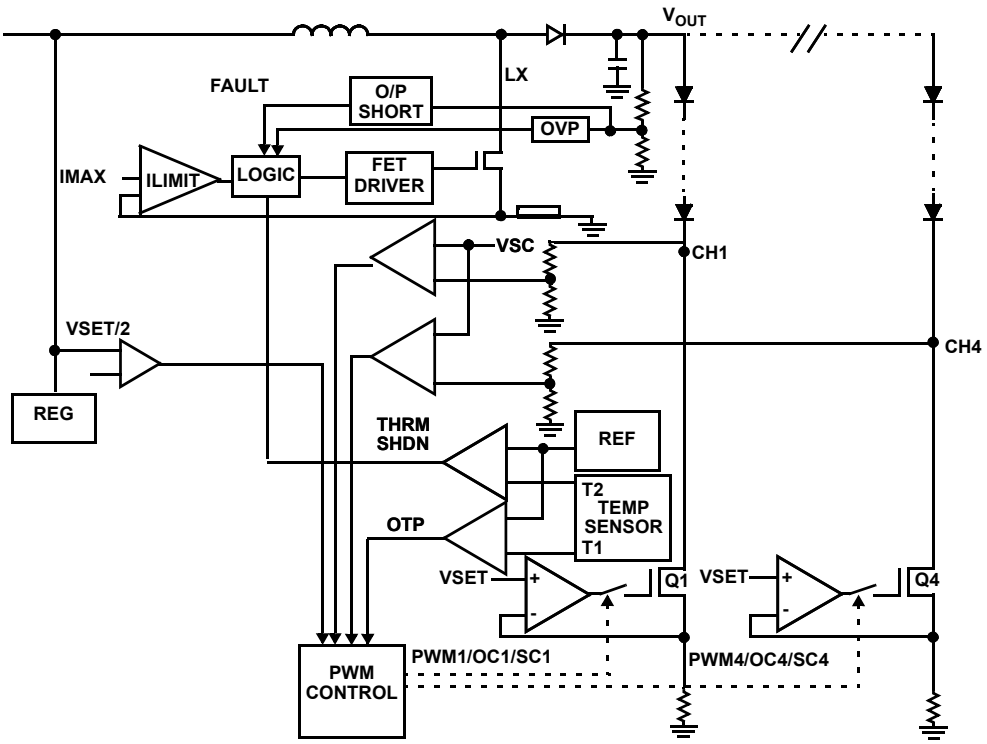


FIGURE 26. SIMPLIFIED FAULT PROTECTIONS

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TABLE 2. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
1	CH1 Short-Circuit	Over-Temperature Protection limit (OTP) not triggered and VCH1 < VSC	CH1 ON and burns power	CH2 through CH4 Normal	Highest VF of CH2 through CH4
2	CH1 Short-Circuit	OTP not triggered but VCH1 > VSC	CH1 disabled after 6 PWM cycles time-out. (**Note:** Time-out can be longer than 6 PWM cycles in direct PWM mode)	If 3 channels are already shut down, all channels are shut down. Otherwise CH2 through CH4 remain as normal	Highest VF of CH2 through CH4
3	CH1 Open Circuit with infinite resistance	OTP not triggered and VCH1 < VSC	V_{OUT} ramps to OVP. CH1 times out after 6 PWM cycles and switch off. V_{OUT} drops to normal level.	CH2 through CH4 Normal	Highest VF of CH2 through CH4
4	CH1 Open Circuit with infinite resistance during operation	OTP triggered and VCH1 < VSC	All IC shut down		V_{OUT} disabled
5	CH1 LED Open Circuit but has paralleled Zener	OTP not triggered and VCH1 < VSC	CH1 remains ON and has highest VF, thus V_{OUT} increases.	CH2 through CH4 ON, Q2 through Q4 burn power. CH2-4 fault out if they reach VSC as a result of V_{OUT} increase due to increase VF in CH1	VF of CH1
6	CH1 LED Open Circuit but has paralleled Zener	OTP not triggered but VCHx > VSC	CH1 remains ON and has highest VF, thus V_{OUT} increases.	V_{OUT} increases then CH-X switches OFF. This is an unwanted shut off and can be prevented by setting OVP at an appropriate level.	VF of CH1
7	Channel-to-Channel ΔVF too high	OTP triggered but VCHx < VSC	All channels switched off		V_{OUT} disabled
8	Output LED string voltage too high	V_{OUT} reaches OVP and not sufficient to regulate LED current	Driven with normal current. Any channel that is below the target current times out after 6 PWM cycles. (**Note:** Time-out can be longer than 6 PWM cycles in case direct PWM mode)		V_{OUT} disabled
9	V_{OUT}/SW shorted to GND		SW does not switch if started up in this condition. V_{OUT} shorted to ground during operation also causes the converter to shut down		

Component Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the power MOSFET switching on-time is equal to the change of inductor current during the power MOSFET switching off-time under steady state operation. The voltage across an inductor is shown in Equation 6:

$$V_L = L \times \Delta I_L / \Delta t \quad \text{(EQ. 6)}$$

and ΔI_L at t_{ON} = ΔI_L at t_{OFF}, therefore:

$$(V_I - 0)/L \times D \times t_{Sw} = (V_O - V_D - V_I)/L \times (1 - D) \times t_{Sw} \quad \text{(EQ. 7)}$$

where D is the switching duty cycle defined by the turn-on time over the switching period. V_D is a Schottky diode forward voltage, which can be neglected for approximation. t_{sw} is the switching period where $t_{sw} = 1/f_{sw}$, and the f_{sw} is the switching frequency of the boost converter.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle respectively as Equations 8 and 9:

$$V_O/V_I = 1/(1 - D) \quad \text{(EQ. 8)}$$

$$D = (V_O - V_I)/V_O \quad \text{(EQ. 9)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, thereby improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

During the normal continuous conduction mode of the boost converter, its input current flows continuously into the inductor; AC ripple component is only proportional to the rate of the inductor charging, thus, smaller value input capacitors can be used. It is recommended that an input capacitor of at least 10µF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

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Inductor

The selection of the inductor should be based on its maximum current (I_{SAT}) characteristics, power dissipation, EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including the inductor ripple current, current limit, efficiency, transient performance, and stability.

The inductor's maximum current capability must be large enough to handle the peak current at the worst case condition. If an inductor core is chosen with a lower current rating, saturation in the core causes the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency, and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the off period, as expressed in Equation 10:

$$IL_{peak} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_{SW})] \quad \text{(EQ. 10)}$$

The choice of 85% is just an average term for the efficiency approximation. The first term is the average current, which is inversely proportional to the input voltage. The second term is the inductor current change, which is inversely proportional to L and f_{SW}. As a result, for a given switching frequency, minimum input voltage must be used to calculate the input/inductor current as shown in Equation 10. For a given inductor size, the larger the inductance value, the higher the series resistance because of the extra number of turns required, thus, higher conductive losses. The ISL97687 current limit should be less than the inductor saturation current.

Output Capacitors

The output capacitor acts to smooth the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of the discharge of the output capacitor during the FET turn-on period and the voltage drop due to load current flowing through the ESR of the output capacitor. The ripple voltage is shown in Equation 11:

$$\Delta V_{CO} = (I_O/C_O \times D/f_{SW}) + (I_O \times ESR) \quad \text{(EQ. 11)}$$

where I_O represents the output current, C_O is the output capacitance, D is the duty ratio as described in Equation 9. ESR is the equivalent series resistance of the output capacitance and f_{sw} is the switching frequency of the converter. Equation 11 shows the importance of using a low ESR output capacitor for minimizing output ripple.

As shown in Equation 11, the output ripple voltage, ΔV_{Co}, can be reduced by increasing the output capacitance, C_O or the switching frequency, f_{SW}, or using output capacitors with small ESR. In general, ceramic capacitors are the best choice for output capacitors in small to medium sized LCD backlight applications due to their cost, form factor, and low ESR.

The choice of X7R over Y5V ceramic capacitors is highly recommended because the X7R type capacitor is less sensitive to capacitance change overvoltage. Y5V's absolute capacitance can be reduced to 10%~20% of its rated capacitance at the maximum voltage. Because of this, Y5V type ceramic capacitors should be avoided.

A larger output capacitor also eases the driver response during PWM dimming off period due to the longer sample and hold effect of the output drooping. The driver does not need to boost as much on the next on period, which minimizes transient current. The output capacitor also plays an important role for system compensation.

Channel Capacitor

It is recommended to use at least 1nF capacitors from CH pins to V_{OUT}. Larger capacitors reduce LED current ripple at boost frequency, but degrades transient performance at high PWM frequencies. The best value is dependant on PCB layout. Up to 4.7nF is sufficient for most configurations.

Schottky Diode

A high speed rectifier diode is necessary to prevent excessive voltage overshoot, especially in the boost configuration. Low forward voltage and reverse leakage current minimizes losses, making Schottky diodes the preferred choice. Although the Schottky diode turns on only during the boost switch off period, it carries the same peak current as the inductor, therefore, a suitable current rated Schottky diode must be used.

High Current Applications

Each channel of the ISL97687 can support up to 160mA. For applications that need higher current, multiple channels can be grouped to achieve the desirable current. For example, in Figure 27, the cathodes of the last LEDs can be connected to CH1/CH2 and CH3/CH4, this configuration can be treated as a single string with up to 350mA current driving capability.

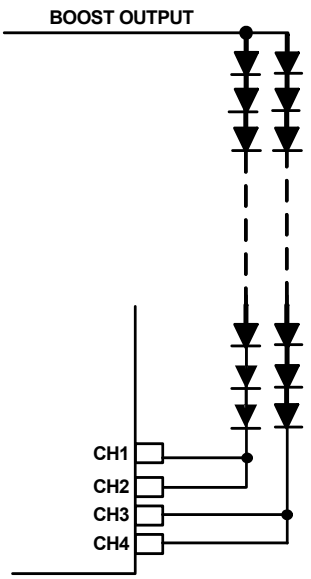


FIGURE 27. GROUPING MULTIPLE CHANNELS FOR HIGH CURRENT APPLICATIONS

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PCB Layout Considerations

Two Layers PCB Layout with TQFN Package

Great care is needed in designing a PC board for stable ISL97687 operation. As shown in the typical application diagram (Figure 1 on page 1), the separation of PGND and AGND of each ISL97687 is essential, keeping the AGND referenced only local to the chip. This minimizes switching noise injection to the feedback sensing and analog areas, and eliminates DC errors form high current flow in resistive PC board traces. PGND and AGND should be on the top and bottom layers respectively in the two layer PCB. Form a star ground connection by connecting the LED ground return and AGND pins to the thermal pad with 9-12 vias. The ground connection should be into this ground net, on the top plane. The bottom plane then forms a quiet analog ground area, that both shields components on the top plane, and provides easy access to all sensitive components. For example, the ground side of the ISET1/2 resistors can be dropped to the bottom plane, providing a very low impedance path back to the AGND pin, which does not have any circulating high currents to interfere with it. The bottom plane can also be used as a thermal ground, so the AGND area should be sized sufficiently large to dissipate the required power. For multi-layer boards, the AGND plane can be the second layer. This provides easy access to the AGND net, but allows a larger thermal ground and main ground supply to come up through the thermal vias from a lower plane.

This type of layout is particularly important for this type of product, as the ISL97687 has a high power boost, resulting in high current flow in the main loop's traces. Careful attention should be focussed on the below layout details:

1. Place boost input capacitors, output capacitors, inductor, and Schottky diode together in a nice tight layout. Keeping the grounds of the input, output, ISL97687 and the current sense resistor connected with a low impedance and wide metal is very important to keep these nodes closely coupled.
2. Figure 29 on page 19 shows important traces of current sensor (RS) and OVP resistors (RU, RL). The current sensor track line should be short, so that it remains as close as possible to the Current Sense (CS) pin. Additionally, the CS pin is referenced from the adjacent PGND pin. It is extremely important that this PGND pin is placed with a good reference to the bottom of the sense resistor. In Figure 29 you can see that this ground pin is not connected to the thermal pad, but instead used to effectively sense the voltage at the bottom of the current sense resistor. However, this pin also takes the gate driver current, so it must still have a wide connection and a good connection back from the sense resistor to the star ground. Also, place the RC filter on CS referenced to this PGND pin and close to the chip.
3. If possible, try to maintain central ground node on the board and use the input capacitors to avoid excessive input ripple for high output current supplies. Place the filtering capacitors close by the VIN pin.
4. For optimum load regulation and true V_{OUT} sensing, connect the OVP resistors independently to the top of the output capacitors and away from the higher dv/dt traces. The OVP connection then needs to be as short as possible to the pin. The AGND connection of the lower OVP components is critical for good regulation. At 70V output, a 100mV change at V_{OUT} translates to a 1.7mV change at OVP, so a small ground error due to high current flow, if referenced to PGND, can be disastrous.
5. The bypass capacitors connected to VDC and VLOGIC need to be as close to the pin as possible, and again should be referenced to AGND. This is also true for the COMP network and the rest of the analog components (on ISEDT1/2, FPWM, etc.).
6. The heat of the chip is mainly dissipated through the exposed thermal pad so maximizing the copper area around it is a good idea. A solid ground is always helpful for the thermal and EMI performance.
7. Mount the inductor and input and output capacitors as tight as possible, to reduce the audible noise and inductive ringing.

General Power PAD Design Considerations

Figure 28 shows an example of how to use vias to remove heat from the IC. Renesas recommends that you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad foot print with vias spaced such that the centre to centre spacing is three times the radius of the via. Keep the vias small, but not so small that their inside diameter prevents solder wicking through the holes during reflow.

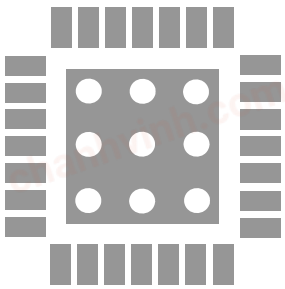


FIGURE 28. ISL97687 TQFN PCB VIA PATTERN

One Layer PCB Layout with SOIC Package

The general rules of two layer PCB layout can be applied to the one layer PCB layout of the SOIC package, although this layout is much more challenging and very easy to get wrong. The noisy PGND of the switching FET area and quiet AGND must be placed on the same plane as shown in Figure 30. Therefore, great care must be taken to maintain stable and clean operation, due to increased risk of noise injection to the quiet area.

1. Extend the GND plane as far as possible as space allows to spread out heat dissipation.
2. All ground pads for input caps, current sensor, output caps should be close to the PGND pin adjacent to the CS pin of ISL97687 with wide metal connection shown in the Figure 30 on page 20. This ensures a low differential voltage between these critical points.
3. The connection point between AGND pin 14 and PGND pin 18 should be "Narrow" neck, effectively making a star ground at the AGND pin.
4. The relatively quiet AGND area, to the right of the neck needs to be traced out carefully in unbroken metal, via the shortest possible path to the ground side of the components connected to OVP, COMP, ISET, PWM_SET/PLL, and ACTL. This

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is also true for the filtering caps on PWMI and STV. These are needed to reject noise and cause decoding errors in some conditions.

5. The current sensing line is shielded by a metal trace, coming from its source, to prevent pickup from the GD pin beside it.
6. Place the filtering cap of the current sensing line close to the CS pin rather than in the area of current sense resistor, as it needs to couple this pin to the adjacent PGND pin.
7. Keep the noisy switching FET far away from the quiet pin area.
8. Determine the area on the switching node by the dissipation requirements of the boost power FET.

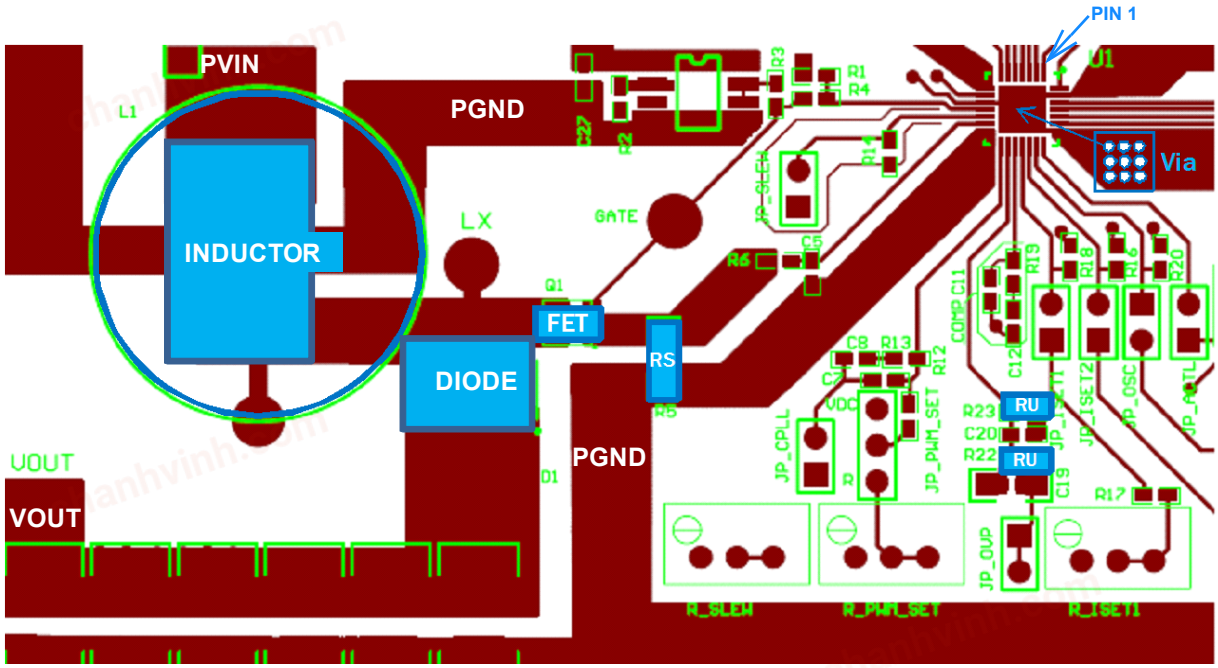


FIGURE 29. EXAMPLE OF TWO LAYER PCB LAYOUT

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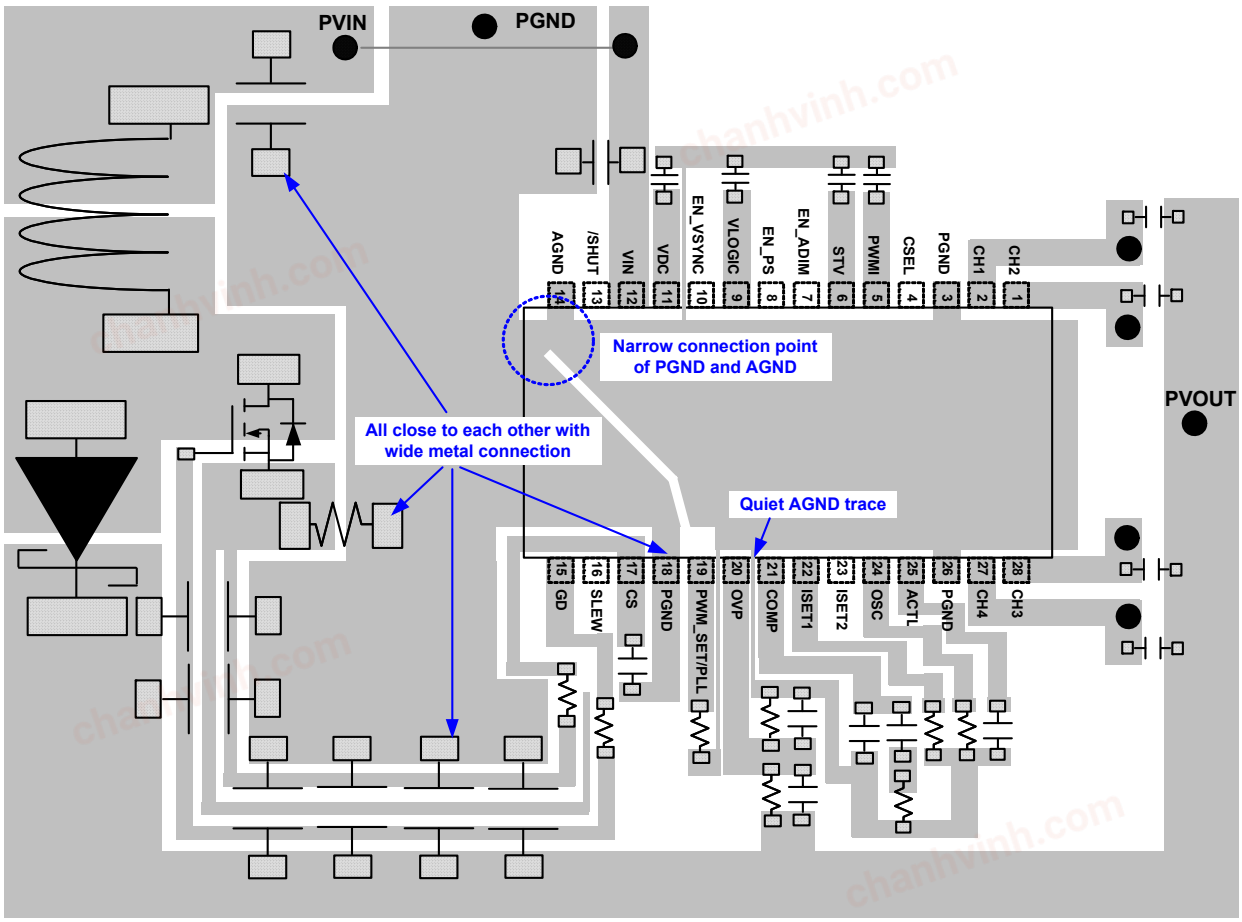
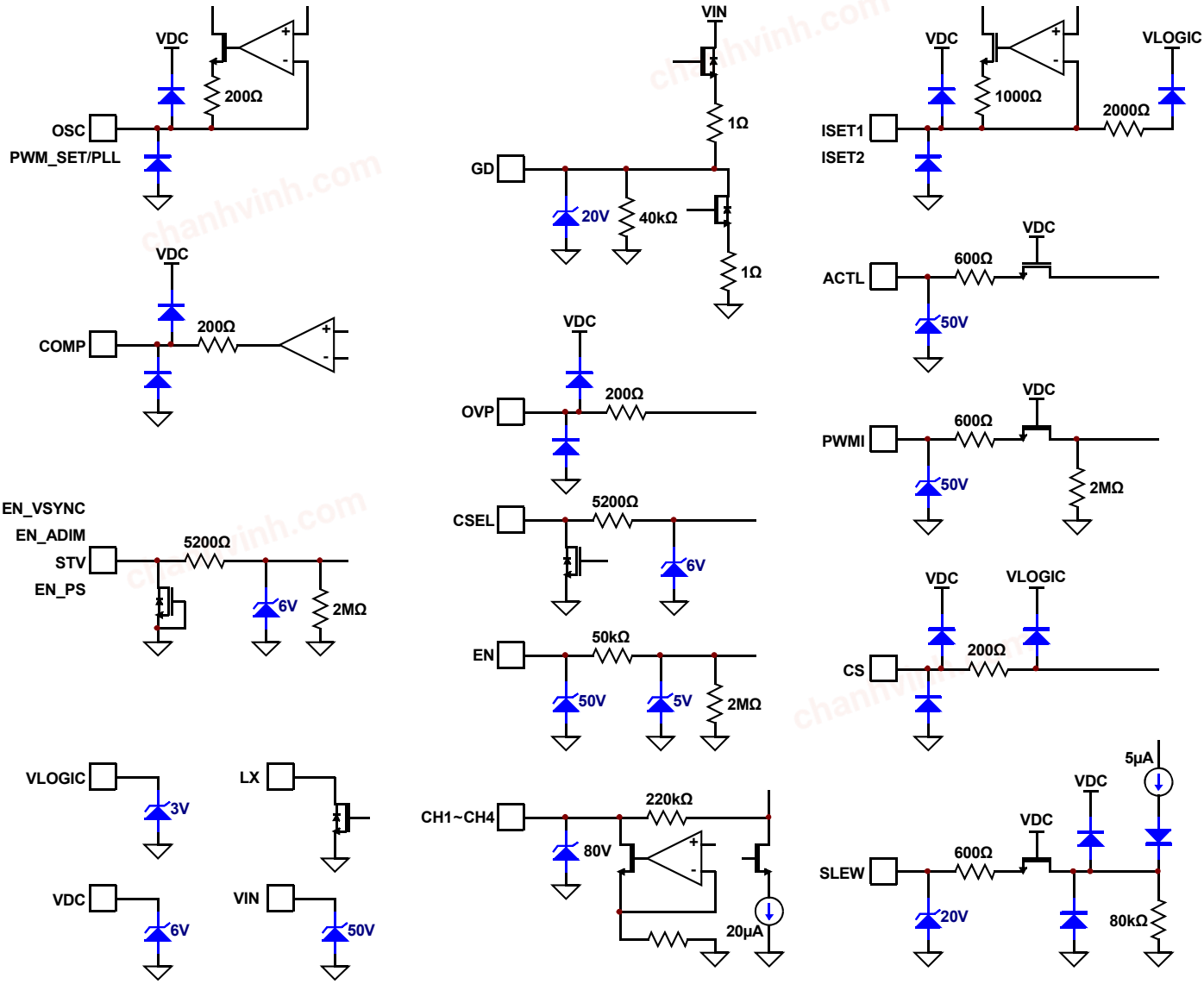


FIGURE 30. EXAMPLE OF ONE LAYER PCB LAYOUT

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Equivalent Circuit Diagrams



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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

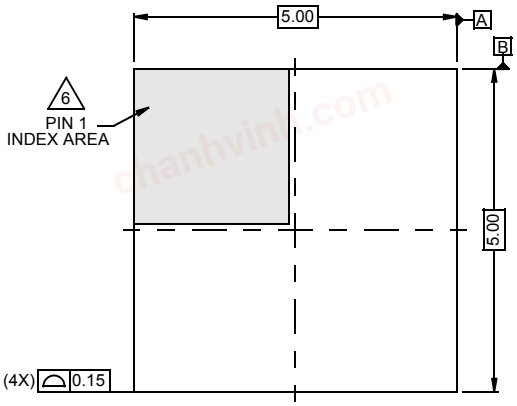
DATE	REVISION	CHANGE
Jun 7, 2019	FN7714.4	Updated links throughout datasheet. Updated Ordering Information table by adding the tape and reel information, removing evaluation board, and updating the notes. Updated LED DC Current Setting section. Added last paragraph in “LED DC Dimming” on page 12. Removed About Intersil section. Updated disclaimer.
Sep 13, 2017	FN7714.3	Applied new header/footer. Updated Ordering Information notes. Added $V_{HEADROOM_RANGE}$ spec to Electrical Specifications table. Added corresponding Note 11. In the Current Matching and Current Accuracy section - updated third sentence in paragraph 2 for clarification. Updated About Intersil section. Updated POD M28.3 to the latest revision. Change: Added land pattern
Nov 13, 2013	FN7714.2	Changed Eval Board name in ordering information on page 4 from “ISL97687IBZ-EVAL1Z” TO “ISL97687IBZEV1Z”
Sep 21, 2012	FN7714.1	Corrected PGND symbol in Figures 1 and 3. Corrected conditions for “VIH” in the “Electrical Specifications” table on page 7 from "Logic input low.." to "Logic input high.." Corrected label typo in Figure 20 from "RSET" to "RISET". Corrected "PWMI" and "CSEL" labels in the “Equivalent Circuit Diagrams” on page 21. Added Note 7 and corrected Note reference in “Thermal Information” on page 6 for SOIC from Note 4 to Note 7. Corrected I_CHI1 to V_CH1 in Figures 16 and 17 on page 10. Corrected FPWM pin to PWM_SET/PLL pin in first paragraph of “V_{sync} Function” on page 13 Added "The PWM dimming frequency, set by the PWM_SET pin, should be at least 1kHz when EN_ADIM is high." to second paragraph of “LED PWM Dimming – Duty Cycle Control” on page 12.
Sep 15, 2011	FN7714.0	Initial Release

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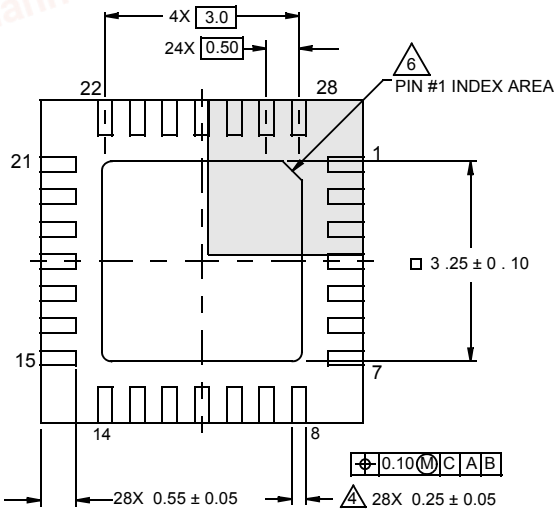
Package Outline Drawings

For the most recent package outline drawing, see L28.5x5B.

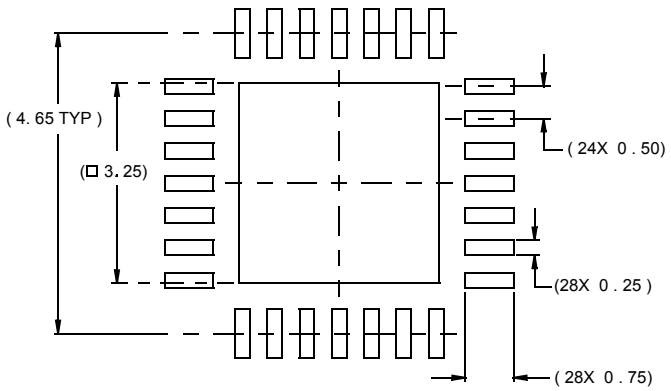
L28.5x5B
28 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 10/07



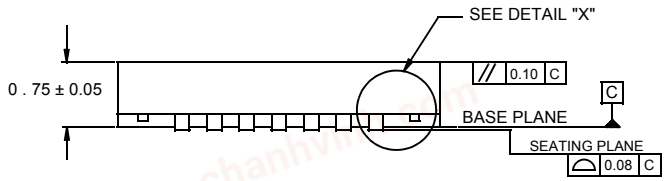
TOP VIEW



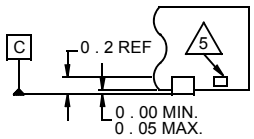
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



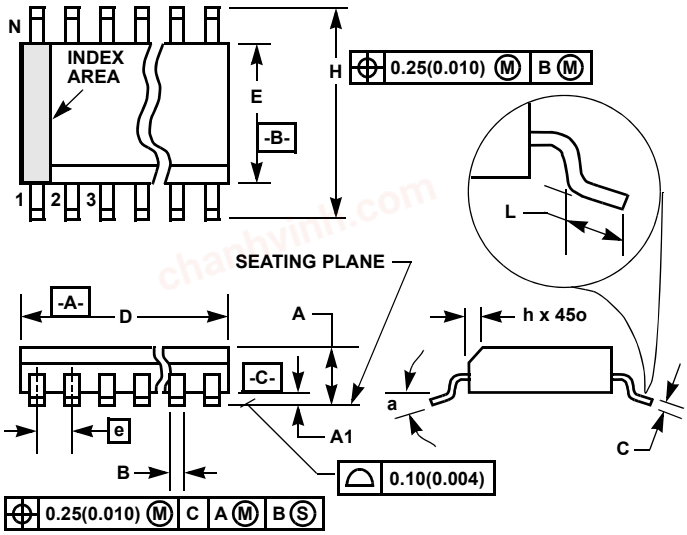
DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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For the most recent package outline drawing, see M28.3.

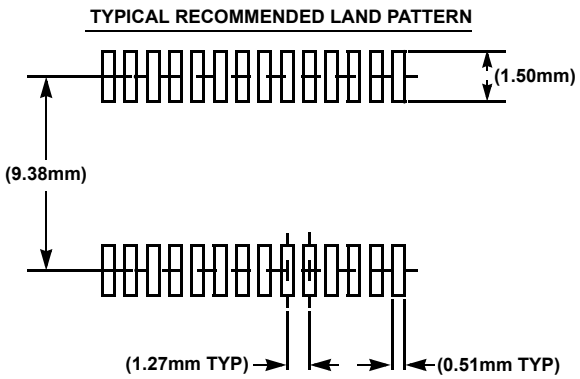


M28.3 (JEDEC MS-013-AE ISSUE C)

28 Lead Wide Body Small Outline Plastic Package (SOIC)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 1, 1/13



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.02 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are no necessarily exact.

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