chanhvinh.com

ISL97682, ISL97683, ISL97684

Compact 2-3-4-Ch LED Drivers with Phase Shift Control

FN7689
Rev.2.00
Sep 19, 2017

The ISL97682, ISL97683, ISL97684 are Intersil's highly integrated 2-3-4-channel LED drivers that are suitable for medium size TFT-LCD backlights. These parts can drive multiple channels of LEDs from inputs as low as 4V to outputs of up to 45V. They can also operate from inputs as low as 3V to outputs of up to 26.5V in bootstrap configuration (see Figure 26 for 3V operation).

The ISL97682, ISL97683, ISL97684 feature optional channels phase shift control. This feature is used to minimize the input, output ripple characteristics and load transient, which help eliminate or reduce the video and audio noise interference from the backlight driver operation.

The ISL97682, ISL97683, ISL97684 offer 8-bit PWM dimming for systems that need frequency tuning flexibility. With the unique adaptive boost switching architecture, the ISL97682, ISL97683, ISL97684 also offer Direct PWM dimming with output, which follows input and achieves linearity as low as 0.009% at 200Hz or 1.35% at 30kHz.

The drivers incorporate dynamic headroom control that monitors the highest LED forward voltage string and uses its feedback signal for the minimum output regulation. The ISL97682, ISL97683, ISL97684 incorporate extensive fault protection functions including string open and short circuit detections, OVP, and OTP. The switching frequency can be selected at either 600kHz or 1.0MHz in PFM or PWM mode. These parts are available in the thin and compact 16 Ld 3mmx3mm TQFN package and operate in ambient temperature from -40°C to +85°C.

Features

- ISL97682 - 2 x 100mA Channels
- ISL97683 - 3 x 50mA Channels
- ISL97684 - 4 x 50mA Channels
- Input Voltage 4.0V~26.5V with Max V_{OUT} of 45V
- Input Voltage 3.0V (see Figure 26)~24V with Max V_{OUT} of 26.5V
- PWM Dimming Linearity
  - PWM Dimming with Adjustable Dimming Frequency with Duty Cycle Linear from 0.4% to 100% <30kHz
  - Direct PWM Dimming with Duty Cycle Linear from 0.009% to 100% at 200Hz
- Current Matching of 0.7% typical from 1%~100% Dimming
- Selectable 600kHz or 1MHz Switching Frequency in PWM/PFM Mode
- Dynamic Headroom Control
- Fault Protection
  - String Open/Short Circuit Protections, OVP, OTP
- Thin and Compact TQFN-16 3mmx3mm Package

Applications

- Tablet to Notebook PC Displays LED Backlighting
- PMP LED Backlighting

Related Literature

- For a full list of related documents, visit our website
  - ISL97682, ISL97683, ISL97684 product page

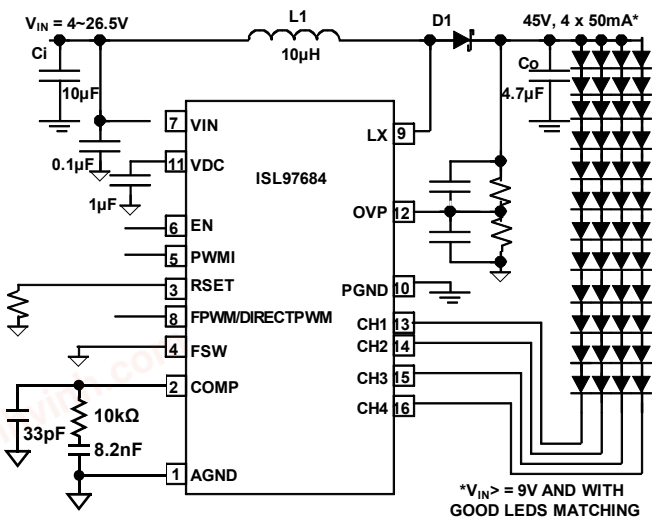


FIGURE 1A. DIRECT PWM DIMMING

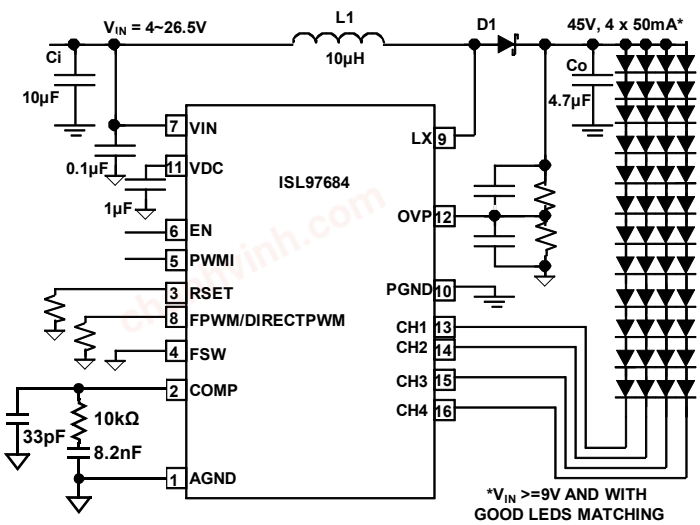


FIGURE 1B. PWM DIMMING WITH DIMMING FREQUENCY ADJUSTMENT USING R_{FPWM}

FIGURE 1. ISL97684 TYPICAL APPLICATION DIAGRAMS

chanhvinh.com

Block Diagram

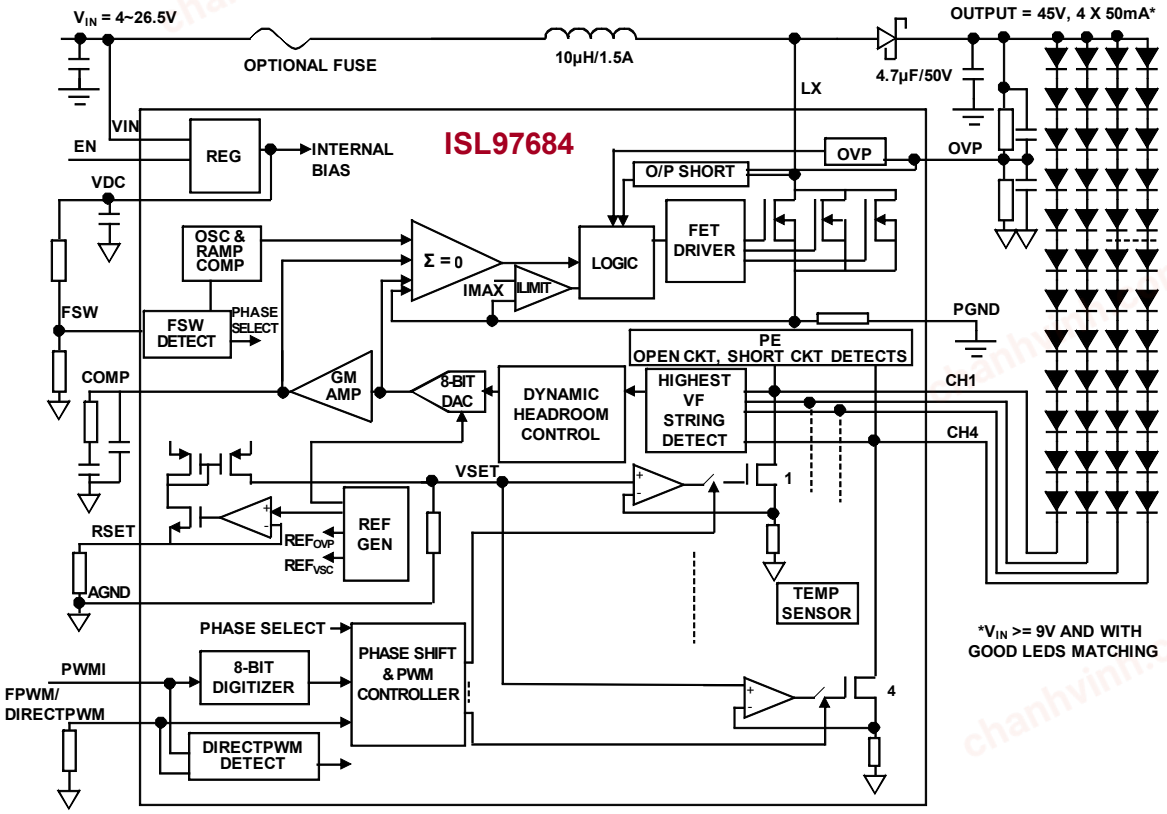


FIGURE 2. ISL97684 BLOCK DIAGRAM

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL97682IRTZ	7682	-40 to +85	16 LD 3x3 TQFN	L16.3x3D
ISL97683IRTZ	7683	-40 to +85	16 LD 3x3 TQFN	L16.3x3D
ISL97684IRTZ	7684	-40 to +85	16 LD 3x3 TQFN	L16.3x3D
ISL97682IRTZEVALZ	Evaluation Board			
ISL97683IRTZEVAL	Evaluation Board			
ISL97684IRTZEVALZ	Evaluation Board			

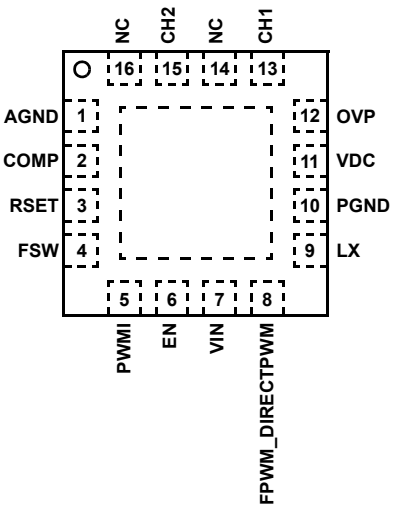
NOTES:

1. Add “-T” suffix for 6k unit or “-TK” suffix for 1k unit tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information page for ISL97682, ISL97683, ISL97684. For more information on MSL, see TB363.

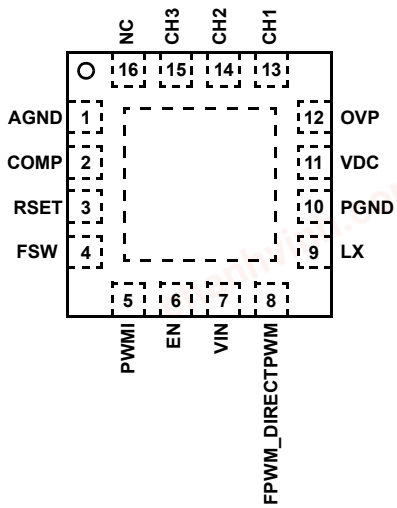
chanhvinh.com

Pin Configurations

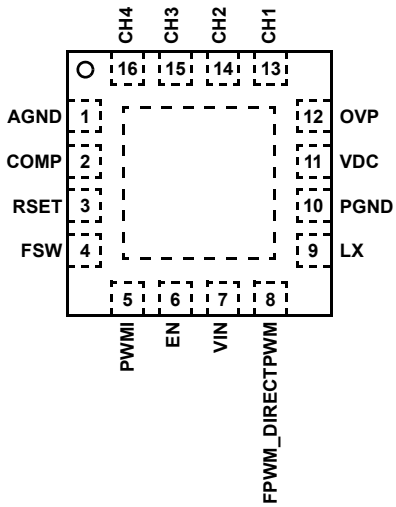
ISL97682
(16 LD TQFN)
TOP VIEW



ISL97683
(16 LD TQFN)
TOP VIEW



ISL97684
(16 LD TQFN)
TOP VIEW



chanhvinh.com

Pin Descriptions

PIN	ISL97682	ISL97683	ISL97684	DESCRIPTION
1	AGND	AGND	AGND	Analog Ground for precision circuits
2	COMP	COMP	COMP	External Compensation Pin
3	RSET	RSET	RSET	Resistor connection for setting LED current, (see Equation 2 for calculating the ILEDpeak)
4	FSW	FSW	FSW	FSW = 0 ~ 0.11 * VDC, Boost Switching Frequency = 600kHz with phase shift and PFM mode enabled. FSW = 0.34 * VDC ~ 0.44 * VDC, Boost Switching Frequency = 600kHz with phase shift and PWM mode enabled. FSW = 0.53 * VDC ~ 0.63 * VDC, Boost Switching Frequency = 1MHz with phase shift and PWM mode enabled. FSW = 0.86 * VDC ~ VDC, Boost Switching Frequency = 1MHz with phase shift and PFM mode enabled.
5	PWMI	PWMI	PWMI	PWM brightness control pin.
6	EN	EN	EN	Enable, can be tied directly to VIN if the system lacks of I/O
7	VIN	VIN	VIN	LED and Driver Supply Voltage. LED supply and Driver supply can be separated if high voltage application is needed and dual supplies are available
8	FPWM/ DirectPWM	FPWM/ DirectPWM	FPWM/ DirectPWM	External PWM dimming with frequency modulation or Direct PWM dimming without frequency modulation. With a resistor connected to ground, the dimming frequency will be set by the Setting Resistor. When this pin is floating, the part enters Direct PWM mode such that the dimming follows the input PWM signal without frequency modulation.
9	LX	LX	LX	Input to boost switch
10	PGND	PGND	PGND	Power ground (LX, C_{IN}, and C_{OUT} Power return)
11	VDC	VDC	VDC	De-couple capacitor for internally generated 5V supply
12	OVP	OVP	OVP	Overvoltage protection input
13	CH1	CH1	CH1	Input 1 to current source, CH, and monitoring
14	NC	CH2	CH2	Input 2 to current source, CH, and monitoring (ISL97682 is No Connect)
15	CH2	CH3	CH3	Input 3 to current source, CH, and monitoring
16	NC	NC	CH4	Input 4 to current source, CH, and monitoring (ISL97682, ISL97683 are No Connect)

chanhvinh.com

Absolute Maximum Ratings

VIN, EN . . . . . -0.3V to 28V
VDC, PWMI, FPWM/DirectPWM, FSW, RSET, COMP, OVP . . . -0.3V to 5.5V
CH1 to CH4, LX . . . . . -0.3V to 45V
PGND, AGND . . . . . -0.3V to +0.3V
Above voltage ratings are all with respect to AGND pin

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 LD TQFN (Notes 4, 5)	51	4.6

Thermal Characterization (Typical)	PSI_{JT} (°C/W)
16 Ld TQFN (Note 6)	0.11

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings.

Electrical Specifications

All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 12V, EN = 5V, R_{SET} = 20kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
GENERAL						
V_{IN}	Backlight Supply Voltage, (Note 8)	T_A = +25°C	4.0		26.5	V
I_{VIN}	VIN Active Current	EN = 3.3V		5		mA
IVIN_STBY	VIN Shutdown Current	EN = 0V, T_A = 25°C			5	µA
V_{OUT}	Output Voltage	4.0V < V_{IN} ≤ 26.5V			**45**	V
V_{UVLO}	Undervoltage Lockout Threshold		**2.2**		**2.5**	V
V_{UVLO_HYS}	Undervoltage Lockout Hysteresis			100		mV
LINEAR REGULATOR						
V_{DC}	LDO Output Voltage	V_{IN} > 6V	**4.6**	4.8	**5**	V
V_{LDO}	VDC LDO Dropout Voltage	V_{IN} = 5V, I_{VDC} = 20mA		30	**200**	mV
EN_{Low}	Guaranteed Range for EN Input Low Voltage				**0.5**	V
EN_{Hi}	Guaranteed Range for EN Input High Voltage		**1.5**			V
$t_{EN(Low)}$	EN low time before shut-down			29.5		ms
BOOST SWITCHING REGULATOR						
SS	Soft-start	100% LED Duty Cycle		7		ms
SW_{ILimit}	Boost FET Current Limit		1.4	1.8	2.3	A
$r_{DS(ON)}$	Internal Boost Switch ON-Resistance			500		mΩ
Eff_peak	Peak Efficiency	V_{IN} = 24V, 48 LEDs, 30mA each, L = 10µH with DCR ≤100mΩ, T_A = +25°C		90.1		%
		V_{IN} = 12V, 48 LEDs, 30mA each, L = 10µH with DCR ≤ 100mΩ, T_A = +25°C		87		%
D_{MAX}	Boost Maximum Duty Cycle	V_{FSW} < 2.4V (F_{SW} = 600kHz)	**92**			%
		V_{FSW} > 2.4V (F_{SW} =1.0MHz)	**85**			%
D_{MIN}	Boost Minimum Duty Cycle	V_{FSW} < 2.4V (F_{SW} = 600kHz)			8	%
		V_{FSW} > 2.4V (F_{SW} = 1.0MHz)			15	%

chanhvinh.com

Electrical Specifications

All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 12V, EN = 5V, R_{SET} = 20kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
F_{SW}	Boost Switching Frequency	F_{SW} < 2.4V	**500**	600	**650**	kHz
		F_{SW} > 2.4V	**0.9**	1.0	**1.1**	MHz
ILX_leakage	LX Leakage Current	LX = 45V, EN = 0			**10**	µA
REFERENCE						
I_{MATCH}	Channel-to-Channel DC Current Matching	R_{SET} = 20kΩ (I_{LED} = 20mA for ISL97683/4 and 40mA for ISL97682)	**-2**		**+2**	%
		R_{SET} = 40kΩ (I_{LED} = 10mA for ISL97683/4 and 20mA for ISL97682)	**-2.5**		**+2.5**	%
I_{ACC}	Current Accuracy	I_{LED} = 20mA (ISL97683/4) I_{LED} = 40mA (ISL97682)	**-2**		**+2**	%
FAULT DETECTION						
V_{SC}	Channel Short Circuit Threshold		**3.8**	4.4	**4.9**	V
V_{temp}	Over-Temperature Threshold			150		°C
V_{temp_acc}	Over-Temperature Threshold Accuracy			5		°C
V_{OVPIo}	Overvoltage Limit on OVP Pin		**1.18**	1.22	**1.24**	V
OVP_{fault}	OVP Short Detection Fault Level			70		mV
CURRENT SOURCES						
$V_{HEADROOM}$	Dominant Channel Current Source Headroom at CHx Pin	I_{LED} = 20mA		500 (Note 9)		mV
$V_{HEADROOM_RANGE}$	Dominant Channel Current Sink Headroom Range at CHx Pin	I_{LED} = 20mA, T_A = +25°C		90		mV
V_{RSET}	Voltage at RSET Pin		**1.2**	1.22	**1.24**	V
$I_{LED(max)}$	Maximum LED Current per Channel	ISL97682		100		mA
		ISL97683		50		mA
		ISL97684		50		mA
PWM GENERATOR						
V_{IL}	Guaranteed Range for PWM Input Low Voltage				**0.8**	V
V_{IH}	Guaranteed Range for PWM Input High Voltage		**1.5**			V
F_{PWMI}	PWMI Input Frequency Range		**100**		**30,000**	Hz
$DPWM_{ACC}$	Direct PWM Dimming Output Maximum Resolution			85		ns
$t_{DPWM_ON_MIN}$	Direct PWM Dimming Minimum On-Time	Direct PWM Mode	**250**		**450**	ns
PWM_{ACC}	PWM Dimming with Adjustable Dimming Frequency Output Resolution			8		bit
PWM_{HYST}	PWMI Input Allowable Jitter Hysteresis		**-0.46**		**+0.46**	LSB
F_{PWM}	Generated PWM Dimming Frequency Range		**100**		**30,000**	Hz
V_{FPWM}	Voltage at FPWM pin	R_{FPWM} = 3.3kΩ	**1.20**	1.22	**1.24**	V

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. At maximum V_{IN} of 26V, minimum V_{OUT} is 28V. Minimum V_{OUT} can be lower at lower V_{IN}.
9. Varies within range specified by $V_{HEADROOM_RANGE}$.

chanhvinh.com

Typical Performance Curves

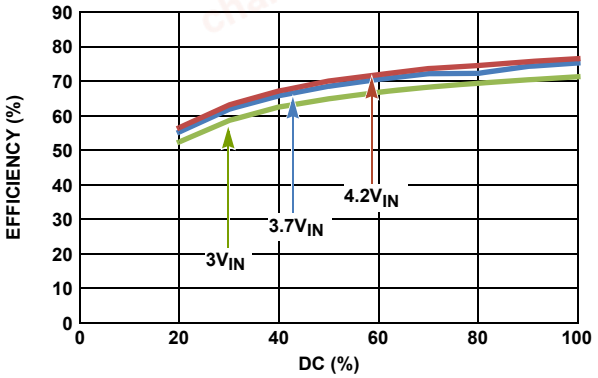


FIGURE 3. ISL97683 TYPICAL EFFICIENCY FOR 3V TO 4.2V IN A 3P7S, ILED = 20mA/CH SINGLE SUPPLY CONFIGURATION AT F_{SW} = 600kHz IN PWM MODE

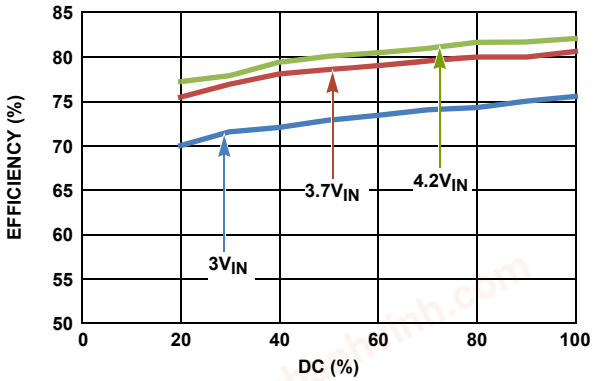


FIGURE 4. ISL97683 TYPICAL EFFICIENCY FOR 3V TO 4.2V IN A 3P7S, ILED = 20mA/CH CONFIGURATION AT F_{SW} = 600kHz IN PWM MODE WITH V_{IN} SUPPLY = 5V

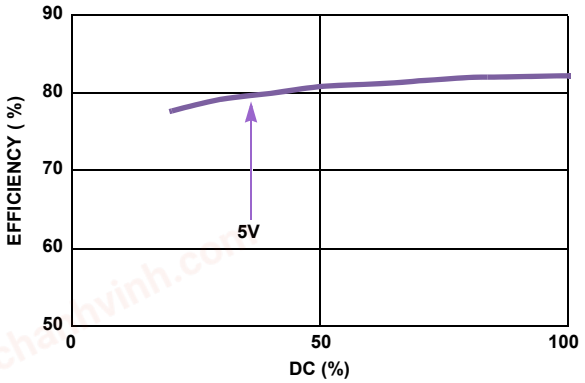


FIGURE 5. ISL97683 TYPICAL EFFICIENCY FOR $5V_{IN}$ IN A 3P7S, ILED = 20mA/CH CONFIGURATION AT F_{SW} = 600kHz IN PWM MODE

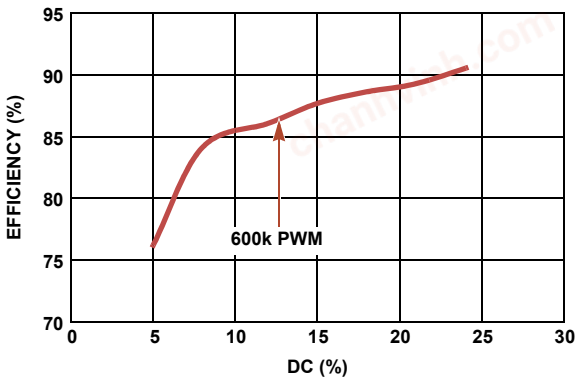


FIGURE 6. ISL97684 EFFICIENCY FOR 4P10S AT 20mA/CH AT 600kHz IN PWM MODE

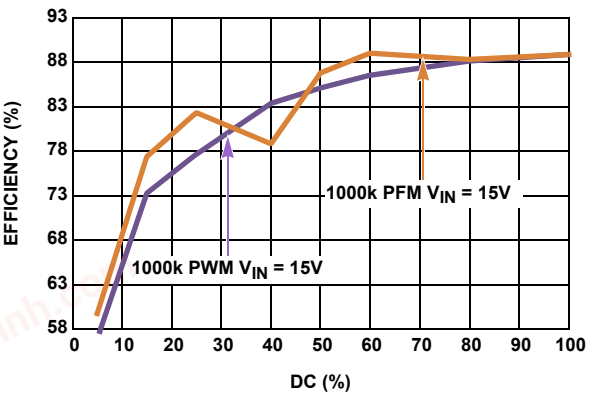


FIGURE 7. ISL97864 PWM vs PFM EFFICIENCY vs DC AT V_{IN} = 15V IN4P8S CONFIGURATION

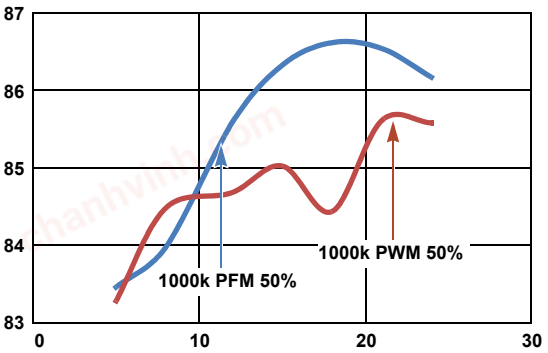


FIGURE 8. PFM vs PFM MODE FOR 4P8S vs V_{IN} AT 1MHz

chanhvinh.com

Typical Performance Curves (Continued)

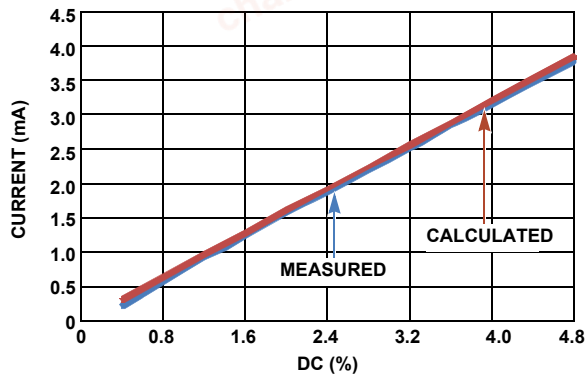


FIGURE 9. CURRENT LINEARITY vs LOW LEVEL PWM DIMMING DUTY CYCLE AT 12V_{IN} FOR 4P10S AT 20mA/CH

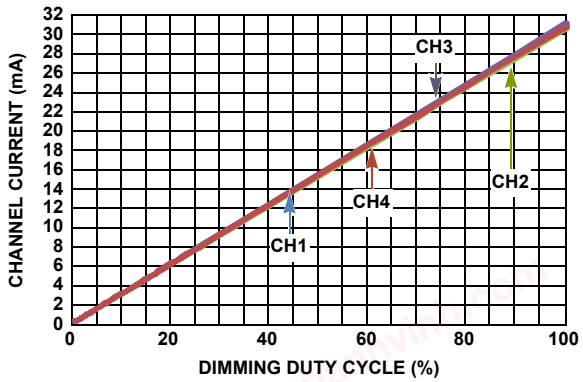


FIGURE 10. CURRENT LINEARITY vs PWM DIMMING DUTY CYCLE AT 12V_{IN} FOR 4P10S AT 20mA/CH

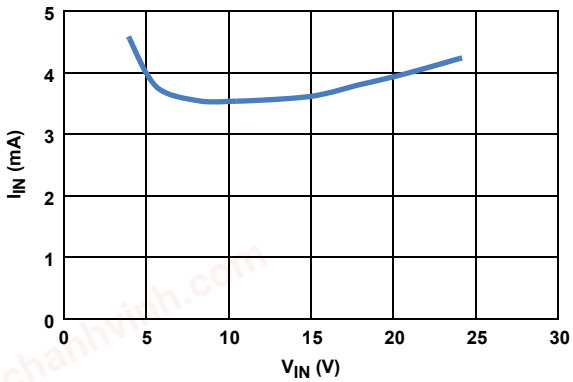


FIGURE 11. QUIESCENT CURRENT vs V_{IN} WITH EN = HIGH, NO LEDS CONNECTED

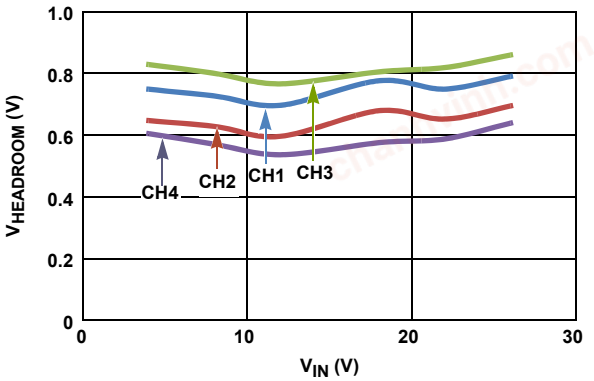


FIGURE 12. CHANNEL VOLTAGE vs V_{IN} FOR V_{IN} = 12V AT 4P10S AT 20mA/CH

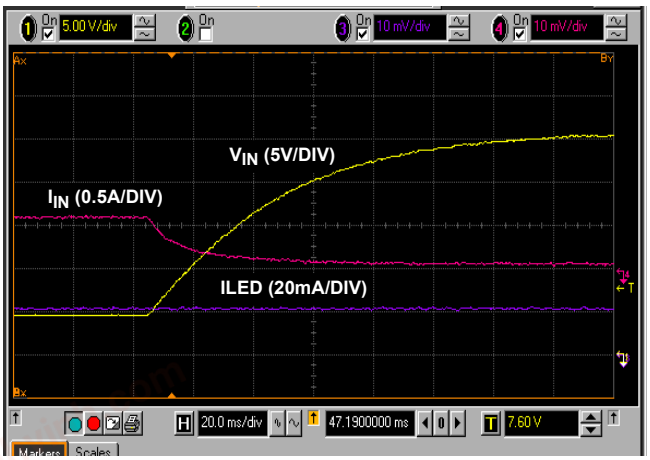


FIGURE 13. LINE REGULATION WITH V_{IN} CHANGE FROM 6V TO 26V FOR 4P10S AT 20mA/C

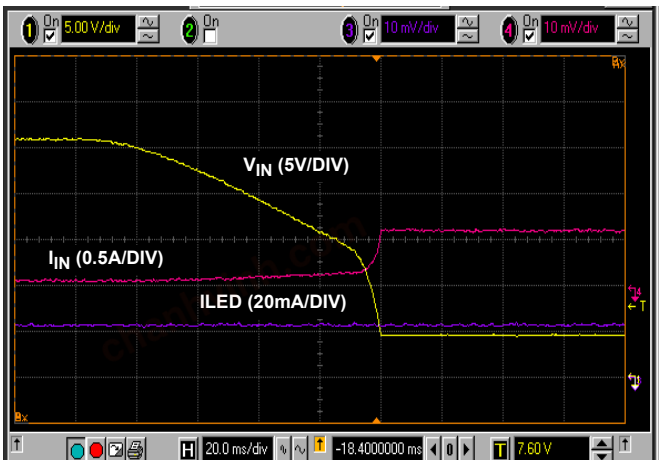


FIGURE 14. LINE REGULATION WITH V_{IN} CHANGE FROM 26V TO 6V FOR 4P10S AT 20mA/CH

chanhvinh.com

Typical Performance Curves (Continued)

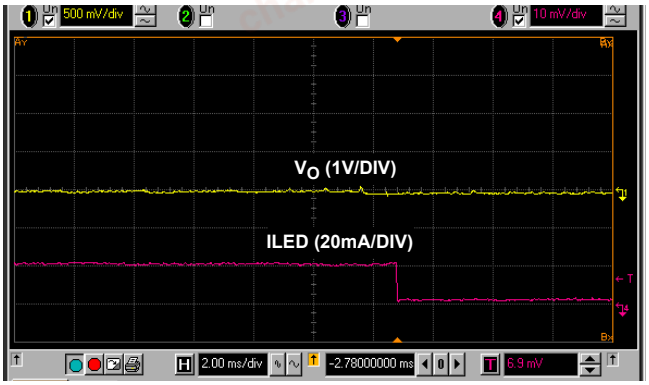


FIGURE 15. LOAD REGULATION WITH ILED CHANGE FDROM 100% TO 0% PWM DIMMING, V_{IN} = 12V AT 20mA/CH

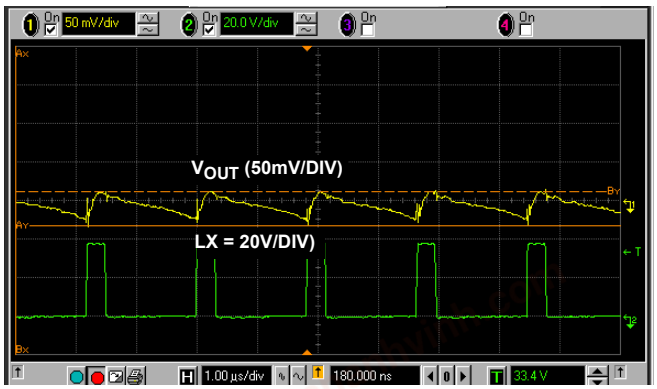


FIGURE 16. V_{OUT} RIPPLE VOLTAGE, V_{IN} = 12V, 4P10S AT 20mA/CH

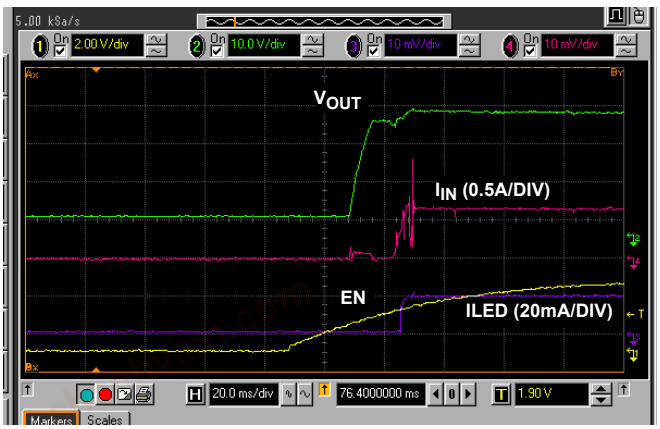


FIGURE 17. IN-RUSH AND LED CURRENT AT V_{IN} = 5V FOR 4P10S AT 20mA/CH

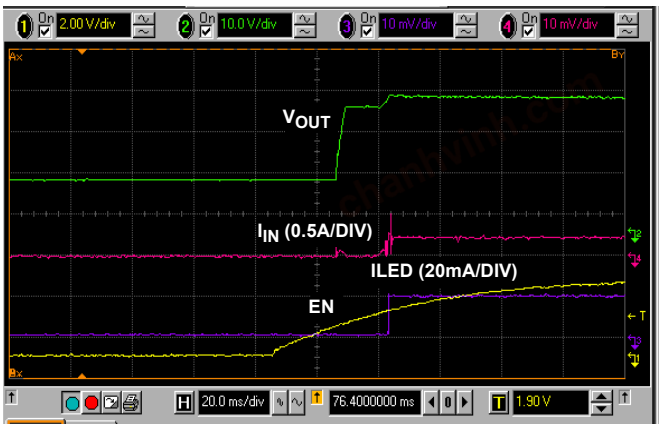


FIGURE 18. IN-RUSH AND LED CURRENT AT V_{IN} = 12V FOR 4P10S AT 20mA/CH

chanhvinh.com

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97682, ISL97683, and ISL97684 employ current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for the notebook backlight application where the power can be a series of drained batteries or instantly change to an AC/DC adapter without rendering a noticeable visual nuisance. The number of LEDs that can be driven by the ISL97682, ISL97683, ISL97684 depends on the type of LED chosen in the application. The ISL97682, ISL97683, ISL97684 are capable of boosting up to 45V and typically driving 13 LEDs in series for each of the 4 channels, enabling a total of 52 pieces of the 3.2V/20mA type of LEDs.

OVP

The Overvoltage Protection (OVP) pin has a function of setting the overvoltage trip level as well as limiting the V_{OUT} regulation range.

The ISL97682, ISL97683, ISL97684 OVP threshold is set by R_{UPPER} and R_{LOWER} shown by Equation 1:

$$V_{OUT_OVP} = 1.22V * (R_{UPPER} + R_{LOWER})/R_{LOWER} \quad \text{(EQ. 1)}$$

V_{OUT} can only regulate between 42% and 100% of the V_{OUT_OVP} such that:

Allowable V_{OUT} = 42% to 100% of V_{OUT_OVP}

For example, if 10 LEDs are used with the worst case being V_{OUT} of 35V. If R_1 and R_2 are chosen such that the OVP level is set at 40V, then the V_{OUT} is allowed to operate between 16.8V and 40V. If the requirement is changed to 4 LEDs of 14V V_{OUT} application, then the OVP level must be reduced and users should follow the V_{OUT} = (42% ~100%) OVP level requirement. Otherwise, the headroom control will be disturbed such that the channel voltage can be much higher than expected and sometimes can prevent the driver from operating properly.

The ratio of the OVP capacitor should be the inverse of the OVP resistor. For example:
if R_{UPPER}/R_{LOWER} = 33/1, then C_{UPPER}/C_{LOWER} = 1/33 with C_{UPPER} = 100pF and C_{UPPER} = 3.3nF.

Enable

An EN signal is required to enable the internal regulator for normal operation. If there is no signal for longer than 28ms, the device will enter shutdown.

Power Sequence

There is no specific power sequence requirement for the ISL97682, ISL97683, ISL97684. The EN signal can be tied to V_{IN} but not the VDC that will prevent the device from powering up.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 19.

The LED peak current is set by translating the R_{SET} current to the output with a scaling factor of $401.8/R_{SET}$. The source terminals of the current source MOSFETs are designed to operate within a range at about 500mV to optimize power loss versus accuracy requirements. The sources of errors of the channel-to-channel current matching come from the op amps offset, internal layout, reference, and current source resistors. These parameters are optimized for current matching and absolute current accuracy. However, the absolute accuracy is additionally determined by the external R_{SET}. A 1% tolerance resistor is recommended.

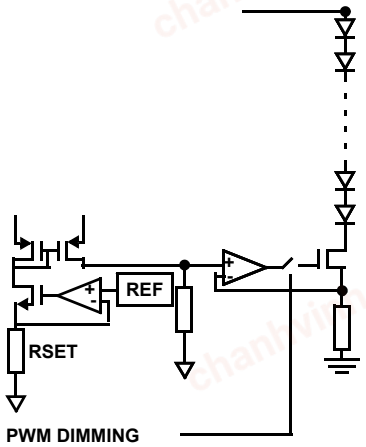


FIGURE 19. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97682, ISL97683, ISL97684 feature a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or the lowest voltage from any of the CH pins digitally. When the lowest CH voltage is lower than the short circuit threshold (V_{SC}), such voltage will be used as the feedback signal for the boost regulator. The boost makes the output to the correct level such that the lowest CH is at the target headroom voltage. Since all LED stacks are connected to the same output voltage, the other CH pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same current. The output voltage will regulate cycle-by-cycle and it is always referenced to the highest forward voltage string in the architecture.

Dimming Controls

The ISL97682, ISL97683, ISL97684 allow two ways of controlling the LED current, and therefore, the brightness. They are:

1. DC current adjustment
2. PWM chopping of the LED current defined in Step 1.

There are various ways to achieve DC or PWM current control, which will be described in the following.

chanhvinh.com

Maximum DC Current Setting

The initial brightness should be set by choosing an appropriate value for R_{SET}. This should be chosen to fix the maximum possible LED current as shown in Equation 2 for ISL97682 and Equation 3 for ISL97683 and ISL97684:

$$I_{LEDmax} = \frac{(804)}{R_{SET}} \quad \text{(EQ. 2)}$$

$$I_{LEDmax} = \frac{(402)}{R_{SET}} \quad \text{(EQ. 3)}$$

DC Current Adjustment

Once R_{SET} is fixed, the LED DC current can be adjusted.

For example, in the 4-channel ISL97684, if the maximum required LED current ($I_{LED(max)}$) is 20mA, rearranging Equation 3 yields Equation 4:

$$R_{SET} = (402)/0.02 = 20.1k\Omega \quad \text{(EQ. 4)}$$

PWM Control

The ISL97682, ISL97683, ISL97684 have high speed 8-bit digitizers that decode the incoming PWM signal and convert it into 2- 3- or 4- channels of 8-bit PWM current with a phase shift function that will be described later. During the PWM On period, the LED peak current is defined by the R_{SET} resistor value. The average LED current of each channel is controlled by I_{LEDmax} and the PWM duty cycle in percent shown by Equation 5:

$$I_{LED(ave)} = I_{LEDmax} \times PWM \quad \text{(EQ. 5)}$$

When the PWM input = 0, all channels are disconnected and the I_{LED} is guaranteed to be <5µA in this state.

The PWM dimming frequency is adjusted by a resistor at the RFPWM pin, described in "PWM Dimming Frequency Adjustment" on page 12.

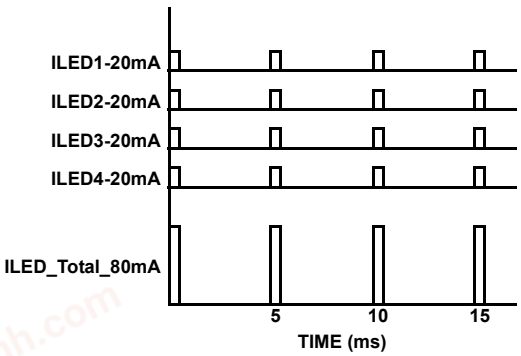


FIGURE 20. CONVENTIONAL 4-Ch LED DRIVER WITH 10% PWM DIMMING CHANNEL CURRENT (UPPER) AND TOTAL CURRENT (LOWER)

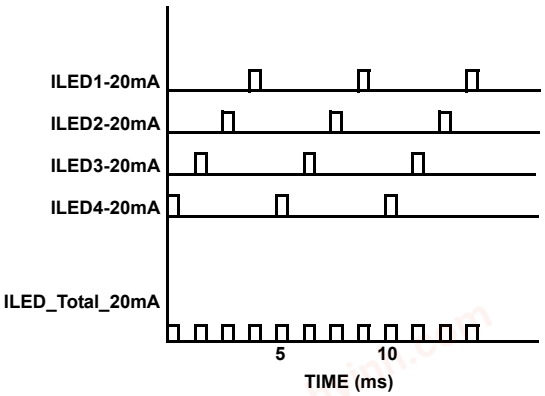


FIGURE 21. PHASE SHIFT 4-Ch LED DRIVER WITH 10% PWM DIMMING CHANNEL CURRENT (UPPER) AND TOTAL CURRENT (LOWER)

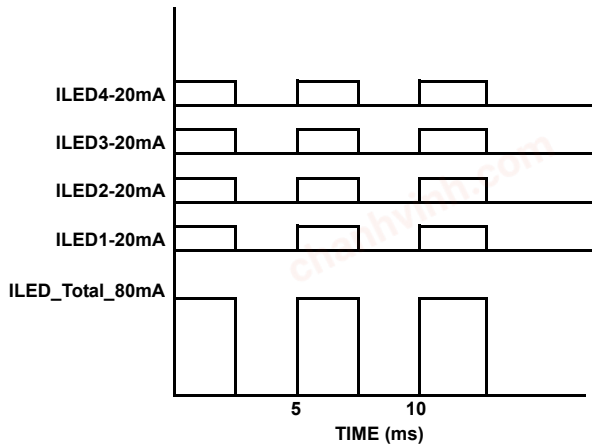


FIGURE 22. CONVENTIONAL LED DRIVER PWM DIMMING CHANNEL AND TOTAL CURRENT AT 50% DUTY CYCLE

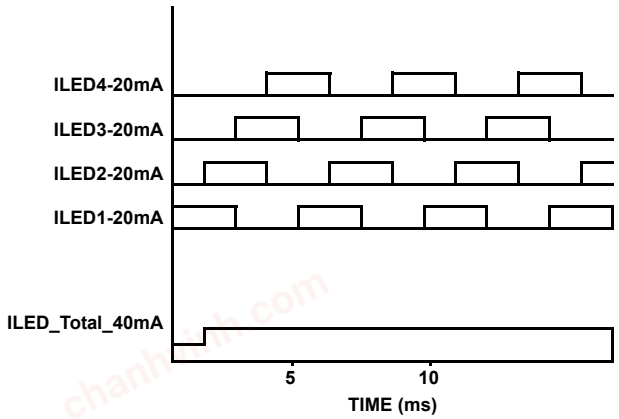


FIGURE 23. EQUAL PHASE SHIFT LED DRIVER PWM DIMMING CHANNEL AT 50% DUTY CYCLE

chanhvinh.com

Phase Shift Control

The ISL97682, ISL97683, ISL97684 are capable of delaying the phase of each current source. Conventional LED drivers exhibit the worst load transients to the boost circuit by turning on all channels simultaneously as shown in Figures 20 and 21. In contrast, the ISL97682, ISL97683, ISL97684 phase shifts each channel by turning them on once during each PWM dimming period as shown in Figures 23 and 24. At each dimming duty cycle except at 100%, the sum of the phase shifted total current will be less than a conventional LED drivers' total current.

For ISL97682, the two channels are separated by 180°. For ISL97683, the three channels are separated by 90° and not 120°. For ISL97684, the four channels are separated by 90°. If the channels are combined for higher current application, the phase shift function must be disabled by running the part in direct PWM mode by floating the RFPWM/DirectPWM and selecting switching frequency by biasing the FSW pin as explained in Table 2.

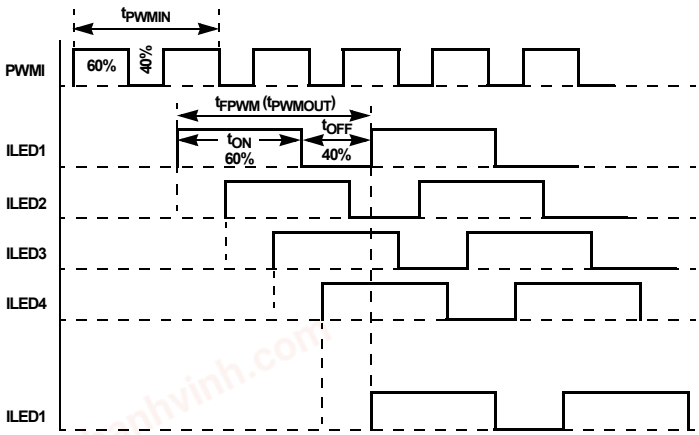


FIGURE 24. ISL97684 4 CHANNELS PHASE SHIFT ILLUSTRATION

PWM Dimming Frequency Adjustment

The dimming frequency is set by an external resistor at the RFPWM/DirectPWM pin to GND calculated by Equation 6:

$$\left(F_{PWM} = \frac{(12.4) \times 10^7}{RFPWM}\right) \quad \text{(EQ. 6)}$$

where FPWM is the desirable PWM dimming frequency and R_{FPWM} is the setting resistor. Do not bias RFPWM/DirectPWM if direct PWM dimming is used; see Table 1 for clarification.

The PWM dimming frequency can be set or applied up to 30kHz with duty cycle from 0.4% to 100%. The lower limit of 0.4% is the result of 8-bit digitizer resolution.

Direct PWM Dimming

The ISL97682, ISL97683, ISL97684 can also operate in direct PWM dimming mode such that the output follows the input PWM signal without phase shifting. The FSW pin can still be used to select between 600kHz and 1MHz in PWM or PFM mode as explained in "Pin Descriptions" on page 4. To use Direct PWM mode, users should float the RFPWM/DirectPWM pin. The input PWM frequency should be limited to 30kHz and the minimum duty cycle be calculated by Equation 7:

$$\text{Min Duty Cycle} = 450\text{ns} \times \text{Input PWM Frequency} \quad \text{(EQ. 7)}$$

For example, for a 200Hz input PWM frequency, the minimum duty cycle is:

$$\text{Min DC} = 450\text{ns} \times 200\text{Hz} = 0.009\% \quad \text{(EQ. 8)}$$

Table 1 shows the PWM Dimming with Phase Shift and Direct PWM Dimming configurations.

TABLE 1.

RFWM/ DIRECTPWM	FUNCTION	PHASE SHIFT	DIMMING RESOLUTION
Connects with Resistor	PWM Dimming with frequency adjust	Yes	8-bit
Floating	DirectPWM without frequency adjust	No	N/A

Switching Frequency and PWM/PFM Mode

When the FSW pin is biased from VDC with a resistor divider R_{UPPER} and R_{LOWER}, the switching frequency and PFM/PWM mode will change according to the following FSW levels shown in Table 2 with the recommended R_{UPPER} and R_{LOWER}.

TABLE 2.

FSW	F_{SW}	PHASE SHIFT	Mode	R_{UPPER}	R_{LOWER}
(0 ~ 0.11)*VDC	600kHz	Yes	PFM	Open	0
(0.34~0.44)*VDC	600kHz	Yes	PWM	187kΩ	120kΩ
(0.53~0.63)*VDC	1.0MHz	Yes	PWM	100kΩ	138kΩ
(0.86~1) VDC	1.0MHz	Yes	PFM	0	Open

The ISL97682, ISL97683, ISL97684 goes into PFM mode at F_{SW} = 600kHz/1MHz when the FSW pin is biased at 0/VDC volts. The part will only go into PFM mode depending on the LED output voltage and loading conditions and can be more efficient than running the part in PWM mode as shown in Figures 5 and 6. The dimming frequency can be set or applied up to 30kHz with duty cycle from 0.4% to 100%. The lower limit of 0.4% is the result of an 8-bit digitizer resolution.

Soft-Start

The in-rush current will flow towards C_{OUT} when V_{IN} is applied and it is determined by the ramp rate of V_{IN} and the values of C_{OUT} and L.

Once the part is enabled, the boost regulator will begin to switch and the current in the inductor will ramp-up. The current in the boost power switch is monitored and the switching is terminated in any cycle where the current exceeds the current limit. The ISL97682, ISL97683, ISL97684 include a soft-start feature where this current limit starts at a low value (225mA). This is stepped up to the final 1.8A current limit in 7 further steps of 225mA. These steps will happen over approximately 8ms and will be extended at a low LED PWM frequency if the LED duty cycle is low. This allows the output capacitor to be charged to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

chanhvinh.com

Fault Protection and Monitoring

The ISL97682, ISL97683, ISL97684 feature extensive protection functions to cover all the perceivable failure conditions. The failure mode of a LED can be either open circuit or as a short. The behavior of an open circuited LED can also take the form of either infinite resistance (or for some LEDs, a zener diode), which is integrated into the device in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes), an open circuit failure of an LED will only result in the loss of one channel of LEDs without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels unless a similar fault is occurring.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97682, ISL97683, ISL97684 use feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. See Table 3 for more details.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are detected above the programmed short circuit threshold. When an LED becomes shorted, the action taken is described in Table 3. The short circuit threshold is 4.4V.

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97682, ISL97683, ISL97684 monitors the current in each channel such that any string which reaches the intended output current, is considered “good”. Should the current subsequently fall below the target, the channel will be considered an “open circuit”. Furthermore, should the boost output of the ISL97682, ISL97683, ISL97684 reach the OVP limit, all channels which are not “good” will immediately be considered as “open circuit”. Detection of an “open circuit” channel will result in a time-out before disabling of the affected channel.

Some users employ some special types of LEDs that have zener diode structure in parallel with the LED for ESD enhancement, thus enabling open circuit operation. When this type of LED goes open circuit, the effect is as if the LED forward voltage has increased, but no light is emitted. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, allowing all other LEDs in the string to remain functional. Care should be taken in this case that the boost OVP limit and SCP limit are set properly, in order to assure that multiple failures on one string do not cause all other good channels to be faulted out. This is due to the increased forward voltage of the faulty channel making all other channels look as if they have LED shorts. See Table 3 for details for responses to fault conditions.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the output voltage and keeps the voltage at a safe level. The OVP threshold is set as Equation 9:

$$OVP = 1.22V \times (R_{UPPER} + R_{LOWER})/R_{LOWER} \quad \text{(EQ. 9)}$$

These resistors should be large to minimize the power loss. For example, a 1MkΩ R_{UPPER} and 30kΩ R_{LOWER} sets OVP to 41.2V. Large OVP resistors also allow C_{OUT} discharges slowly during the PWM Off time. Parallel capacitors should also be placed across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high value resistors.

Undervoltage Lockout

If the input voltage falls below the UVLO level of 2.5V, the device will stop switching and be reset. Operation will restart only if the device is re-powered and re-enabled once the input voltage is back in the normal operating range.

Over-Temperature Protection (OTP)

The ISL97682, ISL97683, ISL97684 over-temperature protection threshold is set to +150°C. Each time this is reached, the boost will stop switching and the output current sources will be switched off.

For the extensive fault protection conditions, please refer to Figure 25 and Table 3 for details.

chanhvinh.com

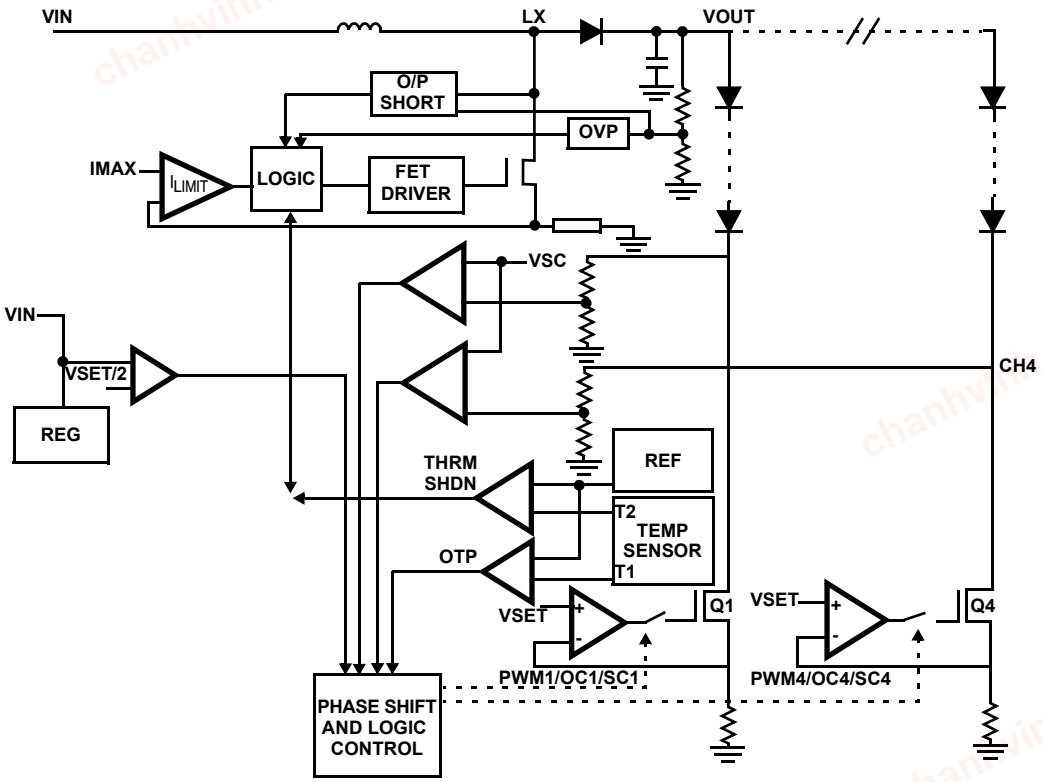


FIGURE 25. SIMPLIFIED FAULT PROTECTIONS

TABLE 3. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
1	CH1 Short Circuit	Over-Temperature Protection limit (OTP) not triggered and CH1 < 4.4V	CH1 ON and burns power	CH2 through CH4 Normal	Highest VF of CH2 through CH4
2	CH1 Short Circuit	OTP triggered but VCH1 < 4.4V	All channels switched off until power-cycled.		Highest VF of CH2 through CH4
3	CH1 Short Circuit	OTP not triggered but CH1 > 4.4V	CH1 faults out after 6 PWM cycle (7-18 in direct PWM) time-out	CH2 through CH4 Normal	Highest VF of CH2 through CH4
4	CH1 Open Circuit with infinite resistance	OTP not triggered and CH1 < 4.4V	V_{OUT} will ramp to OVP. CH1 will time-out after 6 PWM cycles (7-18 in direct PWM) and switch off. V_{OUT} will drop to normal level.	CH2 through CH4 Normal	Highest VF of CH2 through CH4
5	CH1 LED Open Circuit but has paralleled Zener	OTP not triggered and CH1 < 4.4V	CH1 remains ON and has highest VF, thus V_{OUT} increases	CH2 through CH4 ON, Q2 through Q4 burn power	VF of CH1
6	CH1 LED Open Circuit but has paralleled Zener	OTP triggered but CH1 < 4.4V	CH1 goes off	Same as CH1	VF of CH1
7	CH1 LED Open Circuit but has paralleled Zener	OTP not triggered but CHx > 4.4V	CH1 remains ON and has highest VF, thus V_{OUT} increases.	V_{OUT} increases then CH-X switches OFF after 6 PWM cycles. This is an unwanted shut off and can be prevented by setting OVP at an appropriate level.	VF of CH1
8	Channel-to-Channel ΔVF too high	OTP triggered but CHx < 4.4V	All channels switched off until chip cooled		Highest VF of CH1 through CH4
9	Output LED stack voltage too high	$V_{OUT} > V_{OVP}$	Driven with normal current. Any channel that has insufficient headroom will fault out after 6 PWM cycle (7-18 in direct PWM) time-out.		Highest VF of CH1 through CH4

chanhvinh.com

Components Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On-time is equal to the change of inductor current during the switching regulator Off-time. Since the voltage across an inductor is as shown in Equation 10:

$$V_L = L \times \Delta I_L / \Delta t \quad \text{(EQ. 10)}$$

and ΔI_L @ On = ΔI_L @ Off, therefore:

$$(V_I - 0)/L \times D \times t_S = (V_O - V_D - V_I)/L \times (1 - D) \times t_S \quad \text{(EQ. 11)}$$

where D is the switching duty cycle defined by the turn-on time over the switching periods. V_D is a Schottky diode forward voltage that can be neglected for approximation.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle as Equations 12 and 13:

$$V_O/V_I = 1/(1 - D) \quad \text{(EQ. 12)}$$

$$D = (V_O - V_I)/V_O \quad \text{(EQ. 13)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, thereby improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

It is recommended that an input capacitor of at least 10µF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

Inductor

The selection of the inductor should be based on its maximum and saturation current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance and stability.

The inductor's maximum current capability must be adequate enough to handle the peak current at the worst case condition. Additionally if an inductor core is chosen with too low a current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the Off-period, expressed in Equation 14:

$$IL_{peak} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_{SW})] \quad \text{(EQ. 14)}$$

The choice of 85% is just an average term for the efficiency approximation. The first term is the average current, which is inversely proportional to the input voltage. The second term is the inductor current change, which is inversely proportional to L and F_{SW} as a result, for a given switching.

Applications

Low Voltage Operations

The ISL97682, ISL97683, ISL97684 VIN pin can be separately biased from the LEDs power input to allow low voltage operation. For systems that have only single supply, VOUT can be tied to the driver VIN pin to allow initial start-up; see Figure 26. The circuit works as follows; when the input voltage is available and the device is not enabled, the V_{OUT} follows V_{IN} with a Schottky diode voltage drop. The V_{OUT} bootstrapped to VIN pin allows an initial start-up once the part is enabled. Once the driver starts up with V_{OUT} regulating to the target, the VIN pin voltage also increases. As long as the V_{OUT} does not exceed 26.5V and the extra power loss on VIN is acceptable, this configuration can be used for input voltage as low as 3.0V. For systems where a single input supply of 4V to 5.5V is available, the VIN pin can be shorted to VDC, allowing a slight gain in efficiency due to bypassing the internal LDO.

For systems that have dual supplies, the VIN pin can be biased from 5V to 12V. The input voltage can be as low as 2.7V without the limitations previously mentioned; see Figure 27.

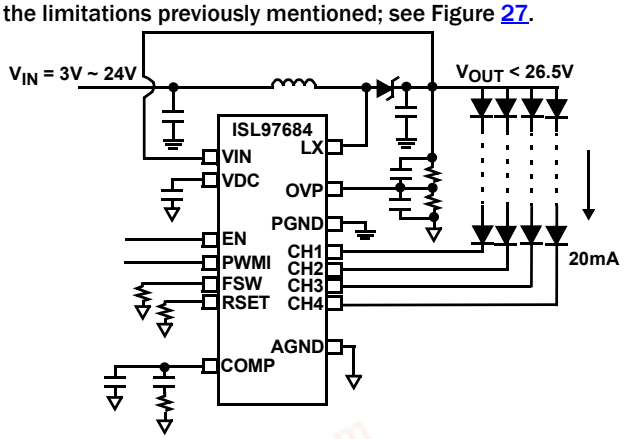


FIGURE 26. SINGLE SUPPLY 3V OPERATION

chanhvinh.com

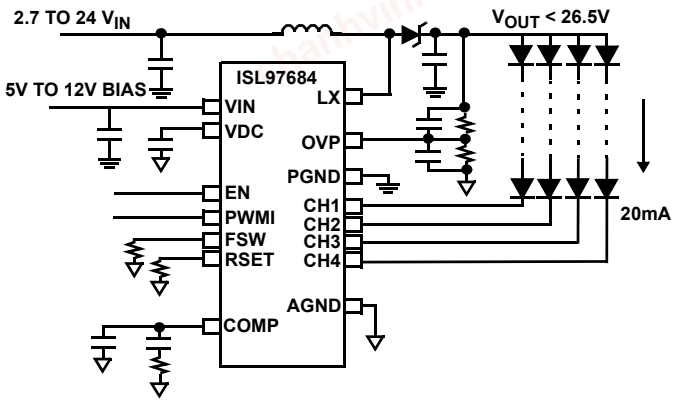


FIGURE 27. DUAL SUPPLIES 2.7V OPERATION

chanhvinh.com

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
September 19, 2017	FN7689.2	Applied new header/footer. Added Related Literature Updated Ordering Information table. Added VHEADROOM_RANGE spec to EC table. Added Note 9. In “Current Matching and Current Accuracy” on page 10 updated 2nd sentence in paragraph 2 for clarification. Replaced Products section with About Intersil.
February 3, 2012	FN7689.1	On page 1, RC values on COMP pin in Figure 1A and 1B were both updated with values of 10kΩ, 8.2nF, and 33pF. On page 4, the pin description for Pin#4 was updated with new numbers to set boost switching frequency and PFM mode. In Table 2 on page 12, the FSW pin setting was updated with new numbers to set boost switching frequency and PFM mode.
March 11, 2011	FN7689.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

© Copyright Intersil Americas LLC 2011-2017. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

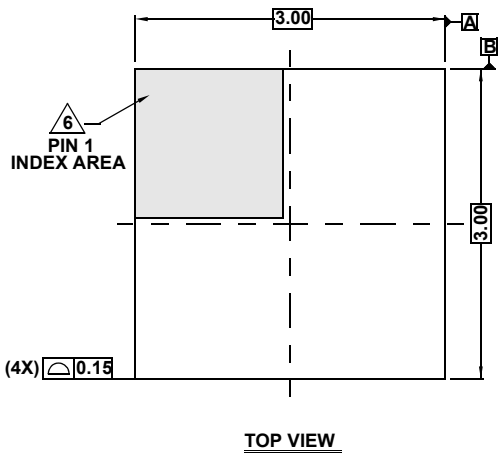
chanhvinh.com

Package Outline Drawing

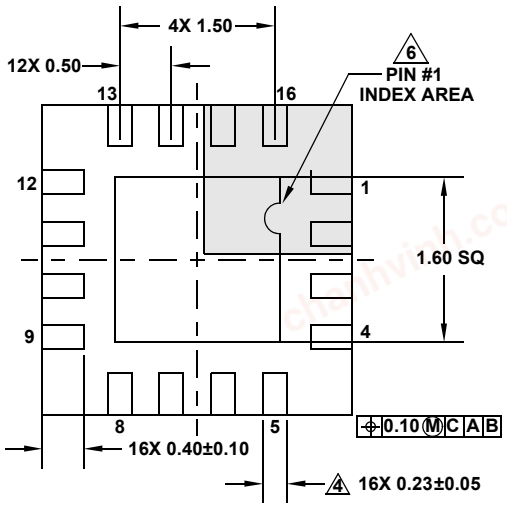
For the most recent package outline drawing, see L16.3x3D.

L16.3x3D

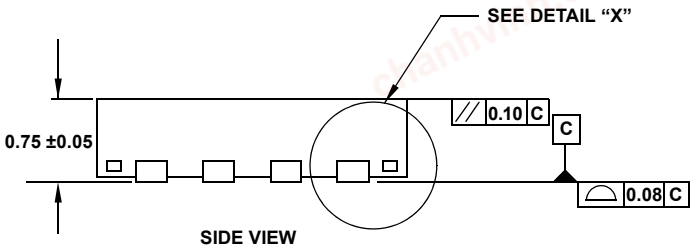
16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 3/10



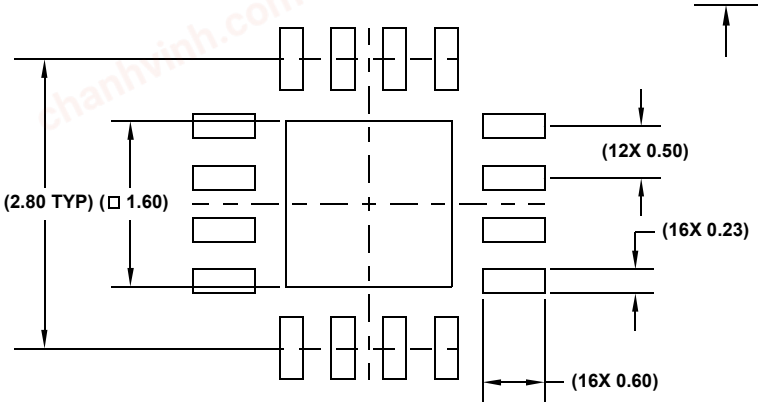
TOP VIEW



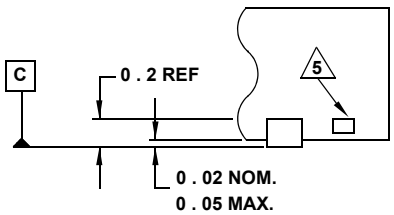
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.