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ISL91110IR

High Efficiency Buck-Boost Regulator with 5.4A Switches

FN8709
Rev 0.00
April 17, 2015

The ISL91110IR is a high-current buck-boost switching regulator for systems using new battery chemistries. It uses Intersil's proprietary buck-boost algorithm to maintain voltage regulation while providing excellent efficiency and very low output voltage ripple when the input voltage is close to the output voltage.

The ISL91110IR is capable of delivering at least 2A continuous output current (V_{OUT} = 3.3V) over a battery voltage range of 2.5V to 4.35V. This maximizes the energy utilization of advanced single-cell Li-ion battery chemistries that have significant capacity left at voltages below the system voltage. Its fully synchronous low ON-resistance 4-switch architecture and a low quiescent current of only 35µA optimize efficiency under all load conditions.

The ISL91110IR supports standalone applications with a fixed 3.3V or 3.5V output voltage or adjustable output voltage with an external resistor divider. Output voltages as low as 1V or as high as 5.2V are supported.

The ISL91110IR requires only a single inductor and very few external components. Power supply solution size is minimized by its 2.5MHz switching frequency, allowing small size external components.

The ISL91110IR is available in a 4mmx4mm, 20 Ld TQFN package.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	ADJ or FIXED V_{OUT}
ISL91110IRNZ-T	3.3
ISL91110IRNZ-T7A	3.3
ISL91110IR2AZ-T	3.5
ISL91110IR2AZ-T7A	3.5
ISL91110IRAZ-T	ADJ
ISL91110IRAZ-T7A	ADJ

Features

- Accepts input voltages above or below regulated output voltage
- Automatic and seamless transitions between buck and boost modes
- Input voltage range: 1.8V to 5.5V
- Output current: up to 2A (PVIN = 3.4V, V_{OUT} = 5V)
- Output current: up to 2A (PVIN = 2.5V, V_{OUT} = 3.3V)
- Burst current: up to 3A (PVIN = 2.9V, V_{OUT} = 3.3V, t_{ON} < 600µs, t = 4.6ms)
- High efficiency: up to 95%
- 35µA quiescent current maximizes light load efficiency
- 2.5MHz switching frequency minimizes external component size
- Fully protected for short-circuit, over-temperature and undervoltage
- Small 4mmx4mm 20 Ld TQFN package

Applications

- Smartphones and tablet PCs
- Wireless communication devices
- Optical modules networking equipment

Related Literature

UG022, "ISL91110IRx-EVZ Evaluation Boards User Guide"

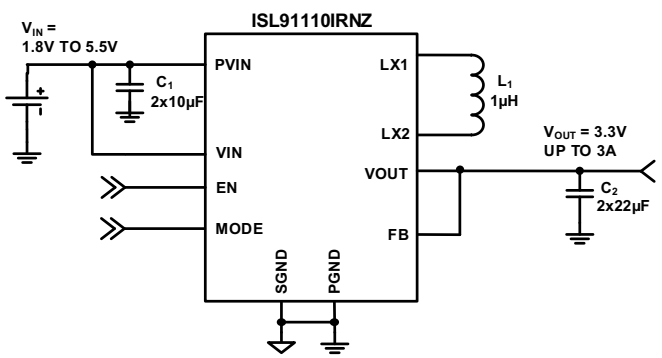


FIGURE 1. TYPICAL APPLICATION: V_{OUT} = 3.3V

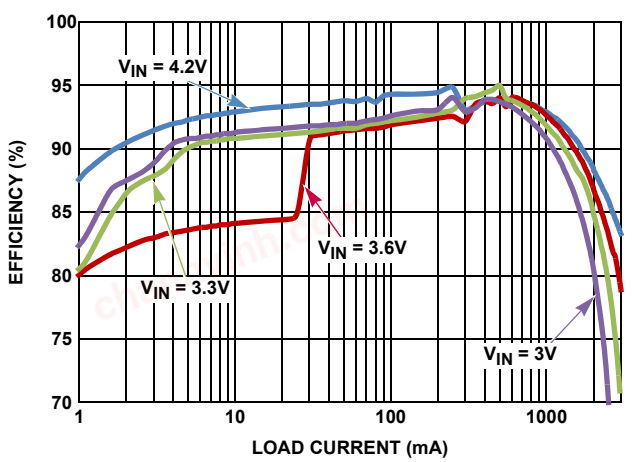


FIGURE 2. EFFICIENCY: V_{OUT} = 3.3V, T_A = +25°C

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Block Diagram

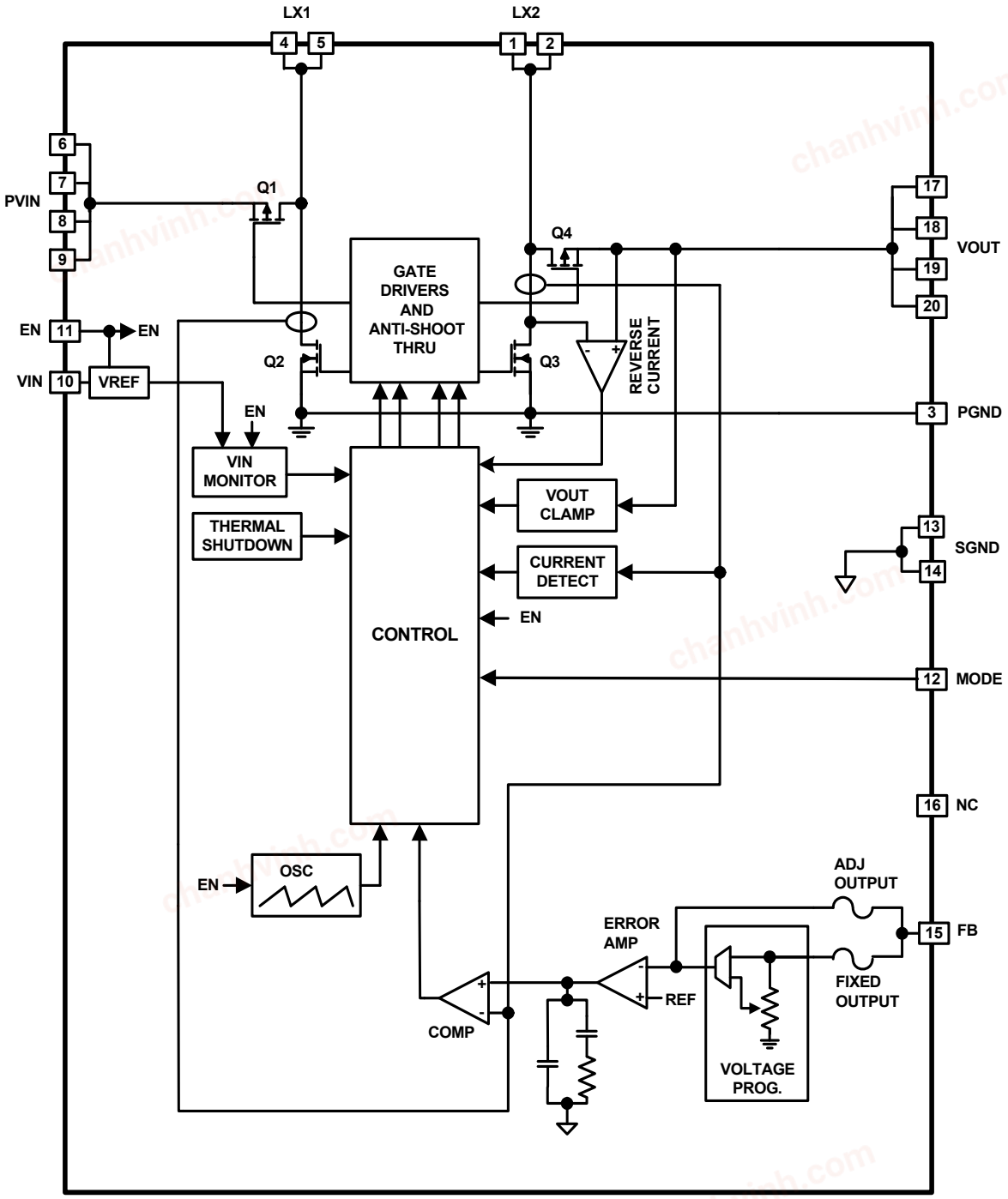
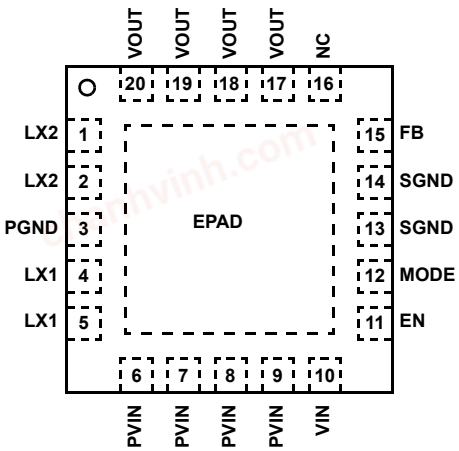


FIGURE 3. BLOCK DIAGRAM

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Pin Configuration

ISL91110IR
(20 LD, 4X4 TQFN)
TOP VIEW



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
6, 7, 8, 9,	PVIN	Power input; Range: 1.8V to 5.5V. Connect 2x10µF capacitors to PGND.
4, 5	LX1	Inductor connection, input side
3	PGND	Power ground for high switching current
1, 2	LX2	Inductor connection, output side
17, 18, 19, 20	VOUT	Buck-boost regulator output; Connect 2x22µF capacitors to PGND for V_{OUT} = 3.3V and 3.5V applications, and 2x47µF capacitors to PGND for V_{OUT} = 4.5V and 5V applications.
12	MODE	Logic input, HIGH for auto PFM mode. LOW for forced PWM operation. Also, this pin can be used with an external clock sync input. Range: 2.75MHz to 3.25MHz. Do not leave floating.
10	VIN	Supply input; Range: 1.8V to 5.5V.
11	EN	Logic input, drive HIGH to enable device. Do not leave floating.
13, 14	SGND	Analog ground pin
15	FB	Voltage feedback pin, connect directly to the VOUT pin for fixed output voltage versions.
16	NC	No connect pin
	Epad	Thermal pad, connect to PGND

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	OUTPUT VOLTAGE (V)	TEMP RANGE (°C)	PACKAGE Tape and Reel (RoHS Compliant)	PKG. DWG. #
ISL91110IRNZ-T	91110N	3.3	-40 to +85	20 Ld 4x4 TQFN	L20.4X4C
ISL91110IRNZ-T7A	91110N	3.3	-40 to +85	20 Ld 4x4 TQFN	L20.4X4C
ISL91110IR2AZ-T	911102	3.5	-40 to +85	20 Ld 4x4 TQFN	L20.4X4C
ISL91110IR2AZ-T7A	911102	3.5	-40 to +85	20 Ld 4x4 TQFN	L20.4X4C
ISL91110IRAZ-T	91110A	ADJ	-40 to +85	20 Ld 4x4 TQFN	L20.4X4C
ISL91110IRAZ-T7A	91110A	ADJ	-40 to +85	20 Ld 4x4 TQFN	L20.4X4C
ISL91110IRN-EVZ	Evaluation Board for ISL91110IRNZ				
ISL91110IR2A-EVZ	Evaluation Board for ISL91110IR2AZ				
ISL91110IRA-EVZ	Evaluation Board for ISL91110IRAZ				

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL91110IR. For more information on MSL please see techbrief TB363.

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Absolute Maximum Ratings

PVIN, VIN . . . . . -0.3V to 6.5V
LX1, LX2. . . . . -0.3V to 6.5V
FB (Adjustable Version) . . . . . -0.3V to 2.7V
FB (Fixed V_{OUT} Versions) . . . . . -0.3V to 6.5V
SGND, PGND . . . . . -0.3V to 0.3V
All Other Pins . . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114E). 3kV
Machine Model (Tested per JESD22-A115-A). 200V
Charge Device Model 2kV
Latch-up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld 4x4 TQFN Package (Notes 4, 5). . . .	39	4

Maximum Junction Temperature . . . . . +125°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range . . . . . 1.8V to 5.5V
Max Load Current (V_{IN} = 3.4V, V_{OUT} = 5V). 2ADC
Max Load Current (V_{IN} = 2.5V, V_{OUT} = 3.3V) 2ADC
Max Load Current (V_{IN} = 2.9V, V_{OUT} = 3.3V, t_{ON} = 600µs, t = 4.6ms) 3A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Analog Specifications

V_{IN} = V_{PVIN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, L1 = 1µH, C1 = 2x10µF, C2 = 2x22µF, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V) unless specified otherwise.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS
POWER SUPPLY						
V_{IN}	Input Voltage Range		**1.8**		**5.5**	V
V_{UVLO}	V_{IN} Undervoltage Lockout Threshold	Rising		1.725	**1.775**	V
		Falling	**1.550**	1.650		V
I_{VIN}	V_{IN} Supply Current	PFM mode, no external load on V_{OUT} (Note 8)		35	**60**	µA
I_{SD}	V_{IN} Supply Current, Shutdown	EN = SGND, V_{IN} = 3.6V		0.05	**1.0**	µA
OUTPUT VOLTAGE REGULATION						
V_{OUT}	Output Voltage Range	ISL91110IRAZ, I_{OUT} = 100mA, V_{IN} = 3.6V	**1.00**		**5.20**	V
	Output Voltage Accuracy	V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 0mA, PWM mode	**-2**		**+2**	%
		V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PFM mode	**-3**		**+4**	%
V_{FB}	FB Pin Voltage Regulation	For adjustable output version, V_{IN} = 3.6V	**0.783**	0.80	**0.813**	V
I_{FB}	FB Pin Bias Current	For adjustable output version			**20**	nA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation, PWM Mode	I_{OUT} = 500mA, V_{OUT} = 3.3V, V_{IN} step from 2.3V to 5.5V		±5		mV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation, PWM Mode	V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} step from 0mA to 1000mA		±0.005		mV/mA
$\Delta V_{OUT}/\Delta V_I$	Line Regulation, PFM Mode	I_{OUT} = 100mA, V_{OUT} = 3.3V, V_{IN} step from 2.3V to 5.5V		±12.5		mV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation, PFM Mode	V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} step from 0mA to 100mA		±0.4		mV/mA
V_{CLAMP}	Output Voltage Clamp	Rising	**5.25**		**5.95**	V
	Output Voltage Clamp Hysteresis			400		mV
DC/DC SWITCHING SPECIFICATIONS						
f_{SW}	Oscillator Frequency		**2.1**	2.50	**2.9**	MHz
t_{ONMIN}	Minimum On Time			80		ns
$I_{PFETLEAK}$	LX1 Pin Leakage Current	V_{IN} = 3.6V	**-1**		**1**	µA
$I_{NFETLEAK}$	LX2 Pin Leakage Current	V_{IN} = 3.6V	**-1**		**1**	µA

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Analog Specifications

$V_{IN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, L1 = 1µH, C1 = 2x10µF, C2 = 2x22µF, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V) unless specified otherwise. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS
SOFT-START AND SOFT DISCHARGE						
t_{SS}	Soft-start Time	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in buck mode. $V_{IN} = 4V$, $V_{OUT} = 3.3V$, $I_O = 200mA$		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in boost mode. $V_{IN} = 2V$, $V_{OUT} = 3.3V$, $I_O = 200mA$		2		ms
R_{DISCHG}	V_{OUT} Soft-discharge ON-resistance	$EN < V_{IL}$		120		Ω
POWER MOSFET						
R_{DSON_P}	P-channel MOSFET ON-resistance	$V_{IN} = 3.6V$, $I_O = 200mA$		47		mΩ
		$V_{IN} = 2.5V$, $I_O = 200mA$		62		mΩ
R_{DSON_N}	N-channel MOSFET ON-resistance	$V_{IN} = 3.6V$, $I_O = 200mA$		40		mΩ
		$V_{IN} = 2.5V$, $I_O = 200mA$		55		mΩ
I_{PK_LMT}	P-channel MOSFET Peak Current Limit		**4.9**	5.4	**5.9**	A
PFM/PWM TRANSITION						
	Load Current Threshold, PFM to PWM	$V_{IN} = 3.6V$, $V_{OUT} = 3.3V$		200		mA
	Load Current Threshold, PWM to PFM	$V_{IN} = 3.6V$, $V_{OUT} = 3.3V$		75		mA
	Thermal Shutdown			155		°C
	Thermal Shutdown Hysteresis			30		°C
LOGIC INPUTS						
I_{LEAK}	Input Leakage	$V_{IN} = 3.6V$		0.05	**1**	µA
V_{IH}	Input HIGH Voltage	$V_{IN} = 3.6V$	**1.4**			V
V_{IL}	Input LOW Voltage	$V_{IN} = 3.6V$			**0.4**	V

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Typical values are for $T_A = +25°C$ and $V_{IN} = 3.6V$.
8. Quiescent current measurements are taken when the output is not switching.

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Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 2x10µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A.

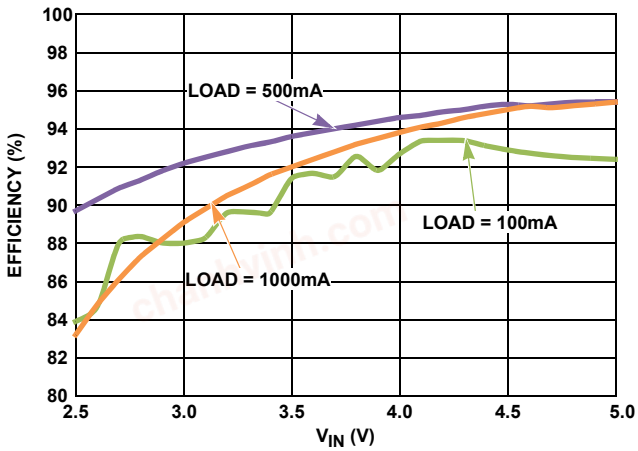


FIGURE 4. EFFICIENCY vs INPUT VOLTAGE (V_{OUT} = 5V)

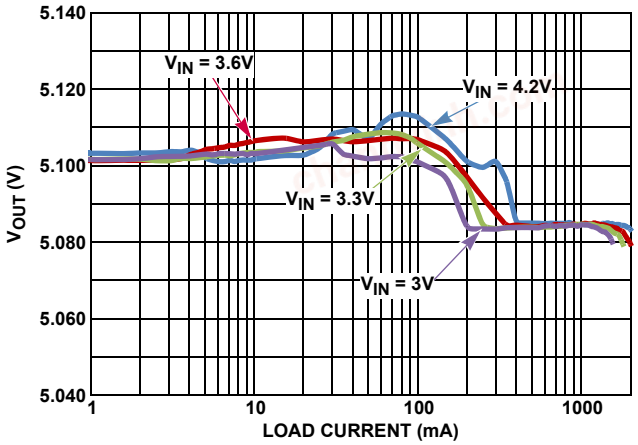


FIGURE 5. OUTPUT VOLTAGE vs LOAD CURRENT (V_{OUT} = 5V)

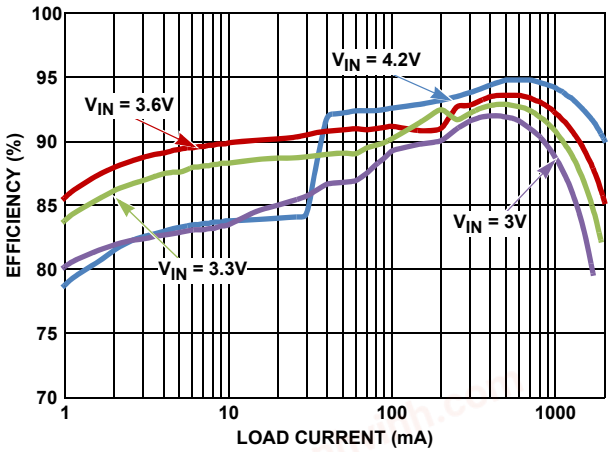


FIGURE 6. EFFICIENCY: V_{OUT} = 5V, T_A = +25°C

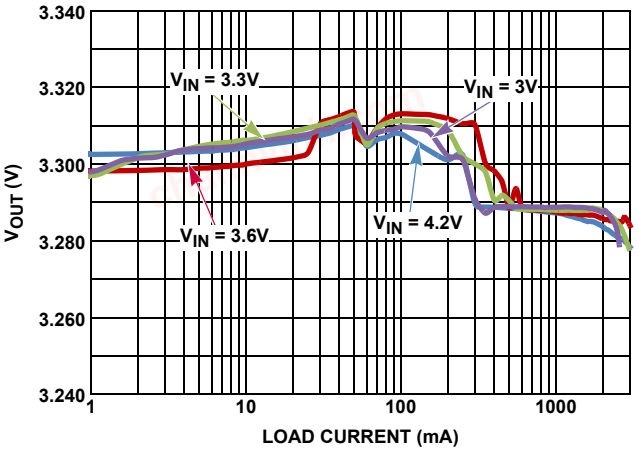


FIGURE 7. OUTPUT VOLTAGE vs LOAD CURRENT (V_{OUT} = 3.3V)

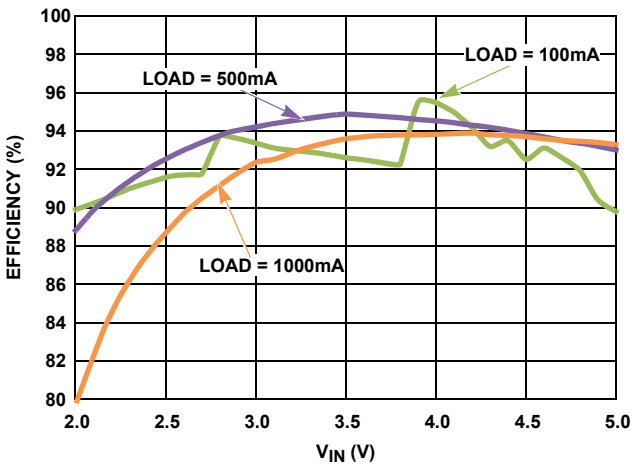


FIGURE 8. EFFICIENCY vs INPUT VOLTAGE (V_{OUT} = 3.3V)

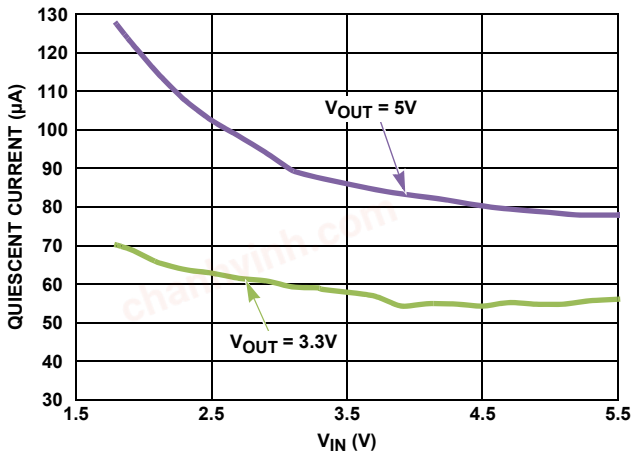


FIGURE 9. QUIESCENT CURRENT vs INPUT VOLTAGE (MODE = HIGH)

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Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 2x10µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A. **(Continued)**

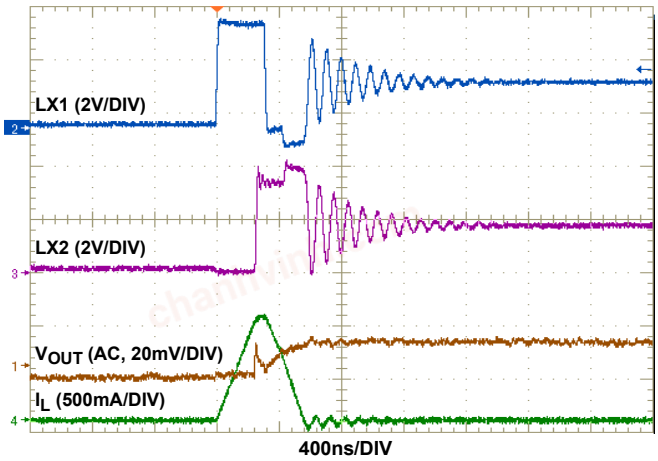


FIGURE 10. STEADY STATE OPERATION IN PFM (V_{IN} = 4V, V_{OUT} = 3.3V, NO LOAD)

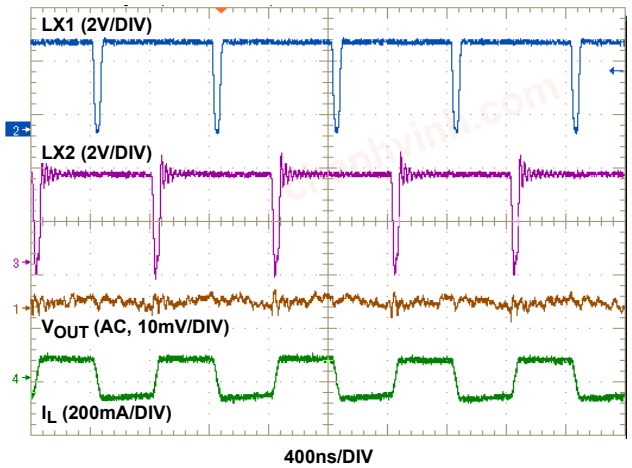


FIGURE 11. STEADY STATE OPERATION IN PWM (V_{IN} = 4V, V_{OUT} = 3.3V, NO LOAD)

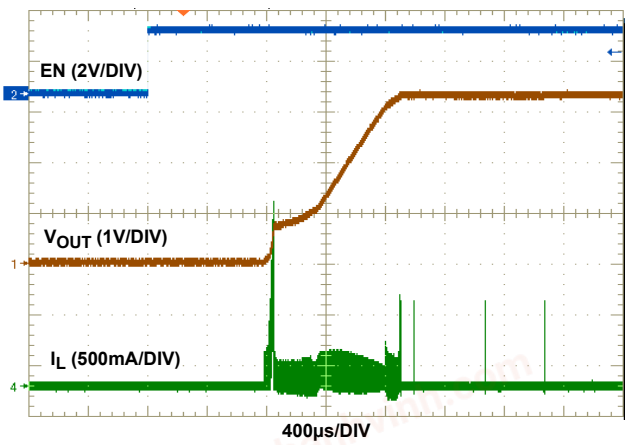


FIGURE 12. SOFT-START (V_{IN} = 3.6V, V_{OUT} = 3.3V, NO LOAD)

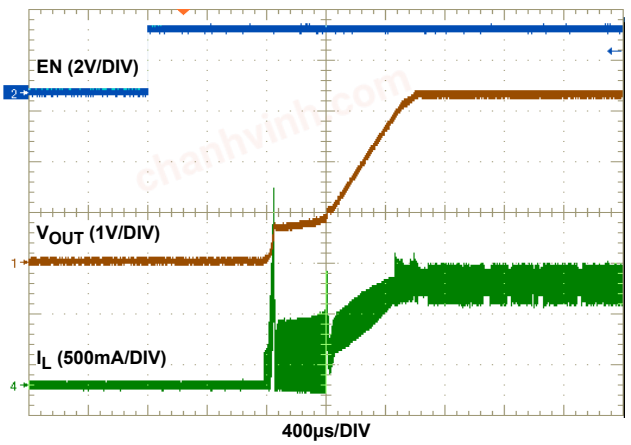


FIGURE 13. SOFT-START (V_{IN} = 3.6V, V_{OUT} = 3.3V, 1A RLOAD)

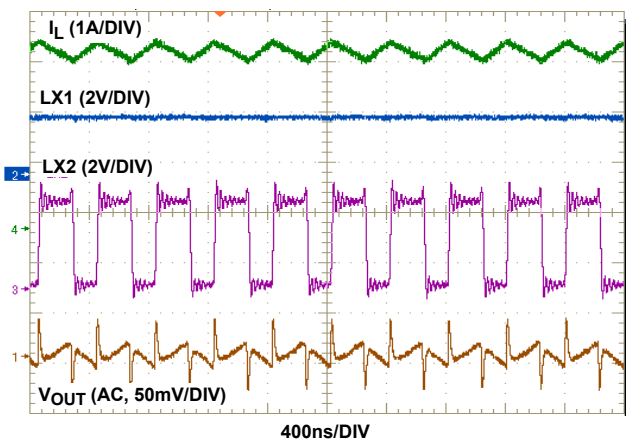


FIGURE 14. STEADY STATE OPERATION (V_{IN} = 2.5V, V_{OUT} = 3.3V, 2A LOAD)

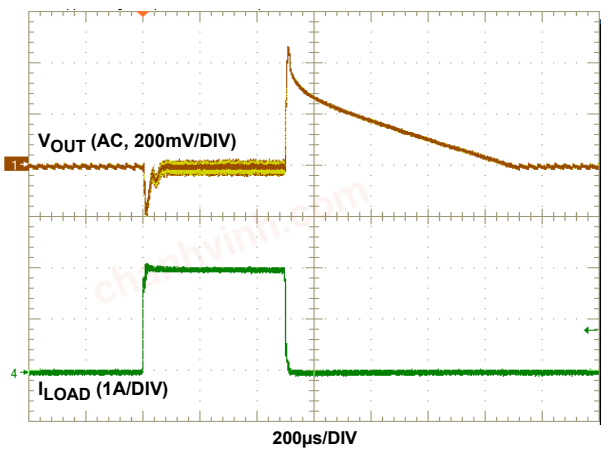


FIGURE 15. 0A TO 2A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 3.3V)

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Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 2x10µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A. **(Continued)**

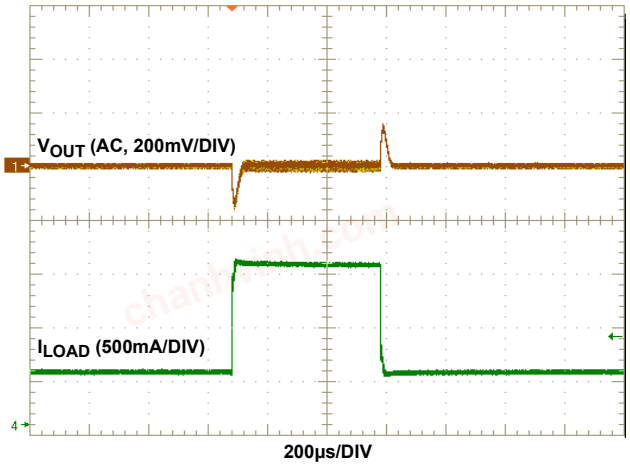


FIGURE 16. 0.5A TO 1.5A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 3.3V)

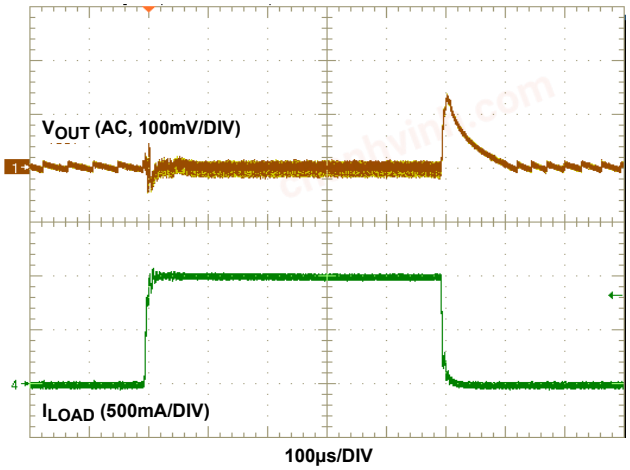


FIGURE 17. 0A TO 1A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 3.3V)

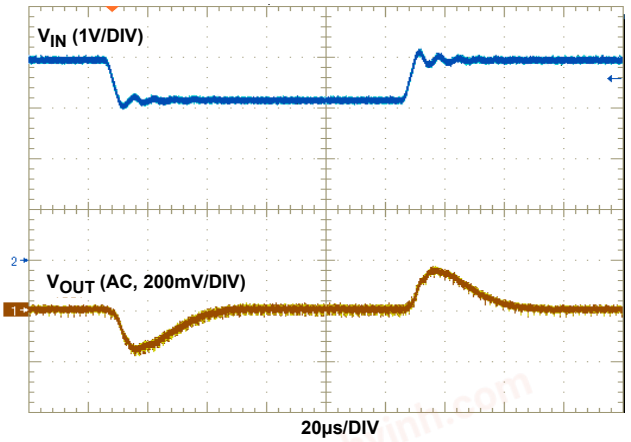


FIGURE 18. 4V TO 3.2V LINE TRANSIENT (V_{OUT} = 3.3V, LOAD = 1A)

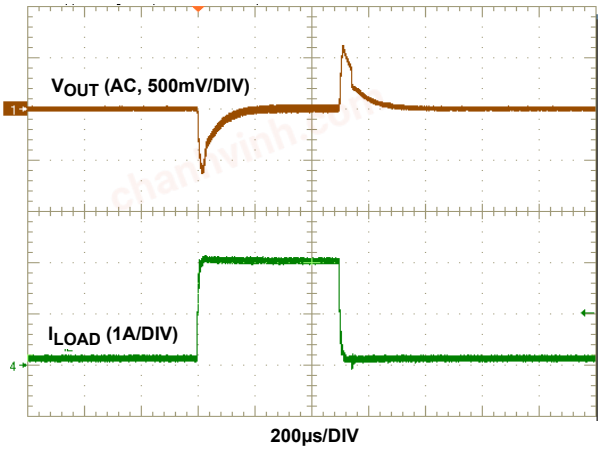


FIGURE 19. 0.1A TO 2A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 5V)

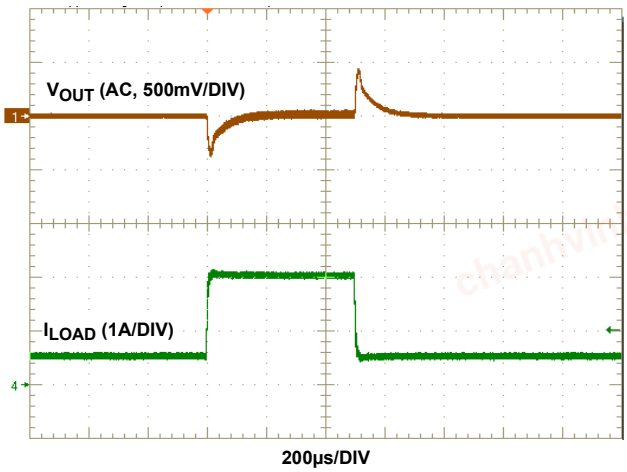


FIGURE 20. 0.5A TO 2A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 5V)

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Functional Description

Functional Overview

Refer to the "Block Diagram" on page 2. The ISL91110IR implements a complete buck boost switching regulator, with PWM controller, internal switches, references, protection circuitry and control inputs.

The PWM controller automatically switches between buck and boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads.

Internal Supply and References

Referring to the "Block Diagram" on page 2, the ISL91110IR provides four power input pins. The PVIN pin supplies input power to the DC/DC converter, while the VIN pin provides operating voltage source required for stable V_{REF} generation. Separate ground pins (SGND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

The device is enabled by asserting the EN pin HIGH. Driving EN LOW invokes a power-down mode, where most internal device functions are disabled.

Soft Discharge

When the device is disabled by driving EN LOW, an internal resistor between VOUT and SGND is activated to slowly discharge the output capacitor. This internal resistor has a typical 120Ω resistance.

POR Sequence and Soft-start

Asserting the EN pin HIGH allows the device to power-up. A number of events occur during the start-up sequence. The internal voltage reference powers up and stabilizes. The device then starts to operate. There is a typical 1ms delay between assertion of the EN pin and the start of switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input in-rush currents. During soft-start, the reference voltage is ramped to provide a ramping V_{OUT} voltage. While the output voltage is lower than approximately 20% of the target output voltage, switching frequency is reduced to a fraction of the normal switching frequency to aid in producing low duty cycles necessary to avoid input in-rush current spikes. Once the output voltage exceeds 20% of the target voltage, switching frequency is increased to its nominal value.

When the target output voltage is higher than the input voltage, there will be a transition from buck mode to boost mode during the soft-start sequence. At the time of this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

The V_{OUT} ramp time is not constant for all operating conditions. Soft-start into boost mode will take longer than soft-start into buck mode. The total soft-start time into buck operating mode is typically 2ms, whereas the typical soft-start time into boost mode operating mode is typically 3ms. Increasing the load current will increase these typical soft-start times.

Short Circuit Protection

The ISL91110IR provides short-circuit protection by monitoring the feedback voltage. When feedback voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The P-channel MOSFET peak current limit remains active during this state.

Thermal Shutdown

A built-in thermal protection feature protects the ISL91110IR, if the die temperature reaches +155°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal shutdown mode. When the die temperature falls to +125°C (typical), the device will resume normal operation. When exiting thermal shutdown, the ISL91110IR will execute its soft-start sequence.

Buck-Boost Conversion Topology

The ISL91110IR operates in either buck or boost mode. When operating in conditions where PVIN is close to VOUT, ISL91110IR alternates between buck and boost mode as necessary to provide a regulated output voltage.

Figure 21 shows a simplified diagram of the internal switches and external inductor.

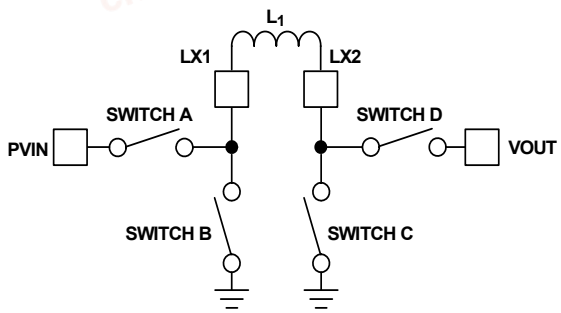


FIGURE 21. BUCK BOOST TOPOLOGY

PWM Operation

In buck PWM mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate as a synchronous buck converter when in this mode.

In boost PWM mode, Switch A remains closed and Switch B remains open. Switches C and D operate as a synchronous boost converter when in this mode.

PFM Operation

During PFM operation in buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation. During PFM operation in boost mode, the ISL91110IR closes Switch A and Switch C to ramp up the current in the inductor. When the inductor current reaches a certain threshold, the device turns off Switches A and C, then turns on Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

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In most operating conditions, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.

Operation With V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL91110IR will rapidly and smoothly switch from boost to buck mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

Output Voltage Programming

The ISL91110IR is available in fixed and adjustable output voltage versions. To use the fixed output version, the VOUT pin must be connected directly to FB.

In the adjustable output voltage version (ISL91110IRAZ), an external resistor divider is required to program the output voltage. The FB pin has very low input leakage current, so it is possible to use large value resistors (e.g., R_1 = 187kΩ and R_2 = 60.4kΩ for V_{OUT} = 3.3V) in the resistor divider connected to the FB input.

Applications Information

Component Selection

The fixed-output version of ISL91110IR requires only three external power components to implement the buck boost converter: an inductor, an input capacitor and an output capacitor.

The adjustable output version of ISL91110IR requires three additional components to program the output voltage, as shown in Figure 22. Two external resistors program the output voltage and a small capacitor is added to improve stability and response.

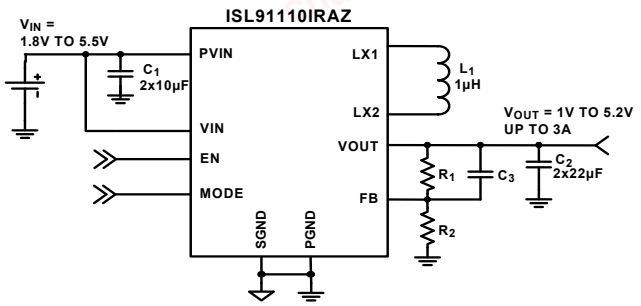


FIGURE 22. ADJUSTABLE OUTPUT APPLICATION

Output Voltage Programming, Adjustable Version

When VREF is connected to SGND, setting and controlling the output voltage of the ISL91110IRAZ (adjustable output version) can be accomplished by selecting the external resistor values.

Equation 1 can be used to derive the R_1 and R_2 resistor values:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

When designing a PCB, include a SGND guard band around the feedback resistor network to reduce noise and improve accuracy and stability. Resistors R_1 and R_2 should be positioned close to the FB pin.

Feed-Forward Capacitor Selection

A small capacitor (C3 in Figure 22) in parallel with resistor R_1 is required to provide the specified load and line regulation. The suggested value of this capacitor is 22pF for R_1 = 187kΩ. An NPO type capacitor is recommended.

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TABLE 2. INDUCTOR VENDOR INFORMATION

MANUFACTURER	MFR. PART NUMBER	DESCRIPTION	DIMENSION (mm)	WEBSITE
Coilcraft	XFL4020-102ME	1µH, 20%, DCR = 10.8mΩ (typ), Isat = 5.4A (typ)	4x4x2.1	www.coilcraft.com
Wurth Elektronik	7847730	1µH, 20%, DCR = 14mΩ (typ), Isat = 5.72A (typ)	4x4.5x3.2	www.we-online.com

Inductor Selection

An inductor with high frequency core material (e.g., ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with ≥5.4A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

PVIN and V_{OUT} Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 2x10µF. The recommended input capacitor must meet the following requirements: Minimum type is X5R, minimum voltage rating is 16V and minimum case size is 0603. The recommended output capacitor value is 2x22µF for 3.3V and 3.5V V_{OUT} applications and 2x47µF for 4.5V and 5V V_{OUT} applications. The recommended output capacitor must meet the following requirements: For 22µF, the minimum type is X5R, minimum voltage rating is 10V, and minimum case size is 0603. For 47µF, the minimum type is X5R, minimum voltage rating is 6.3V, and minimum case size is 0603.

TABLE 3. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
Taiyo Yuden	X5R	www.t-yuden.com
TDK	X5R	www.tdk.com

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL91110IR. The following are some general guidelines for the recommended layout:

1. The input and output capacitors should be positioned as close to the IC as possible.
2. The ground connections of the input and output capacitors should be kept as short as possible. The objective is to minimize the current loop between the ground pads of the input and output capacitors and the PGND pins of the IC. Use vias, if required, to take advantage of a PCB ground layer underneath the regulator.
3. The analog ground pin (SGND) should be connected to a large/low-noise ground plane on the top or an intermediate layer on the PCB, away from the switching current path of PGND. This ensures a low noise signal ground reference.
4. Minimize the trace lengths on the feedback loop to avoid switching noise pick-up. Vias should be avoided on the feedback loop to minimize the effect of board parasitic, particularly during load transients.

The LX1 and LX2 traces should be short and must be routed on the same layer as the IC.

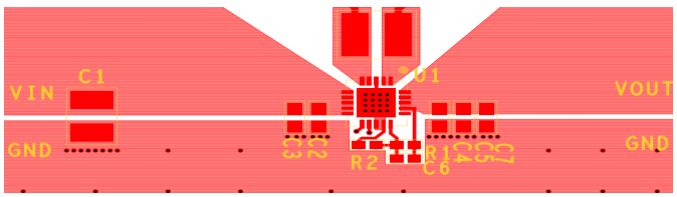


FIGURE 23. RECOMMENDED LAYOUT

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
April 17, 2015	FN8709.0	Initial Release

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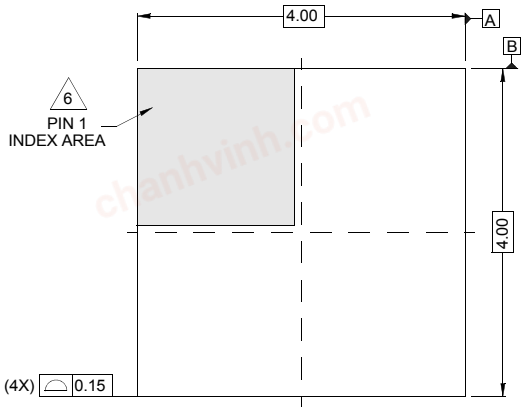
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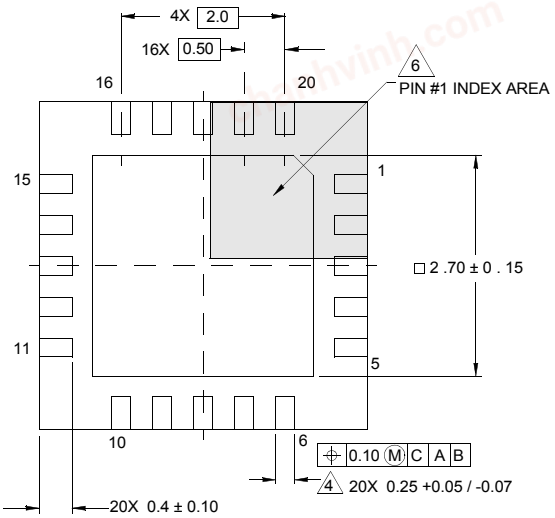
Package Outline Drawing

L20.4x4C

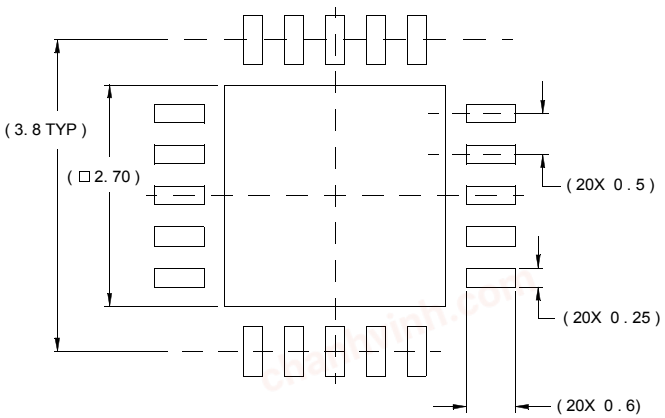
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 11/06



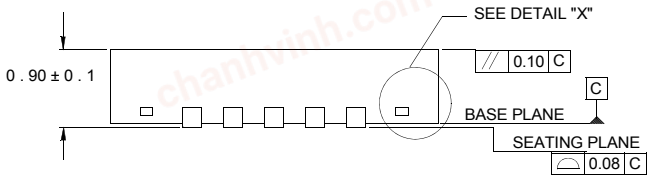
TOP VIEW



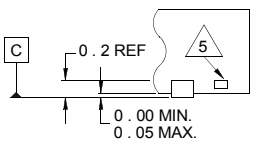
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.