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DATASHEET

ISL90842

Quad Digitally Controlled Variable Resistors Low Noise, Low Power I²C Bus, 256 Taps

FN8096
Rev 1.00
January 16, 2006

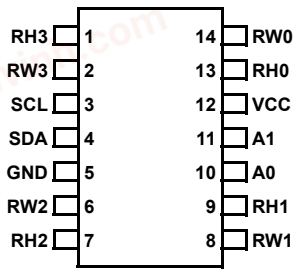
The ISL90842 integrates four digitally controlled potentiometers (DCP) configured as variable resistors on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I²C bus interface. Each potentiometer has an associated Wiper Register (WR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper.

The DCPs can be used as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

Pinout

ISL90842
(14 LEAD TSSOP)
TOP VIEW



Features

- Four variable resistors in one package
- 256 resistor taps - 0.4% resolution
- I²C serial interface
- Wiper resistance: 70Ω typical @ 3.3V
- Standby current <5µA max
- Power supply: 2.7V to 5.5V
- 50kΩ, 10kΩ total resistance
- 14 Lead TSSOP
- Pb-free plus anneal available (RoHS compliant)

Ordering Information

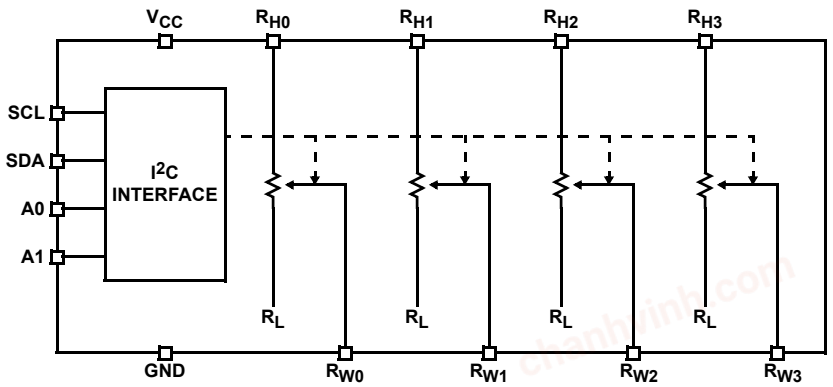
PART NUMBER	PART MARKING	RESISTANCE OPTION (Ω)	TEMP RANGE (°C)	PACKAGE
ISL90842UIV1427Z (Notes 1 & 2)	90842UI27Z	50K	-40 to +85	14 Ld TSSOP (Pb-Free)
ISL90842WIV1427Z (Notes 1 & 2)	90842WI27Z	10K	-40 to +85	14 Ld TSSOP (Pb-Free)

NOTES:

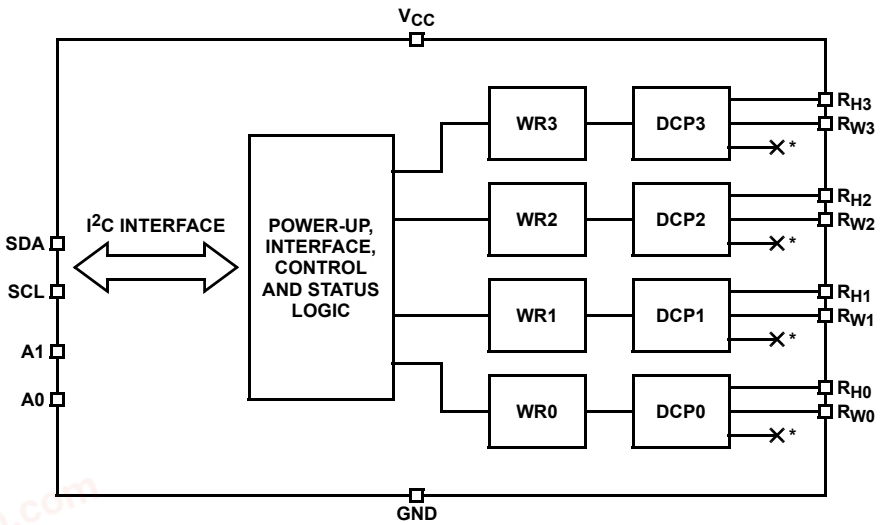
1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add “-TK” suffix for Tape and Reel.

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Functional Diagram



Block Diagram



* THE R_L PINS OF EACH DCP ARE LEFT FLOATING

Pin Descriptions

TSSOP PIN	SYMBOL	DESCRIPTION
1	RH3	“High” terminal of DCP3
2	RW3	“Wiper” terminal of DCP3
3	SCL	I^2C interface clock
4	SDA	Serial data I/O for the I^2C interface
5	GND	Device ground pin
6	RW2	“Wiper” terminal of DCP2
7	RH2	“High” terminal of DCP2
8	RW1	“Wiper” terminal of DCP1
9	RH1	“High” terminal of DCP1
10	A0	Device address for the I^2C interface
11	A1	Device address for the I^2C interface
12	VCC	Power supply pin
13	RH0	“High” terminal of DCP0
14	RW0	“Wiper” terminal of DCP0

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Absolute Maximum Ratings

Storage temperature . . . . . -65°C to +150°C
Voltage at any digital interface pin with respect to GND . . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . . . -0.3V to +6V
Voltage at any DCP pin with respect to GND. . . . . -0.3V to V_{CC}
Lead temperature (soldering, 10s). . . . . 300°C
I_W (10s) . . . . . ±6mA
Latchup . . . . . Class II, Level B at +85°C
ESD . . . . . >2kV Human Body Model

Recommended Operating Conditions

Industrial . . . . . -40°C to +85°C
V_{CC} . . . . . 2.7V to 5.5V
Power rating of each DCP 5mW
Wiper current of each DCP . . . . . ±3.0mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 1)	MAX	UNIT
R_{TOTAL}	R_H to R_W resistance	W option, wiper counter = 00h		10		kΩ
		U option, wiper counter = 00h		50		kΩ
	R_H to R_W resistance tolerance	Wiper counter = 00h	-20		+20	%
R_W	Wiper resistance	V_{CC} = 3.3V @ 25°C, wiper current = V_{CC}/R_{TOTAL}		70	200	Ω
$C_H/C_L/C_W$	Potentiometer capacitance (Note 15)			10/10/25		pF
I_{LkgDCP}	Leakage on DCP pins (Note 15)	Voltage at pin from GND to V_{CC}		0.1	1	µA
RESISTOR MODE (Measurements between R_Wi and R_Hi, i = 0, 1, 2 or 3)						
RINL (Note 5)	Integral non-linearity	DCP register set between 20 hex and FF hex; monotonic over all tap positions	-1		1	MI (Note 2)
RDNL (Note 4)	Differential non-linearity		-0.5		0.5	MI (Note 2)
Roffset (Note 3)	Offset	U option	0	1	7	MI (Note 2)
		W option	0	0.5	2	MI (Note 2)
R_{MATCH} (Note 6)	DCP to DCP matching	Any two DCPs at the same tap position with the same terminal voltages	-2		2	MI (Note 2)
TC_R (Note 7)	Resistance temperature coefficient	DCP register set between 20 hex and FF hex		±45		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 1)	MAX	UNIT
I_{CC1}	V_{CC} supply current (volatile write/read)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)			1	mA
I_{SB}	V_{CC} current (standby)	V_{CC} = +5.5V, I^2C interface in standby state			5	µA
		V_{CC} = +3.6V, I^2C interface in standby state			2	µA
I_{LkgDig}	Leakage current, at pins A0, A1, SDA, and SCL	Voltage at pin from GND to V_{CC}	-10		10	µA

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Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

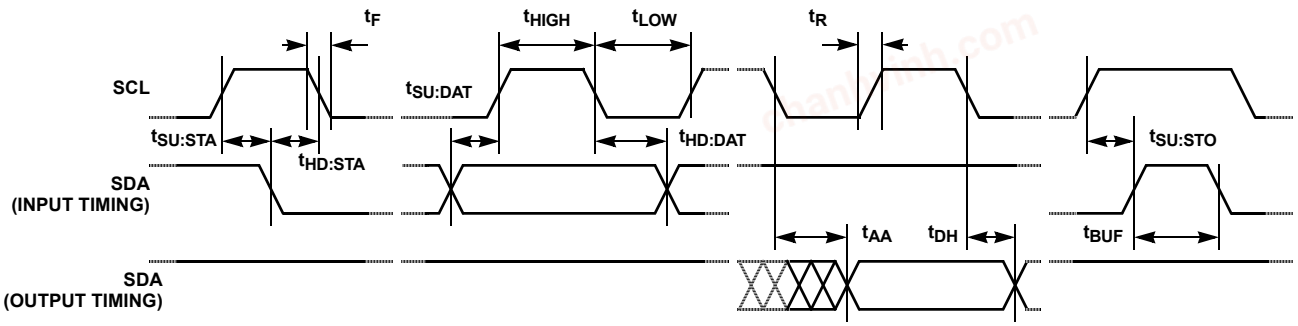
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 1)	MAX	UNIT
t_{DCP} (Note 8)	DCP wiper response time	SCL falling edge of last bit of DCP data byte to wiper change			1	µs
SERIAL INTERFACE SPECS						
V_{IL}	A1, A0, SDA, and SCL input buffer LOW voltage		-0.3		$0.3*V_{CC}$	V
V_{IH}	A1, A0, SDA, and SCL input buffer HIGH voltage		$0.7*V_{CC}$		$V_{CC}+0.3$	V
Hysteresis (Note 8)	SDA and SCL input buffer hysteresis		$0.05*V_{CC}$			V
V_{OL} (Note 8)	SDA output buffer LOW voltage, sinking 4mA		0		0.4	V
Cpin (Note 8)	A1, A0, SDA, and SCL pin capacitance				10	pF
f_{SCL}	SCL frequency				400	kHz
t_{IN} (Note 8)	Pulse width suppression time at SDA and SCL inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA} (Note 8)	SCL falling edge to SDA output data valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			900	ns
t_{BUF} (Note 8)	Time the bus must be free before the start of a new transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300			ns
t_{LOW}	Clock LOW time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START condition setup time	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START condition hold time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns
$t_{SU:DAT}$	Input data setup time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input data hold time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns
$t_{SU:STO}$	STOP condition hold time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP condition hold time for read, or volatile only write	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}	600			ns
t_{DH} (Note 8)	Output data hold time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns
t_R (Note 8)	SDA and SCL rise time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F (Note 8)	SDA and SCL fall time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 8)	Capacitive loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 8)	SDA and SCL bus pull-up resistor off-chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2~2.5kΩ For Cb = 40pF, max is about 15~20kΩ	1			kΩ

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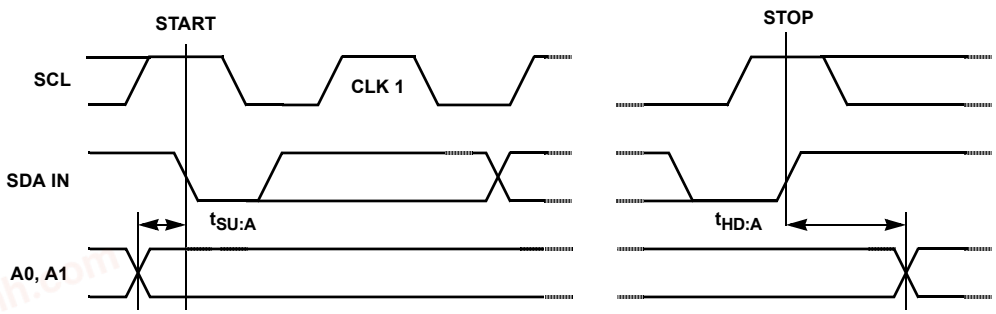
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 1)	MAX	UNIT
$t_{SU:A}$	A1 and A0 setup time	Before START condition	600			ns
$t_{HD:A}$	A1 and A0 hold time	After STOP condition	600			ns

SDA vs SCL Timing



A0 and A1 Pin Timing



NOTES:

1. Typical values are for T_A = 25°C and 3.3V supply voltage.
2. MI = $|R_{255} - R_0|$ / 255. R_{255} and R_0 are the measured resistances for the DCP register set to FF hex and 00 hex, respectively.
3. Roffset = R_{255} / MI, when measuring between R_W and R_H.
4. RDNL = $(R_i - R_{i-1})$ / MI, for i = 32 to 255.
5. RINL = $[R_i - (MI \bullet i) - R_0]$ / MI, for i = 32 to 255.
6. $R_{MATCH} = (R_{i,x} - R_{i,y})$ / MI, for i = 0 to 255, x = 0 to 3 and y = 0 to 3.
7. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$ for i = 32 to 255, T = -40°C to 85°C. Max ( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
8. This parameter is not 100% tested.

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Typical Performance Curves

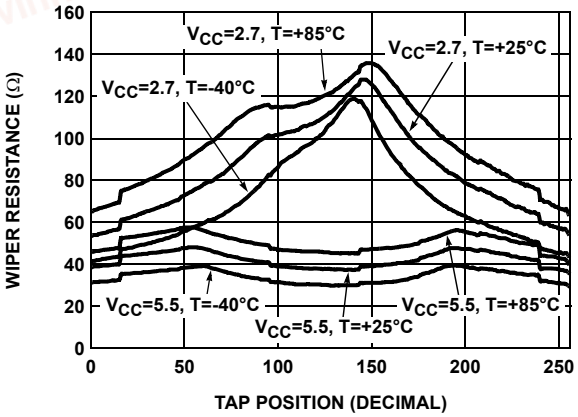


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(R_W) = V_{CC} / R_{TOTAL}] FOR 50kΩ (U)

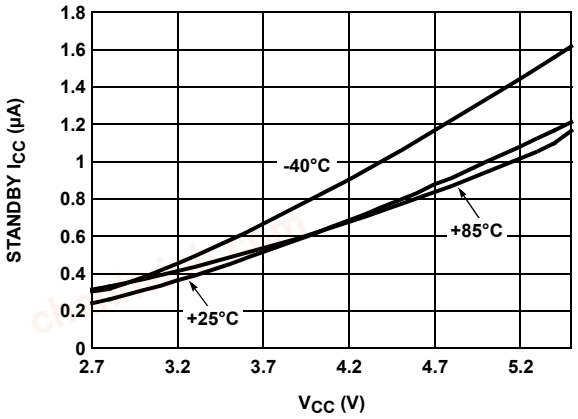


FIGURE 2. STANDBY I_{CC} vs Vcc

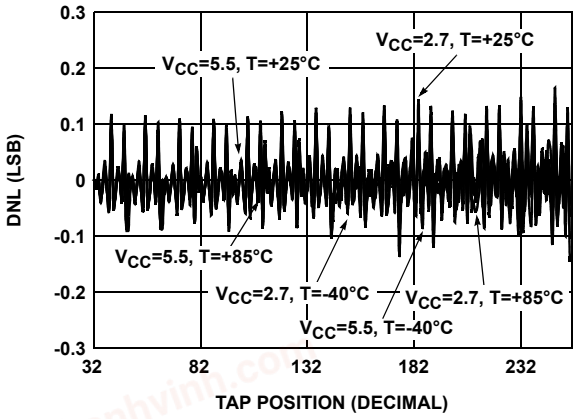


FIGURE 3. DNL vs TAP POSITION FOR 50kΩ (U)

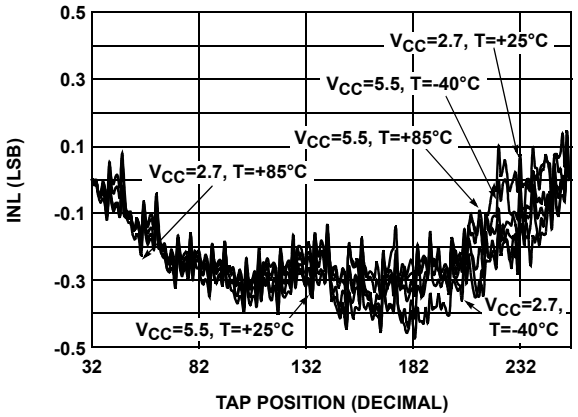


FIGURE 4. INL vs TAP POSITION FOR 50kΩ (U)

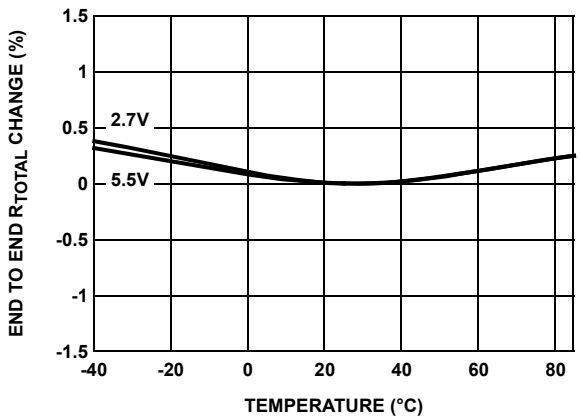


FIGURE 5. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

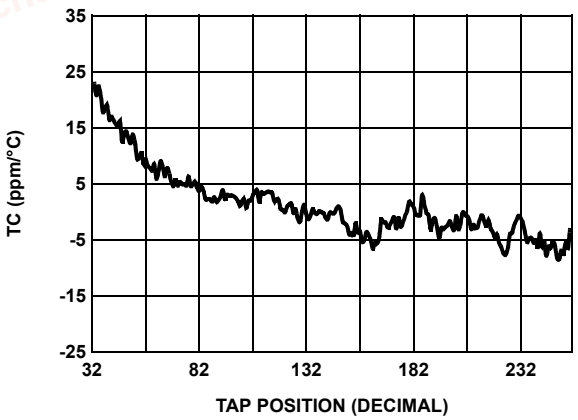


FIGURE 6. TC IN ppm

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Typical Performance Curves (Continued)

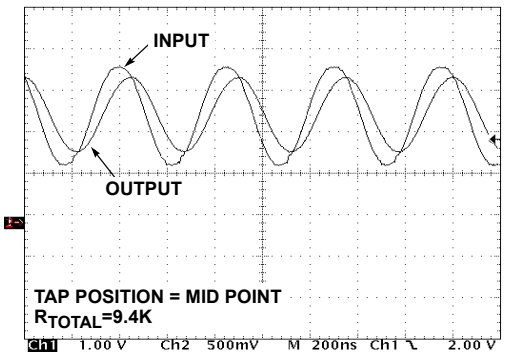


FIGURE 7. FREQUENCY RESPONSE (2.2MHz)

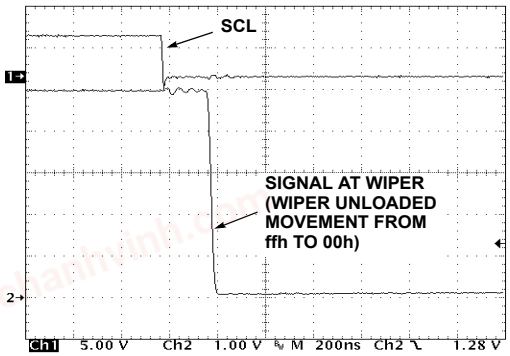


FIGURE 8. LARGE SIGNAL SETTLING TIME

Principles of Operation

The ISL90842 is an integrated circuit incorporating four DCPs with their associated registers, and an I^2C serial interface providing direct communication between a host and the DCPs.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer. The R_W pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR<7:0>: 00h), its wiper terminal (R_W) is closest to its R_L terminal. When the WR of a DCP contains all ones (WR<7:0>: FFh), its wiper terminal (R_W) is furthest from the R_H terminal. As the value of the WR increases from all zeroes (00h) to all ones (255 decimal), the wiper moves monotonically from the position furthest from R_H to a position closer to R_H. At the same time, the resistance between R_H and R_W decreases monotonically. Note that the R_L terminals for all four pots are not connected (left floating).

While the ISL90842 is being powered up, all four WRs are reset to 80h (128 decimal), which locates R_W roughly at a position which yields a rheostat setting that is about 1/2 of R_{TOTAL}.

The WRs can be read or written directly using the I^2C serial interface as described in the following sections. The I^2C interface Address Byte has to be set to 00h, 01h, 02h, and 03h to access the WR of DCP0, DCP1, DCP2, and DCP3, respectively.

I^2C Serial Interface

The ISL90842 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL90842 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 9). On power-up of the ISL90842 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL90842 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 9). A START condition is ignored during the power-up of the device.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 9). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 10).

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The ISL90842 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL90842 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following two bits matching the logic values present at pins A1 and A0. The LSB is the Read/$\overline{\text{Write}}$ bit. Its value is "1" for a Read operation, and "0" for a Write operation (See Table 1).

TABLE 1. IDENTIFICATION BYTE FORMAT

					Logic values at pins A1, and A0 respectively		
0	1	0	1	0	A1	A0	R/$\overline{\text{W}}$
(MSB)							(LSB)

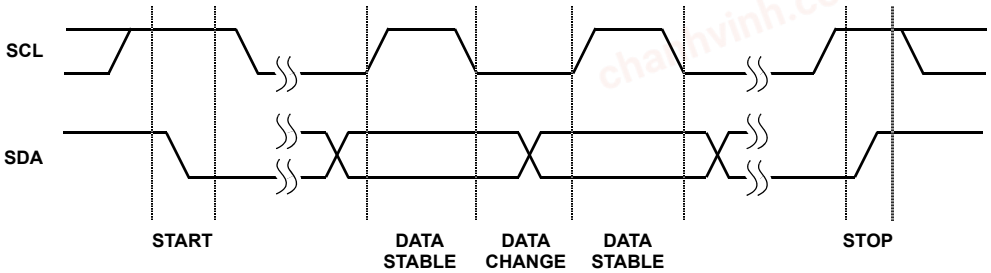


FIGURE 9. VALID DATA CHANGES, START, AND STOP CONDITIONS

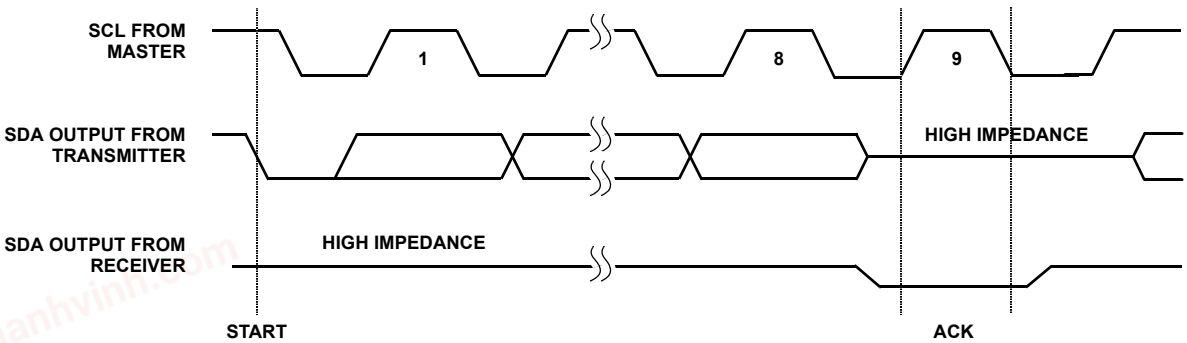


FIGURE 10. ACKNOWLEDGE RESPONSE FROM RECEIVER

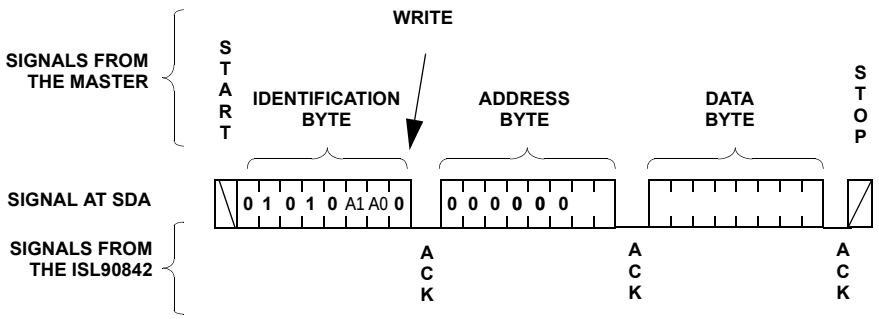


FIGURE 11. BYTE WRITE SEQUENCE

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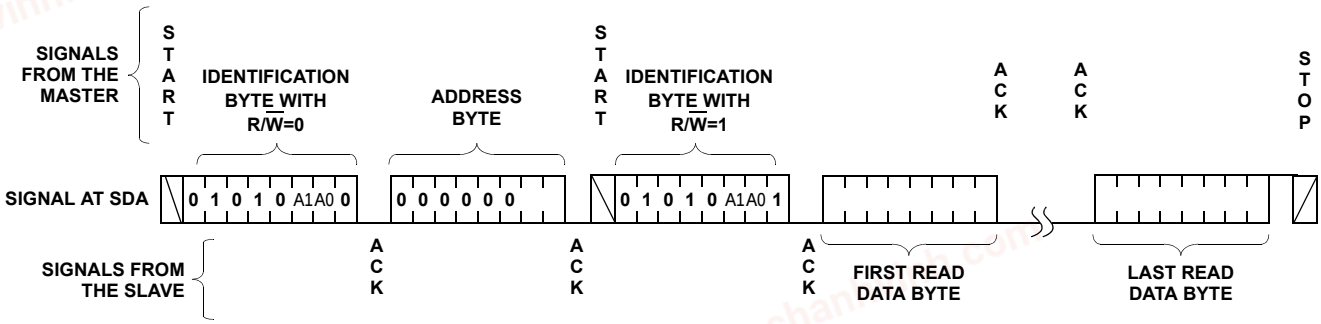


FIGURE 12. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL90842 responds with an ACK. At this time, the device enters its standby state (See Figure 11).

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 12). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL90842 responds with an ACK. Then the ISL90842 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (See Figure 12).

The Data Bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 03h the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

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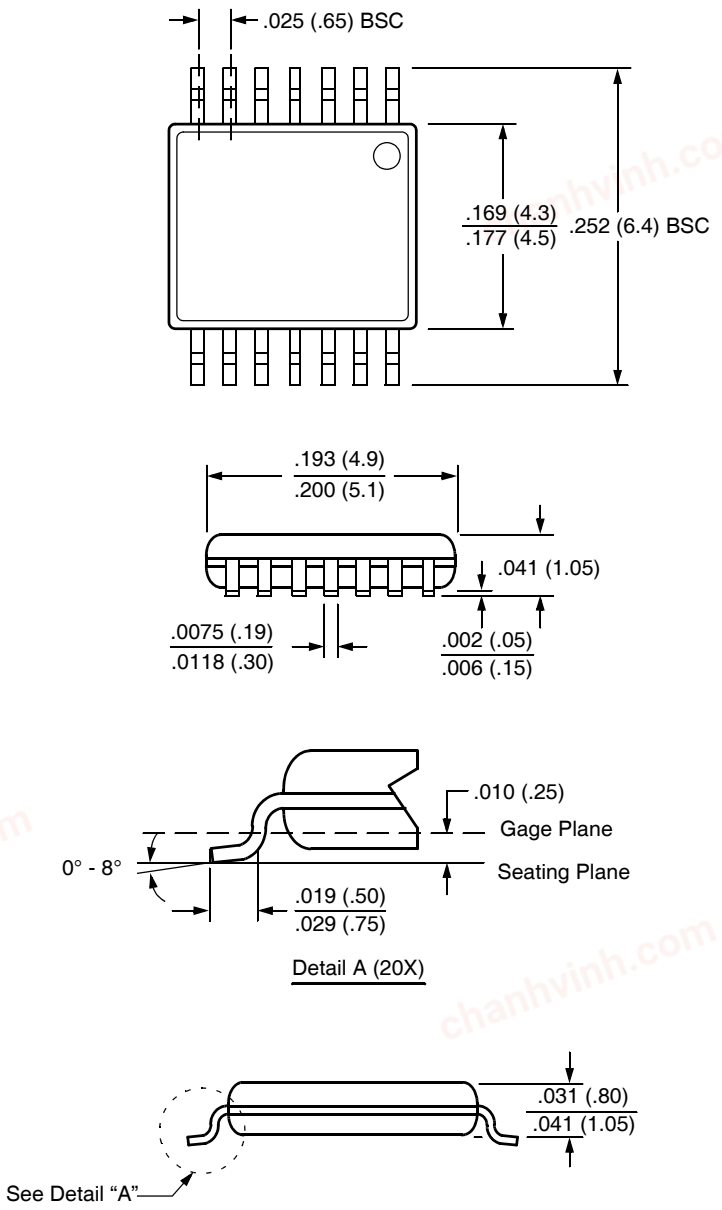
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14-Lead Plastic, TSSOP, Package Code V14



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)