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DATASHEET

ISL8485, ISL8490, ISL8491

5V, Low Power, High Speed, RS-485/RS-422 Transceivers

FN6046
Rev 10.01
Oct 14, 2021

The ISL8485, ISL8490, and ISL8491 RS-485/RS-422 devices are BiCMOS 5V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. Unlike competitive devices, this family is specified for 10% tolerance supplies (4.5V to 5.5V).

The ISL8485, ISL8490, and ISL8491 feature data rates up to 5Mbps.

All devices present a single unit load to the RS-485 bus, which allows up to 32 transceivers on the network.

The receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high Rx output if the Rx inputs are floating.

The driver (Tx) outputs are short-circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

The ISL8490 and ISL8491 are configured for full duplex (separate Rx input and Tx output pins) applications. Half duplex configurations (ISL8485) multiplex the Rx inputs and Tx outputs to allow transceivers with Rx and Tx disable functions in 8 Ld packages.

Features

- Specified for 10% tolerance supplies
- Class 3 ESD protection (HBM) on all pins: 7kV
- High data rates: up to 5Mbps
- Single unit load allows up to 32 devices on the bus
- Low quiescent current: 500µA
- -7V to +12V common-mode input voltage range
- Three state Rx and Tx outputs (except ISL8490)
- 30ns propagation delays, 5ns skew
- Full duplex and half duplex pinouts
- Operation from a single +5V supply (10% tolerance)
- Current limiting and thermal shutdown for driver overload protection
- Pb-free plus anneal (RoHS compliant)

Applications

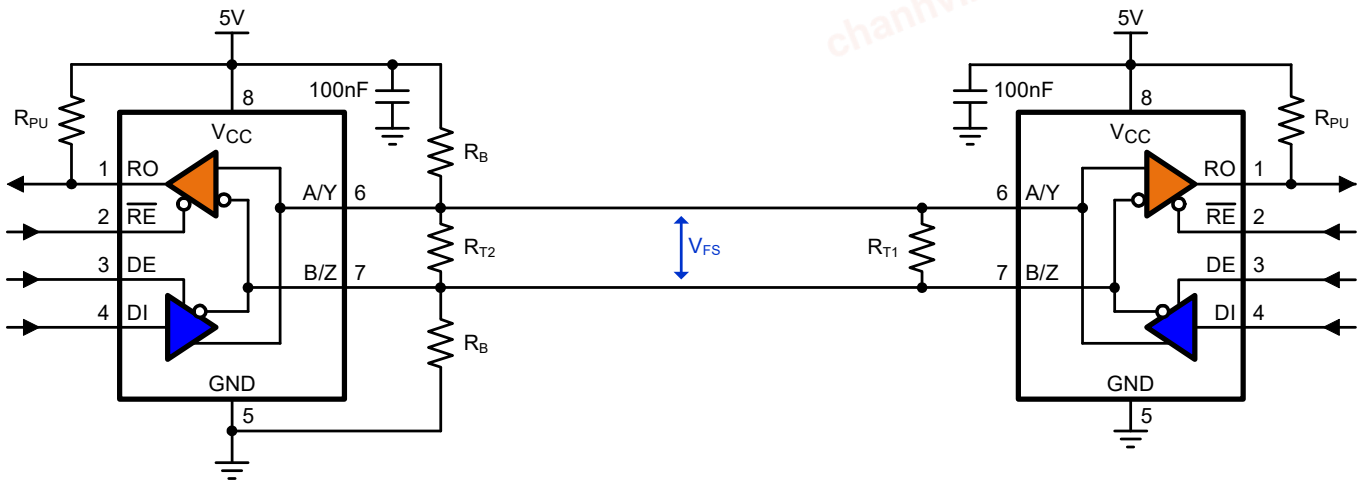
- Factory automation
- Security networks
- Building environmental control systems
- Industrial/process control networks
- Level translators (for example, RS-232 to RS-422)
- RS-232 “extension cords”

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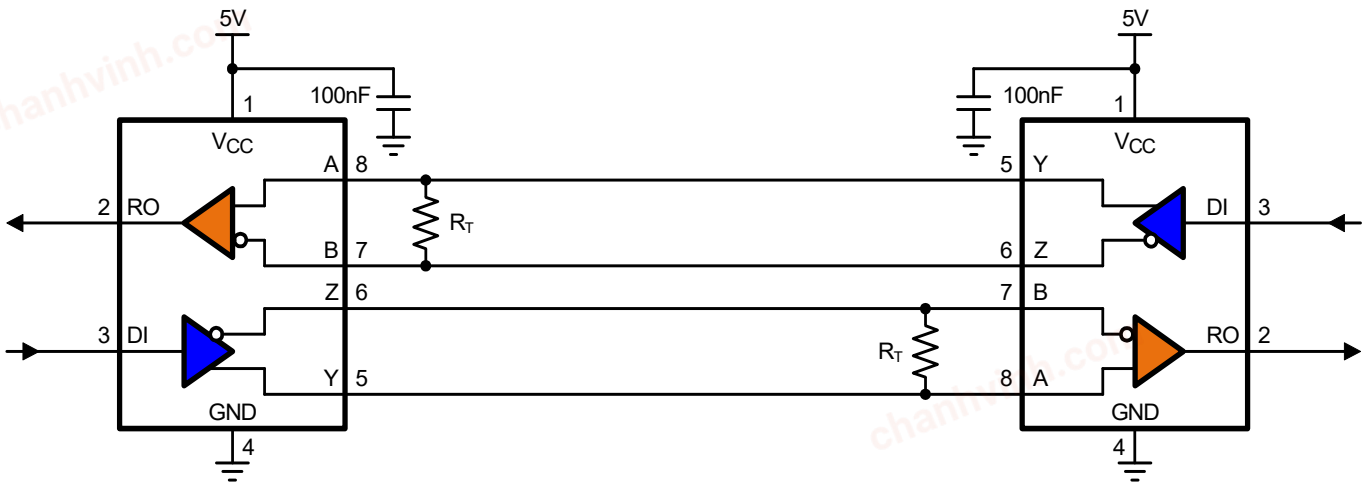
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Typical Operating Circuits

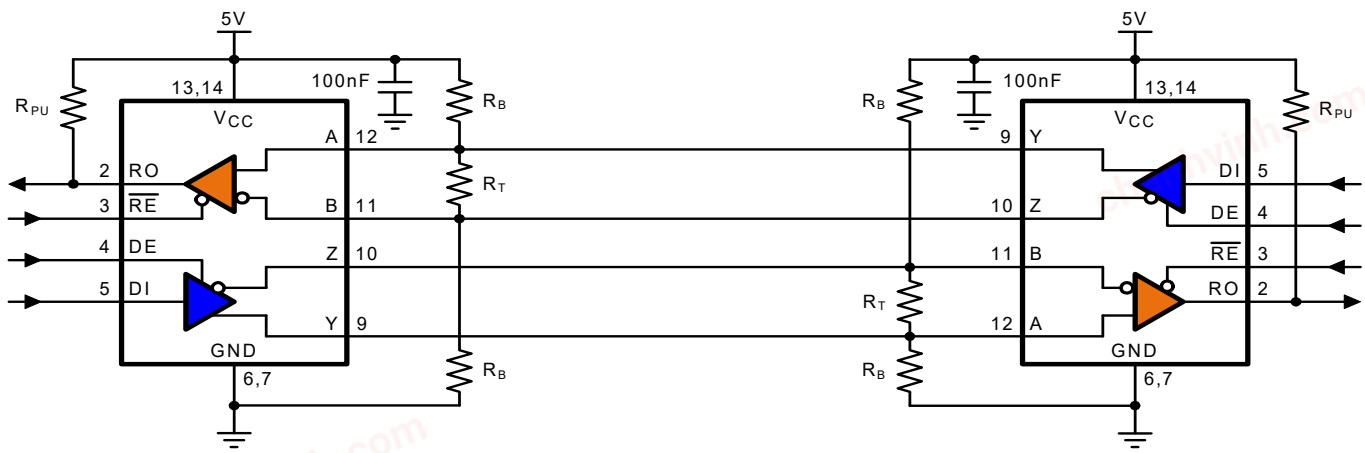
ISL8485



ISL8490



ISL8491



To calculate the resistor values, refer to TB509.

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TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	NO. OF DEVICES ALLOWED ON BUS	DATA RATE (Mbps)	SLEW-RATE LIMITED?	RECEIVER/ DRIVER ENABLE?	QUIESCENT I_{CC} (µA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL8485	Half	32	5	No	Yes	500	No	8
ISL8490	Full	32	5	No	No	500	No	8
ISL8491	Full	32	5	No	Yes	500	No	14

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE DESCRIPTION (RoHS COMPLIANT)	PKG. DWG. #	Carrier Type (Note 1)	TEMP. RANGE
ISL8485CBZ	8485 CBZ	8 Ld SOIC	M8.15	Tube	0 to +70°C
ISL8485CBZ-T				Reel, 2.5k	
ISL8485CPZ **(No longer available, recommended replacement: ISL8485ECBZ-T)**	ISL 8485CPZ	8 Ld PDIP (Note 4)	E8.3	Tube	
ISL8485IBZ	8485 IBZ	8 Ld SOIC	M8.15	Tube	-40 to +85°C
ISL8485IBZ-T				Reel, 2.5k	
ISL8485IPZ **(No longer available, recommended replacement: ISL8485EIBZ-T)**	ISL 8485IPZ	8 Ld PDIP (Note 4)	E8.3	Tube	
ISL8490IBZ	8490 IBZ	8 Ld SOIC	M8.15	Tube	
ISL8490IBZ-T				Reel, 2.5k	
ISL8491IBZ	8491IBZ	14 Ld SOIC	M14.15	Tube	

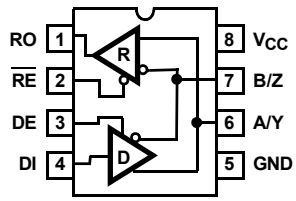
NOTE:

1. See TB347 for details about reel specifications.
2. Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL8485, ISL8490, and ISL8491 product information pages. For more information about MSL, see TB363.
4. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications

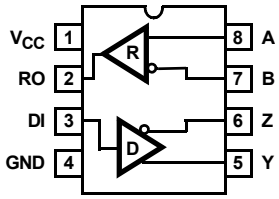
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Pinouts

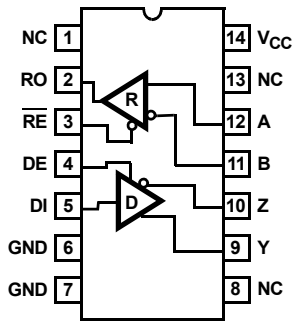
ISL8485 (PDIP, SOIC)
TOP VIEW



ISL8490 (SOIC)
TOP VIEW



ISL8491 (SOIC)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
RO	Receiver output: RO is high if A > B by at least 0.2V; RO is low if A < B by 0.2V or more; RO = high if A and B are unconnected (floating).
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs Y and Z are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	Noninverting receiver input and noninverting driver output. Pin is an input (A) if DE = 0; pin is an output (Y) if DE = 1.
B/Z	Inverting receiver input and inverting driver output. Pin is an input (B) if DE = 0; pin is an output (Z) if DE = 1.
A	Noninverting receiver input.
B	Inverting receiver input.
Y	Noninverting driver output.
Z	Inverting driver output.
V_{CC}	System power supply input (4.5V to 5.5V).
NC	No connection.

Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z

RECEIVING				
INPUTS				OUTPUT
$\overline{RE}$	DE Half Duplex	DE Full Duplex	A-B	RO
0	0	X	≥ +0.2V	1
0	0	X	≤ -0.2V	0
0	0	X	Inputs Open	1
1	1	1	X	High-Z

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Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . . -0.5V to (V_{CC} +0.5V)
Input/Output Voltages
A, B, Y, Z . . . . . -8V to +12.5V
RO . . . . . -0.5V to (V_{CC} +0.5V)
Short Circuit Duration
Y, Z . . . . . Continuous
ESD Rating
HBM (Per MIL-STD-883, Method 3015.7) . . . . . >7kV

Operating Conditions

Temperature Range
ISL84XXCX . . . . . 0°C to +70°C
ISL84XXIX . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
8 Ld SOIC Package	170
8 Ld PDIP Package (Note 6)	140
14 Ld SOIC Package	120

Moisture Sensitivity (see TB363)
All Packages . . . . . Level 1
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile (SOIC only) . . . . . see TB493

CAUTION: Stresses above those listed in Absolute Maximum Ratings can permanently damage the device. This is a stress only rating.Operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379 for details.
6. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C, Note 7

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS								
Driver Differential V_{OUT} (No Load)	V_{OD1}			Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (with Load)	V_{OD2}	R = 50Ω (RS-422), Figure 1		Full	2	3	-	V
		R = 27Ω (RS-485), Figure 1		Full	1.5	2.3	5	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 1		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R = 27Ω or 50Ω, Figure 1		Full	-	-	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R = 27Ω or 50Ω, Figure 1		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DI (ISL8485, ISL8490, ISL8491)		Full	-2	-	2	µA
	I_{IN1}	DE, $\overline{RE}$ (ISL8485, ISL8491)		Full	-25	-	25	µA
Input Current (A, B), Note 10	I_{IN2}	DE = 0V, V_{CC} = 0V or 4.5 to 5.5V	V_{IN} = 12V	Full	-	-	1	mA
			V_{IN} = -7V	Full	-	-	-0.8	mA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-0.2	-	0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25	-	70	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		Full	3.5	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = 200mV		Full	-	-	0.4	V
Three-State (high impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V		Full	-	-	±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	12	-	-	kΩ

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Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C, Note 7 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
No-Load Supply Current, Note 8	I_{CC}							
		ISL8490, ISL8491, DE, DI, $\overline{RE}$ = 0V or V_{CC}		Full	-	500	565	µA
		ISL8485, DI, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	Full	-	700	900	µA
			DE = 0V	Full	-	500	565	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V, Note 9		Full	35	-	250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	7	-	85	mA
SWITCHING CHARACTERISTICS (ISL8485, ISL8490, ISL8491)								
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF, Figure 2		Full	18	30	50	ns
Driver Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF, Figure 2		Full	-	2	10	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF, Figure 2		Full	3	11	25	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF, SW = GND, Figure 3		Full	-	17	70	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF, SW = V_{CC}, Figure 3		Full	-	14	70	ns
Driver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, Figure 3		Full	-	19	70	ns
Driver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, Figure 3		Full	-	13	70	ns
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	Figure 4		Full	30	40	150	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	Figure 4		25	-	5	-	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND, Figure 5		Full	-	9	50	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC}, Figure 5		Full	-	9	50	ns
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, Figure 5		Full	-	9	50	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, Figure 5		Full	-	9	50	ns
Maximum Data Rate	f_{MAX}	Note 11		Full	5	-	-	Mbps

NOTES:

7. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
8. Supply current specification is valid for loaded drivers when DE = 0V.
9. Applies to peak current. See "Typical Performance Curves" on page 10 for more information.
10. Devices meeting these limits are denoted as "single unit load (1 UL)" transceivers. The RS-485 standard allows up to 32 unit loads on the bus.
11. Ensured by characterization, but not tested.

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Test Circuits and Waveforms

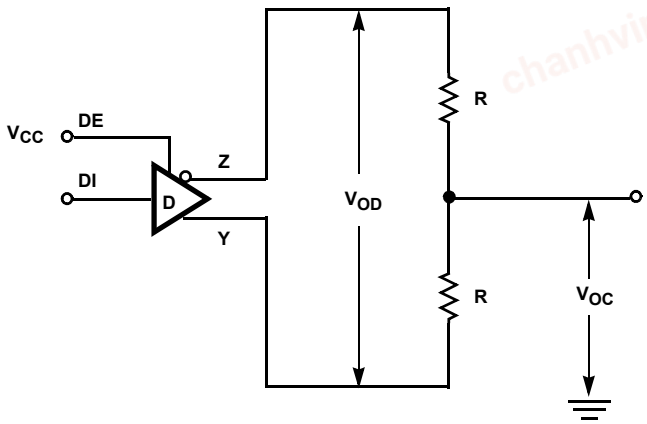


FIGURE 1. DRIVER V_{OD} AND V_{OC}

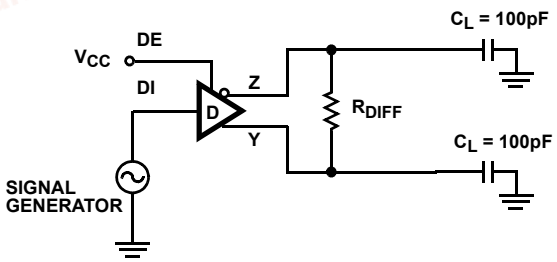
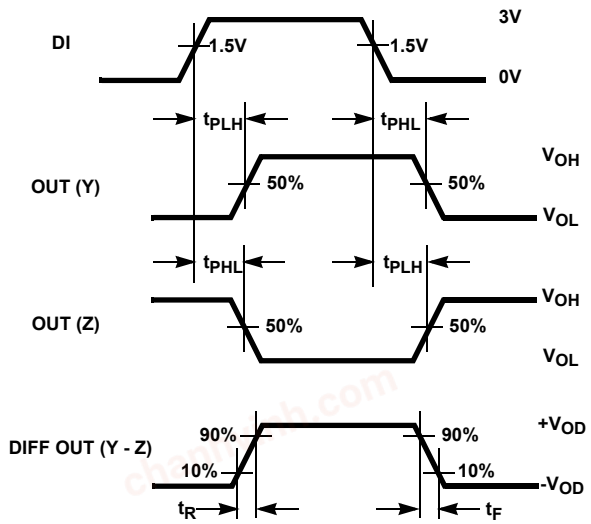


FIGURE 2A. TEST CIRCUIT



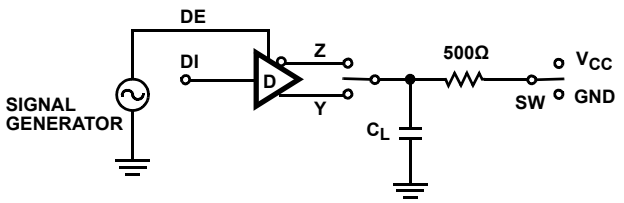
SKEW = $|t_{PLH}$ (Y or Z) - t_{PHL} (Z or Y)$|$

FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES

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Test Circuits and Waveforms (Continued)



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	15
t_{LZ}	Y/Z	X	0/1	V_{CC}	15
t_{ZH}	Y/Z	0	1/0	GND	100
t_{ZL}	Y/Z	0	0/1	V_{CC}	100

FIGURE 3A. TEST CIRCUIT

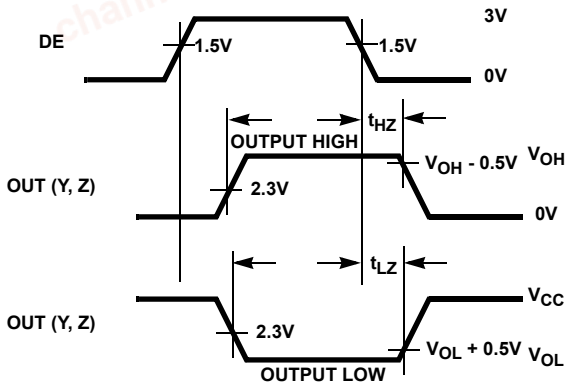


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES (EXCLUDING ISL8490)

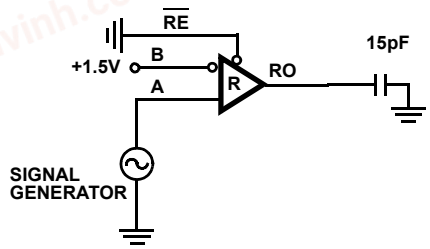


FIGURE 4A. TEST CIRCUIT

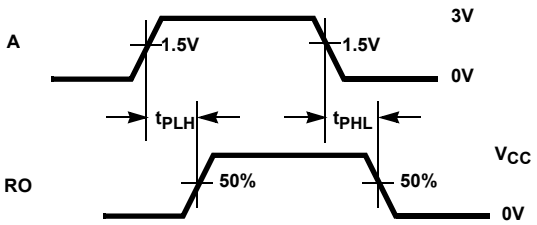
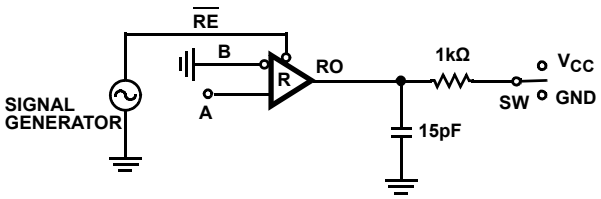


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. RECEIVER PROPAGATION DELAY



PARAMETER	DE	AΩ	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH}	0	+1.5V	GND
t_{ZL}	0	-1.5V	V_{CC}

FIGURE 5A. TEST CIRCUIT

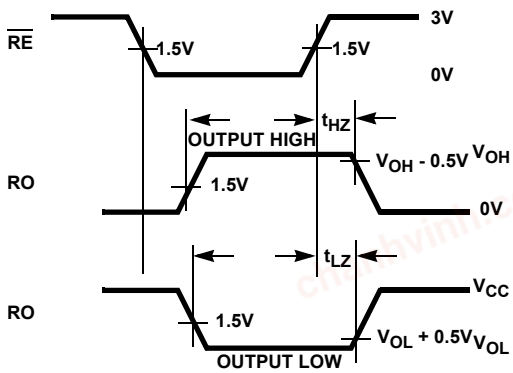


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER ENABLE AND DISABLE TIMES (EXCLUDING ISL8490)

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Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 receivers on each bus, assuming one unit load devices. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

An important advantage of RS-485 is the extended Common-Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000ft, so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

These devices use a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input impedance surpasses the RS-422 specification of 4kΩ, and meets the RS-485 unit load requirement of 12kΩ minimum.

Receiver inputs function with common-mode voltages as great as ±7V outside the power supplies (+12V and -7V), making them ideal for long networks in which induced voltages are a realistic concern.

All the receivers include a “fail-safe if open” function that ensures a high level receiver output if the receiver inputs are unconnected (floating).

Receivers easily meet the data rates supported by the corresponding driver.

The ISL8485 and ISL8491 receiver outputs are three-statable using the active low $\overline{RE}$ input.

Driver Features

The RS-485/RS-422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485), and at least 2V across a 100Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width and to minimize EMI.

The ISL8485 and ISL8491 drivers are three-statable using the active high DE input.

The ISL8485 and ISL8491 driver outputs are not limited, so faster output transition times allow data rates of at least 5Mbps.

Data Rate, Cables, and Terminations

RS-485/RS-422 are intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. Devices operating at 5Mbps are limited to lengths less than 100ft.

Twisted pair cable is the cable of choice for RS-485/422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative to minimize reflections when using the 5Mbps devices.

In point-to-point networks or point-to-multipoint (single driver on bus) networks, terminate the main cable in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. In multipoint (multi-driver) systems, terminate the main cable in its characteristic impedance at both ends. Keep stubs connecting a transceiver to the main cable as short as possible.

Built-In Driver Overload Protection

The RS-485 specification requires that drivers survive worst case bus contentions undamaged. The ISL84XX devices meet this requirement using driver output short circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry that ensures the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes. These devices also use a foldback circuit that reduces the short-circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short-circuit condition, the ISL84XX devices’ thermal shutdown feature disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15°C. If the condition persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

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Typical Performance Curves V_{CC} = 5V, T_A = 25°C, ISL8485, ISL8490, ISL8491; unless otherwise specified

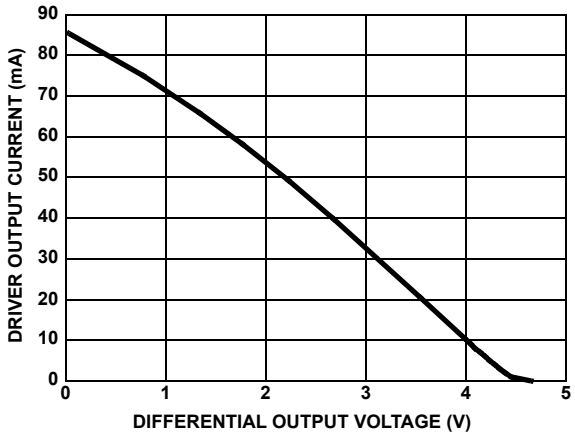


FIGURE 6. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

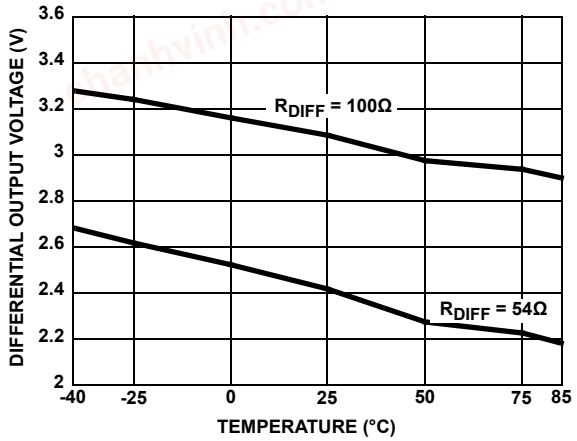


FIGURE 7. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

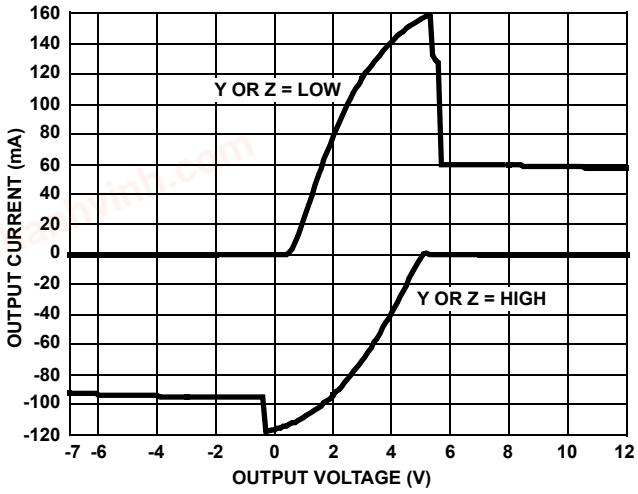


FIGURE 8. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

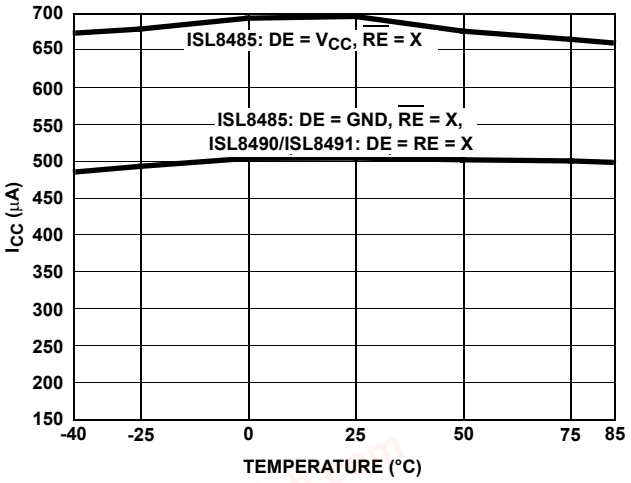


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE

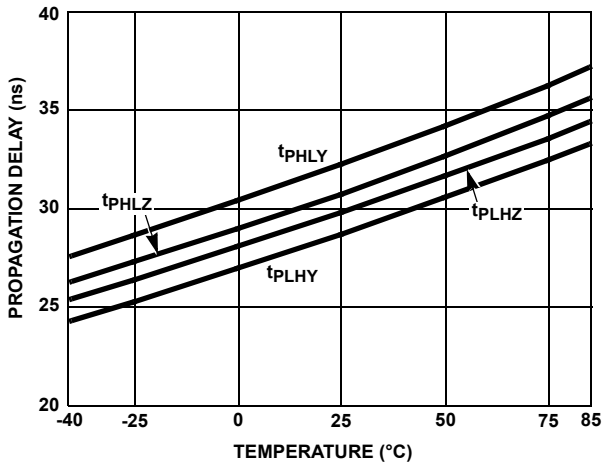


FIGURE 10. DRIVER PROPAGATION DELAY vs TEMPERATURE

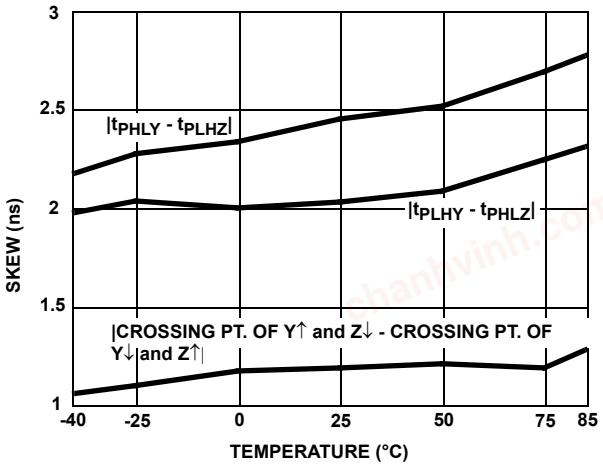


FIGURE 11. DRIVER SKEW vs TEMPERATURE

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Typical Performance Curves V_{CC} = 5V, T_A = 25°C, ISL8485, ISL8490, ISL8491; unless otherwise specified **(Continued)**

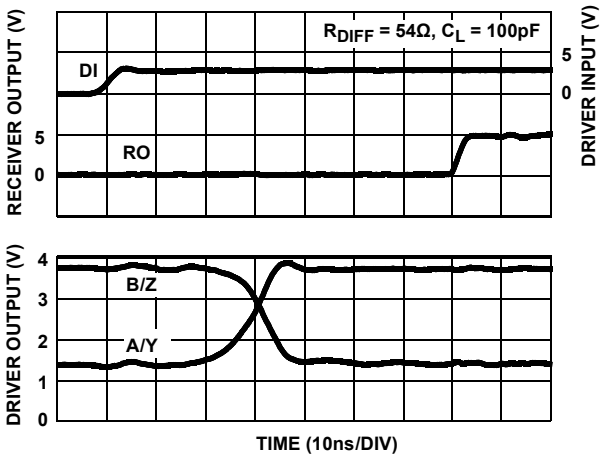


FIGURE 12. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH

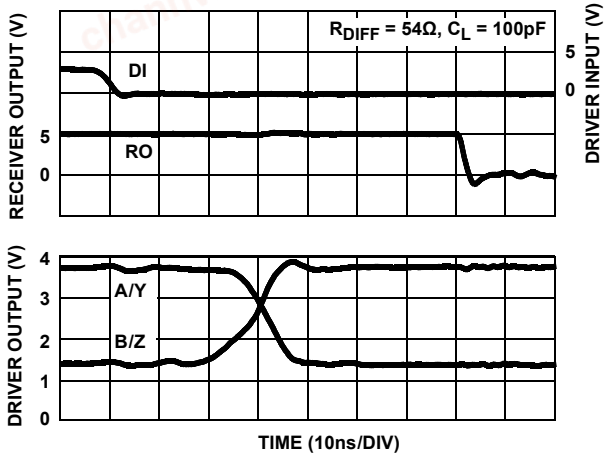


FIGURE 13. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

518

PROCESS:

Si Gate CMOS

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Revision History

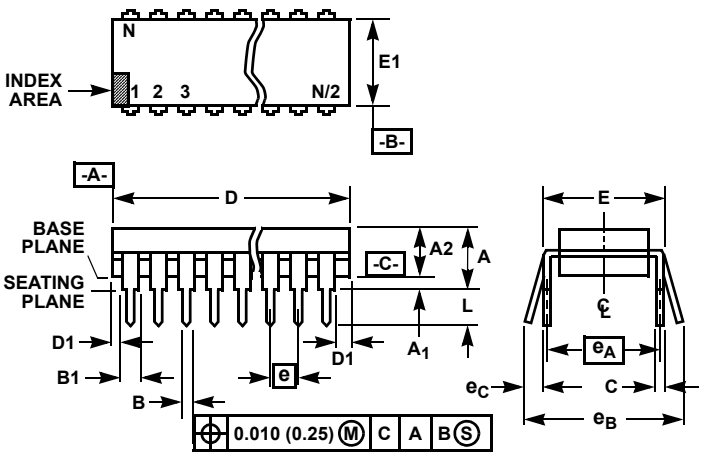
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit out website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Oct 14, 2021	10.01	Fixed the formatting on Ordering table. Removed Related Literature section. Updated POD M8.15 to the latest version, changes are as follows: -Added the coplanarity spec into the drawing. Updated POD M14.15 to the latest version, changes are as follows: -Added lead length dimension (1.27 – 0.40) -Changed angle of the lead to 0-8 degrees.
Oct 18, 2018	10.00	Removed ISL8483, ISL8488, and ISL8489 information from the datasheet. Updated Typical Operating Circuits on page 2. Updated Features bullets on page 1. Added Related Literature section to page 1. Updated Ordering Information table on page 3: -Added Tape and Reel column. -Added information about replacements for the ISL8485CPZ and ISL8485IPZ. Removed About Intersil section and updated Renesas disclaimer.
Feb 16, 2016	9.00	Added Rev History and About Intersil verbiage. Updated “Ordering Information” table on page 3. Updated following PODs to current revisions listing POD updates: **POD M8.15**: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Changed Note 1 "1982" to "1994 **POD M14.15** Added land pattern and moved dimensions from table onto drawing

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Package Outline Drawings

For the most recent package outline drawing, see E8.3.



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE (PDIP)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

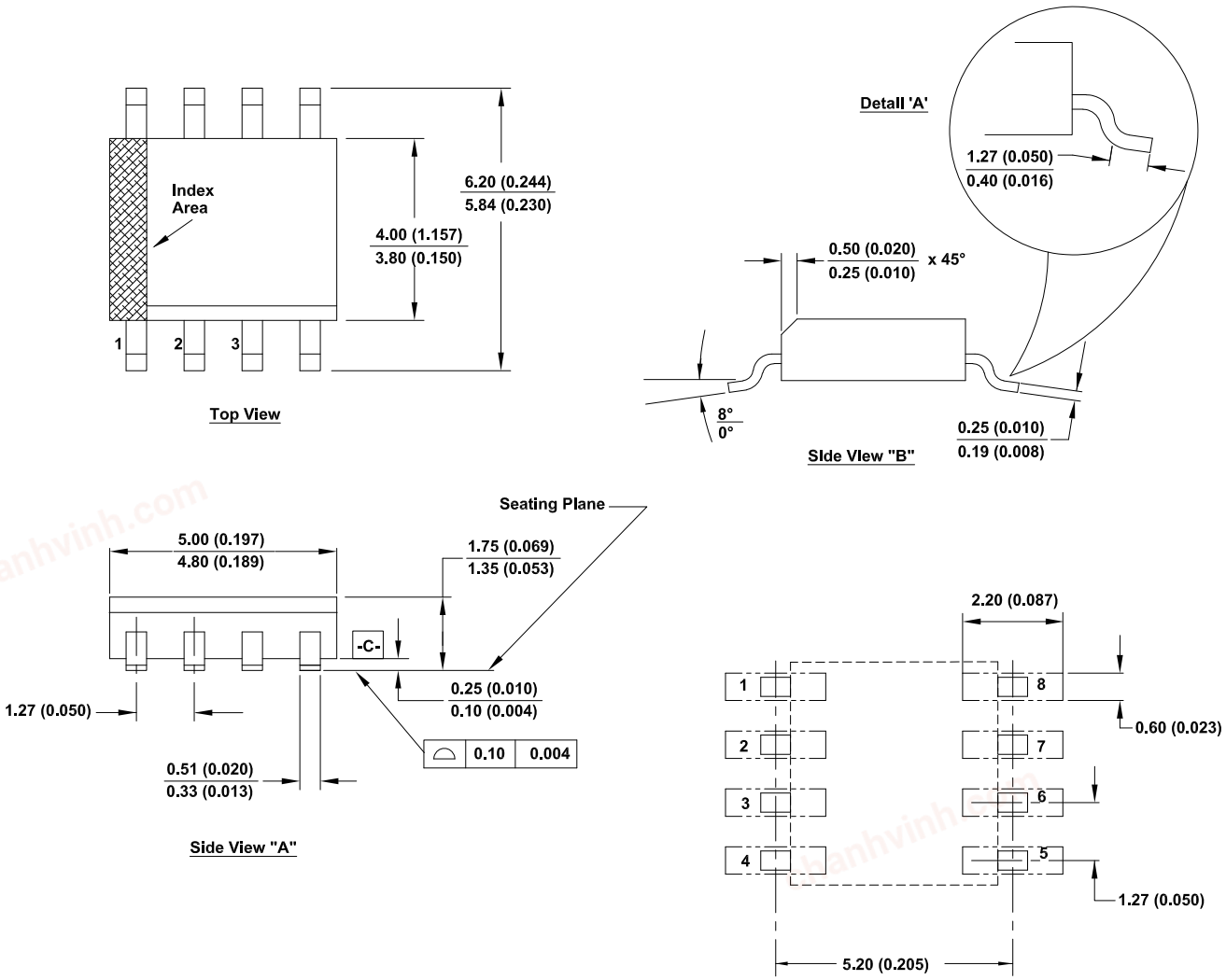
Rev. 0 12/93

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For the most recent package outline drawing, see M8.15.

M8.15

8 Lead Narrow Body Small Outline Plastic Package
Rev 5, 4/2021



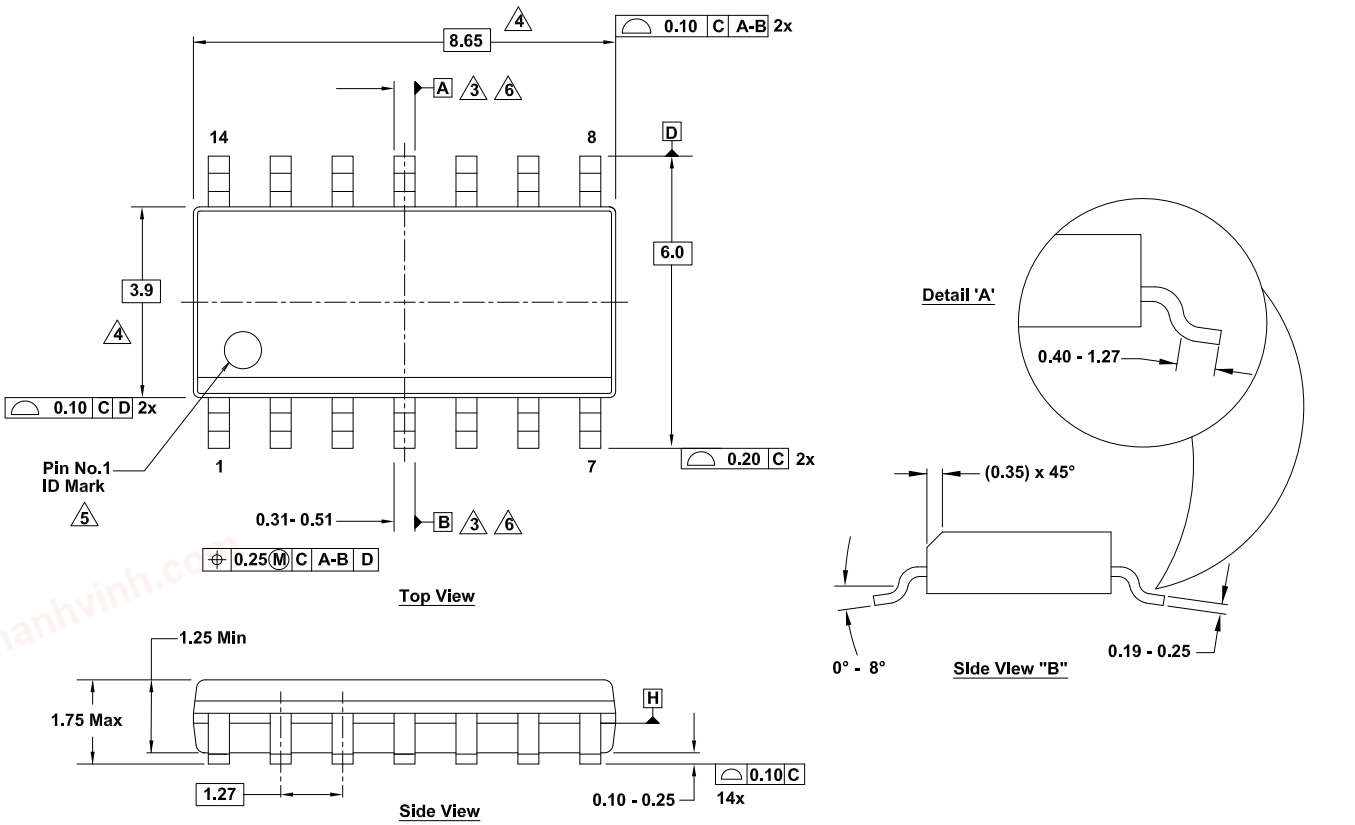
NOTES:

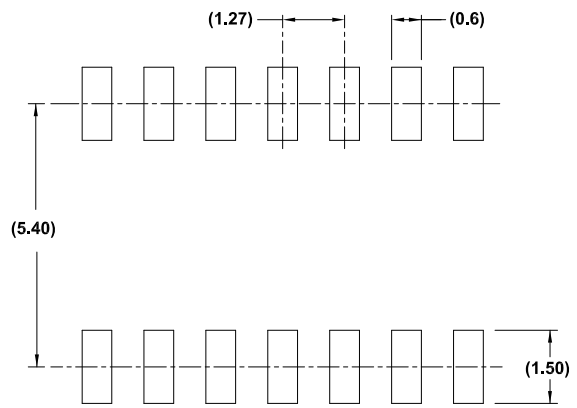
1. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
2. Package length does not include mold flash, protrustion or gate burrs. Mold flash, protrustion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrustions. Interlead flash and protrustions shallnot exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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For the most recent package outline drawing, see M14.15.

M14.15
14 Lead Narrow Body Small Outline Plastic Package
Rev 2, 6/20





Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Datums A and B are determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier can be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

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(Rev.1.0 Mar 2020)

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