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ISL84781

Ultra Low ON-Resistance, Low-Voltage, Single Supply, 8-to-1 Analog Multiplexer

FN6095
Rev 4.00
October 28, 2010

The Intersil ISL84781 device contains precision, bidirectional, analog switches configured as an 8-channel multiplexer/demultiplexer. It is designed to operate from a single +1.6V to +3.6V supply. The device has an inhibit pin to simultaneously open all signal paths.

ON-resistance is 0.4Ω with a +3.0V supply and 0.55Ω with a single +1.8V supply. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 4nA max at +25°C or 40nA max at +85°C with a +3.3V supply.

All digital inputs are 1.8V logic-compatible when using a single +3V supply.

The ISL84781 is a 8-to-1 multiplexer device that is offered in a 16 Ld TSSOP package, and a 16 Ld thin QFN package.

Table 1 summarizes the performance of this family.

TABLE 1. FEATURES AT A GLANCE

	ISL84781
Configuration	8:1 Mux
3V r_{ON}	0.4Ω
3V t_{ON}/t_{OFF}	16ns/13ns
1.8V r_{ON}	0.55Ω
1.8V t_{ON}/t_{OFF}	24ns/16ns
Packages	16 Ld TSSOP, 16 Ld 3x3 thin QFN

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Features

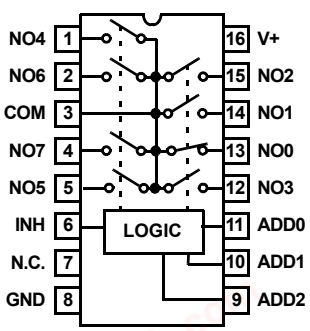
- Pin Compatible Replacement for the MAX4781, and MAX4617
- ON-resistance (r_{ON})
  - V+ = +3.0V 0.4Ω
  - V+ = +1.8V 0.55Ω
- r_{ON} Matching Between Channels 0.12Ω
- r_{ON} Flatness Across Signal Range 0.056Ω
- Single Supply Operation. . . . . +1.6V to +3.6V
- Low Power Consumption (PD). . . . . <0.2µW
- Fast Switching Action (V_S = +3V)
  - t_{ON} 16ns
  - t_{OFF} 13ns
- Guaranteed Break-Before-Make
- High Current Handling Capacity (300mA Continuous)
- Available in 16 Ld TSSOP and 16 Ld 3x3 Thin QFN
- 1.8V CMOS-Logic Compatible (+3V Supply)
- Pb-Free (RoHS Compliant)
- ISL84781IR Replaces the ISL43L680IR.

Applications

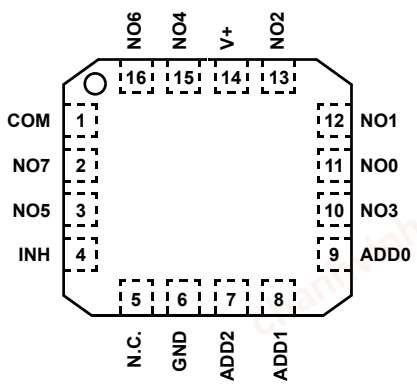
- Battery Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio Switching and Routing

Pinouts (Note 1)

ISL84781
(16 LD TSSOP)
TOP VIEW



ISL84781
(16 LD 3x3 THIN QFN)
TOP VIEW



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Pinouts (Note 1) (Continued)

NOTE:

1. Switches Shown for Logic “0” Inputs.

Truth Table

ISL84781				
INH	**ADD2**	**ADD1**	**ADD0**	**SWITCH ON**
1	X	X	X	NONE
0	0	0	0	NO0
0	0	0	1	NO1
0	0	1	0	NO2
0	0	1	1	NO3
0	1	0	0	NO4
0	1	0	1	NO5
0	1	1	0	NO6
0	1	1	1	NO7

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V, with a 3V supply. X = Don’t Care.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (1.6V to 3.6V)
N.C.	No Connect. Not internally connected.
GND	Ground Connection
INH	Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off.
COM	Analog Switch Common Pin
NO0 - NO7	Analog Switch Input Pin
ADD	Address Input Pin

Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL84781IVZ	84781 IVZ	-40 to +85	16 Ld TSSOP	M16.173
ISL84781IRZ	781Z	-40 to +85	16 Ld TQFN	L16.3x3A

2. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL84781. For more information on MSL, please see Technical Brief TB363.

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Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to 4.7V
Input Voltages
INH, NO, ADD (Note 5) . . . . . -0.3 to (V+) + 0.3V
Output Voltages
COM (Note 5) . . . . . -0.3 to (V+) + 0.3V
Continuous Current NO or COM . . . . . ±300mA
Peak Current NO or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD Rating
Human Body Model . . . . . >4kV
Machine Model . . . . . >300V
Charged Device Model . . . . . >1000V

Thermal Information

Thermal Resistance (Typical, Note 6)	θ_{JA} (°C/W)
16 Ld TSSOP Package	150
16 Ld 3x3 Thin QFN Package	75

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Signals on NO, COM, ADD, or INH exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 3V Supply

Test Conditions: V_{SUPPLY} = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 7), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 8, 11)	TYP	MAX (Notes 8, 11)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON-resistance, r_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} = 0V to V+, (See Figure 5)	25	-	0.41	0.75	Ω
		Full	-	-	**0.8**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} = Voltage at max r_{ON}, (Note 9)	25	-	0.12	0.2	Ω
		Full	-	-	**0.2**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} = 0V to V+, (Note 10)	25	-	0.056	0.15	Ω
		Full	-	-	**0.15**	Ω
NO OFF Leakage Current, $I_{NO(OFF)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, V_{NO} = 3V, 0.3V	25	-4	-	4	nA
		Full	**-40**	-	**40**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.3V, V_{COM} = V_{NO} = 0.3V, 3V	25	-15	-	15	nA
		Full	**-70**	-	**70**	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	**1.4**	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	**0.5**	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V+ = 3.6V, V_{INH} = V_{ADD} = 0V or V+ (Note 12)	Full	**-0.5**	-	**0.5**	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 12)	25	-	16	25	ns
		Full	-	-	**27**	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 12)	25	-	14	23	ns
		Full	-	-	**25**	ns
Address Transition Time, t_{TRANS}	V+ = 2.7V, V_{NO} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 12)	25	-	19	28	ns
		Full	-	-	**30**	ns
Break-Before-Make Time, t_{BBM}	V+ = 3.3V, V_{NO} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 3, Note 12)	25	-	4	-	ns
		Full	**1**	-	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2)	25	-	-39	-	pC
Input OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} = V_{COM} = 0V, (See Figure 6)	25	-	65	-	pF

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Electrical Specifications - 3V Supply

Test Conditions: V_{SUPPLY} = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 7), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 8, 11)	TYP	MAX (Notes 8, 11)	UNITS
COM OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} = V_{COM} = 0V, (See Figure 6)	25	-	470	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} = V_{COM} = 0V, (See Figure 6)	25	-	485	-	pF
OFF-Isolation	R_L = 50Ω, C_L = 35pF, f = 100kHz, (See Figure 4)	25	-	65	-	dB
Total Harmonic Distortion (THD)	f = 20Hz to 20kHz, $0.5V_{P-P}$, R_L = 32Ω	25	-	0.014	-	%
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	**1.6**	-	**3.6**	V
Positive Supply Current, I+	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	25	-	-	0.05	µA
		Full	-	-	**1.2**	µA

NOTES:

7. V_{IN} = Input voltage to perform proper function.
8. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
9. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
10. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
12. Limits established by characterization and are not production tested.

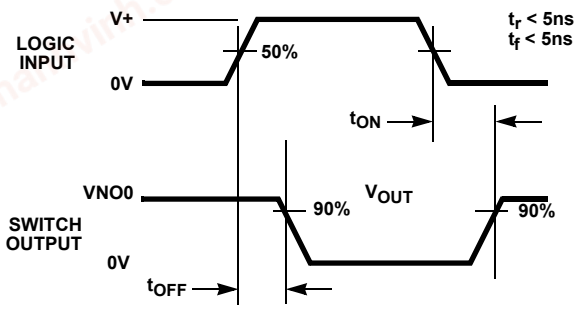
Electrical Specifications: 1.8V Supply

Test Conditions: V+ = +1.8V, GND = 0V, V_{INH} = 1V, V_{INL} = 0.4V (Note 7), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 8, 11)	TYP	MAX (Notes 8, 11)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON-resistance, r_{ON}	V+ = 1.8V, I_{COM} = 10.0mA, V_{NO} = 1.0V, (See Figure 5)	25	-	0.55	0.85	Ω
		Full	-	-	**0.9**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 1.8V, I_{COM} = 10.0mA, V_{NO} = 1.0V, (See Figure 5)	25	-	0.1	-	Ω
		Full	-	0.13	-	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 1.8V, I_{COM} = 10.0mA, V_{NO} = 0V, 0.9V, 1.6V, (See Figure 5)	25	-	0.14	-	Ω
		Full	-	0.16	-	Ω
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	**1**	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	**0.4**	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V+ = 1.8V, V_{INH}, V_{ADD} = 0V or V+ (Note 12)	Full	**-0.5**	-	**0.5**	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 1.8V, V_{NO} = 1.0V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 12)	25	-	24	33	ns
		Full	-	-	35	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 1.8V, V_{NO} = 1.0V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 12)	25	-	16	25	ns
		Full	-	-	27	ns
Address Transition Time, t_{TRANS}	V+ = 1.8V, V_{NO} = 1.0V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 12)	25	-	25	34	ns
		Full	-	-	36	ns
Break-Before-Make Time, t_{BBM}	V+ = 1.8V, V_{NO} = 1.0V, R_L = 50Ω, C_L = 35pF, (See Figure 3, Note 12)	25	-	9	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2)	25	-	-20	-	pC

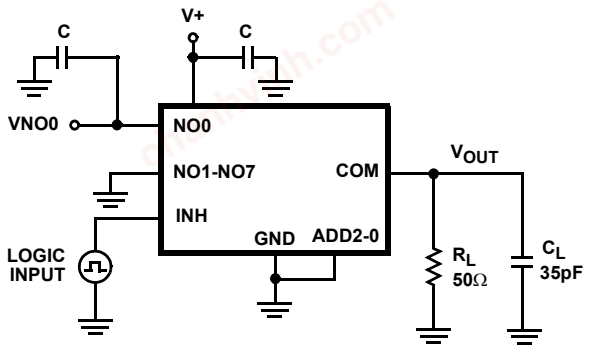
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Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

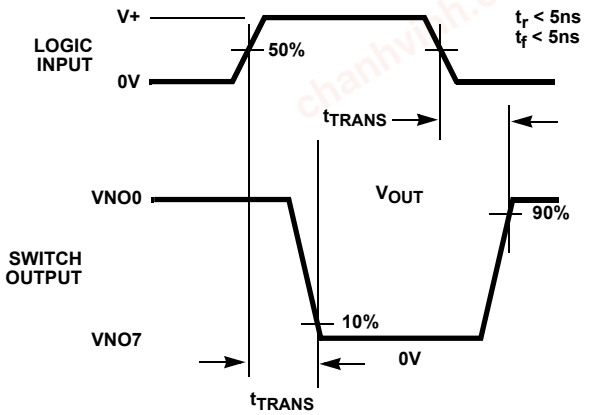
FIGURE 1A. INHIBIT t_{ON}/t_{OFF} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

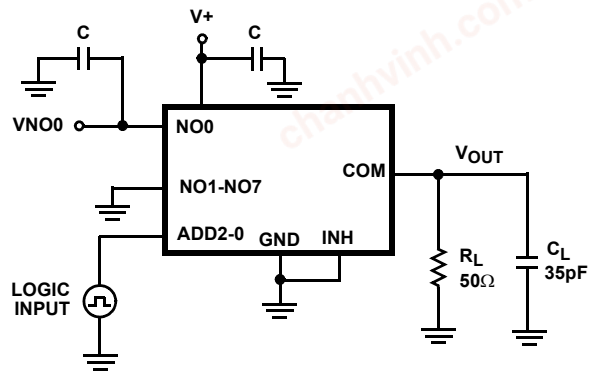
$$V_{OUT} = V_{NOx} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. INHIBIT t_{ON}/t_{OFF} TEST CIRCUIT



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{NOx} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1D. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

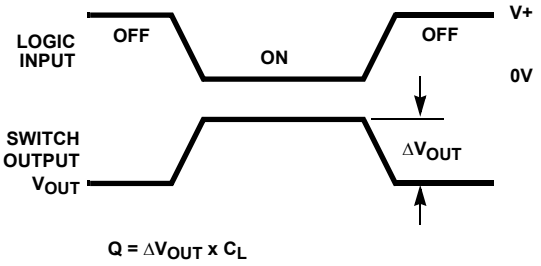
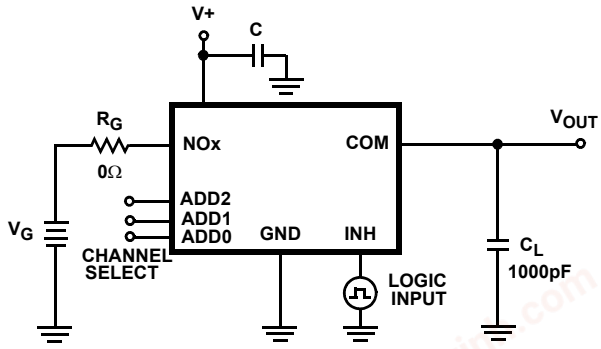


FIGURE 2A. Q MEASUREMENT POINTS



Repeat test for other switches.

FIGURE 2B. Q TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

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Test Circuits and Waveforms (Continued)

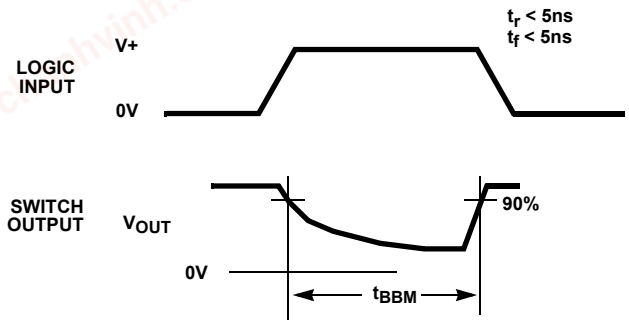
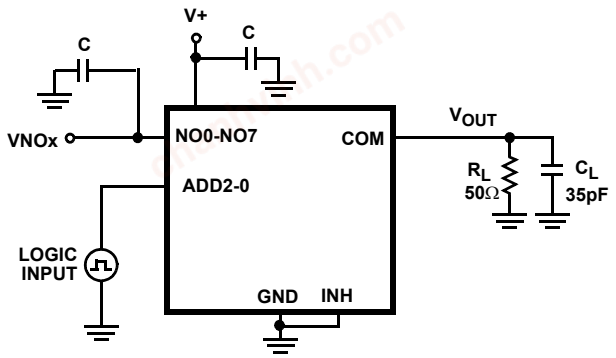


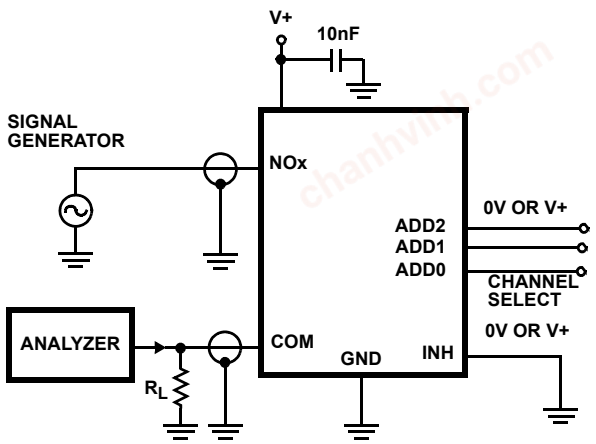
FIGURE 3A. t_{BBM} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

FIGURE 3B. t_{BBM} TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME



Off-Isolation is measured between COM and “Off” NO terminal on each switch.

Signal direction through switch is reversed and worst case values are recorded.

FIGURE 4. OFF-ISOLATION TEST CIRCUIT

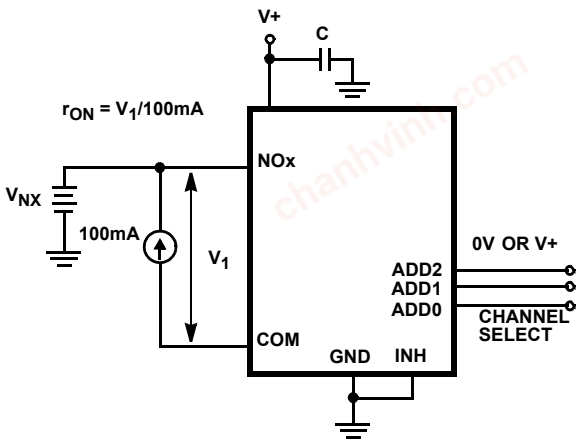


FIGURE 5. r_{ON} TEST CIRCUIT

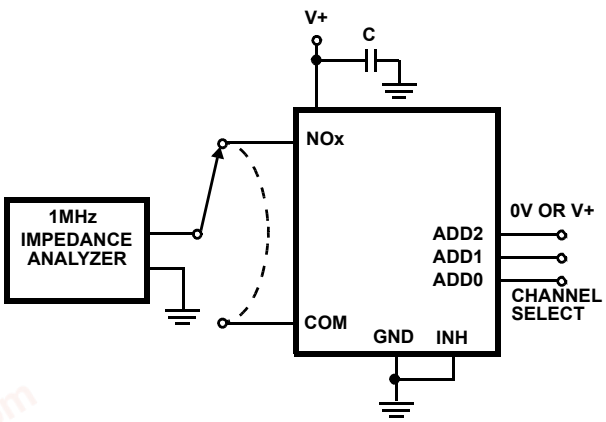


FIGURE 6. CAPACITANCE TEST CIRCUIT

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Detailed Description

The ISL84781 analog multiplexer offers precise switching capability from a single 1.6V to 3.6V supply with ultra low ON-resistance (0.41Ω) and high speed operation (t_{ON} = 16ns, t_{OFF} = 13ns) with +3V supply. The device is especially well-suited for portable battery powered equipment thanks to the low operating supply voltage (1.6V), low power consumption (0.2µW), and low leakage currents (70nA max). High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (See Figure 7). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 7). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 7). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch signal range is reduced and the resistance may increase, especially at low supply voltages.

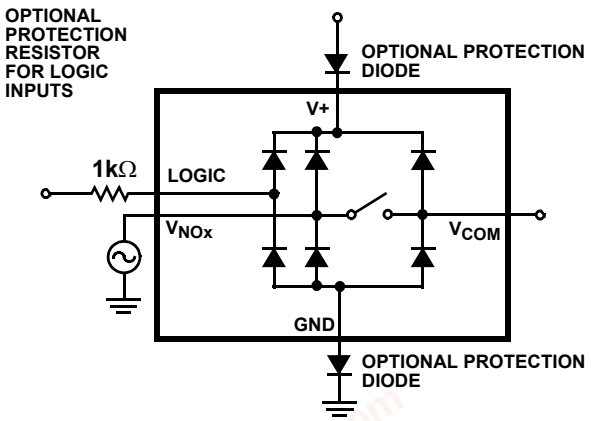


FIGURE 7. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL84781 construction is typical of most single supply CMOS analog multiplexers, in that it has two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set its analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL84781 4.7V maximum supply voltage provides plenty of room for the 10% tolerance of 3.6V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.6V but the part will operate with a supply below 1.5V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the electrical specification tables and “Typical Performance Curves” beginning on page 8 for details.

V+ and GND power the internal logic and level shifters. The level shifters convert the logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

These multiplexers cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This device is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2.0V to 3.6V (See Figure 12). At 3.6V the V_{IH} level is about 1.27V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 10MHz with a -3dB bandwidth of 52MHz (See Figure 16). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch’s input to its output. Off-Isolation is the resistance to this feed-through. Figure 17 details the high Off Isolation provided by these devices. At 100kHz, Off Isolation is about 65dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

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Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

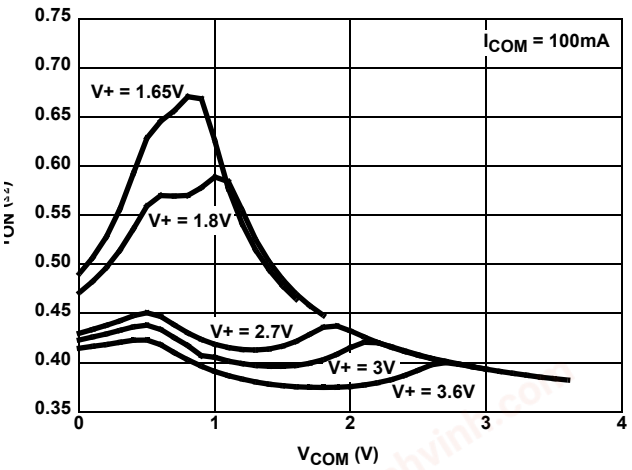


FIGURE 8. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

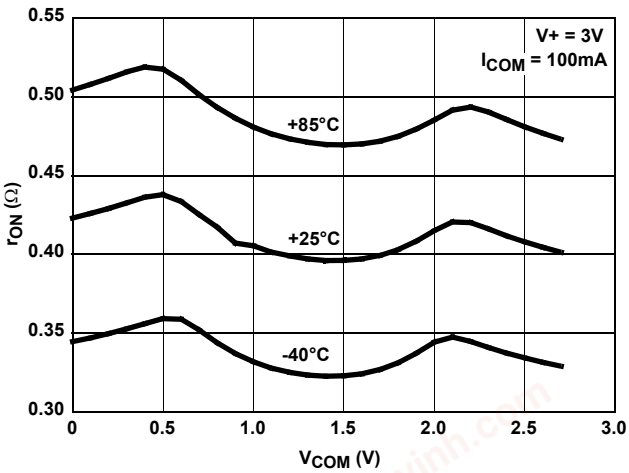


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE

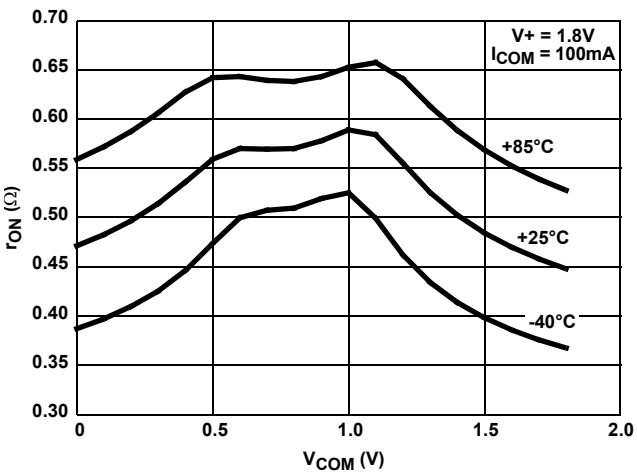


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

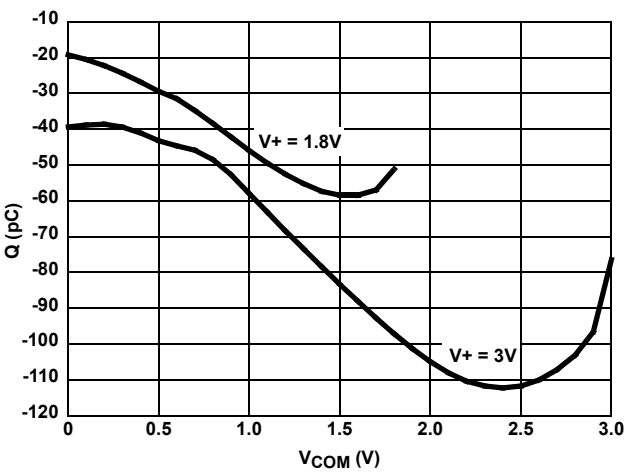


FIGURE 11. CHARGE INJECTION vs SWITCH VOLTAGE

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Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

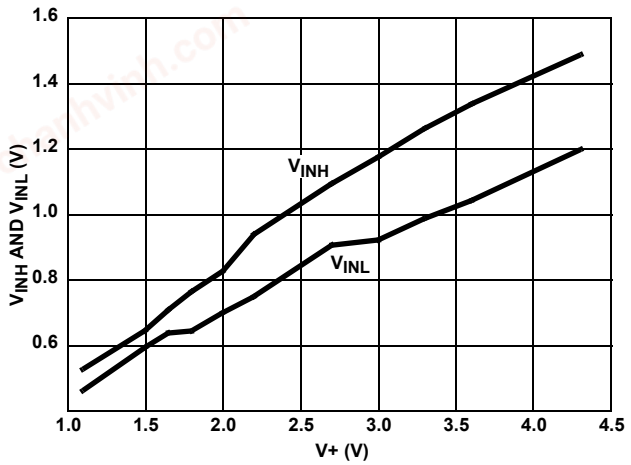


FIGURE 12. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

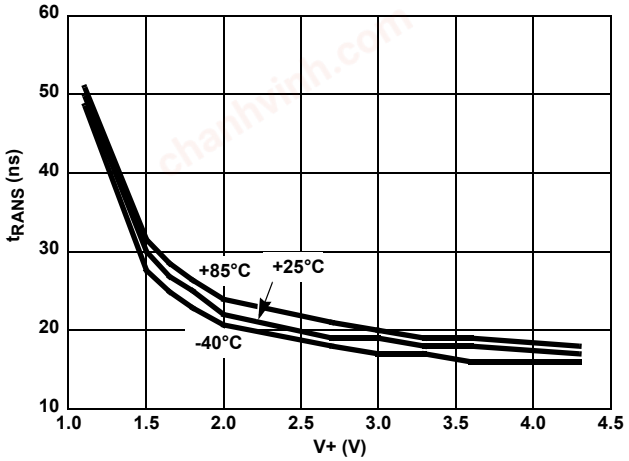


FIGURE 13. ADDRESS TRANS TIME vs SUPPLY VOLTAGE

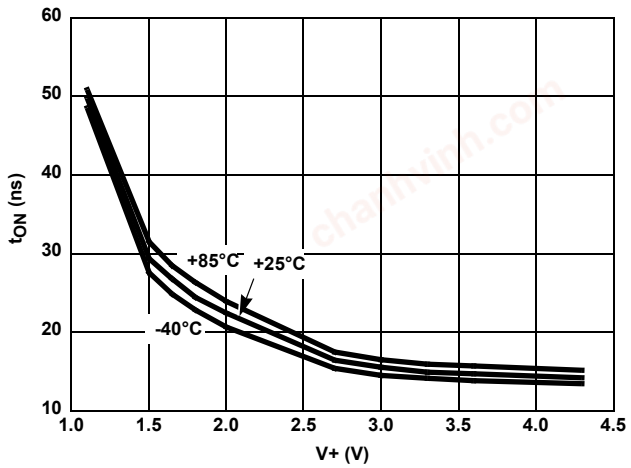


FIGURE 14. INHIBIT TURN-ON TIME vs SUPPLY VOLTAGE

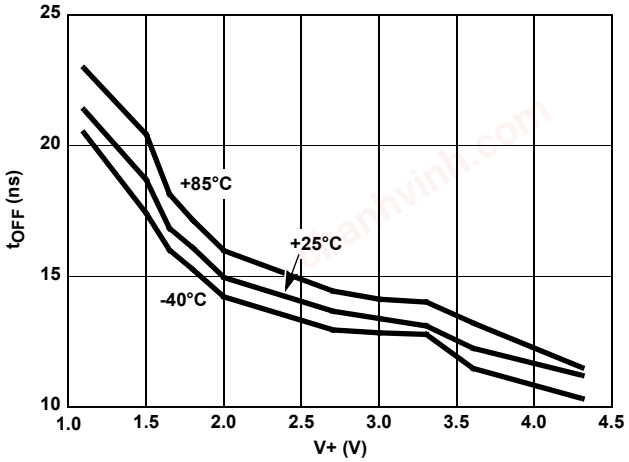


FIGURE 15. INHIBIT TURN-OFF TIME vs SUPPLY VOLTAGE

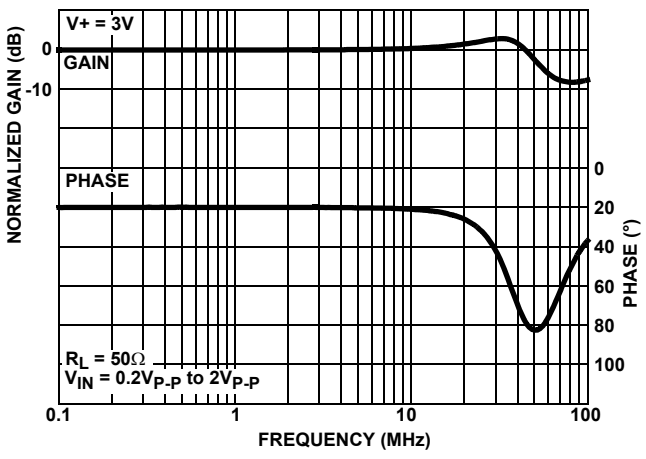


FIGURE 16. FREQUENCY RESPONSE

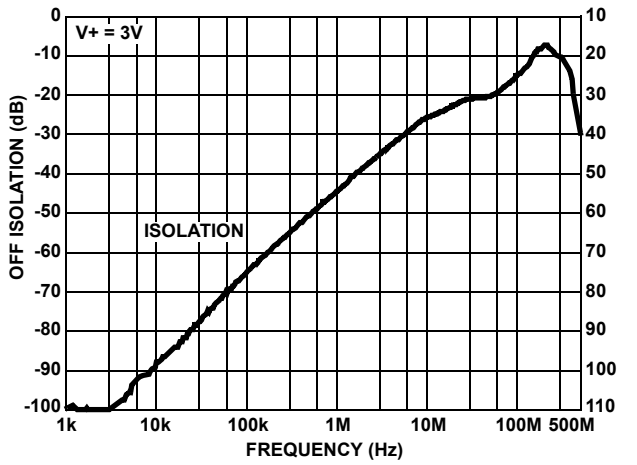


FIGURE 17. OFF-ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND (QFN Paddle Connection: To Ground or Float)

TRANSISTOR COUNT:

228

PROCESS:

Submicron CMOS

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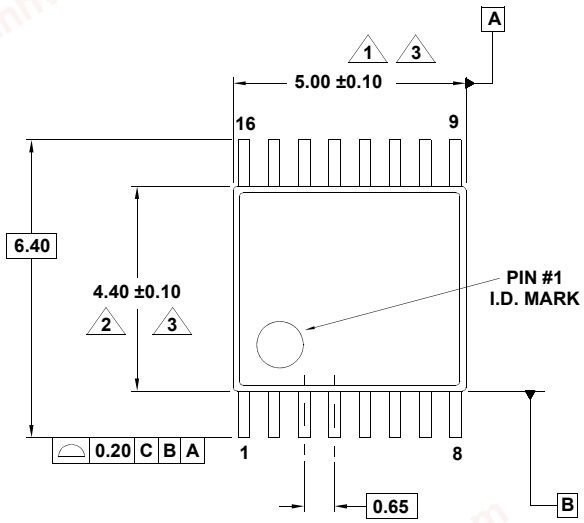
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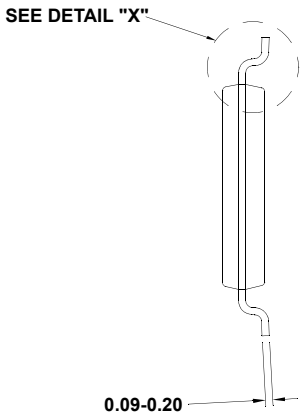
Package Outline Drawing

M16.173

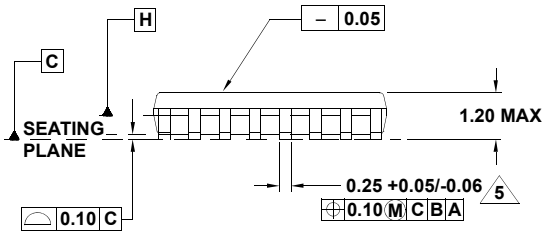
16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



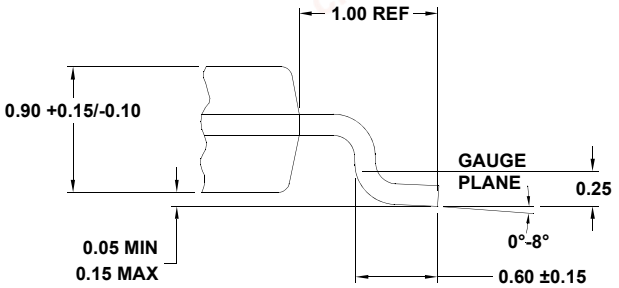
TOP VIEW



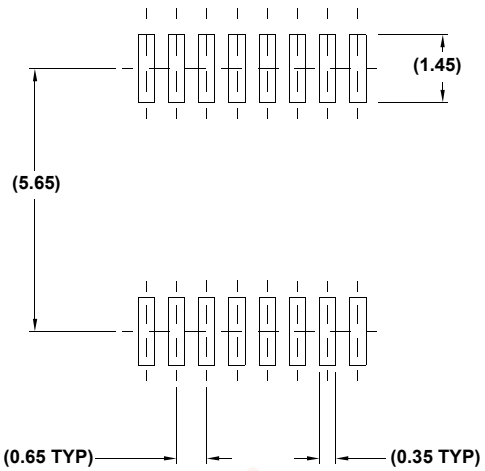
END VIEW



SIDE VIEW



DETAIL "X"



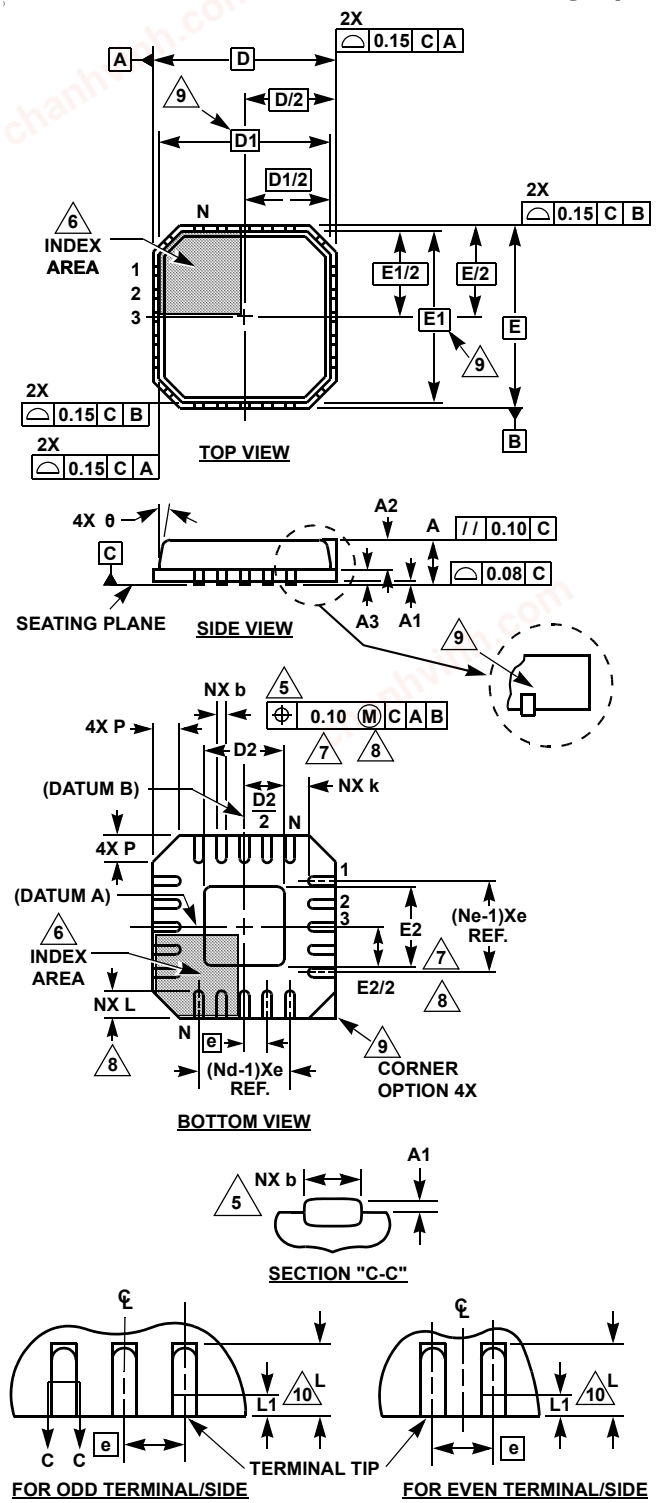
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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Thin Quad Flat No-Lead Plastic Package (TQFN)
Thin Micro Lead Frame Plastic Package (TMLFP)



L16.3x3A

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A2	-	-	0.80	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		3.00 BSC		-
D1		2.75 BSC		9
D2	1.35	1.50	1.65	7, 8, 10
E		3.00 BSC		-
E1		2.75 BSC		9
E2	1.35	1.50	1.65	7, 8, 10
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220WEED-2 Issue C, except for the E2 and D2 MAX dimension.