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Datasheet

ISL83386E

±15kV ESD Protected, +3V to +5.5V, 1µA, 250kbps, RS-232 Transmitters/Receivers with Separate Logic Supply

The ISL83386E contains 3.0V to 5.5V powered RS-232 transmitters/receivers that meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Targeted applications are PDAs, Palmtops, and cell phones in which the low operational power consumption, and even lower standby power consumption is critical. Efficient on-chip charge-pumps, coupled with a manual power-down function reduces the standby supply current to a 1µA trickle. Small footprint packaging and the use of small, low value capacitors ensures board space savings as well. Data rates greater than 250kbps are ensured at worst case load conditions.

The ISL83386E features a V_L pin that adjusts the logic pin (see "Pin Descriptions" on page 3) output levels and input thresholds to values compatible with the V_{CC} powering the external logic (such as a UART).

The single pin powerdown function ($\overline{SHDN}$ = 0) disables all the receiver and transmitter outputs, while shutting down the charge pump to minimize supply current drain.

Table 1 summarizes the features of the ISL83386E, and Application Note AN9863 summarizes the features of each device comprising the 3V RS-232 family.

Related Literatures

For a full list of related documents, visit our website:

- ISL83386E device page

Features

- V_L pin for compatibility with mixed voltage systems
- ESD protection for RS-232 I/O pins to ±15kV (IEC61000)
- Low power, pin compatible upgrade for MAX3386E and SP3203E
- Single $\overline{SHDN}$ pin disables transmitters and receivers
- Meets EIA/TIA-232 and V.28/V.24 specifications at 3V
- On-chip charge pumps require only four external 0.1µF capacitors at V_{CC} = 3.3V
- Receiver hysteresis for improved noise immunity
- Very low supply current: 300µA
- Ensured minimum data rate: 250kbps
- Wide power supply range: Single +3V to +5.5V
- Low supply current in powerdown state: <1µA
- Pb-free available (RoHS compliant)

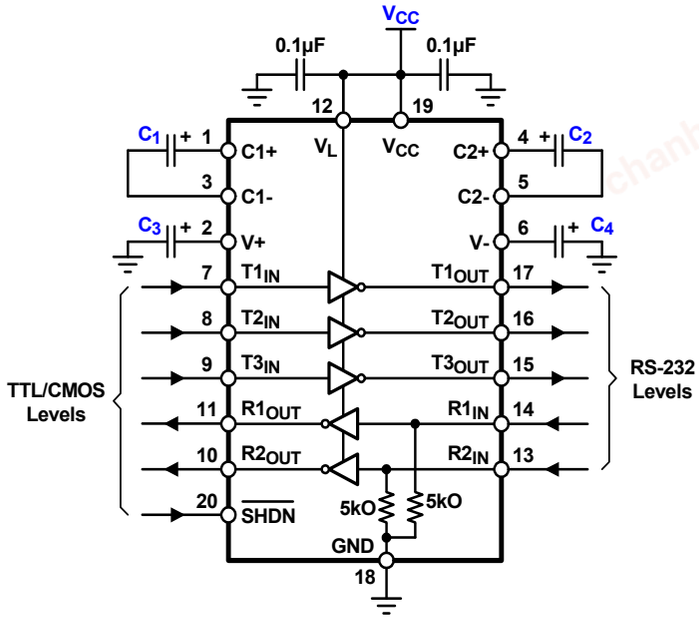
Applications

- Any system requiring RS-232 communication ports
  - Battery powered, hand-held, and portable equipment
  - Laptop computers, Notebooks, Palmtops
  - Digital cameras
  - PDAs and PDA cradles
  - Cellular/mobile phones

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1. Overview

1.1 Typical Operating Circuit



V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.0 - 3.6	0.1	0.1
4.5 - 5.5	0.047	0.33
3.0 - 5.5	0.22	1

Figure 1. Typical Operating Circuit

1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL83386EIVZ	83386EIVZ	-40 to +85	-	20 Ld TSSOP	M20.173
ISL83386EIVZ-T	83386EIVZ	-40 to +85	2.5k	20 Ld TSSOP	M20.173

Notes:

1. See TB347 for details about reel specifications.
2. Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.
3. For Moisture Sensitivity Level (MSL), see the ISL83386E device page. For more information about MSL, see TB363.

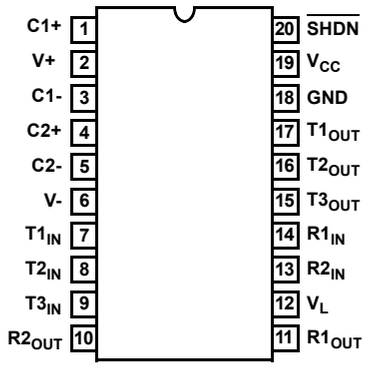
Table 1. Summary of Features

Part Number	No. of Tx.	No. of Rx.	Data Rate (kbps)	Rx. Enable Function?	V_L Logic Supply Pin?	Manual Powerdown?	Automatic Powerdown Function?
ISL83386E	3	2	250	No	Yes	Yes	No

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1.3 Pin Configuration

20 Ld TSSOP
Top View



1.4 Pin Descriptions

Pin	Function
V_{CC}	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	
T_{IN}	TTL/CMOS compatible transmitter inputs. The switching point is a function of the V_L voltage.
T_{OUT}	±15kV ESD protected, RS-232 level (nominally ±5.5V) transmitter outputs.
R_{IN}	±15kV ESD protected, RS-232 compatible receiver inputs.
R_{OUT}	TTL/CMOS level receiver outputs. Swings between GND and V_L.
V_L	Logic-Level Supply. All TTL/CMOS inputs and outputs are powered by this supply.
$\overline{SHDN}$	Active low TTL/CMOS input to tri-state receiver and transmitter outputs and to shut down the on-board power supply to place the device in Low-Power mode. The switching point is a function of the V_L voltage.

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2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{CC} to Ground	-0.3	6	V
V_L to Ground	-0.3	7	V
V+ to Ground	-0.3	7	V
V- to Ground	+0.3	7	V
V+ to V-	14		V
Input Voltages			
T_{IN}, $\overline{SHDN}$	-0.3	6	V
R_{IN}		±28	V
Output Voltages			
T_{OUT}		±13.2	V
R_{OUT}	-0.3V	V_L +0.3V	V
Short Circuit Duration			
T_{OUT}	Continuous		V
ESD Rating	See "ESD Performance" on page 5		

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
20 Ld TSSOP Package	140

Note:
4. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range	-40	+85	°C

2.4 Electrical Specifications

Test conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF, V_L = V_{CC}; unless otherwise specified.
Typicals are at T_A = +25°C, V_{CC} = V_L = 3.3V.

Parameter	Test Conditions	Temp (°C)	Min	Typ	Max	Unit
DC Characteristics						
Supply Current, Powerdown	$\overline{SHDN}$ = GND, all inputs at V_{CC} or GND	+25	-	1	10	µA
Supply Current	All outputs unloaded, $\overline{SHDN}$ = V_{CC}, V_{CC} = 3.15V	+25	-	0.3	1	mA

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Test conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF, V_L = V_{CC}; unless otherwise specified.
Typicals are at T_A = +25°C, V_{CC} = V_L = 3.3V. **(Continued)**

Parameter	Test Conditions		Temp (°C)	Min	Typ	Max	Unit
Logic and Transmitter Inputs							
Input Logic Threshold Low	T_{IN}, $\overline{SHDN}$	V_L = 3.3V or 5V	Full	-	-	0.8	V
		V_L = 2.5V	Full	-	-	0.6	V
Input Logic Threshold High	T_{IN}, $\overline{SHDN}$	V_L = 5V	Full	2.4	-	-	V
		V_L = 3.3V	Full	2.0	-	-	V
		V_L = 2.5V	Full	1.4	-	-	V
		V_L = 1.8V	+25	-	0.9	-	V
Transmitter Input Hysteresis			+25	-	0.5	-	V
Input Leakage Current	T_{IN}, $\overline{SHDN}$		Full	-	±0.01	±1	µA
Receiver Outputs							
Output Leakage Current	V_{CC} = 0V or 3V to 5.5V, $\overline{SHDN}$ = GND		Full	-	±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_L - 0.6	V_L - 0.1	-	V
Receiver Inputs							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low	V_L = 5.0V		+25	0.8	1.5	-	V
	V_L = 3.3V		+25	0.6	1.2	-	V
Input Threshold High	V_L = 5.0V		+25	-	1.8	2.4	V
	V_L = 3.3V		+25	-	1.5	2.4	V
Input Hysteresis			+25	-	0.5	-	V
Input Resistance			+25	3	5	7	kΩ
Transmitter Outputs							
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, transmitter output = ±2V		Full	300	10M	-	Ω
Output Short-Circuit Current	Shorted to GND		Full	-	-	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 5.5V, $\overline{SHDN}$ = GND		Full	-	-	±25	µA
Timing Characteristics							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		Full	250	500	-	kbps
Receiver Propagation Delay	Receiver input to receiver output, C_L = 150pF	t_{PHL}	+25	-	0.15	-	µs
		t_{PLH}	+25	-	0.15	-	µs
Receiver Output Enable Time			+25	-	200	-	ns
Receiver Output Disable Time			+25	-	200	-	ns
Transmitter Output Enable Time	From $\overline{SHDN}$ rising edge to T_{OUT} = ±3.7V		+25	-	100	-	µs
Transmitter Skew	t_{PHL} - t_{PLH} (Note 5)		+25	-	100	-	ns
Receiver Skew	t_{PHL} - t_{PLH}		+25	-	50	-	ns
Transition Region Slew Rate	R_L = 3kΩ to 7kΩ, measured from 3V to -3V or -3V to 3V, V_{CC} = 3.3V	C_L = 150pF to 1000pF	+25	6	18	30	V/µs
		C_L = 150pF to 2500pF	+25	4	13	30	V/µs
ESD Performance							
RS-232 Pins (T_{OUT}, R_{IN})	Human Body Model		+25	-	±15	-	kV
	IEC61000-4-2 Air Gap Discharge		+25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge		+25	-	±8	-	kV

Note:
5. Transmitter skew is measured at the transmitter zero crossing points.

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3. Typical Performance Curves

V_{CC} = 3.3V, T_A = +25°C

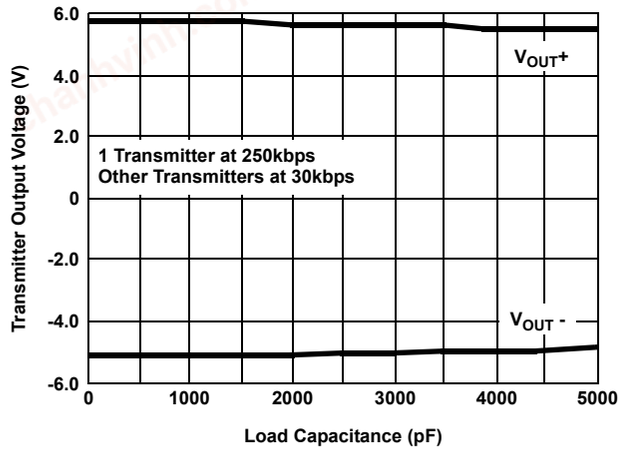


Figure 2. Transmitter Output Voltage vs Load Capacitance

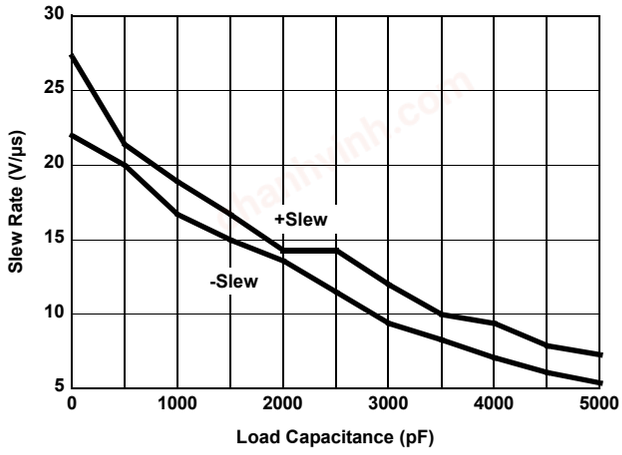


Figure 3. Slew Rate vs Load Capacitance

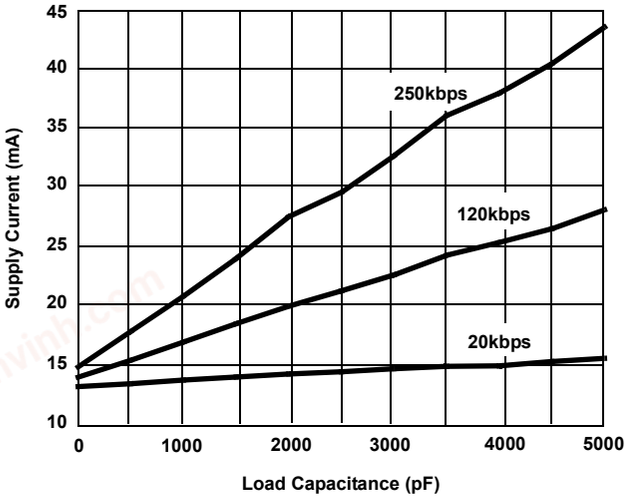


Figure 4. Supply Current vs Load Capacitance when Transmitting Data

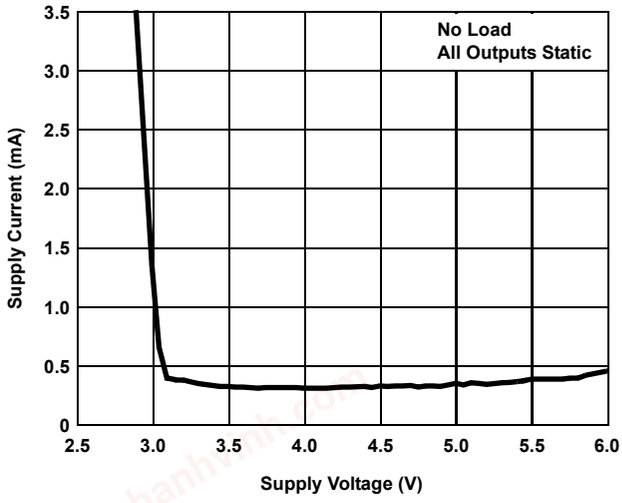


Figure 5. Supply Current vs Supply Voltage

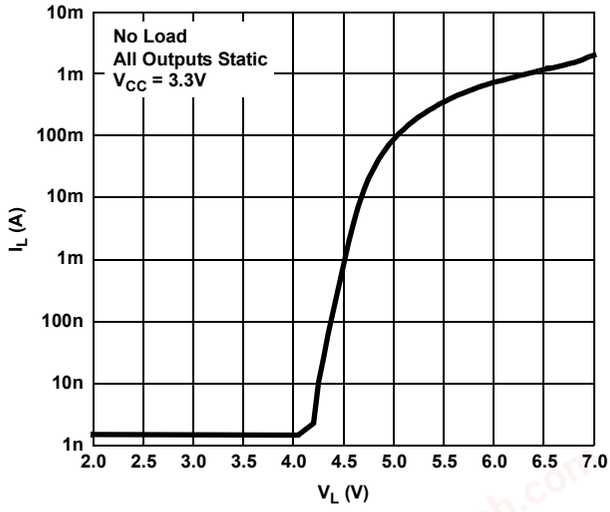


Figure 6. V_L Supply Current vs V_L Voltage

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4. Application Information

The ISL83386E operates from a single +3V to +5.5V supply and requires only four small external capacitors. The device ensures a minimum data rate of 250kbps, features low power consumption, and meets all EIA RS-232C and V.28 specifications.

4.1 Charge Pump

The ISL83386E uses regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. The charge pumps allow the devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external capacitors whose values are listed under the Typical Operating Circuit in Figure 1 on page 2. The charge pumps operate discontinuously (turning off when the V+ and V- supplies are pumped up to the nominal values) and provide significant power savings.

4.1.1 Charge Pump Abs-Max Ratings

These 3V to 5V RS-232 transceivers have been fully characterized for 3.0V to 3.6V operation, and for critical points at 4.5V to 5.5V operation. Furthermore, load conditions were favorable using static logic states only.

The specified maximum values for V+ and V- are +7V and -7V, respectively. These limits apply for V_{CC} values set to 3.0V and 3.6V (see Table 2). For V_{CC} values set to 4.5V and 5.5V, the maximum values for V+ and V- can approach +9V and -7V, respectively (see Table 3 on page 8). Also, the breakdown characteristics for V+ and V- were measured with ±13V.

Table 2. V+ and V- Values for V_{CC} = 3.0V to 3.6V

C_1 (µF)	C_2, C_3, C_4 (µF)	Load	$T1_{IN}$ (Logic State)	V+ (V)		V- (V)	
				V_{CC} = 3.0V	V_{CC} = 3.6V	V_{CC} = 3.0V	V_{CC} = 3.6V
0.1	0.1	Open	H	5.80	6.56	-5.60	-5.88
			L	5.80	6.56	-5.60	-5.88
			2.4kbps	5.80	6.56	-5.60	-5.88
		3kΩ // 1000pF	H	5.88	6.60	-5.56	-5.92
			L	5.76	6.36	-5.56	-5.76
			2.4kbps	6.00	6.64	-5.64	-5.96
0.047	0.33	Open	H	5.68	6.00	-5.60	-5.60
			L	5.68	6.00	-5.60	-5.60
			2.4kbps	5.68	6.00	-5.60	-5.60
		3kΩ // 1000pF	H	5.76	6.08	-5.64	-5.64
			L	5.68	6.04	-5.60	-5.60
			2.4kbps	5.84	6.16	-5.64	-5.72
1	1	Open	H	5.88	6.24	-5.60	-5.60
			L	5.88	6.28	-5.60	-5.64
			2.4kbps	5.80	6.20	-5.60	-5.60
		3kΩ // 1000pF	H	5.88	6.44	-5.64	-5.72
			L	5.88	6.04	-5.64	-5.64
			2.4kbps	5.92	6.40	-5.64	-5.64

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Table 3. V+ and V- Values for V_{CC} = 4.5V to 5.5V

C_1 (µF)	C_2, C_3, C_4 (µF)	Load	$T1_{IN}$ (Logic State)	V+ (V)		V- (V)	
				V_{CC} = 4.5V	V_{CC} = 5.5V	V_{CC} = 4.5V	V_{CC} = 5.5V
0.1	0.1	Open	H	7.44	8.48	-6.16	-6.40
			L	7.44	8.48	-6.16	-6.44
			2.4kbps	7.44	8.48	-6.17	-6.44
		3kΩ // 1000pF	H	7.76	8.88	-6.36	-6.72
			L	7.08	8.00	-5.76	-5.76
			2.4kbps	7.76	8.84	-6.40	-6.64
0.047	0.33	Open	H	6.44	6.88	-5.80	-5.88
			L	6.48	6.88	-5.84	-5.88
			2.4kbps	6.44	6.88	-5.80	-5.88
		3kΩ // 1000pF	H	6.64	7.28	-5.92	-6.04
			L	6.24	6.60	-5.52	-5.52
			2.4kbps	6.72	7.16	-5.92	-5.96
1	1	Open	H	6.84	7.60	-5.76	-5.76
			L	6.88	7.60	-5.76	-5.76
			2.4kbps	6.92	7.56	-5.72	-5.76
		3kΩ // 1000pF	H	7.28	8.16	-5.80	-5.92
			L	6.44	6.84	-5.64	-6.84
			2.4kbps	7.08	7.76	-5.80	-5.80

The resulting new maximum voltages at V+ and V- are listed in Table 4.

Table 4. New Measured Withstanding Voltages

V+, V- to Ground	±13V
V+ to V-	20V

4.2 Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. These transmitters are coupled with the on-chip ±5.5V to deliver true RS-232 levels across a wide range of single supply system voltages.

All transmitter outputs disable and assume a high impedance state when the device enters the Powerdown mode (see Table 5). These outputs can be driven to ±12V when disabled.

All devices ensure a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq 3.0V$.

The transmitter input threshold is set by the voltage applied to the V_L pin. Transmitter inputs float if they remain unconnected (there are no pull-up resistors), and can cause I_{CC} increases. Connect unused inputs to GND for the best performance.

Table 5. Powerdown Truth Table

$\overline{SHDN}$ Input	Transmitter Outputs	Receiver Outputs	Mode of Operation
L	High-Z	High-Z	Manual Powerdown
H	Active	Active	Normal Operation

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4.3 Receivers

The ISL83386E contains standard inverting receivers that convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 7) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions. Receiver outputs swing from GND to V_L and tristate in powerdown.

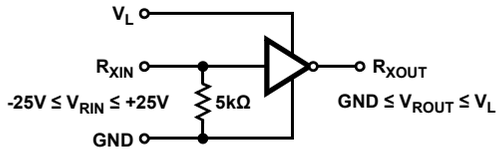


Figure 7. Receiver Connections

4.4 Low Power Operation

During normal operation (not in powerdown mode), this 3V device requires a nominal supply current of 0.3mA, even at V_{CC} = 5.5V. This current is considerably less than the 11mA current required by comparable 5V RS-232 devices and it allows you to reduce system power simply by replacing the old style device with the ISL83386E in new designs.

4.5 Powerdown Functionality

The already low current requirement drops significantly when the device enters powerdown mode. In power-down, the supply current drops to 1µA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND) and the transmitter and receiver outputs tri-state. This micro-power mode makes the devices ideal for battery powered and portable applications.

4.5.1 Software Controlled (Manual) Powerdown

The ISL83386E can be forced into its low power, standby state through a simple shutdown ($\overline{SHDN}$) pin (see Figure 8). Driving this pin high enables normal operation, while driving it low forces the IC into its powerdown state. The time required to exit powerdown and resume transmission is less than 100µs. Connect $\overline{SHDN}$ to V_{CC} if the powerdown function is not needed.

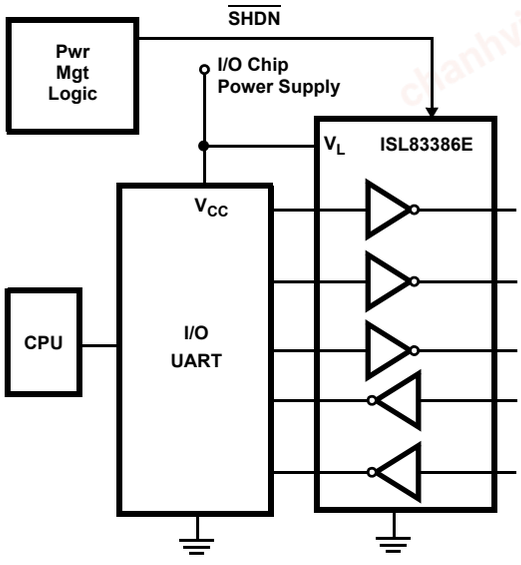


Figure 8. Connections for Manual Powerdown

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4.6 V_L Logic Supply Input

Unlike other RS-232 interface devices in which the CMOS outputs swing between 0 and V_{CC}, the ISL83386E features a separate logic supply input (V_L; 1.8V to 5V, regardless of V_{CC}) that sets V_{OH} for the receiver outputs. Connecting V_L to a host logic supply lower than V_{CC} prevents the ISL83386E outputs from forward biasing the input diodes of a logic device powered by the lower supply. Connecting V_L to a logic supply greater than V_{CC} ensures that the receiver output levels are compatible even with the CMOS input V_{IH} of AC, HC, and CD4000 devices. Note: the V_L supply current increases to 100µA with V_L = 5V and V_{CC} = 3.3V (see Figure 6 on page 6). V_L also powers the transmitter and logic inputs, and sets their switching thresholds to levels compatible with the logic supply. This separate logic supply pin allows a great deal of flexibility in interfacing to systems with different logic supplies. If logic translation is not required, connect V_L to the ISL83386E V_{CC} pin.

4.7 Capacitor Selection

The ISL83386E charge pumps require only four small capacitors for the full operational voltage range. Their values depend on the applied supply voltage and are listed in Table 6. Do not use values smaller than those listed in the table. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption.

Table 6. Required Capacitor Values

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.22	1

Make sure that the capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with larger nominal values. The capacitor's Equivalent Series Resistance (ESR), usually rises at low temperatures, which might slightly increase the ripple on V+ and V-.

4.8 Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

4.9 Transmitter Outputs when Exiting Powerdown

Figure 9 shows the response of two transmitter outputs when exiting powerdown mode. As the transmitter outputs activate, the two properly go to opposite RS-232 levels, with no glitching, ringing, or undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

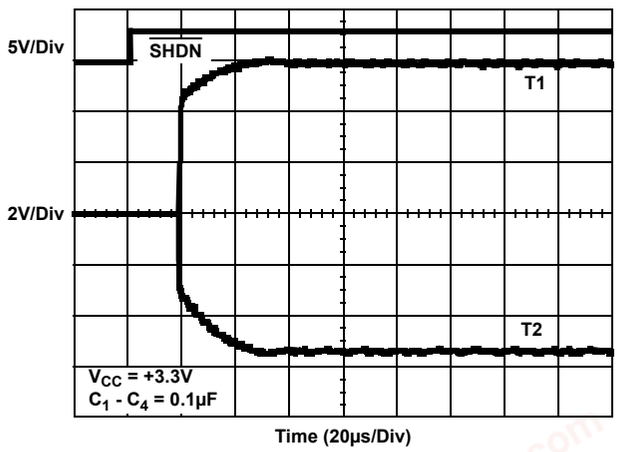


Figure 9. Transmitter Outputs when Exiting Powerdown

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4.10 High Data Rates

The ISL83386E maintains the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 10 shows a transmitter loopback test circuit, and Figure 11 on page 11 shows the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 12 on page 11 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

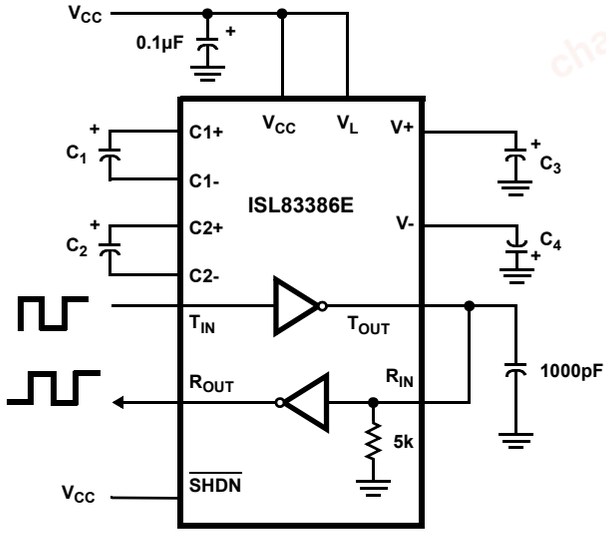


Figure 10. Transmitter Loopback Test Circuit

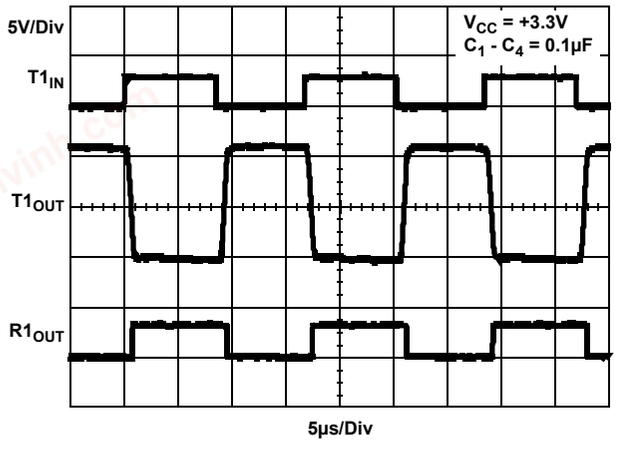


Figure 11. Loopback Test at 120kbps

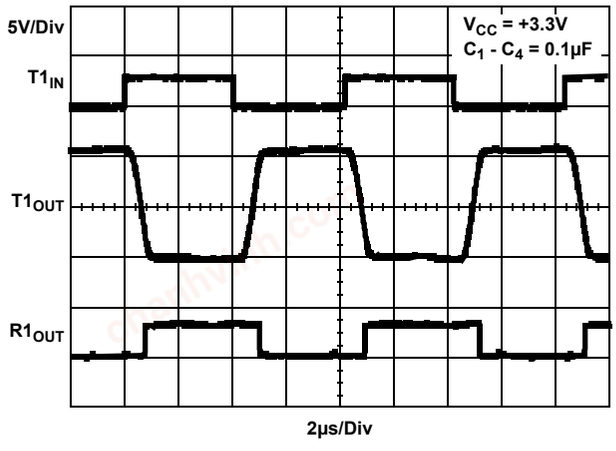


Figure 12. Loopback Test at 250kbps

4.11 Interconnection with 3V and 5V Logic

Standard 3.3V powered RS-232 devices interface well with 3V and 5V powered TTL compatible logic families (for example, ACT and HCT), but the logic outputs (for example, R_{OUTS}) fail to reach the V_{IH} level of 5V powered CMOS families like HC, AC, and CD4000. The ISL83386E V_L supply pin solves this problem. By connecting V_L to the same supply (1.8V to 5V) powering the logic device, the ISL83386E logic outputs swing from GND to the logic V_{CC}.

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5. ±15kV ESD Protection

All pins on the 3V interface devices include ESD protection structures, but the ISL83386E incorporates advanced structures that allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. The ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and do not interfere with RS-232 signals as large as ±25V.

5.1 Human Body Model (HBM) Testing

The Human Body Model (HBM) test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor and makes the test less severe than the IEC61000 test, which uses a 330Ω limiting resistor. The HBM method determines an IC's ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

5.2 IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment that meets Level 4 criteria without the need for additional board level protection on the RS-232 port.

5.3 Air-Gap Discharge Test Method

For the Air-Gap Discharge test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, and temperature, so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

5.4 Contact Discharge Test Method

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, and eliminates the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

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6. Die Characteristics

Substrate Potential (Powered Up)	GND
Transistor Count	422
Process	Si Gate CMOS

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7. Revision History

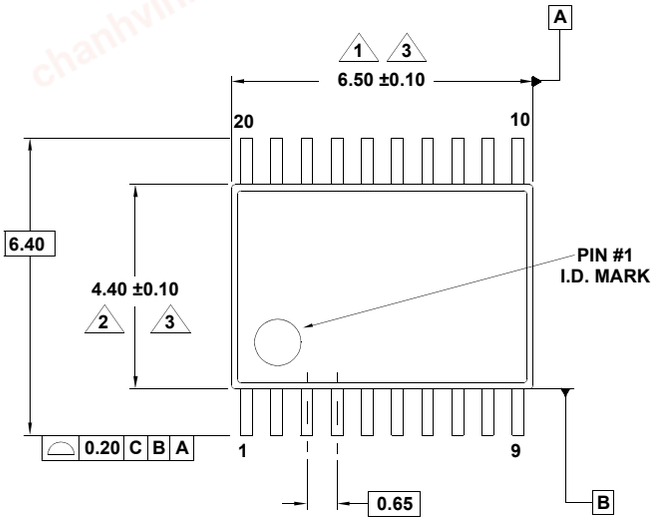
Rev.	Date	Description
3.00	Apr.19.19	Updated to new template. Updated links. Added “Charge Pump Abs Max Ratings” on page 7. Updated disclaimer.
2.00	Sep.24.18	Applied Renesas Header/Footer. Added Related Literature Updated Ordering Information table by removing retired parts, updating column headers and adding Notes 1 and 3. Updated Figure 1 on page 2. Updated Abs Max section R_{IN} changed from ±25 to ±28. Updated Detailed Description section. Updated Charge Pump section. Updated Capacitor Selection section. Added Revision History and updated disclaimer. Updated POD M20.173 to the latest revision. The changes are as follows: Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes.

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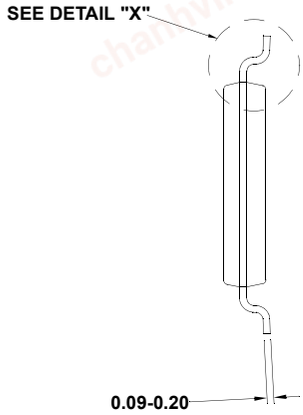
8. Package Outline Drawing

For the most recent package outline drawing, see M20.173.

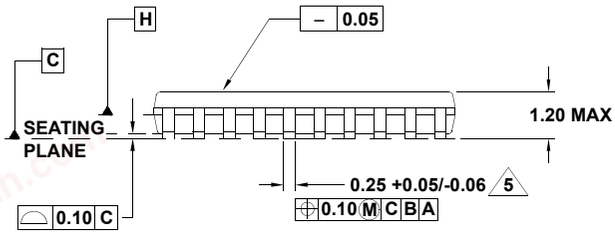
M20.173
20 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



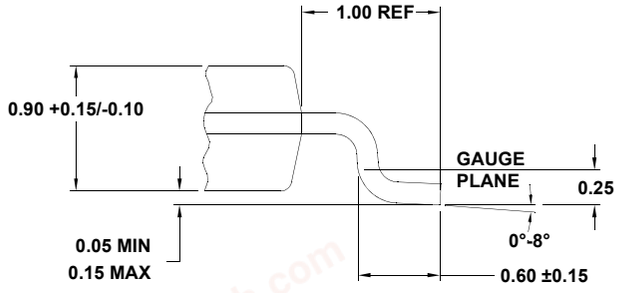
TOP VIEW



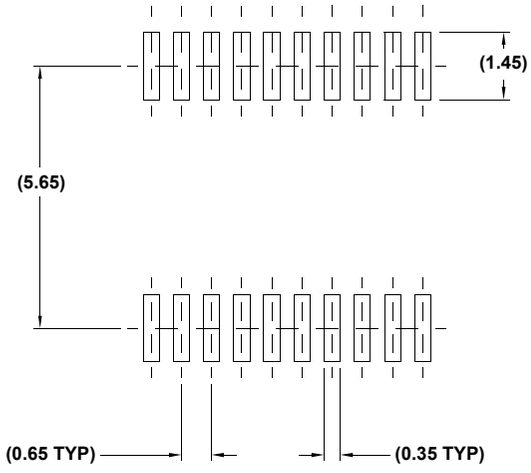
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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