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DATASHEET

ISL83080E/82E/83E/85E/86E/88E

±15kV ESD, 5V, Full Fail-Safe, 1/8 Unit Load, RS-485/RS-422 Transceivers

FN6085
Rev 10.01
Jul 5, 2022

The ISL8308xE (ISL83080E, ISL83082E, ISL83083E, ISL83085E, ISL83086E, ISL83088E) are BiCMOS, ESD protected, 5V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. Each driver output, and receiver input, is protected against ±15kV ESD strikes without latch-up, and unlike competitive products, this family is specified for 10% tolerance supplies (4.5V to 5.5V).

These devices have very low bus currents (+125µA/-75µA), so they present a true 1/8 unit load to the RS-485 bus. This allows up to 256 transceivers on the network without violating the RS-485 specification's 32 unit load maximum, and without using repeaters. For example, in a remote utility meter reading system, individual meter readings are routed to a concentrator via an RS-485 network, so the high allowed node count minimizes the number of repeaters required. Data for all meters is then read out from the concentrator via a single access port, or a wireless link.

Receiver (Rx) inputs feature a "Full Fail-Safe" design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or terminated but undriven.

The ISL83080E, ISL83082E, ISL83083E, ISL83085E use slew rate limited drivers which reduce EMI, and minimize reflections from improperly terminated transmission lines, or unterminated stubs in multidrop and multipoint applications. Slew rate limited versions also include receiver input filtering to enhance noise immunity in the presence of slow input signals.

Hot Plug circuitry ensures that the Tx and Rx outputs remain in a high impedance state until the power supply has stabilized, and the Tx outputs are fully short circuit protected.

The ISL83080E, ISL83083E, ISL83086E are configured for full duplex (separate Rx input and Tx output pins) applications. The half duplex versions multiplex the Rx inputs and Tx outputs to allow transceivers with output disable functions in 8 Ld packages.

Features

- Pb-Free Available (RoHS Compliant)
- RS-485 I/O Pin ESD Protection . . . . . ±15kV HBM
  Class 3 ESD Protection (HBM) on all Pins. . . . . >7kV
- Tiny MSOP Packages Save 50% Board Space
- Full Fail-Safe (Open, Short, Terminated and Floating) Receivers
- Hot Plug Circuitry (ISL83080E, ISL83082E, ISL83083E, ISL83085E)
  - Tx and Rx Outputs Remain Three-state During Power-up/Power-down
- True 1/8 Unit Load Allows up to 256 Devices on the Bus
- Specified for Single 5V, 10% Tolerance, Supplies
- High Data Rates. . . . . up to 10Mbps
- Low Quiescent Supply Current 530µA
  Ultra Low Shutdown Supply Current 70nA
- -7V to +12V Common Mode Input Voltage Range
- Half and Full Duplex Pinouts
- Three-State Rx and Tx Outputs
- Current Limiting and Thermal Shutdown for driver Overload Protection

Applications

- Automated Utility Meter Reading Systems
- High Node Count Systems
- Factory Automation
- Field Bus Networks
- Security Camera Networks
- Building Environmental Control Systems
- Industrial/Process Control Networks

TABLE 1. SUMMARY OF FEATURES

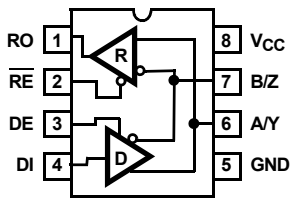
PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED?	HOT PLUG	# DEVICES ON BUS	Rx/Tx ENABLE?	QUIESCENT I_{CC} (µA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL83080E	Full	0.115	Yes	Yes	256	Yes	530	Yes	10, 14
ISL83082E	Half	0.115	Yes	Yes	256	Yes	530	Yes	8
ISL83083E	Full	0.5	Yes	Yes	256	Yes	530	Yes	10, 14
ISL83085E	Half	0.5	Yes	Yes	256	Yes	530	Yes	8
ISL83086E	Full	10	No	No	256	Yes	530	Yes	10, 14
ISL83088E	Half	10	No	No	256	Yes	530	Yes	8

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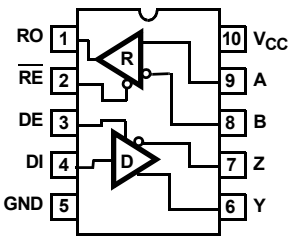
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Pinouts

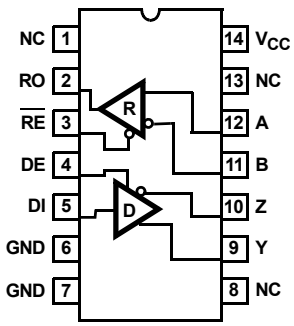
ISL83082E, ISL83085E, ISL83088E
(8 LD MSOP, SOIC)
TOP VIEW



ISL83080E, ISL83083E, ISL83086E
(10 LD MSOP)
TOP VIEW



ISL83080E, ISL83083E, ISL83086E
(14 LD SOIC)
TOP VIEW



Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z *	High-Z*

NOTE: *Shutdown Mode (See Note 11).

RECEIVING				
INPUTS				OUTPUT
$\overline{RE}$	DE Half Duplex	DE Full Duplex	A-B	RO
0	0	X	≥ -0.05V	1
0	0	X	≤ -0.2V	0
0	0	X	Inputs Open/Shorted	1
1	0	0	X	High-Z*
1	1	1	X	High-Z

NOTE: *Shutdown Mode (See Note 11).

Pin Descriptions

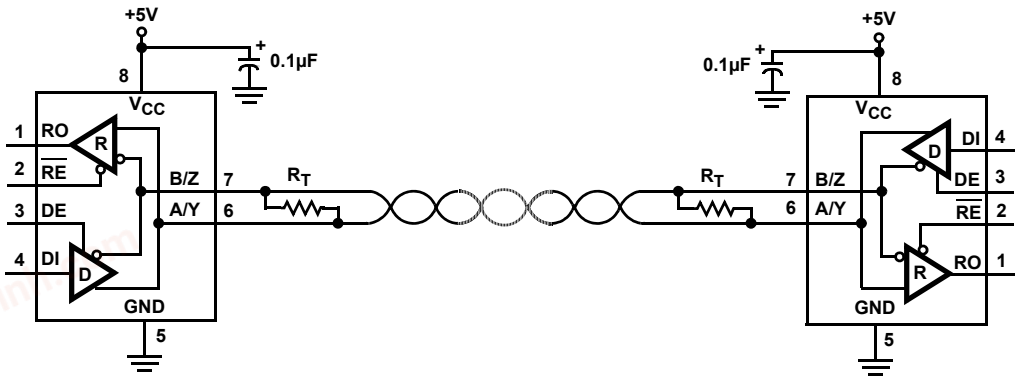
PIN	FUNCTION
RO	Receiver output: If A - B ≥ -50mV, RO is high; If A - B ≤ -200mV, RO is low; RO = High if A and B are unconnected (floating) or shorted.
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	±15kV HBM ESD Protected RS-485/RS-422 level, noninverting receiver input and noninverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.

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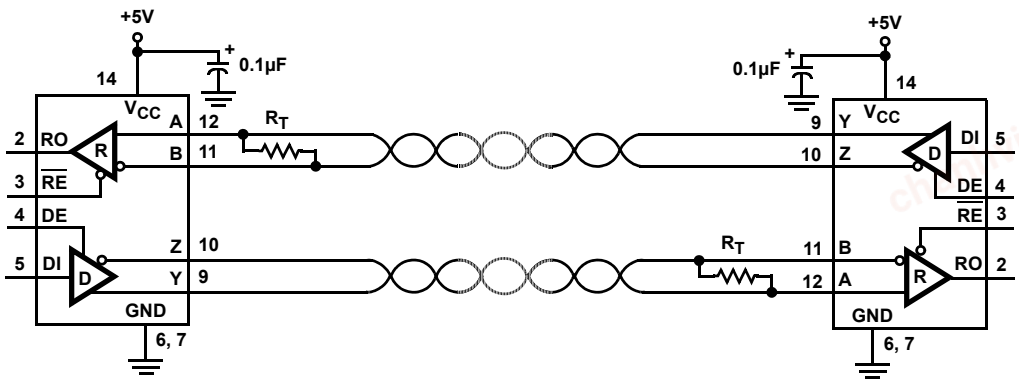
Pin Descriptions (Continued)

PIN	FUNCTION
B/Z	±15kV HBM ESD Protected RS-485/RS-422 level, Inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
A	±15kV HBM ESD Protected RS-485/RS-422 level, noninverting receiver input.
B	±15kV HBM ESD Protected RS-485/RS-422 level, inverting receiver input.
Y	±15kV HBM ESD Protected RS-485/RS-422 level, noninverting driver output.
Z	±15kV HBM ESD Protected RS-485/RS-422 level, inverting driver output.
V_{CC}	System power supply input (4.5V to 5.5V).
NC	No Connection.

Typical Operating Circuit



ISL83082E, ISL83085E, ISL83088E



ISL83080E, ISL83083E, ISL83086E

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Ordering Information

PART NUMBER (Note 2)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP. RANGE
ISL83080EIBZ	83080EIBZ	14 Ld SOIC	M14.15	Tube	-40 to +85°C
ISL83080EIBZ-T				Reel, 2.5k	
ISL83080EIUZ	3080Z	10 Ld MSOP	M10.118	Tube	
ISL83080EIUZ-T				Reel, 2.5k	
ISL83082EIBZ	83082 EIBZ	8 Ld SOIC	M8.15	Tube	
ISL83082EIBZ-T				Reel, 2.5k	
ISL83082EIUZ	3082Z	8 Ld MSOP	M8.118	Tube	
ISL83082EIUZ-T				Reel, 2.5k	
ISL83083EIBZ	83083EIBZ	14 Ld SOIC	M14.15	Tube	
ISL83083EIBZ-T				Reel, 2.5k	
ISL83083EIUZ	3083Z	10 Ld MSOP	M10.118	Tube	
ISL83083EIUZ-T				Reel, 2.5k	
ISL83085EIBZ	83085 EIBZ	8 Ld SOIC	M8.15	Tube	
ISL83085EIBZ-T				Reel, 2.5k	
ISL83085EIUZ	3085Z	8 Ld MSOP	M8.118	Tube	
ISL83085EIUZ-T				Reel, 2.5k	
ISL83086EIBZ	83086EIBZ	14 Ld SOIC	M14.15	Tube	
ISL83086EIBZ-T				Reel, 2.5k	
ISL83086EIUZ	3086Z	10 Ld MSOP	M10.118	Tube	
ISL83086EIUZ-T				Reel, 2.5k	
ISL83088EIBZ	83088 EIBZ	8 Ld SOIC	M8.15	Tube	
ISL83088EIBZ-T				Reel, 2.5k	
ISL83088EIUZ	3088Z	8 Ld MSOP	M8.118	Tube	
ISL83088EIUZ-T				Reel, 2.5k	

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL83080E, ISL83082E, ISL83083E, ISL83085E, ISL83086E, ISL83088E product pages. For more information about MSL, see TB363.

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Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . . -0.3V to (V_{CC} + 0.3V)
Input/Output Voltages
A, B, Y, Z . . . . . -9V to +13V
A, B, Y, Z (Transient Pulse Through 100Ω, Note 14) . . . . . ±75V
RO . . . . . -0.3V to (V_{CC} + 0.3V)
Short Circuit Duration
Y, Z . . . . . Continuous
ESD Rating . . . . . See Specification Table

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
8 Ld SOIC Package	105
8 Ld MSOP Package	140
10 Ld MSOP Package	190
14 Ld SOIC Package	128

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 6).

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
DC CHARACTERISTICS								
Driver Differential V_{OUT} (no load)	V_{OD1}	R_L = ∞		Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (with load)	V_{OD2}	R_L = 100Ω (RS-422) (Figure 1A)		Full	2	2.9	-	V
		R_L = 54Ω (RS-485) (Figure 1A)		Full	1.5	2.4	-	V
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 1B)		Full	1.5	2.6	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	2.85	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	0.01	0.1	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	0.8	V
DI Input Hysteresis Voltage	V_{HYS}			25	-	100	-	mV
Logic Input Current	I_{IN1}	DE, DI, $\overline{RE}$		Full	-2	-	2	µA
Input Current (A, B)	I_{IN2}	DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	70	125	µA
			V_{IN} = -7V	Full	-75	55	-	µA
Output Leakage Current (Y, Z) (Full Duplex Versions Only)	I_{IN3}	$\overline{RE}$ = 0V, DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	7	125	µA
			V_{IN} = -7V	Full	-75	11	-	µA
Output Leakage Current (Y, Z) in Shutdown Mode (Full Duplex)	I_{IN3}	$\overline{RE}$ = V_{CC}, DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	0	20	µA
			V_{IN} = -7V	Full	-20	9	-	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V (Note 8)		Full	-	-	±250	mA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-200	-90	-50	mV

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Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 6). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V	25	-	20	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = -50mV	Full	V_{CC} - 1	4.6	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = -200mV	Full	-	0.2	0.4	V
Three-State (high impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V	Full	-1	0.03	1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V	Full	96	160	-	kΩ
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}	Full	±7	-	±85	mA
SUPPLY CURRENT							
No-Load Supply Current (Note 7)	I_{CC}	Half Duplex Versions, DE = V_{CC}, $\overline{RE}$ = X, DI = 0V or V_{CC}	Full	-	560	700	µA
		All Versions, DE = 0V, $\overline{RE}$ = 0V, or Full Duplex Versions, DE = V_{CC}, $\overline{RE}$ = X. DI = 0V or V_{CC}	Full	-	530	650	µA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}	Full	-	0.07	2	µA
ESD PERFORMANCE							
RS-485 Pins (A, Y, B, Z)		Human Body Model (HBM), Pin to GND	25	-	±15	-	kV
All Other Pins		HBM, per MIL-STD-883 Method 3015	25	-	±7	-	kV
		Machine Model	25	-	> ±250	-	V
DRIVER SWITCHING CHARACTERISTICS (115kbps Versions; ISL83080E, ISL83082E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	500	780	1300	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	-	40	100	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	667	1000	1500	ns
Maximum Data Rate	f_{MAX}	C_D = 820pF (Figure 4) (Note 15)	Full	115	666	-	kbps
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 3), (Note 9)	Full	-	278	1500	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 3) (Note 9)	Full	-	35	1500	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 15pF, SW = V_{CC} (Figure 3)	Full	-	67	100	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 15pF, SW = GND (Figure 3)	Full	-	38	100	ns
Time to Shutdown	t_{SHDN}	(Note 11)	Full	60	160	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 3) (Notes 11, 12)	Full	-	400	2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 3) (Notes 11, 12)	Full	-	155	2000	ns
DRIVER SWITCHING CHARACTERISTICS (500kbps Versions; ISL83083E, ISL83085E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	250	360	1000	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	-	20	100	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	200	475	750	ns
Maximum Data Rate	f_{MAX}	C_D = 820pF (Figure 4) (Note 15)	Full	500	1000	-	kbps

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Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 6). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 3), (Note 9)	Full	-	137	1000	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 3), (Note 9)	Full	-	35	1000	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 15pF, SW = V_{CC} (Figure 3)	Full	-	65	100	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 15pF, SW = GND (Figure 3),	Full	-	38	100	ns
Time to Shutdown	t_{SHDN}	(Note 11)	Full	60	160	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 3), (Notes 11, 12)	Full	-	260	1500	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 3), (Notes 11, 12)	Full	-	155	1500	ns
DRIVER SWITCHING CHARACTERISTICS (10Mbps Versions; ISL83086E, ISL83088E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	-	20	60	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	-	1	10	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	-	13	25	ns
Maximum Data Rate	f_{MAX}	C_D = 470pF (Figure 4) (Note 15)	Full	10	15	-	Mbps
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 3), (Note 9)	Full	-	35	150	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 3), (Note 9)	Full	-	30	150	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 15pF, SW = V_{CC} (Figure 3)	Full	-	66	100	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 15pF, SW = GND (Figure 3)	Full	-	38	100	ns
Time to Shutdown	t_{SHDN}	(Note 11)	Full	60	160	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 3), (Notes 11, 12)	Full	-	115	250	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 3), (Notes 11, 12)	Full	-	84	250	ns
RECEIVER SWITCHING CHARACTERISTICS (115kbps and 500kbps Versions; ISL83080E THRU ISL83085E)							
Maximum Data Rate	f_{MAX}	(Figure 5) (Note 15)	Full	0.5	10	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 5)	Full	-	100	150	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 5)	Full	-	7	10	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6), (Note 10)	Full	-	10	50	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6), (Note 10)	Full	-	10	50	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6)	Full	-	10	50	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6),	Full	-	10	50	ns
Time to Shutdown	t_{SHDN}	(Note 11)	Full	60	160	600	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6), (Notes 11, 13)	Full	-	150	2000	ns

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Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 6). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6), (Notes 11, 13)	Full	-	150	2000	ns
RECEIVER SWITCHING CHARACTERISTICS (10Mbps Versions; ISL83086E, ISL83088E)							
Maximum Data Rate	f_{MAX}	(Figure 5) (Note 15)	Full	10	15	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 5)	Full	-	70	125	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 5)	Full	-	0	10	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6) (Note 10)	Full	-	10	30	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6) (Note 10)	Full	-	10	30	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6)	Full	-	10	30	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6)	Full	-	10	30	ns
Time to Shutdown	t_{SHDN}	(Note 11)	Full	60	160	600	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6) (Notes 11, 13)	Full	-	150	2000	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6) (Notes 11, 13)	Full	-	150	2000	ns

NOTES:

5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
6. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
7. Supply current specification is valid for loaded drivers when DE = 0V.
8. Applies to peak current. See “Typical Performance Curves” beginning on page 12 for more information.
9. Keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
10. The $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
11. Transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See “Low Power Shutdown Mode” on page 12.
12. Keep $\overline{RE}$ = VCC, and set the DE signal low time >600ns to ensure that the device enters SHDN.
13. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.
14. Tested according to TIA/EIA-485-A, section 4.2.6 (±75V for 15µs at a 1% duty cycle).
15. Limits established by characterization and are not production tested.

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Test Circuits and Waveforms

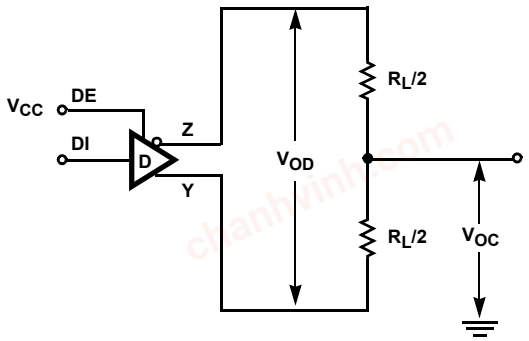


FIGURE 1A. V_{OD} AND V_{OC}

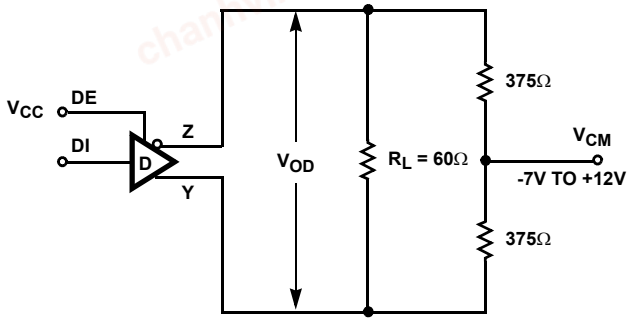


FIGURE 1B. V_{OD} WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

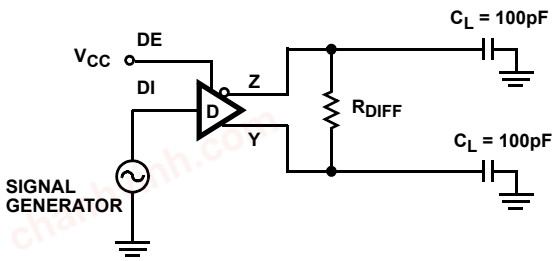


FIGURE 2A. TEST CIRCUIT

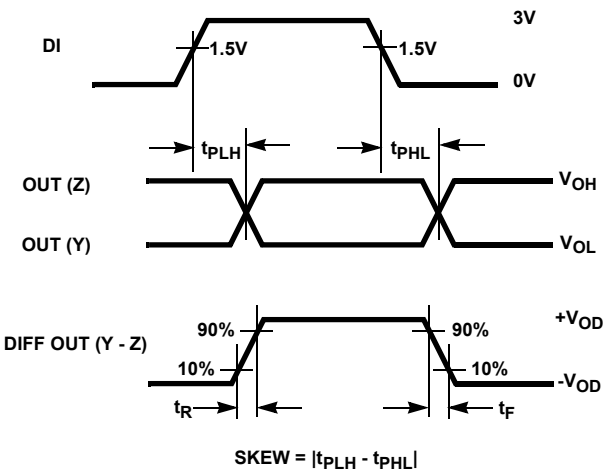
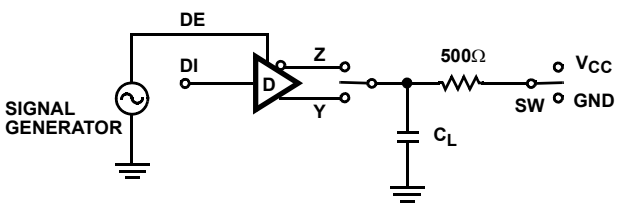


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	15
t_{LZ}	Y/Z	X	0/1	V_{CC}	15
t_{ZH}	Y/Z	0 (Note 9)	1/0	GND	100
t_{ZL}	Y/Z	0 (Note 9)	0/1	V_{CC}	100
$t_{ZH(SHDN)}$	Y/Z	1 (Note 12)	1/0	GND	100
$t_{ZL(SHDN)}$	Y/Z	1 (Note 12)	0/1	V_{CC}	100

FIGURE 3A. TEST CIRCUIT

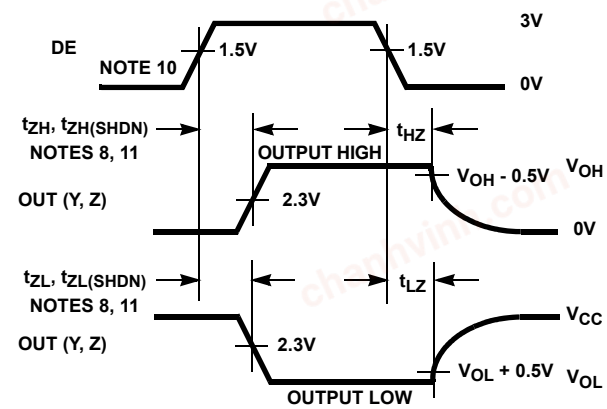


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

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Test Circuits and Waveforms (Continued)

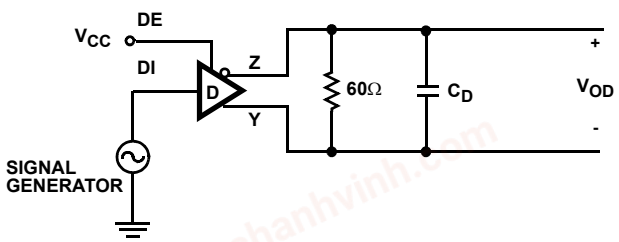


FIGURE 4A. TEST CIRCUIT

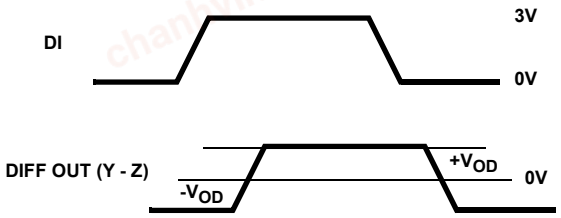


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER DATA RATE

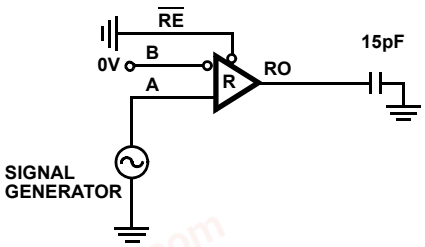


FIGURE 5A. TEST CIRCUIT

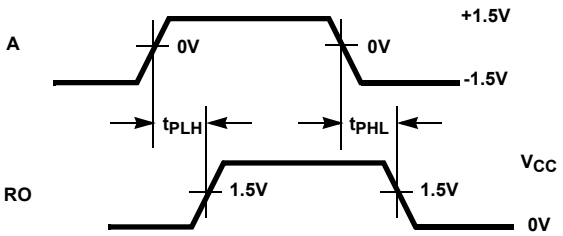
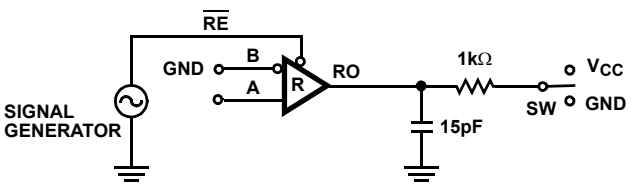


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 10)	0	+1.5V	GND
t_{ZL} (Note 10)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 13)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 13)	0	-1.5V	V_{CC}

FIGURE 6A. TEST CIRCUIT

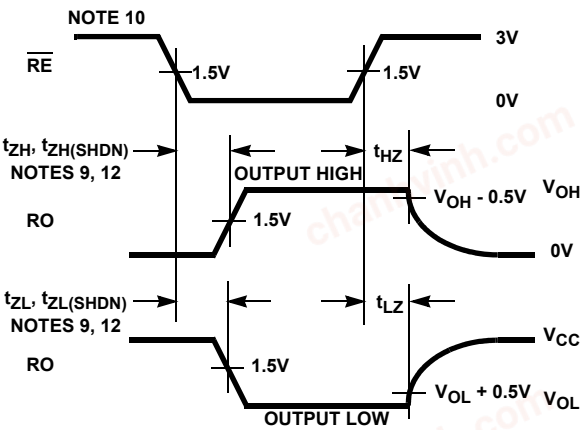


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES

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Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

These devices utilize a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input resistance of 96kΩ surpasses the RS-422 specification of 4kΩ, and is eight times the RS-485 "Unit Load (UL)" requirement of 12kΩ minimum. Thus, these products are known as "one-eighth UL" transceivers, and there can be up to 256 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common mode voltages as great as ±7V outside the power supplies (i.e., +12V and -7V), making them ideal for long networks where induced voltages are a realistic concern.

All the receivers include a "full fail-safe" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating) or shorted.

Receivers easily meet the data rates supported by the corresponding driver, and all receiver outputs are three-statable through the active low $\overline{RE}$ input.

Driver Features

The RS-485/RS-422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485), and at least 2V across a 100Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI.

All drivers are three-statable through the active high DE input.

The 115kbps and 500kbps driver outputs are slew rate limited to minimize EMI, and to minimize reflections in unterminated or improperly terminated networks. Outputs of the ISL83086E, ISL83088E drivers are not limited, so faster output transition times allow data rates of at least 10Mbps.

Hot Plug Function

When a piece of equipment powers up, there is a period of time where the processor or ASIC driving the RS-485 control lines (DE, $\overline{RE}$) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the ISL83080, ISL83082, ISL83083, ISL83085 versions incorporate a "Hot Plug" function. Circuitry monitoring V_{CC} ensures that, during power-up and power-down, the Tx and Rx outputs remain disabled, regardless of the state of DE and $\overline{RE}$, if V_{CC} is less than ~3.4V. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

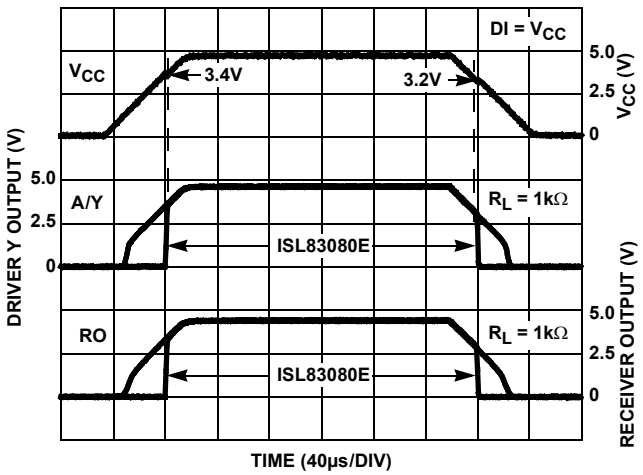


FIGURE 7. HOT PLUG PERFORMANCE (ISL83080E) vs DEVICE WITHOUT HOT PLUG CIRCUITRY (ISL83086E)

ESD Protection

All pins on these devices include class 3 Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (e.g., transient suppression diodes), and the associated, undesirable capacitive load they present.

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Data Rate, Cables, and Terminations

RS-485/RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Devices operating at 10Mbps are limited to lengths less than 100', while the 115kbps versions can operate at full data rates with lengths of several 1000'.

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative (when using the 10Mbps devices) to minimize reflections. Short networks using the 115kbps versions need not be terminated, but, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. These devices meet this requirement via driver output short circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 specification, even at the common mode voltage range extremes. Additionally, these devices utilize a foldback circuit which reduces the short circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short circuit condition, devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about +15°C. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts, but they also include a shutdown feature that reduces the already low quiescent I_{CC} to a 70nA trickle. These devices enter shutdown whenever the receiver and driver are ***simultaneously*** disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver will not enter shutdown.

Note that receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 9 thru 13, at the end of the "Electrical Specification Table" on page 8, for more information.

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified

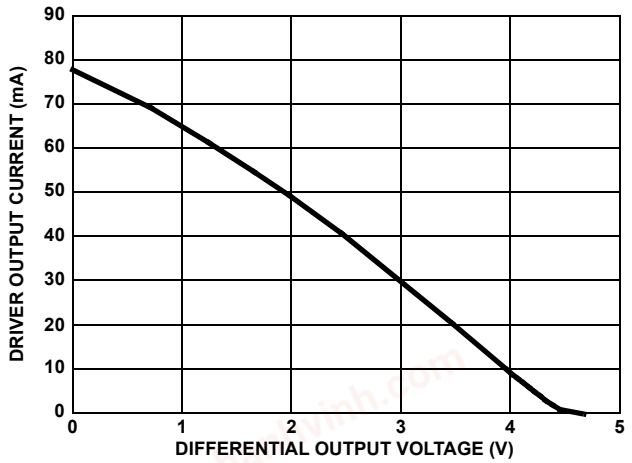


FIGURE 8. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

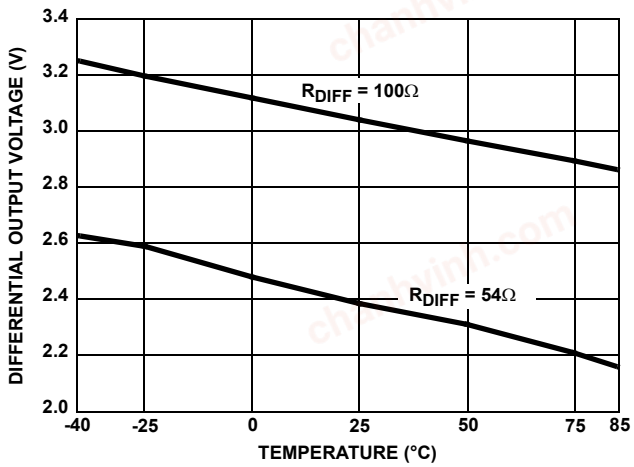


FIGURE 9. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

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Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified **(Continued)**

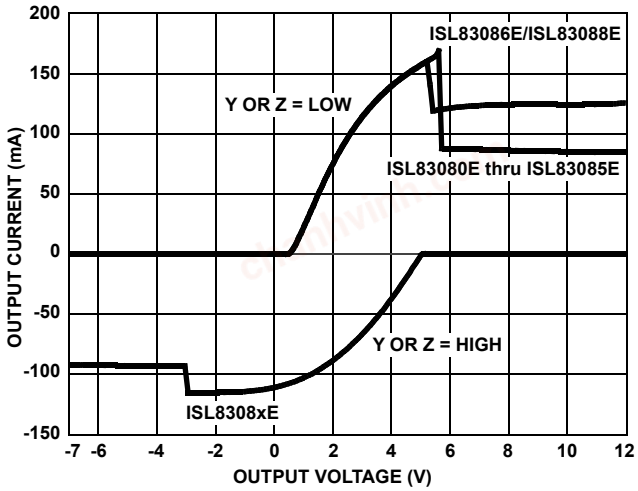


FIGURE 10. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

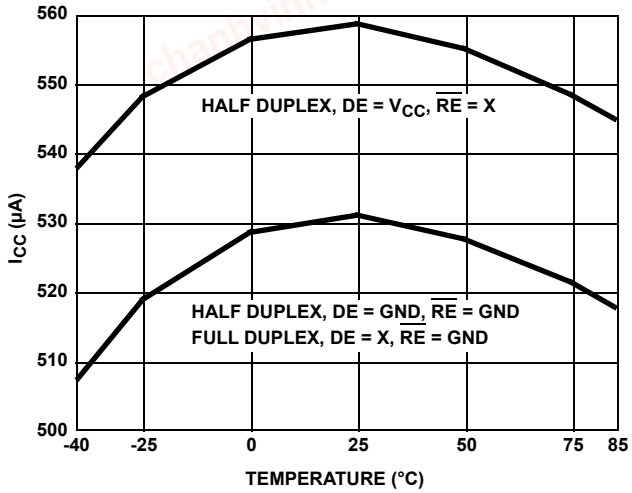


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

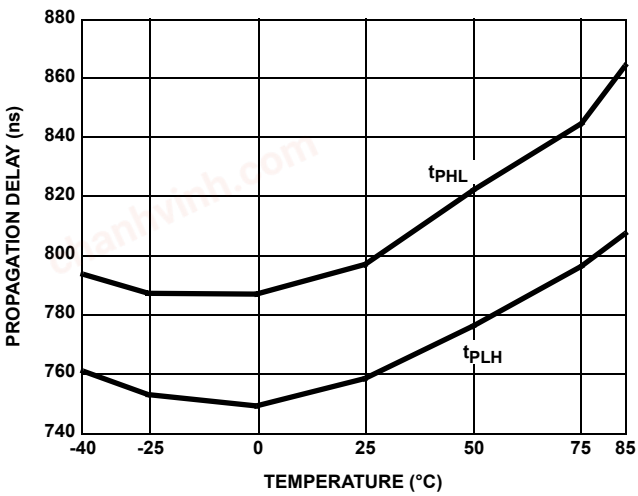


FIGURE 12. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL83080E, ISL83082E)

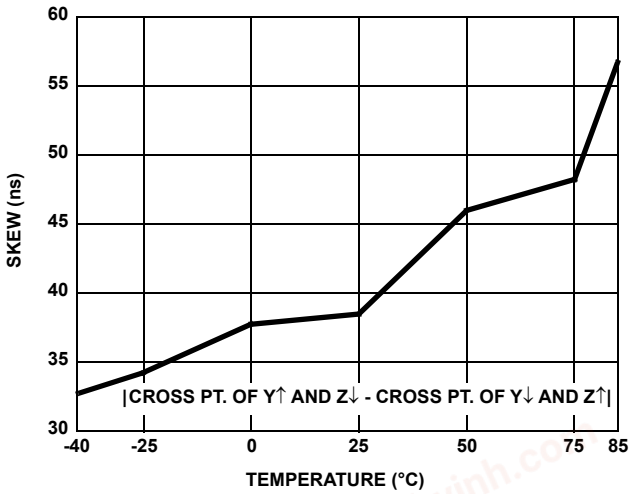


FIGURE 13. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL83080E, ISL83082E)

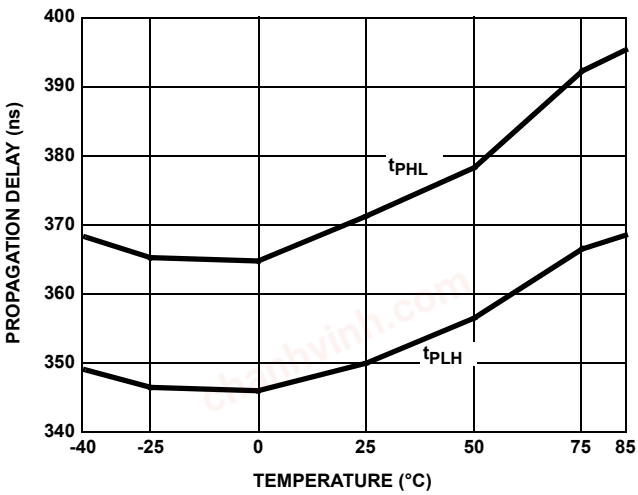


FIGURE 14. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL83083E, ISL83085E)

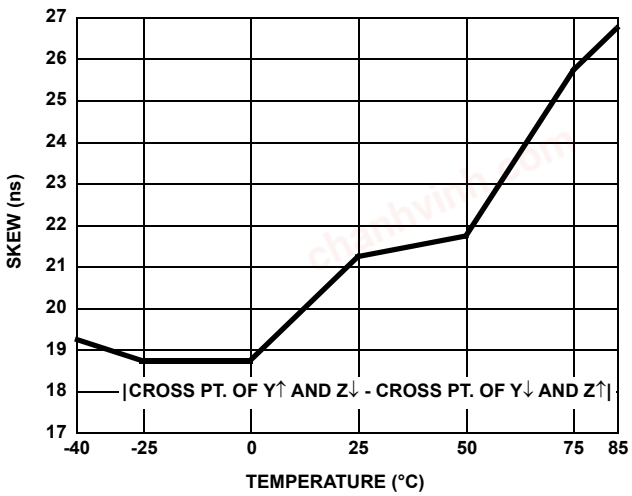


FIGURE 15. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL83083E, ISL83085E)

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Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified **(Continued)**

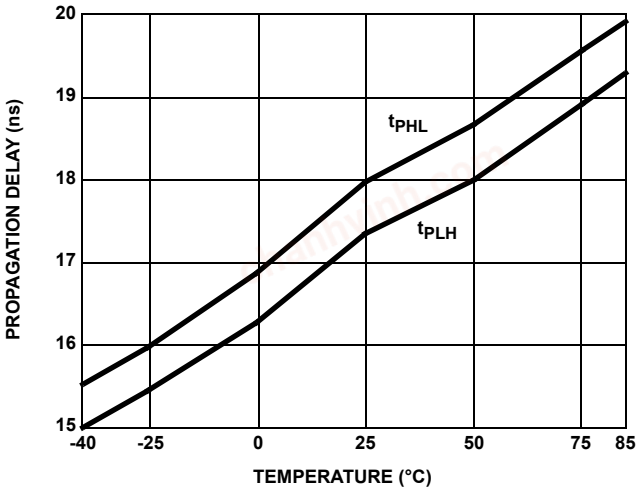


FIGURE 16. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL83086E, ISL83088E)

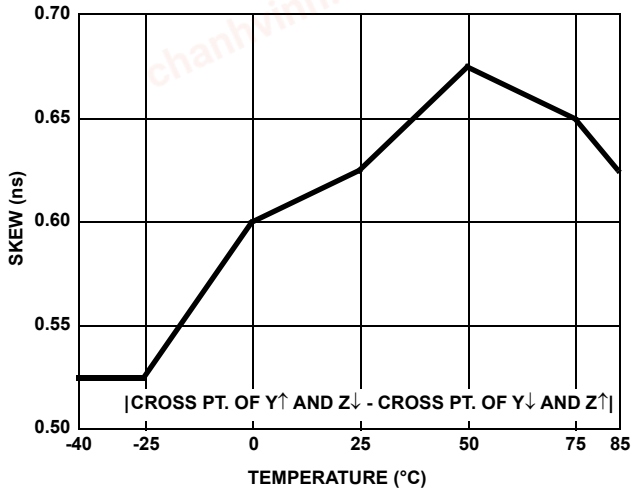


FIGURE 17. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL83086E, ISL83088E)

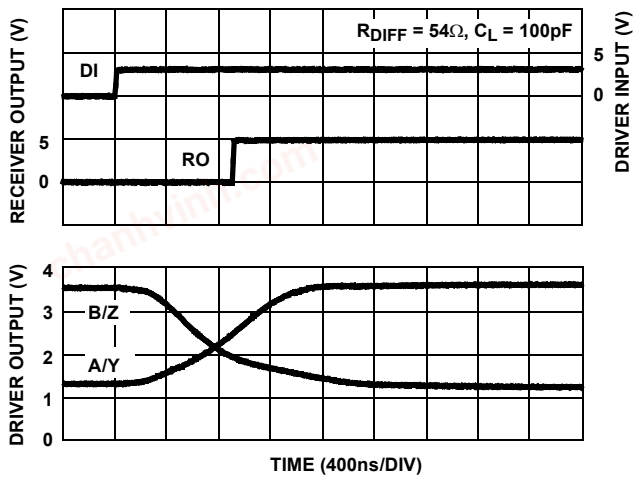


FIGURE 18. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83080E, ISL83082E)

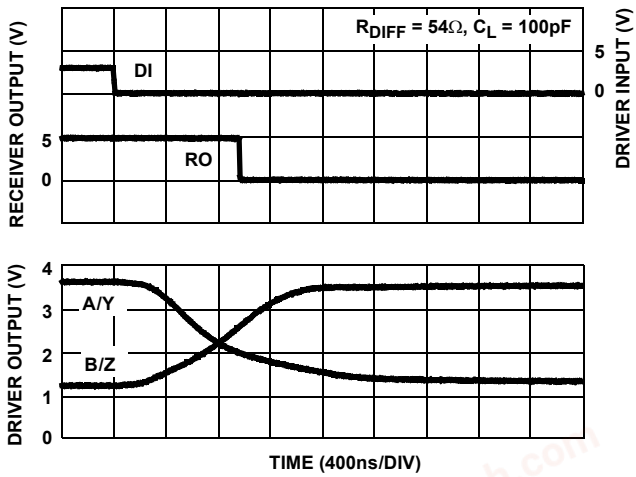


FIGURE 19. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83080E, ISL83082E)

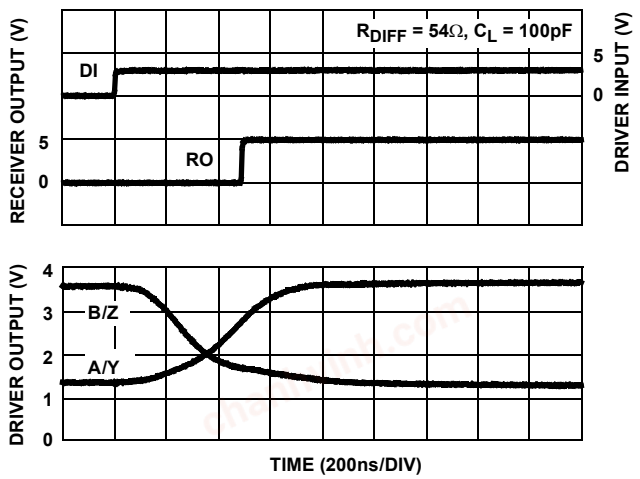


FIGURE 20. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83083E, ISL83085E)

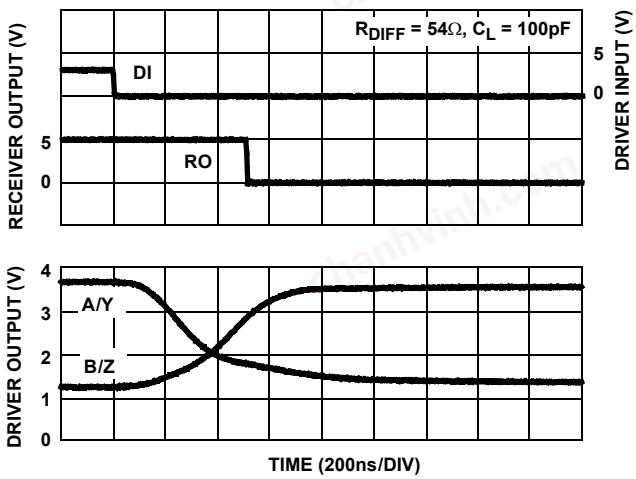


FIGURE 21. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83083E, ISL83085E)

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Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified **(Continued)**

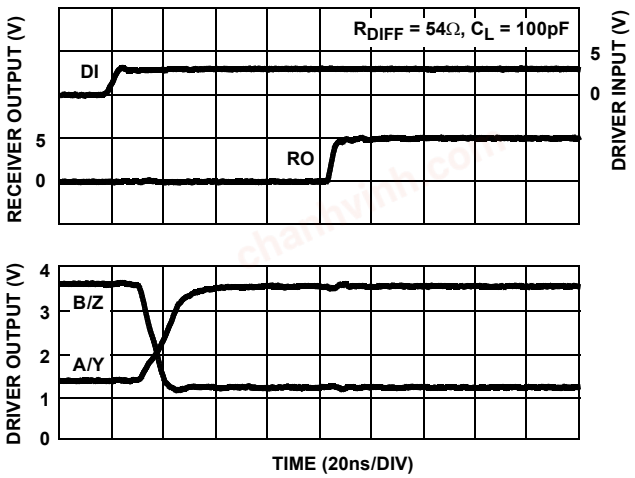


FIGURE 22. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83086E, ISL83088E)

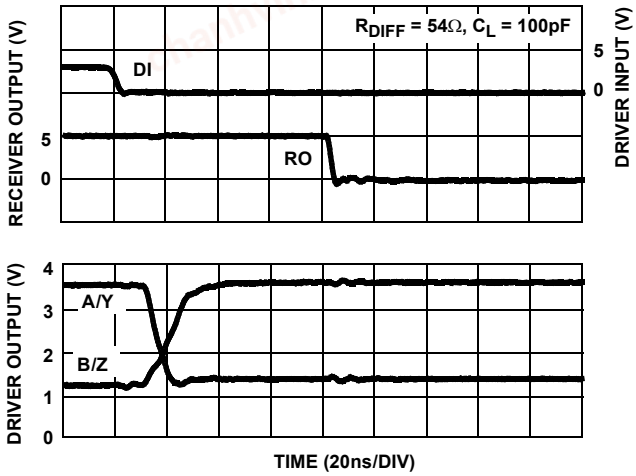


FIGURE 23. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83086E, ISL83088E)

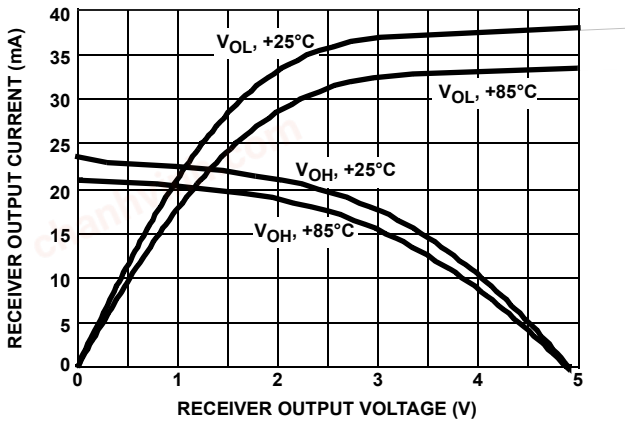


FIGURE 24. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

525

PROCESS:

Si Gate BiCMOS

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

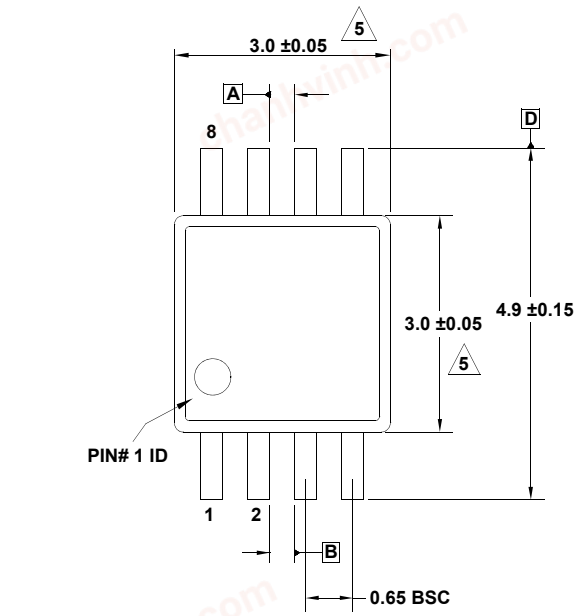
DATE	REVISION	CHANGE
Jul 5, 2022	10.01	Removed ISL83084E information from datasheet. Updated Ordering Information table format and added Note 3. Added test condition for VOD1. Removed maximum limit for VOD2. Removed About Intersil section. Updated M8.118 POD to the latest revision, changes are as follows: -Corrected typo in the side view 1 updating package thickness tolerance from ±010 to ±0.10. Updated M10.118 POD to the latest revision, changes are as follows: -Corrected typo in the side view 1 updating package thickness tolerance from ±010 to ±0.10. Updated M14.15 POD to the latest revision, changes are as follows: -In Side View B and Detail A: Added lead length dimension (1.27 – 0.40) Changed angle of the lead to 0-8 degrees. Updated M8.15 POD to the latest revision, changes are as follows: -Added the coplanarity spec into the drawing.
Feb 15, 2016	10.00	Added Rev History and About Intersil verbiage. Updated “Ordering Information” on page 4. Updated POD M8.118 to current version with following changes: Updated to new Intersil format by adding land pattern and moving dimensions from table onto drawing Corrected lead width dimension in side view 1 from “0.25 - 0.036" to “0.25 - 0.36" Updated POD M10.118 to current version with following change: Updated to new POD template. Added land pattern Updated POD M14.15 to current version with following change: Added land pattern and moved dimensions from table onto drawing. Updated POD M8.15 to current version with following changes: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Changed Note 1 “1982” to “1994”

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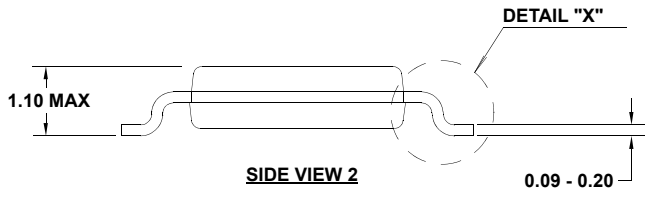
Package Outline Drawings

For the most recent package outline drawing, see M8.118.

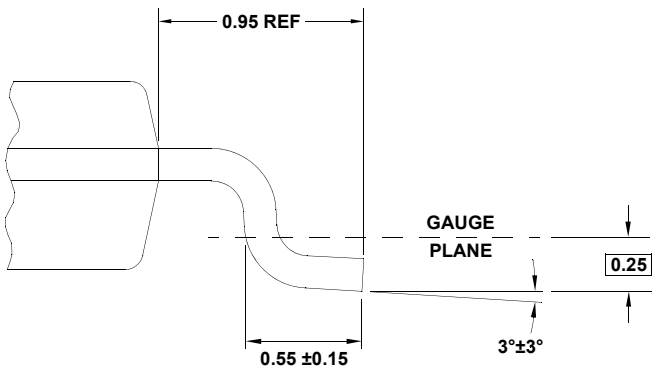
M8.118
8 Lead Mini Small Outline Plastic Package
Rev 5, 5/2021



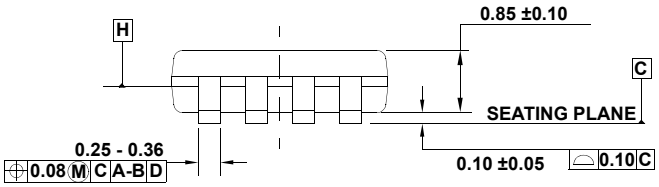
TOP VIEW



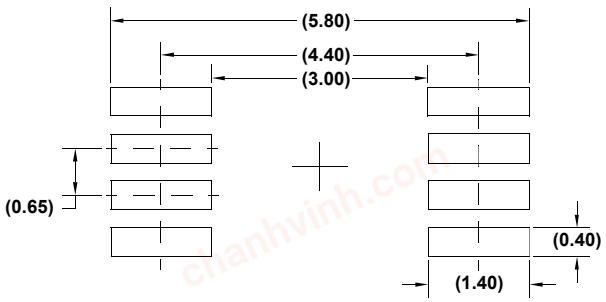
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

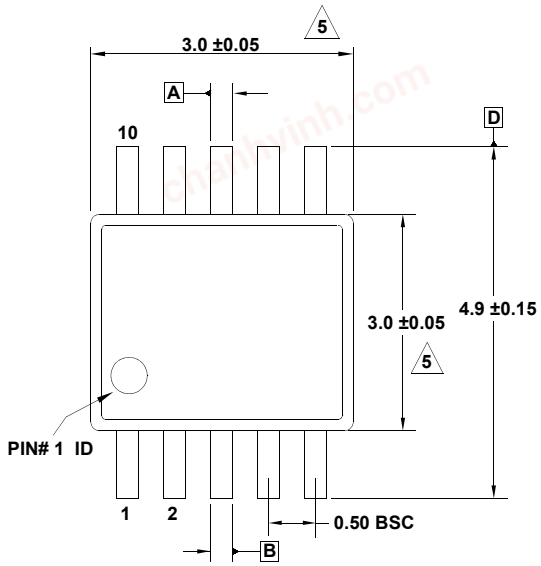
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

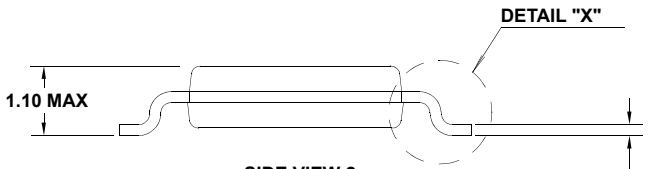
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For the most recent package outline drawing, see M10.118.

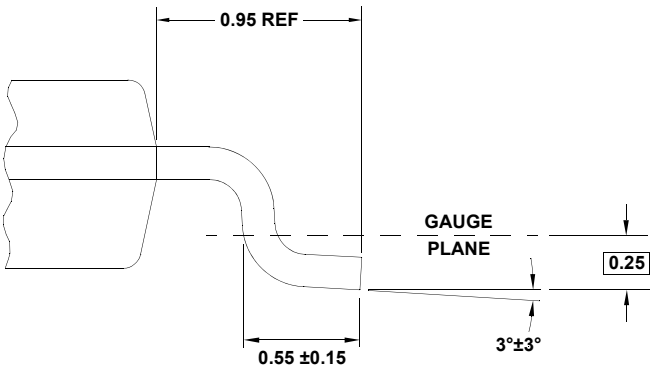
M10.118
10 Lead Mini Small Outline Plastic Package
Rev 2, 5/2021



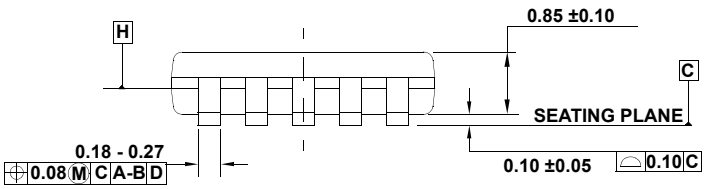
TOP VIEW



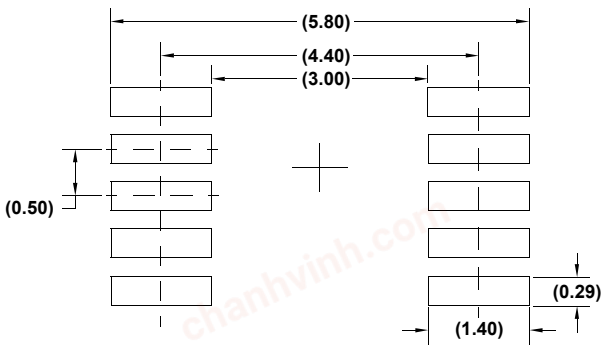
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

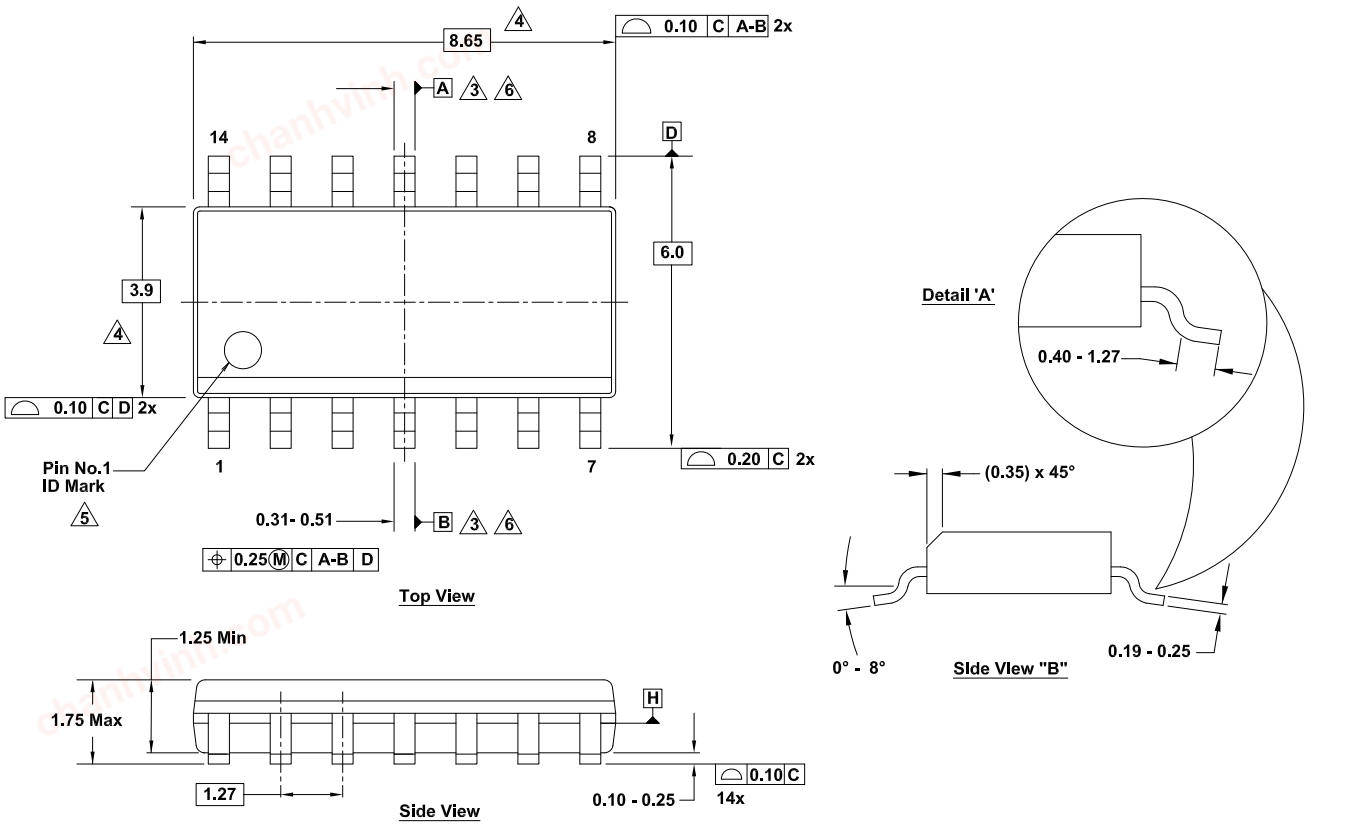
NOTES:

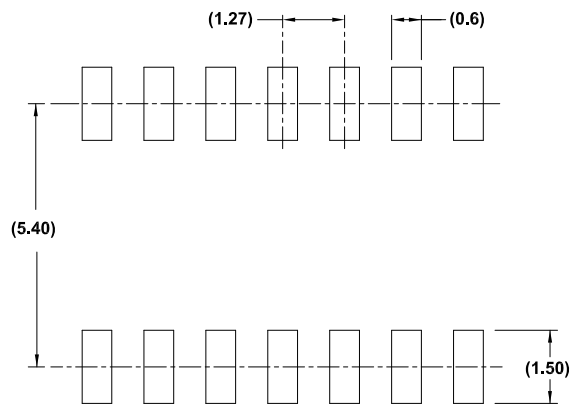
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

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For the most recent package outline drawing, see M14.15.

M14.15
14 Lead Narrow Body Small Outline Plastic Package
Rev 2, 6/20





Typical Recommended Land Pattern

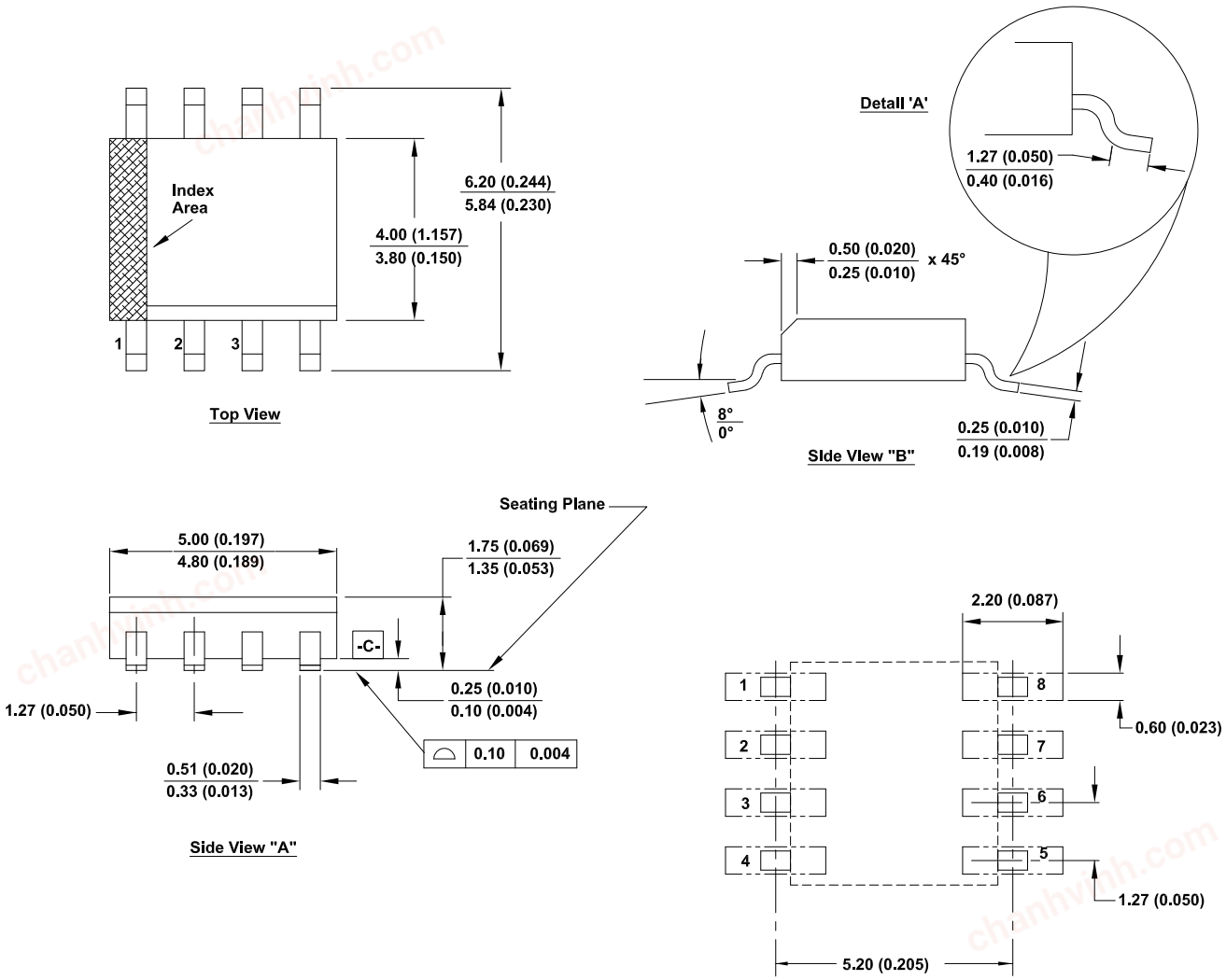
Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Datums A and B are determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier can be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

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For the most recent package outline drawing, see M8.15.

M8.15
8 Lead Narrow Body Small Outline Plastic Package
Rev 5, 4/2021



NOTES:

1. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
2. Package length does not include mold flash, protrustion or gate burrs. Mold flash, protrustion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrustions. Interlead flash and protrustions shallnot exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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