chanhvinh.com

ISL8036, ISL8036A

Dual 3A 1MHz/2.5MHz High Efficiency Synchronous Buck Regulator

FN6853
Rev 3.00
August 17, 2012

ISL8036, ISL8036A are integrated power controllers rated for dual 3A output current or current sharing operation with a 1MHz (ISL8036)/2.5MHz (ISL8036A) step-down regulator, which is ideal for any low power low-voltage applications. The channels are 180° out-of-phase for input RMS current and EMI reduction. It is optimized for generating low output voltages down to 0.8V each. The supply voltage range is from 2.8V to 6V, allowing for the use of a single Li+ cell, three NiMH cells or a regulated 5V input. The two channels are 180° out-of-phase, and each one has a guaranteed minimum output current of 3A. They can be combined to form a single 6A output in the current sharing mode. While in current sharing, the interleaved PWM signals reduce input and output ripple.

The ISL8036, ISL8036A includes a pair of low ON-resistance P-channel and N-channel internal MOSFETs to maximize efficiency and minimize external component count. 100% duty-cycle operation allows less than 250mV dropout voltage at 3A each.

The ISL8036, ISL8036A offers an independent 1ms Power-good (PG) timer at power-up. When shutdown, ISL8036, ISL8036A discharges the output capacitor. Other features include internal digital soft-start, enable for power sequence, overcurrent protection, and thermal shutdown.

The ISL8036, ISL8036A is offered in a 24 Ld 4mmx4mm QFN package with 1mm maximum height. The complete converter occupies less than 1.5cm^2 area.

Features

- 3A High Efficiency Synchronous Buck Regulator with up to 95% Efficiency
- 2% Output Accuracy Over-Temperature/Load/Line
- Internal Digital Soft-Start - 1.5ms
- 6A Current Sharing Mode Operation
- External Synchronization up to 6MHz
- Internal Current Mode Compensation
- Peak Current Limiting and Hiccup Mode Short Circuit Protection
- Reverse Overcurrent Protection

Applications

- DC/DC POL Modules
- µC/µP, FPGA and DSP Power
- Plug-in DC/DC Modules for Routers and Switchers
- Test and Measurement Systems
- Li-ion Battery Power Devices
- Bar Code Reader

Related Literature

- AN1616, “ISL8036CRSHEVAL1Z Current Sharing 6A Low Quiescent Current High Efficiency Synchronous Buck Regulator”
- AN1617, “ISL8036DUALEVAL1Z Dual 3A Low Quiescent Current High Efficiency Synchronous Buck Regulator”
- AN1615, “ISL8036ACRSHEVAL1Z Current Sharing 6A Low Quiescent Current High Efficiency Synchronous Buck Regulator”
- AN1618, “ISL8036ADUALEVAL1Z Dual 3A Low Quiescent Current High Efficiency Synchronous Buck Regulator”

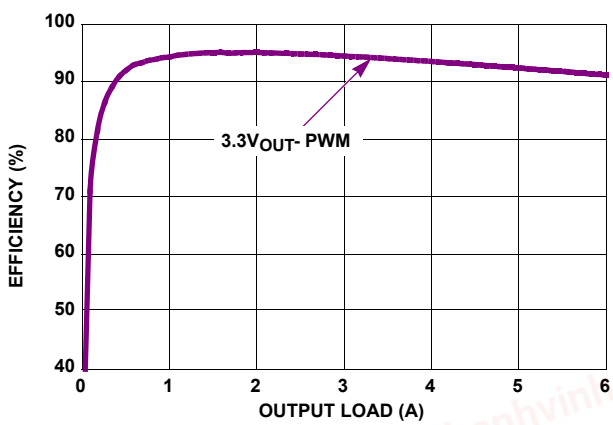


FIGURE 1. EFFICIENCY vs LOAD, 1MHz 5V_{IN} PWM, T_A = +25°C

chanhvinh.com

Typical Applications

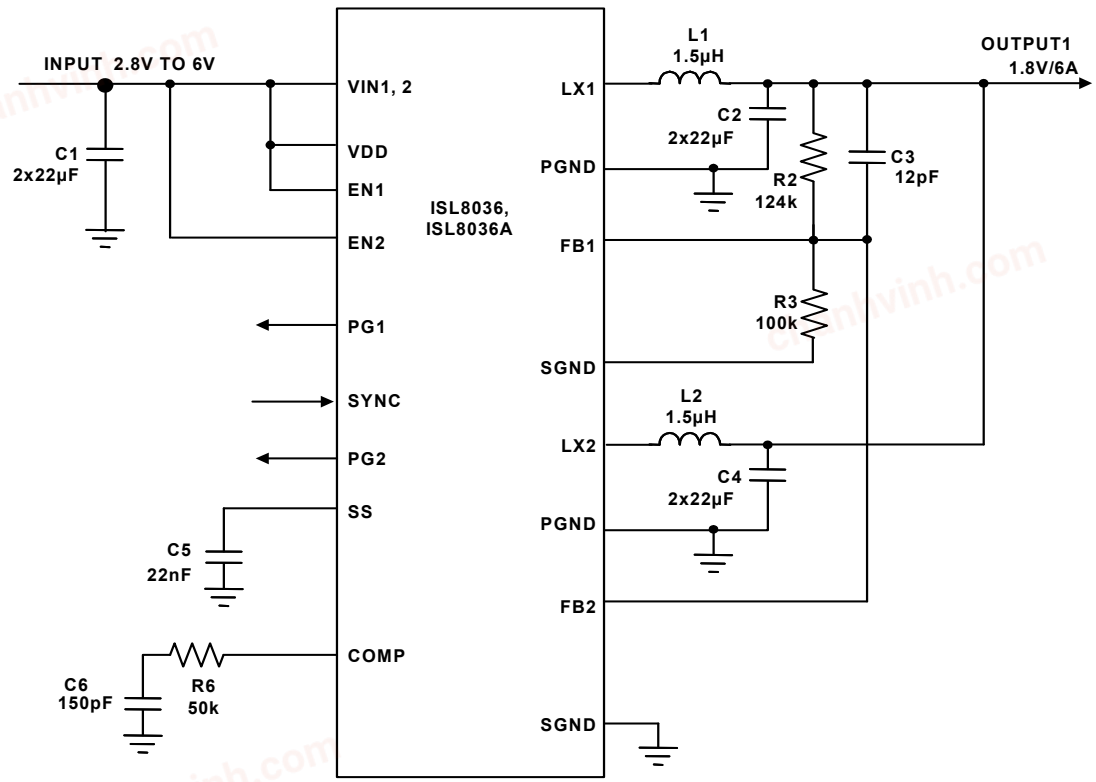


FIGURE 2. TYPICAL APPLICATION DIAGRAM - SINGLE 6A

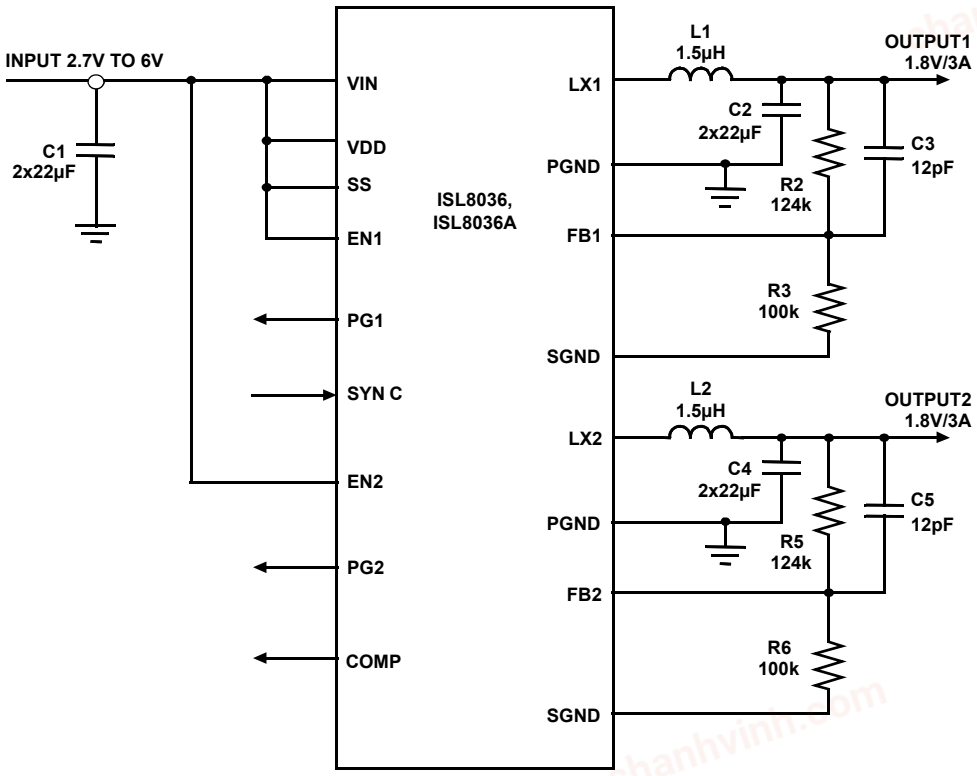


FIGURE 3. TYPICAL APPLICATION DIAGRAM - DUAL 3A OUTPUTS

chanhvinh.com

TABLE 1. COMPONENT VALUE SELECTION FOR DUAL OPERATION

V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
C1	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF
C2 (or C4)	2X22µF	2X22µF	2X22µF	2X22µF	2X22µF	2X22µF
L1 (or L2)*	1.0~2.2µH	1.0~2.2µH	1.0~2.2µH	1.0~3.3µH	1.0~3.3µH	1.0~4.7µH
R2 (or R5)	0	50k	87.5k	124k	212.5k	312.5k
R3 (or R6)	100k	100k	100k	100k	100k	100k

*For ISL8036A, the values used for L1 (or L2) are half the values specified above for each V_{OUT}.

TABLE 2. COMPONENT VALUE SELECTION FOR CURRENT SHARING OPERATION

V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
C1	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF
C2 (or C4)	2X22µF	2X22µF	2X22µF	2X22µF	2X22µF	2X22µF
L1 (or L2)*	1.0~2.2µH	1.0~2.2µH	1.0~2.2µH	1.0~3.3µH	1.0~3.3µH	1.0~4.7µH
R2	0	50k	87.5k	124k	212.5k	312.5k
R3	100k	100k	100k	100k	100k	100k
R6	30k	33k	31k	30k	29k	28k
C6	250pF	180pF	150pF	150pF	150pF	150pF

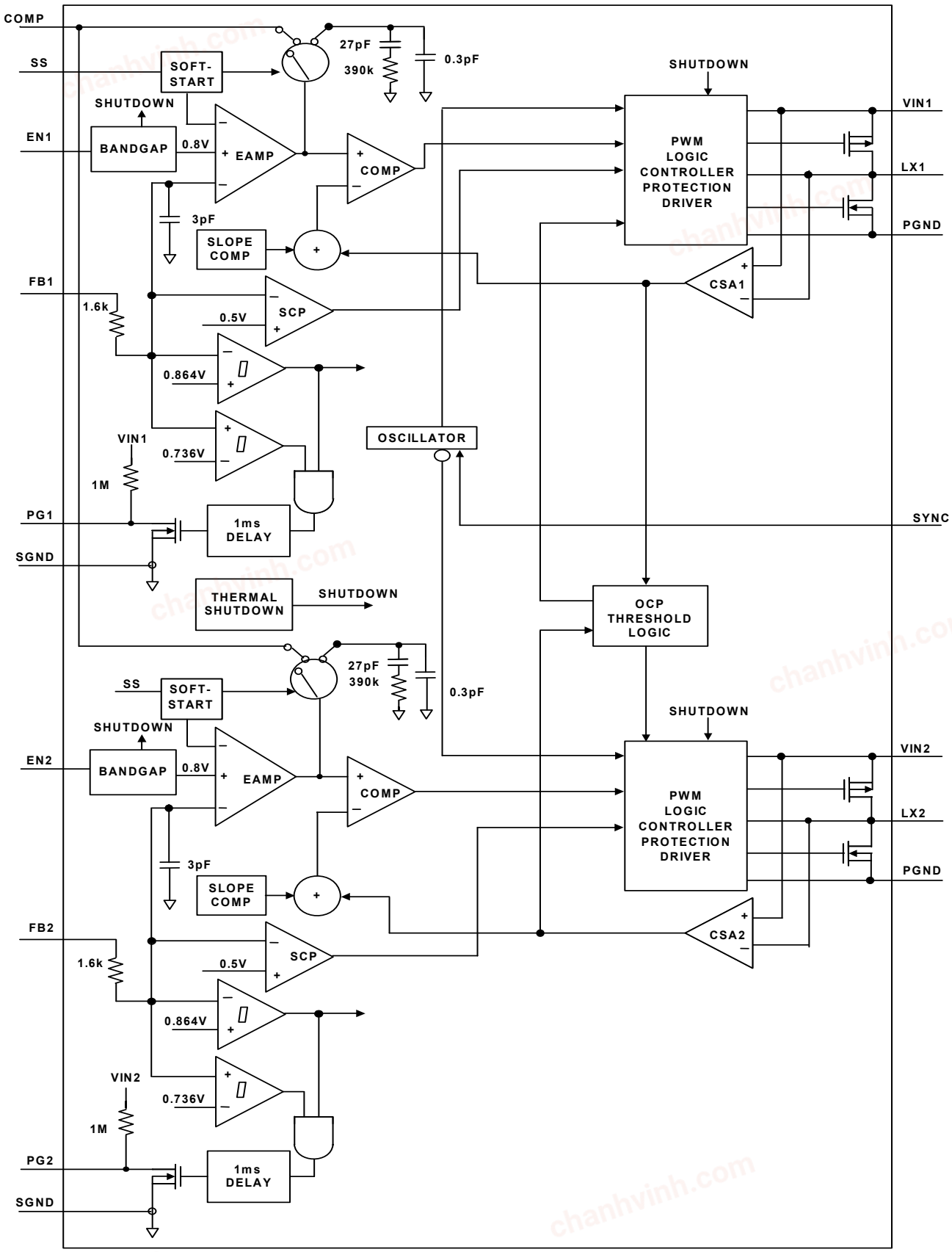
*For ISL8036A, the values used for L1 (or L2) are half the values specified above for each V_{OUT}.
NOTE: C5 value (22nF) is given by Equation 1 corresponding to the desired soft-start time.

TABLE 3. SUMMARY OF DIFFERENCES

PART NUMBER	SWITCHING FREQUENCY
ISL8036	Internally fixed switching frequency F_{SW} = 1MHz
ISL8036A	Internally fixed switching frequency F_{SW} = 2.5MHz

chanhvinh.com

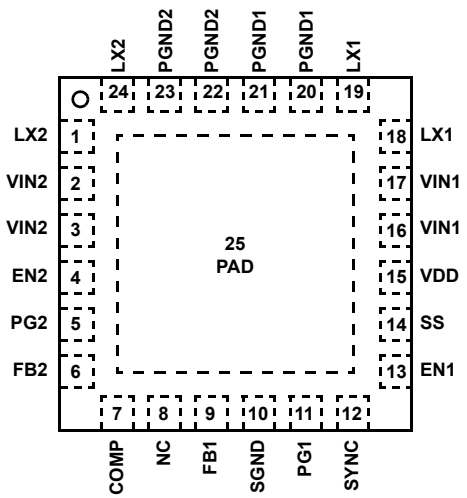
Block Diagram



chanhvinh.com

Pin Configuration

ISL8036, ISL8036A
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 24	LX2	Switching node connection for Channel 2. Connect to one terminal of inductor for VOUT2.
22, 23	PGND2	Negative supply for the power stage of Channel 2.
4	EN2	Regulator Channel 2 enable pin. Enable the output, VOUT2, when driven to high. Shutdown the VOUT2 and discharge output capacitor when driven to low. Do not leave this pin floating.
5	PG2	1ms timer output. At power-up or EN HI, this output is a 1ms delayed Power-Good signal for the VOUT2 voltage.
6	FB2	The feedback network of the Channel 2 regulator. To be connected to FB1 (current sharing)
7	COMP	An additional external network across COMP and SGND is required to improve the loop compensation of the amplifier channel parallel operation. The soft-start pin should be tied to the external capacitor. COMP pin is NC in dual mode operation, using internal compensation. If SS pin is tied to CSS (without connection to VIN), external compensation is automtaically used. Connect an external R,C network on COMP pin for parallel mode operation.
8	NC	No connect pin; please tie to GND.
9	FB1	The feedback network of the Channel 1 regulator. FB1 is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB1. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.8V reference. There is an internal compensation to meet a typical application. In addition, the regulator power-good and undervoltage protection circuitry use FB1 to monitor the Channel 1 regulator output voltage.
10	SGND	System ground.
11	PG1	1ms timer output. At power-up or EN HI, this output is a 1ms delayed Power-Good signal for the VOUT1 voltage.
12	SYNC	Connect to logic high or input voltage VIN . Connect to an external function generator for external Synchronization. Negative edge trigger. Do not leave this pin floating. **Do not tie this pin low (or to SGND).**
13	EN1	Regulator Channel 1 enable pin. Enable the output, VOUT1, when driven to high. Shutdown the VOUT1 and discharge output capacitor when driven to low. Do not leave this pin floating.

chanhvinh.com

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
14	SS	SS is used to adjust the soft-start time. When SS pin is tied to VIN, SS time is 1.5ms. SS pin is tied to VIN only in dual mode operation. SS pin is tied to CSS only in parallel mode operation, using only external compensation. Connect a capacitor from SS to SGND to adjust the soft-start time (current sharing). C_{SS} should not be larger than 33nF. This capacitor, along with an internal 5µA current source sets the soft-start interval of the converter, t_{SS}. $C_{SS}[\mu F] = 6.25 \cdot t_{SS}[s]$ (EQ. 1)
15	VDD	Input supply voltage for the logic. VDD to be at the same potential as VIN +0.3/-0.5V.
20, 21	PGND1	Negative supply for the power stage of Channel 1.
18, 19	LX1	Switching node connection for Channel 1. Connect to one terminal of inductor for VOUT1.
16, 17 2, 3	VIN1, VIN2	Input supply voltage. Connect 22µF ceramic capacitor to power ground per channel.
25	PAD	The exposed pad must be connected to the SGND pin for proper electrical performance. Add as much vias as possible for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8036IRZ	80 36IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4D
ISL8036IRZ-T (Note 1)	80 36IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4D
ISL8036AIRZ	80 36AIRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4D
ISL8036AIRZ-T (Note 1)	80 36AIRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4D
ISL8036CRSHEVAL1Z	Evaluation Board			
ISL8036DUALEVAL1Z	Evaluation Board			
ISL8036ACRSHEVAL1Z	Evaluation Board			
ISL8036ADUALEVAL1Z	Evaluation Board			

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8036, ISL8036A. For more information on MSL, please see Technical Brief TB363.

chanhvinh.com

Table of Contents

Absolute Maximum Ratings 8
Thermal Information 8
Recommended Operating Conditions 8
Electrical Specifications 8
ISL8036 Typical Operating Performance for Dual PWM Operation 10
ISL8036A Typical Operating Performance for Dual PWM Operation 15
ISL8036 Typical Operating Performance for Current Sharing PWM Operation 17
ISL8036A Typical Operating Performance for Current Sharing PWM Operation 21
Theory of Operation 22
PWM Control Scheme 22
Synchronization Control 22
Output Current Sharing 22
Overcurrent Protection 22
PG 22
UVLO 23
Enable 23
Soft-start-up 23
Discharge Mode (Soft-Stop) 23
Power MOSFETs 23
100% Duty Cycle 23
Thermal Shutdown 23
Applications Information 23
Output Inductor and Capacitor Selection 23
Output Voltage Selection 23
Input Capacitor Selection 23
PCB Layout Recommendation 24
Revision History 25
Products 25
Package Outline Drawing 26

chanhvinh.com

Absolute Maximum Ratings (Reference to SGND)

VIN1, VIN2, VDD . . . . . -0.3V to 6.5V (DC) or 7V (20ms)
LX1, LX2 . . . . . -3V/(10ns)/-1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or
. . . . . 7V (20ms)/8.5V(10ns)
EN1, EN2, PG1, PG2, SYNC, SS. . . . . -0.3V to +6.5V
FB1, FB2, COMP . . . . . -0.3V to 2.7V
NC. . . . . -0.3V to 0.3V
ESD Ratings
Human Body Model (Tested per JESD22-A114) 4kV
Charged Device Model (Tested per JESD22-C101E). 2kV
Machine Model (Tested per JESD22-A115). 300V
Latch Up (Tested per JESD-78A; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld 4x4 QFN (Notes 4, 5).	36	2

Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature Range. . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +85°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

VIN Supply Voltage Range. . . . . 2.85V to 6V
Load Current Range per Channel. . . . . 0A to 3A
Ambient Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, the typical specifications are measured at the following conditions: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN1 = EN2 = VDD, L = 1.5µH, C1 = C2 = C4 = 2x22µF, I_{OUT1} = I_{OUT2} = 0A to 3A, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT SUPPLY						
VIN Undervoltage Lockout Threshold	V_{UVLO}	Rising		2.5	**2.85**	V
		Hysteresis	**50**	100		mV
Quiescent Supply Current	I_{VDD}	SYNC = VDD, EN1 = EN2 = VDD, F_S = 1MHz, no load at the output		15	**40**	mA
		F_S = 2.5MHz, no load at the output		30	**70**	mA
Shutdown Supply Current	I_{SD}	V_{DD} = 6V, EN1 = EN2 = SGND		8	**20**	µA
OUTPUT REGULATION						
FB1, FB2 Regulation Voltage	V_{FB}		**0.790**	0.8	**0.810**	V
FB1, FB2 Bias Current	I_{FB}	VFB = 0.75V		0.1		µA
Load Regulation		SYNC = VDD, output load from 0A to 6A		2		mV/A
Line Regulation		V_{IN} = V_O + 0.5V to 6V (minimal 2.85V)		0.1		%/V
Soft-start Ramp Time Cycle		SS = VDD		1.5		ms
Soft-start Charging Current	I_{SS}		**4**	5	**6**	µA
COMPENSATION						
Error Amplifier Trans-Conductance		SS = VDD		20		µA/V
		SS with Capacitor		100		µA/V
Trans-resistance	RT		**0.180**	0.2	**0.220**	Ω
Trans-resistance Matching	RT_match		**-0.03**		**+0.03**	Ω
OVERCURRENT PROTECTION						
Dynamic Current Limit ON-time	t_{OCON}			17		Clock pulses
Dynamic Current Limit OFF-time	t_{OCOFF}			8		SS cycle
Positive Peak Overcurrent Limit	I_{poc1}		**4.1**	4.8	**5.5**	A
	I_{poc2}		**4.1**	4.8	**5.5**	A
Negative Peak Overcurrent Limit	I_{noc1}		**-3.5**	-2.5	**-1.5**	A
	I_{noc2}		**-3.5**	-2.5	**-1.5**	A

chanhvinh.com

Electrical Specifications

Unless otherwise noted, the typical specifications are measured at the following conditions: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN1 = EN2 = VDD, L = 1.5µH, C1 = C2 = C4 = 2x22µF, I_{OUT1} = I_{OUT2} = 0A to 3A, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
LX1, LX2						
P-Channel MOSFET ON-Resistance		V_{IN} = 6V, I_O = 200mA		50	**75**	mΩ
		V_{IN} = 2.7V, I_O = 200mA		70	**100**	mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 6V, I_O = 200mA		50	**75**	mΩ
		V_{IN} = 2.7V, I_O = 200mA		70	**100**	mΩ
LX_ Maximum Duty Cycle				100		%
PWM Switching Frequency	F_S	ISL8036	**0.88**	1.1	**1.32**	MHz
		ISL8036A	**2.15**	2.5	**2.85**	MHz
Synchronization Frequency Range	F_{SYNC}	ISL8036 (Note 7)	**2.64**		**6**	MHz
Channel 1 to Channel 2 Phase Shift		Rising edge to rising edge timing		180		°
LX Minimum On Time		SYNC = High (PWM mode)			**140**	ns
Soft Discharge Resistance	R_{DIS}	EN = LOW	**80**	100	**120**	Ω
LX Leakage Current		Pulled up to 6V		0.1	**1**	µA
PG1, PG2						
Output Low Voltage		Sinking 1mA, VFB = 0.7V			**0.3**	V
PG Pin Leakage Current		PG = V_{IN} = 6V		0.01	**0.1**	µA
Internal PGOOD Low Rising Threshold		Percentage of nominal regulation voltage	**89.5**	92	**94.5**	%
Internal PGOOD Low Falling Threshold		Percentage of nominal regulation voltage	**85**	88	**91**	%
Delay Time (Rising Edge)		Time from VOUT_ reached regulation		1		ms
Internal PGOOD Delay Time (Falling Edge)				7	**10**	µs
EN1, EN2, SYNC						
Logic Input Low					**0.4**	V
Logic Input High			**1.5**			V
SYNC Logic Input Leakage Current	I_{SYNC}	Pulled up to 6V		0.1	**1**	µA
Enable Logic Input Leakage Current	I_{EN}	Pulled up to 6V		0.1	**1**	µA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				25		°C

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. The operational frequency per switching channel will be half of the SYNC frequency.

chanhvinh.com

ISL8036 Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT1} = 1.8V; V_{OUT2} = 0.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, F_{SW} = 1MHz.

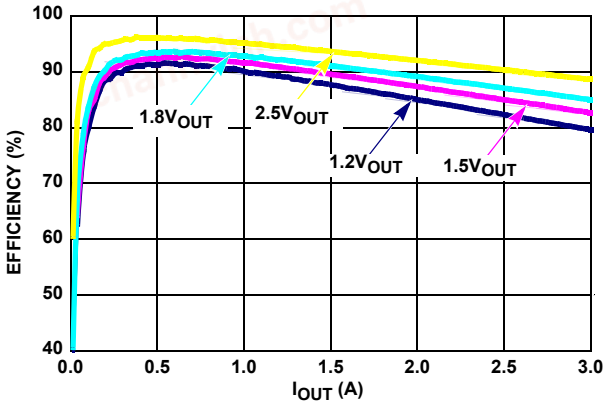


FIGURE 4. EFFICIENCY, V_{IN} = 3.3V, T_A = +25°C

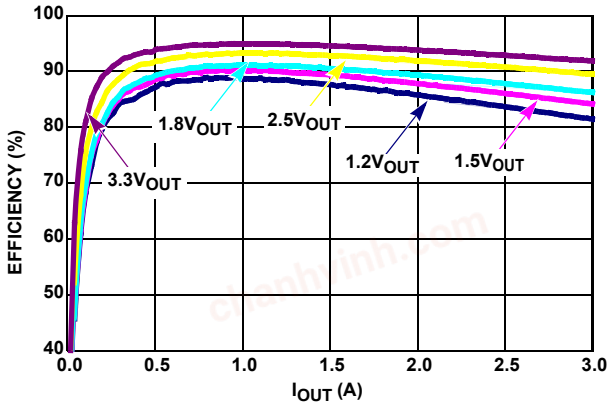


FIGURE 5. EFFICIENCY, V_{IN} = 5V, T_A = +25°C

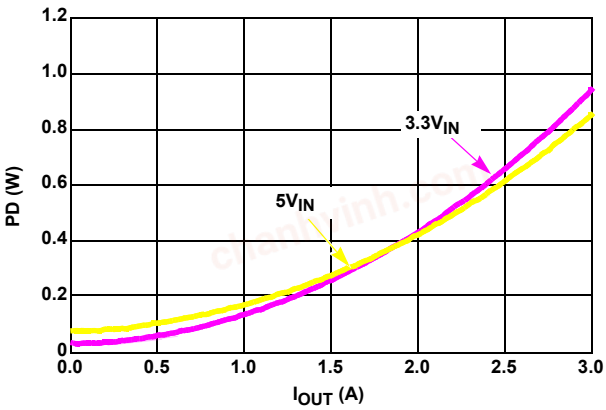


FIGURE 6. POWER DISSIPATION, V_{OUT} = 1.8V, T_A = +25°C

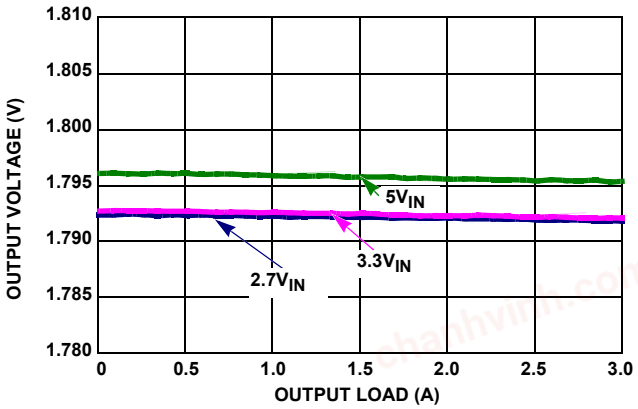


FIGURE 7. V_{OUT} REGULATION vs LOAD, 1.8V, T_A = +25°C

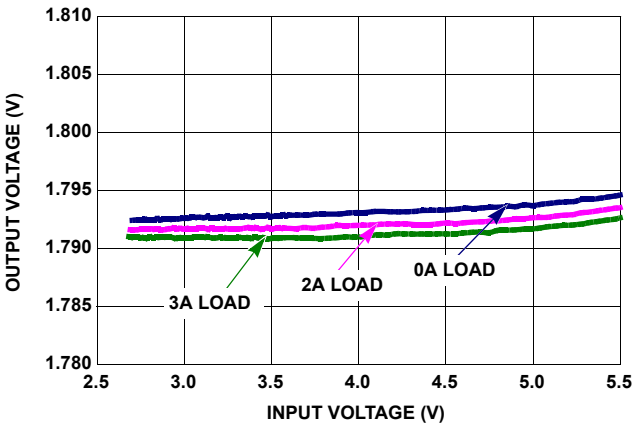


FIGURE 8. OUTPUT VOLTAGE REGULATION vs V_{IN}, 1.8V, T_A = +25°C

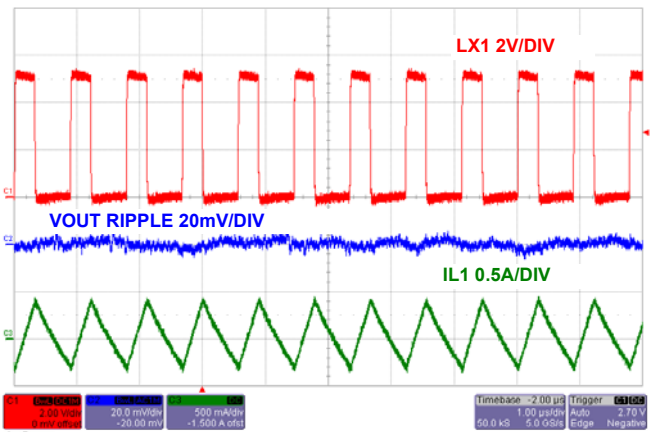


FIGURE 9. STEADY STATE OPERATION AT NO LOAD CHANNEL 1

chanhvinh.com

ISL8036 Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT1} = 1.8V; V_{OUT2} = 0.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, F_{SW} = 1MHz. **(Continued)**

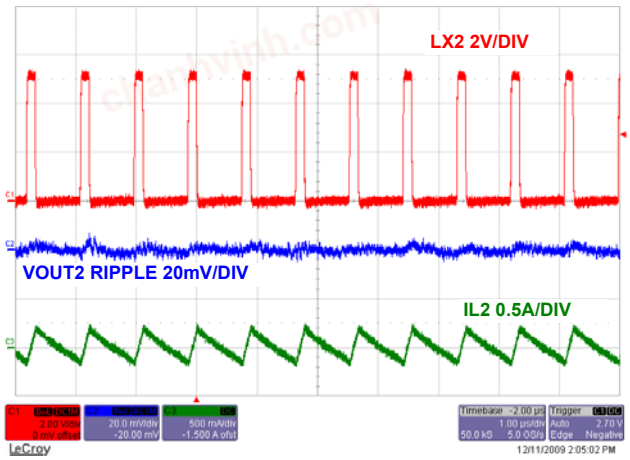


FIGURE 10. STEADY STATE OPERATION AT NO LOAD CHANNEL 2

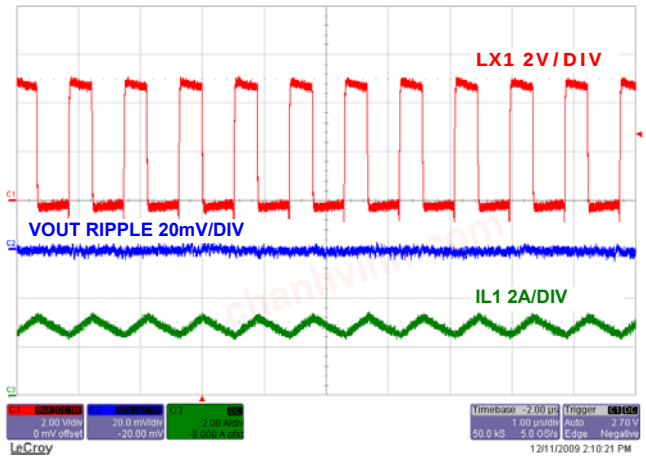


FIGURE 11. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 1

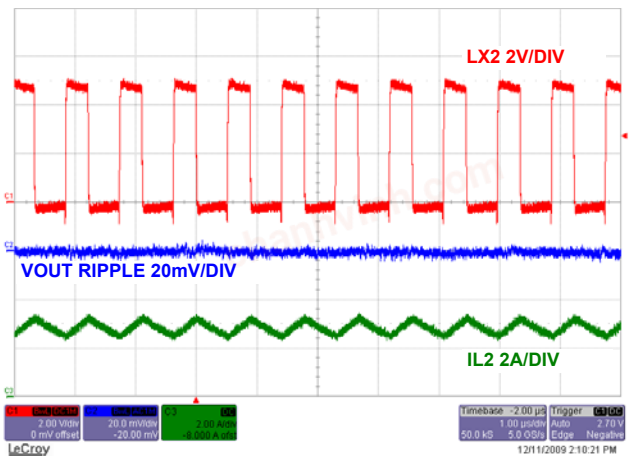


FIGURE 12. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 2

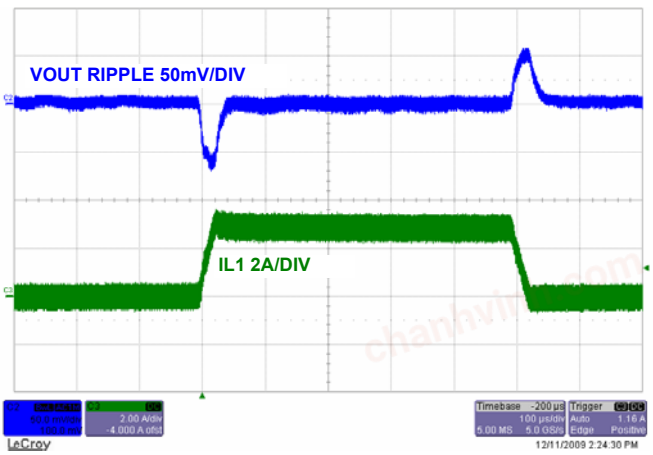


FIGURE 13. LOAD TRANSIENT CHANNEL 1

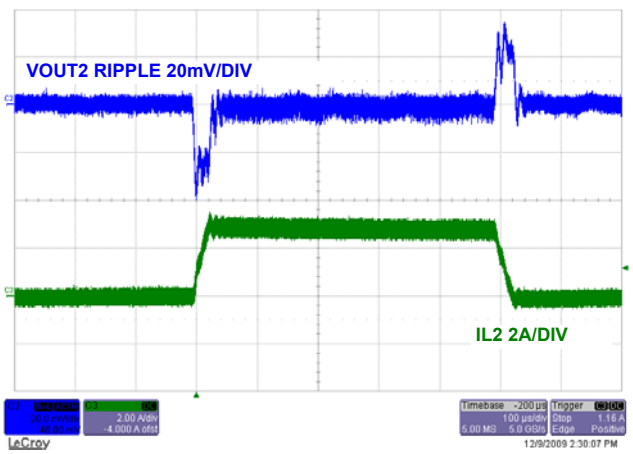


FIGURE 14. LOAD TRANSIENT CHANNEL 2

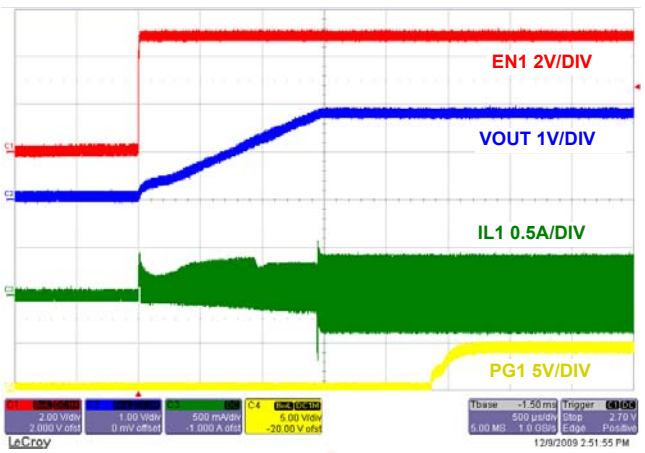


FIGURE 15. SOFT-START WITH NO LOAD CHANNEL 1

chanhvinh.com

ISL8036 Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT1} = 1.8V; V_{OUT2} = 0.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, F_{SW} = 1MHz. **(Continued)**

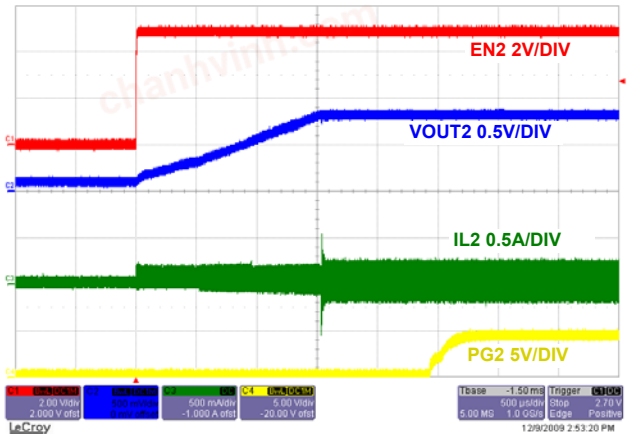


FIGURE 16. SOFT-START WITH NO LOAD CHANNEL 2

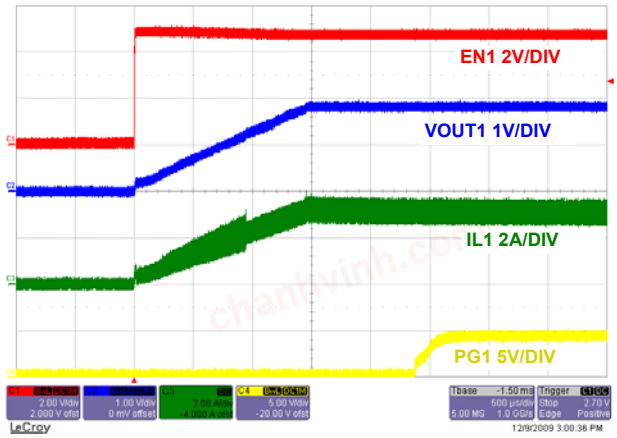


FIGURE 17. SOFT-START AT FULL LOAD CHANNEL 1

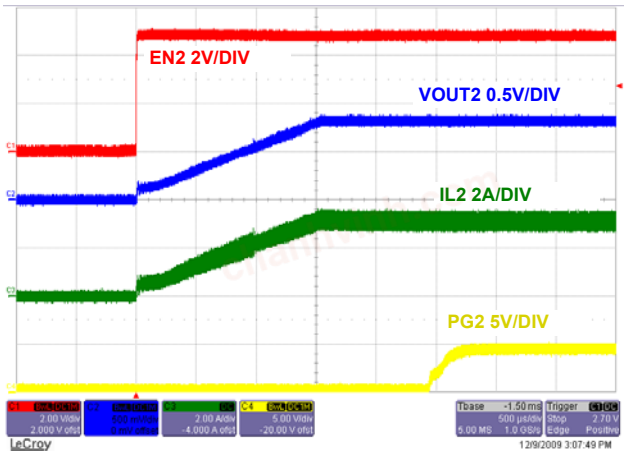


FIGURE 18. SOFT-START AT FULL LOAD CHANNEL 2

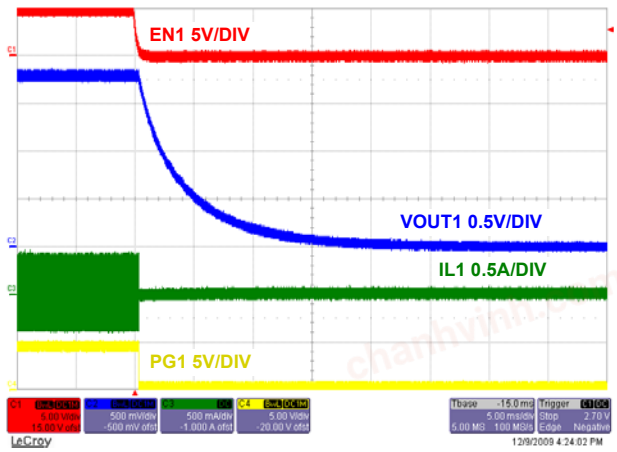


FIGURE 19. SOFT-DISCHARGE SHUTDOWN CHANNEL 1

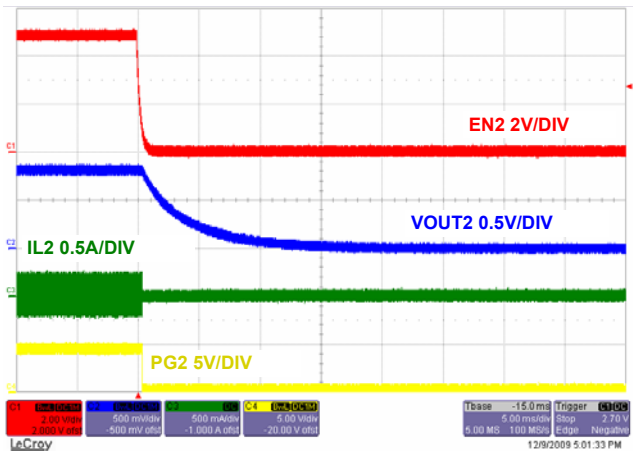


FIGURE 20. SOFT-DISCHARGE SHUTDOWN CHANNEL 2

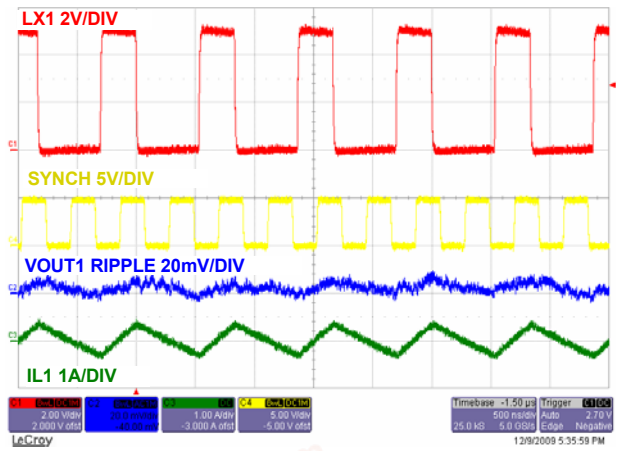


FIGURE 21. STEADY STATE OPERATION CHANNEL 1 AT NO LOAD WITH F_{SW} = 2.4MHz

chanhvinh.com

ISL8036 Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT1} = 1.8V; V_{OUT2} = 0.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, F_{SW} = 1MHz. **(Continued)**

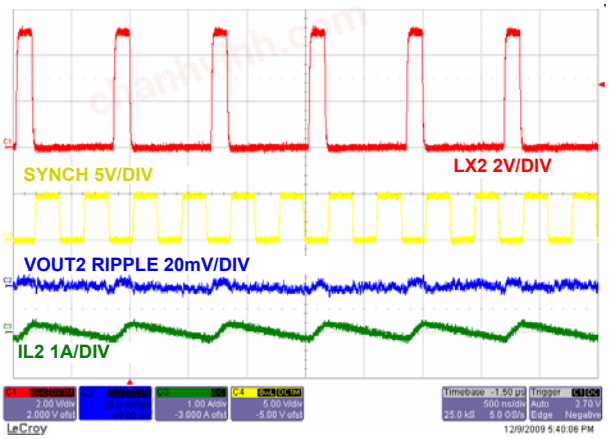


FIGURE 22. STEADY STATE OPERATION CHANNEL 2 AT NO LOAD WITH F_{SW} = 2.4MHz

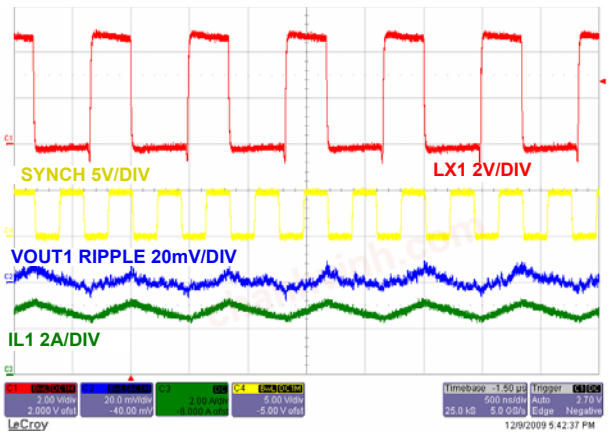


FIGURE 23. STEADY STATE OPERATION CHANNEL 1 AT FULL LOAD WITH F_{SW} = 2.4MHz

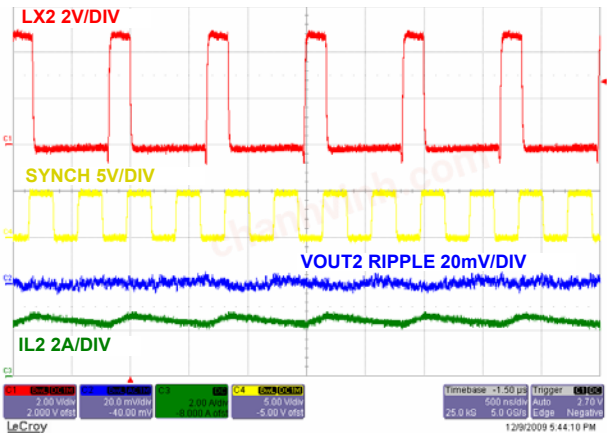


FIGURE 24. STEADY STATE OPERATION CHANNEL 2 AT FULL LOAD WITH F_{SW} = 2.4MHz

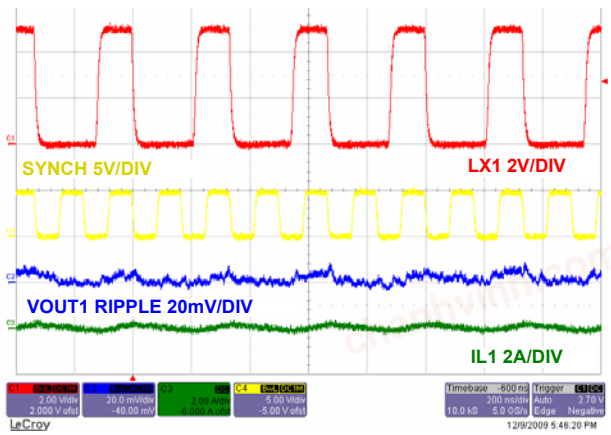


FIGURE 25. STEADY STATE OPERATION CHANNEL 1 AT NO LOAD WITH F_{SW} = 6MHz

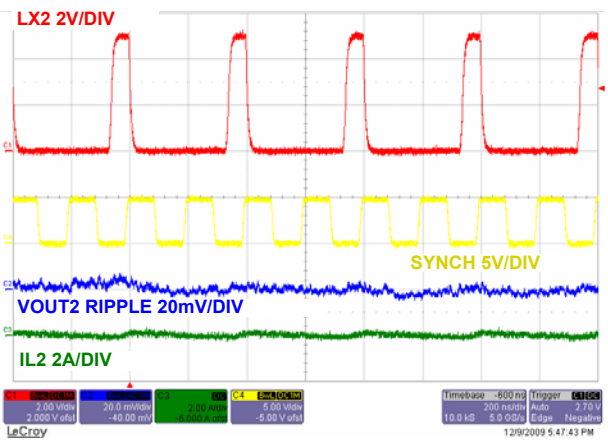


FIGURE 26. STEADY STATE OPERATION CHANNEL 2 AT NO LOAD WITH F_{SW} = 5MHz

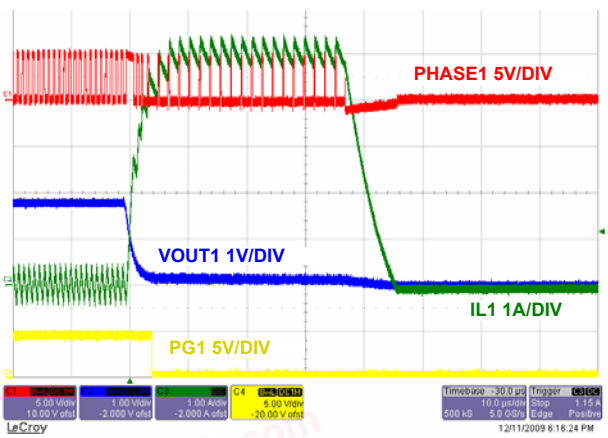


FIGURE 27. OUTPUT SHORT CIRCUIT CHANNEL 1

chanhvinh.com

ISL8036 Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT1} = 1.8V; V_{OUT2} = 0.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, F_{SW} = 1MHz. **(Continued)**

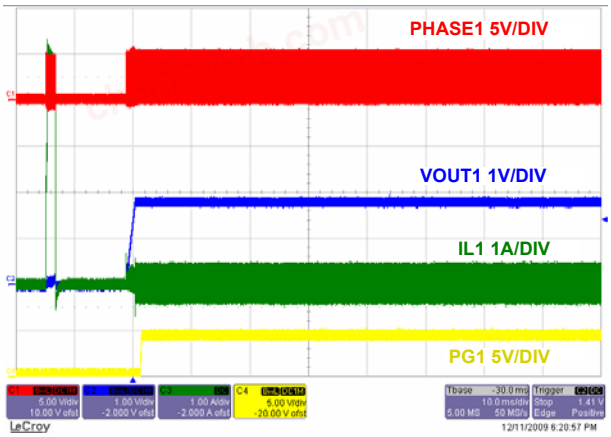


FIGURE 28. OUTPUT SHORT CIRCUIT RECOVERY (FROM HICCUP) CHANNEL 1

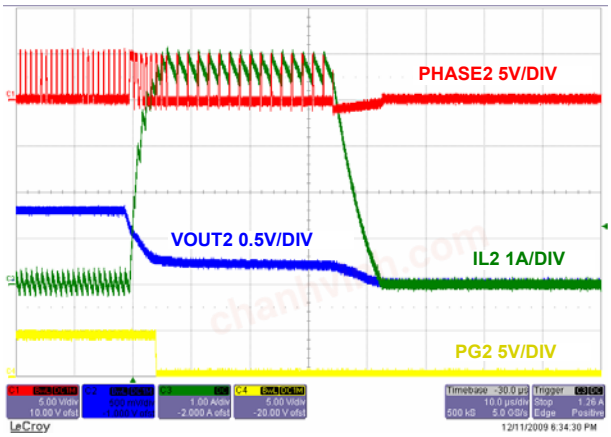


FIGURE 29. OUTPUT SHORT CIRCUIT CHANNEL 2

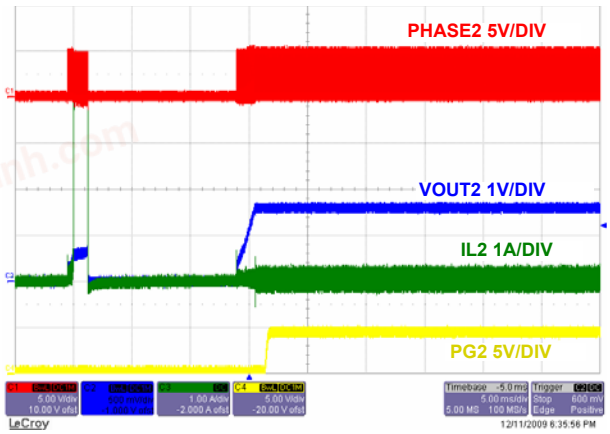


FIGURE 30. OUTPUT SHORT CIRCUIT RECOVERY (FROM HICCUP) CHANNEL 2

chanhvinh.com

ISL8036A Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT1} = 1.8V; V_{OUT2} = 0.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, L1 = L2 = 0.6µH, F_{SW} = 2.5MHz.

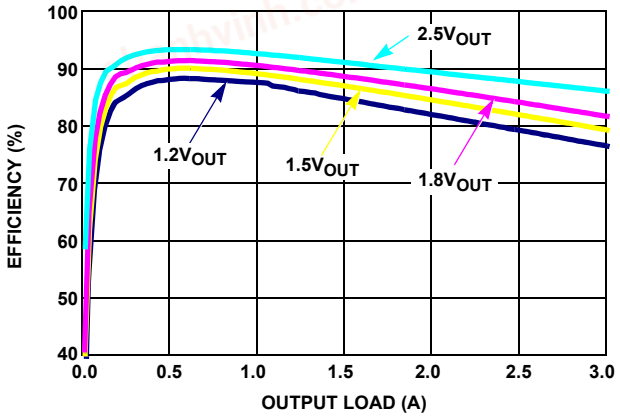


FIGURE 31. EFFICIENCY vs LOAD, 3.3V_{IN} DUAL CHANNEL 1, T_A = +25°C

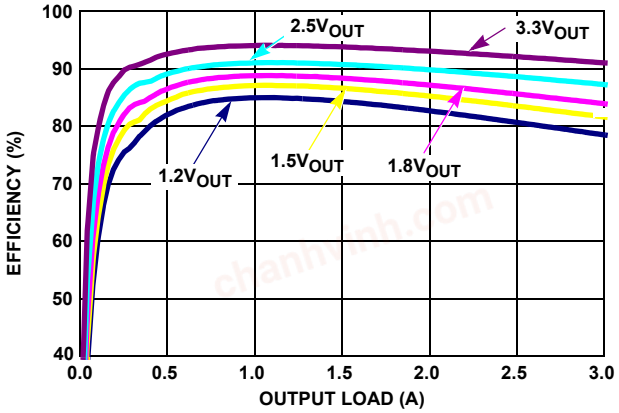


FIGURE 32. EFFICIENCY vs LOAD, 5V_{IN} DUAL CHANNEL 1, T_A = +25°C

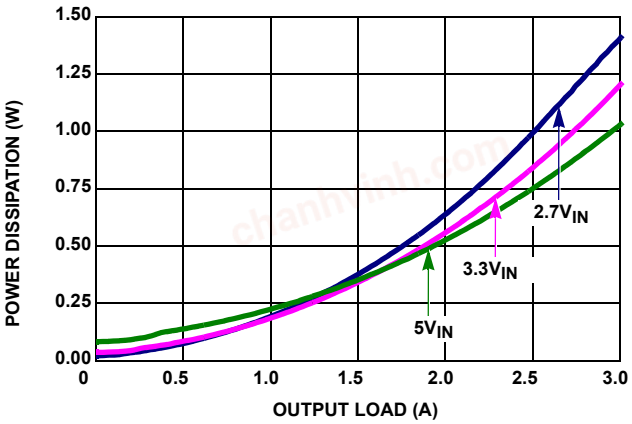


FIGURE 33. POWER DISSIPATION vs LOAD, 1.8V_{OUT} DUAL CHANNEL 1, T_A = +25°C

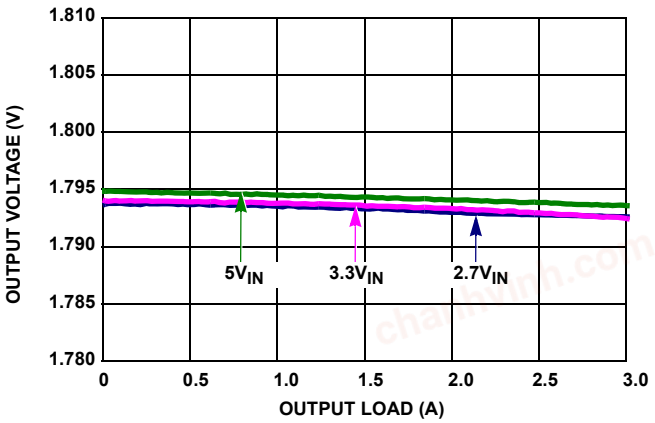


FIGURE 34. V_{OUT} REGULATION vs LOAD, 1.8V_{OUT} DUAL CHANNEL 1, T_A = +25°C

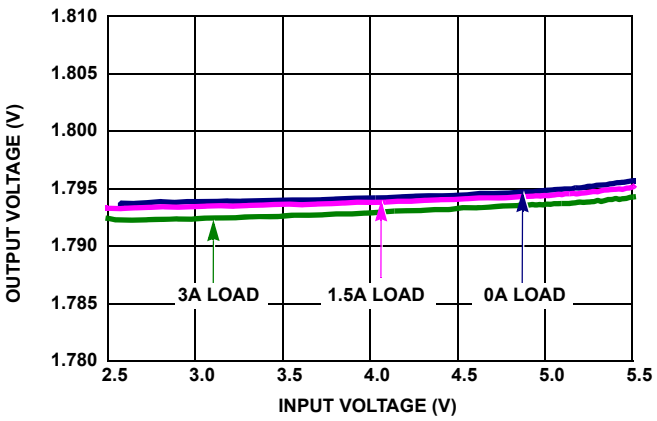


FIGURE 35. V_{OUT} REGULATION vs V_{IN}, 1.8V_{OUT} DUAL CHANNEL 1, T_A = +25°C

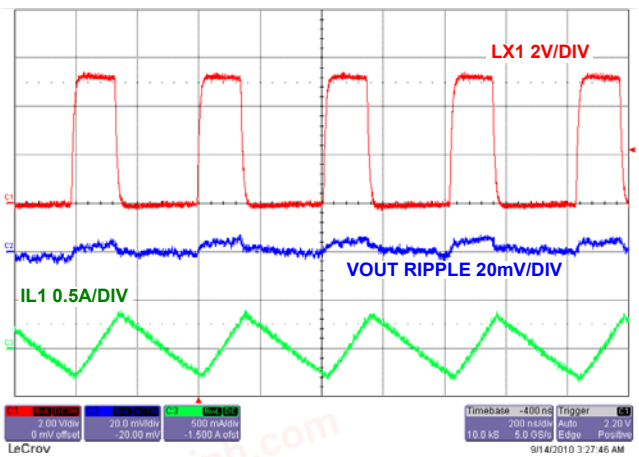


FIGURE 36. STEADY STATE OPERATION AT NO LOAD CHANNEL 1

chanhvinh.com

ISL8036A Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT1} = 1.8V; V_{OUT2} = 0.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, L1 = L2 = 0.6µH, F_{SW} = 2.5MHz. **(Continued)**

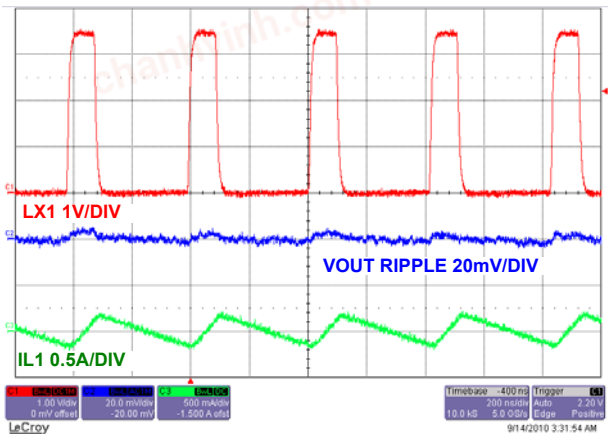


FIGURE 37. STEADY STATE OPERATION AT NO LOAD CHANNEL 2

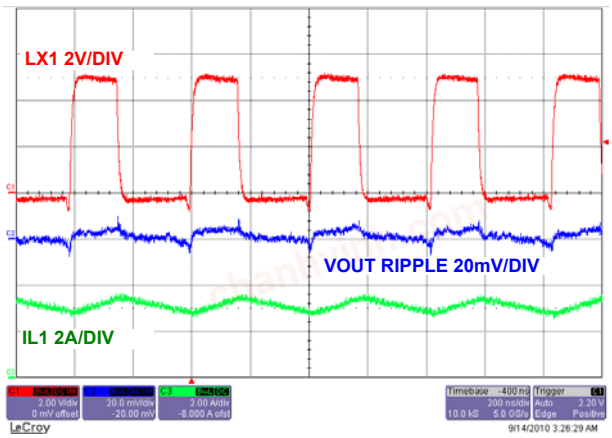


FIGURE 38. STEADY STATE OPERATION AT FULL LOAD CHANNEL 1

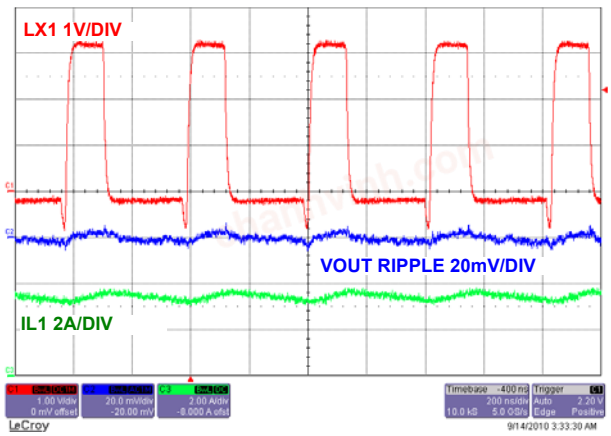


FIGURE 39. STEADY STATE OPERATION AT FULL LOAD CHANNEL 2

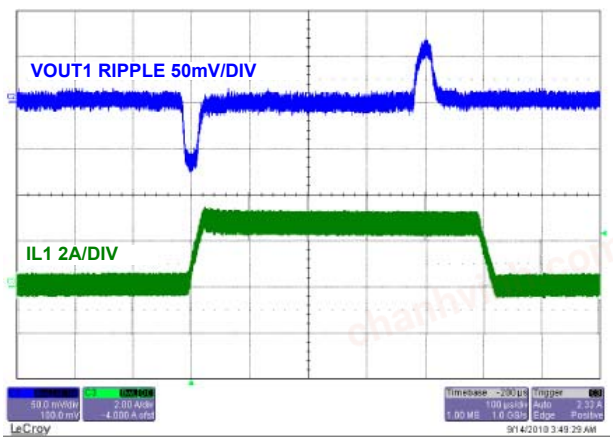


FIGURE 40. LOAD TRANSIENT CHANNEL 1

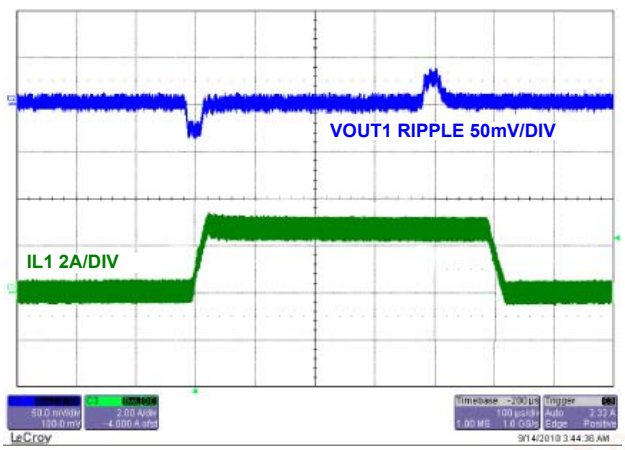


FIGURE 41. LOAD TRANSIENT CHANNEL 2

chanhvinh.com

ISL8036 Typical Operating Performance for Current Sharing PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT} = 1.8V, I_{OUT1} + I_{OUT2} = 0A to 6A, F_{SW} = 1MHz.

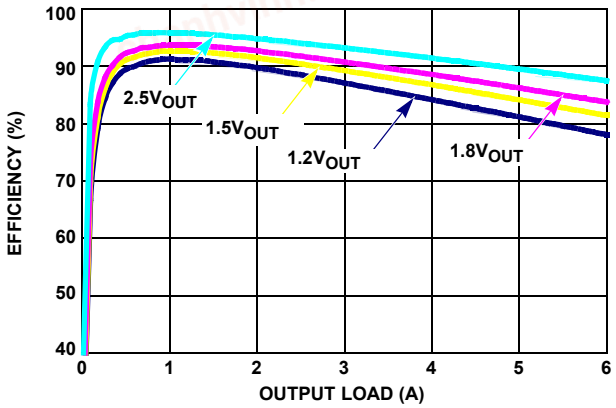


FIGURE 42. EFFICIENCY vs LOAD, V_{IN} = 3.3V, T_A = +25°C

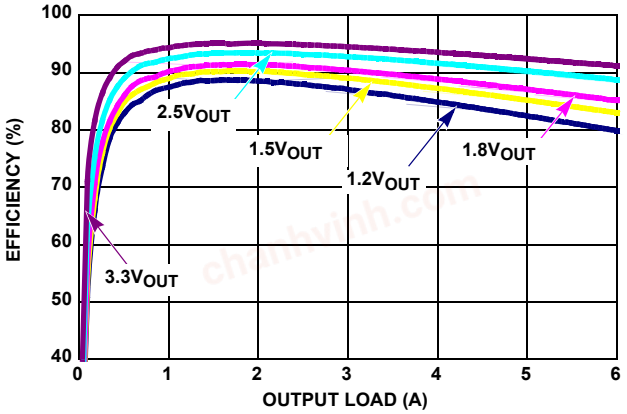


FIGURE 43. EFFICIENCY vs LOAD, V_{IN} = 5V, T_A = +25°C

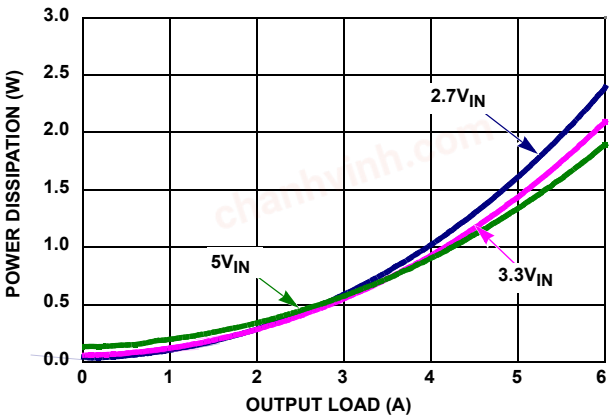


FIGURE 44. POWER DISSIPATION vs LOAD, 1.8V, T_A = +25°C

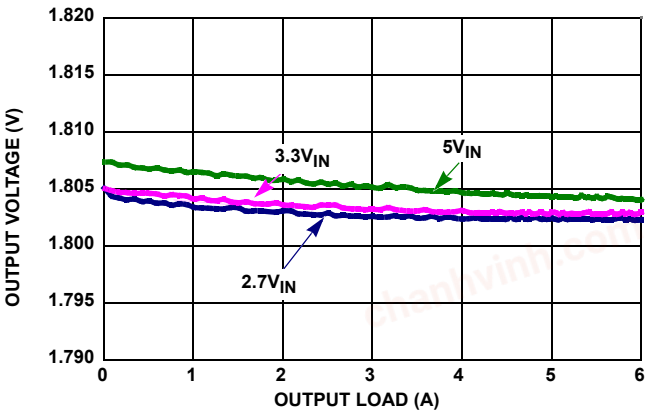


FIGURE 45. V_{OUT} REGULATION vs LOAD, 1.8V, T_A = +25°C

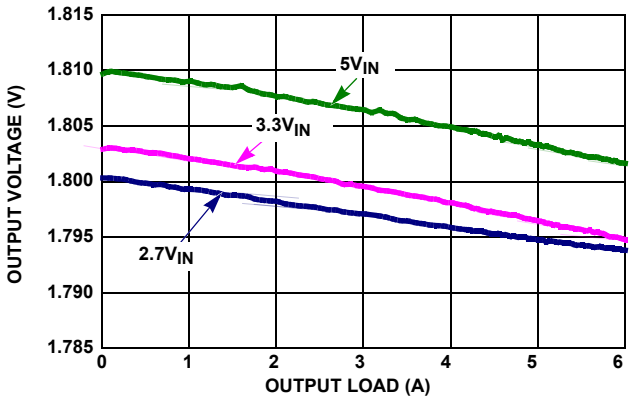


FIGURE 46. V_{OUT} REGULATION vs LOAD, 1.8V, T_A = -40°C

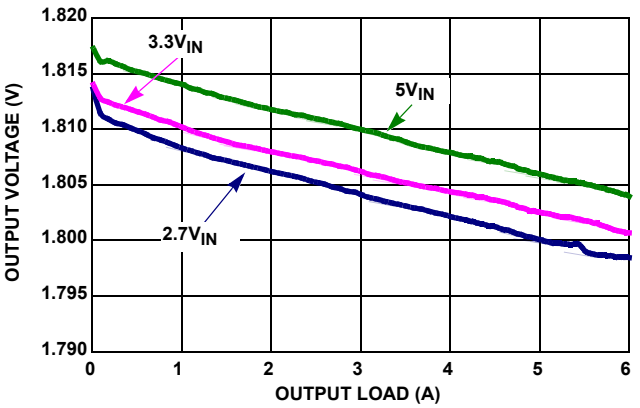


FIGURE 47. V_{OUT} REGULATION vs LOAD, 1.8V, T_A = +85°C

chanhvinh.com

ISL8036 Typical Operating Performance for Current Sharing PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT} = 1.8V, I_{OUT1} + I_{OUT2} = 0A to 6A, F_{SW} = 1MHz. **(Continued)**

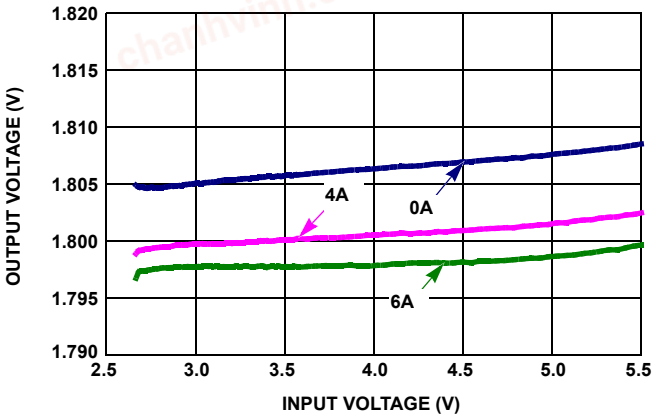


FIGURE 48. OUTPUT VOLTAGE REGULATION vs V_{IN}, T_A = +25°C

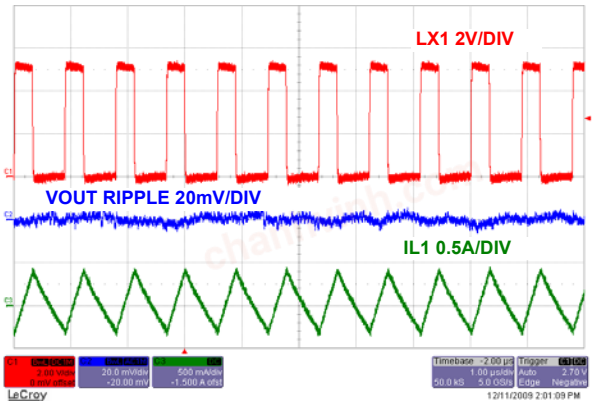


FIGURE 49. STEADY STATE OPERATION AT NO LOAD CHANNEL 1

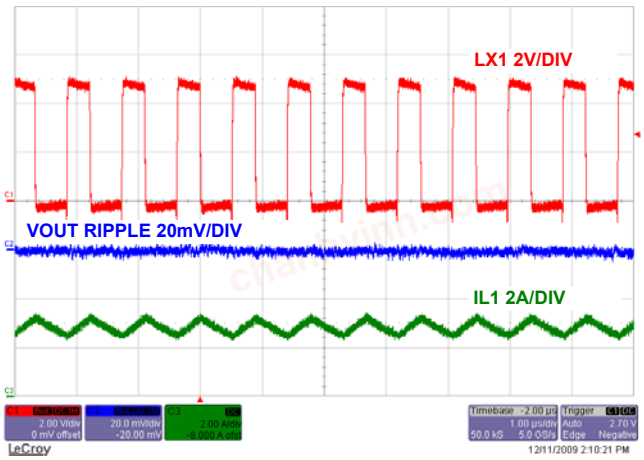


FIGURE 50. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 1

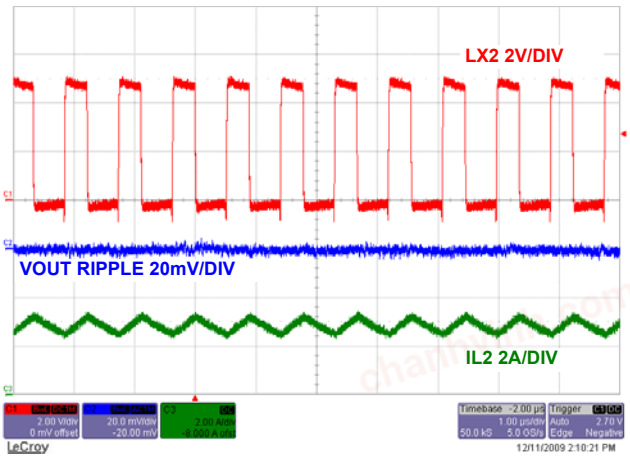


FIGURE 51. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 2

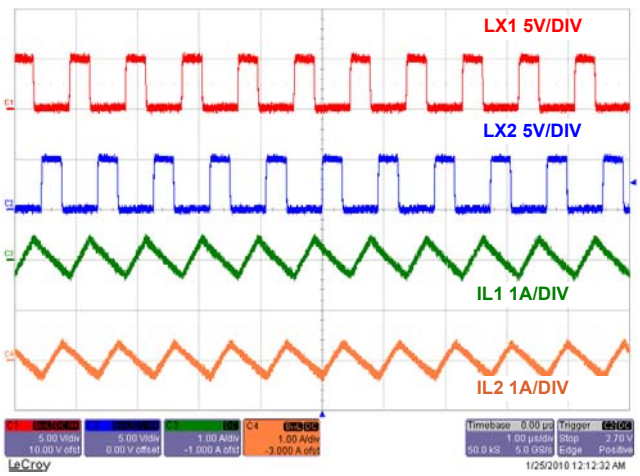


FIGURE 52. STEADY STATE OPERATION AT NO LOAD CHANNEL 1 AND 2

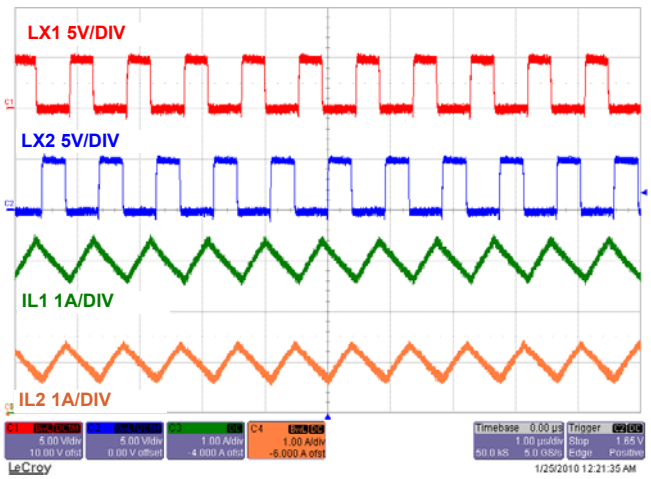


FIGURE 53. STEADY STATE OPERATION AT FULL LOAD CHANNEL 1 AND 2

chanhvinh.com

ISL8036 Typical Operating Performance for Current Sharing PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT} = 1.8V, I_{OUT1} + I_{OUT2} = 0A to 6A, F_{SW} = 1MHz. **(Continued)**

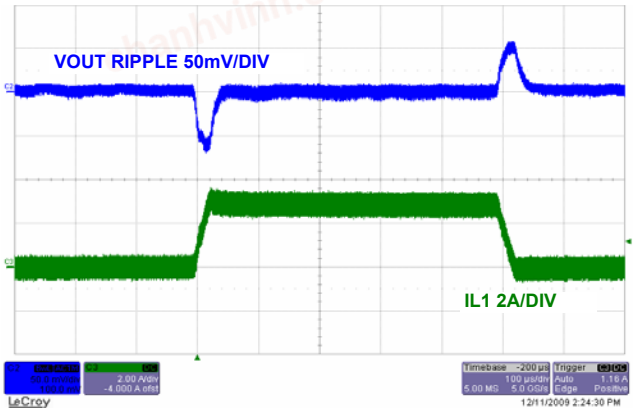


FIGURE 54. LOAD TRANSIENT CHANNEL 1

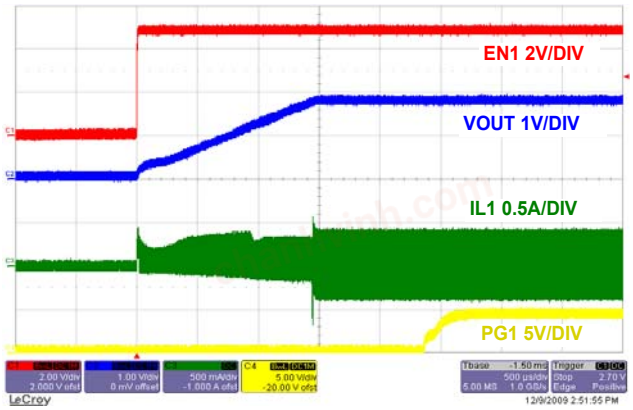


FIGURE 55. SOFT-START WITH NO LOAD CHANNEL 1

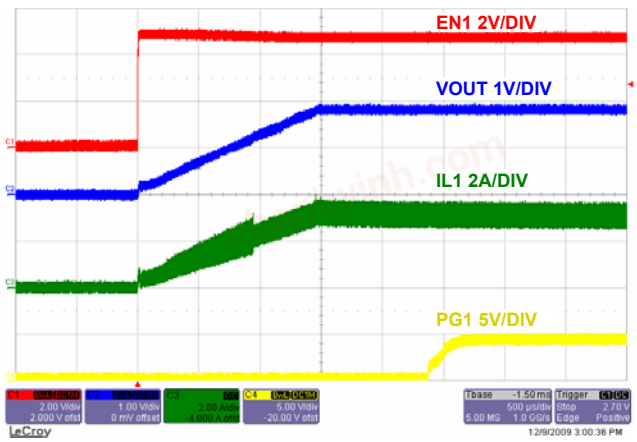


FIGURE 56. SOFT-START AT FULL LOAD CHANNEL 1

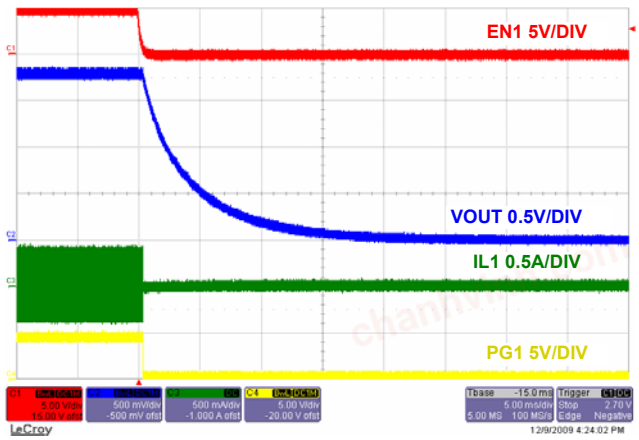


FIGURE 57. SOFT-DISCHARGE SHUTDOWN CHANNEL 1

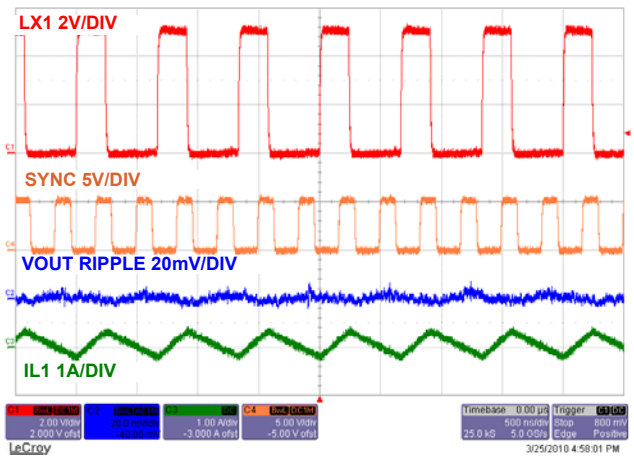


FIGURE 58. STEADY STATE OPERATION CH1 AT NO LOAD WITH F_{SW} = 3MHz

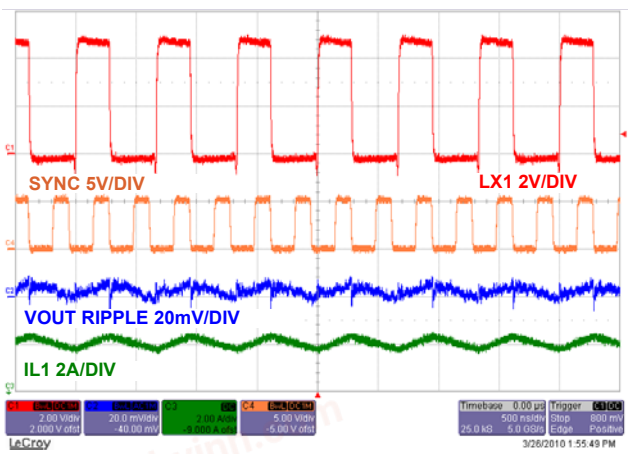


FIGURE 59. STEADY STATE OPERATION CH1 AT FULL LOAD WITH F_{SW} = 3MHz

chanhvinh.com

ISL8036 Typical Operating Performance for Current Sharing PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT} = 1.8V, I_{OUT1} + I_{OUT2} = 0A to 6A, F_{SW} = 1MHz. **(Continued)**

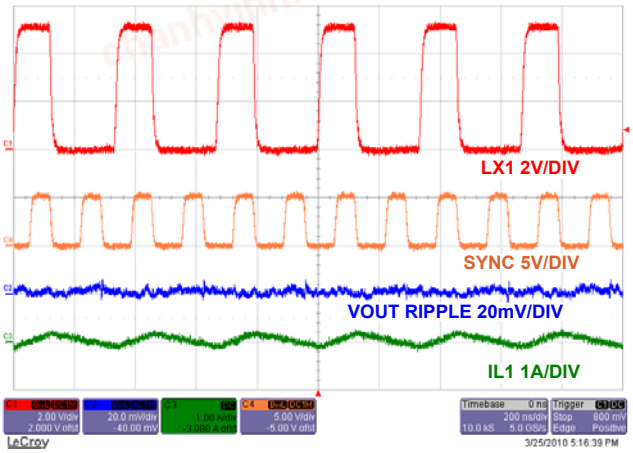


FIGURE 60. STEADY STATE OPERATION CH1 AT NO LOAD WITH F_{SW} = 6MHz

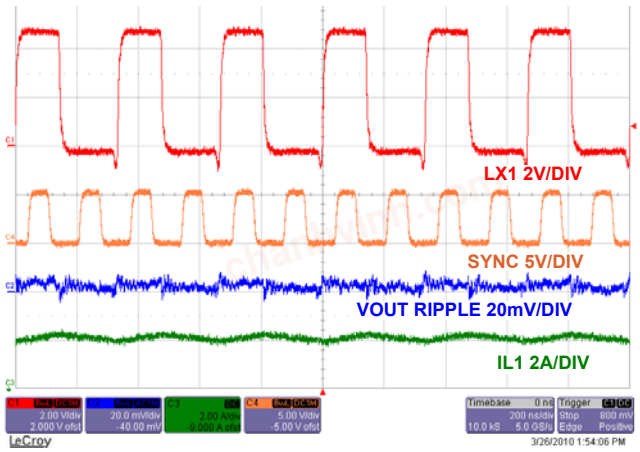


FIGURE 61. STEADY STATE OPERATION CH1 AT FULL LOAD WITH F_{SW} = 6MHz

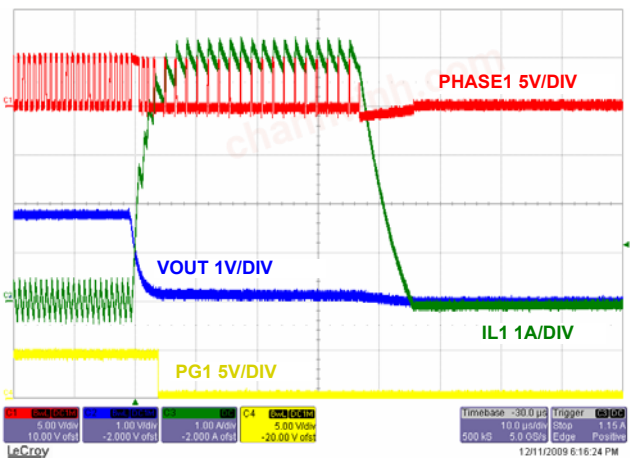


FIGURE 62. OUTPUT SHORT CIRCUIT CHANNEL 1

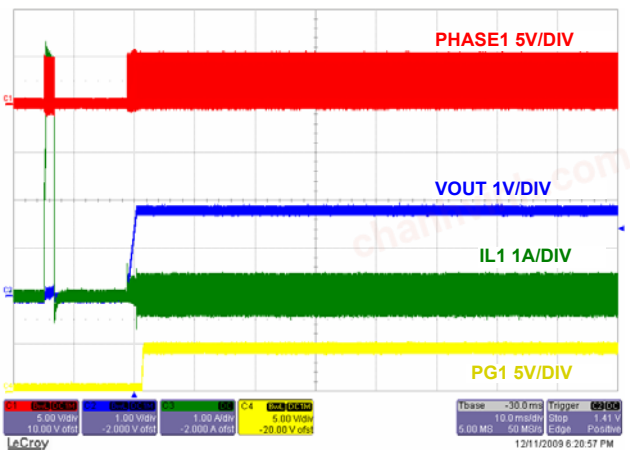


FIGURE 63. OUTPUT SHORT CIRCUIT RECOVERY (FROM HICCUP) CHANNEL 1

chanhvinh.com

ISL8036A Typical Operating Performance for Current Sharing PWM Operation

Unless otherwise noted, operating conditions are: V_{OUT} = 1.8V, I_{OUT1} + I_{OUT2} = 0A to 6A, L1 = L2 = 0.6µH, F_{SW} = 2.5MHz.

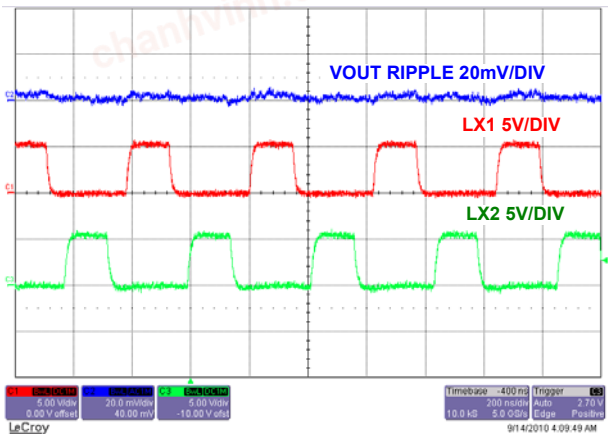


FIGURE 64. STEADY STATE OPERATION AT NO LOAD

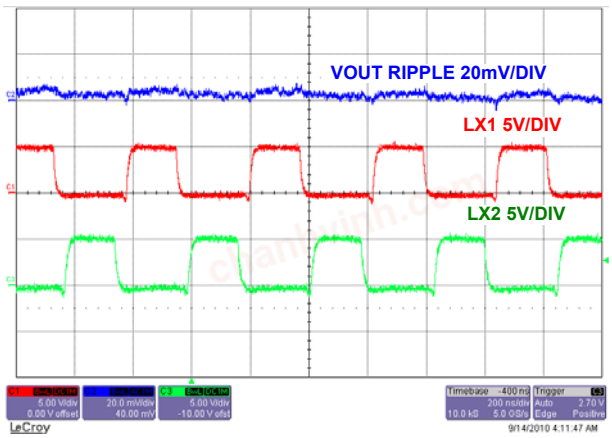


FIGURE 65. STEADY STATE OPERATION AT FULL 6A LOAD

chanhvinh.com

Theory of Operation

The ISL8036, ISL8036A is a dual 3A or current sharing 6A step-down switching regulator optimized for battery-powered or mobile applications. The regulator operates at 1MHz (ISL8036) or 2.5MHz (ISL8036A) fixed switching frequency under heavy load condition. The two channels are 180° out-of-phase operation. The supply current is typically only 8µA when the regulator is shutdown.

PWM Control Scheme

Pulling the SYNC pin HI (>1.5V) forces the converter into PWM mode in the next switching cycle regardless of output current. Each of the channels of the ISL8036, ISL8036A employ the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting, as shown in the "Block Diagram" on page 4 with waveforms in Figure 66. The current loop consists of the oscillator, the PWM comparator COMP, current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-channel MOSFET when it is turned on and the current sense amplifier CSA1. The gain for the current sensing circuit is typically 0.2V/A. The control reference for the current loops comes from the error amplifier EAMP of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA1 (or CSA2 on Channel 2) and the compensation slope (0.46V/µs) reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-MOSFET and to turn on the N-channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 66 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier CSA_ output.

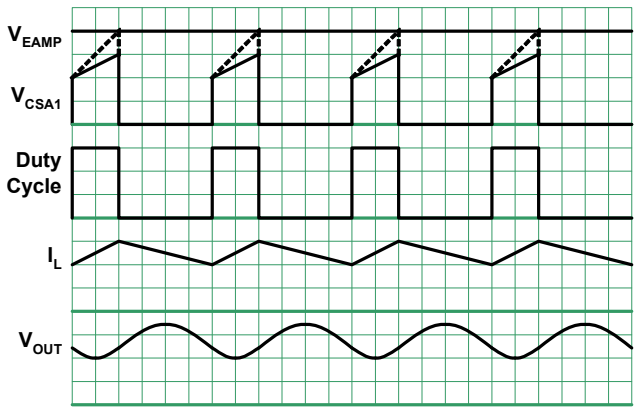


FIGURE 66. PWM OPERATION WAVEFORMS

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage control loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 390kΩ RC network. The maximum EAMP voltage output is precisely clamped to the bandgap voltage (1.172V).

Synchronization Control

The frequency of operation can be synchronized up to 6MHz by an external signal applied to the SYNC pin. The 1st falling edge on the SYNC triggered the rising edge of the PWM ON pulse of Channel 1. The 2nd falling edge of the SYNC triggers the rising edge of the PWM ON pulse of the Channel 2. This process alternate indefinitely allowing 180° output phase operation between the two channels.

Output Current Sharing

The ISL8036, ISL8036A dual outputs are paralleled for multi-phase operation in order to support a 6A output. Connect the FBs together and connect all the COMPs together. Channel 1 and Channel 2 will be 180° out-of-phase. In parallel configuration, external soft-start should be used to ensure proper full loading start-up. Before using full load in current sharing mode, PWM mode should be enabled. Likewise, multiple regulators can be paralleled by connecting the FBs, COMPs, and SS for higher current capability. External compensation is required.

Overcurrent Protection

CAS1 and CSA2 are used to monitor Output 1 and Output 2 channels respectively. The overcurrent protection is realized by monitoring the CSA output with the OCP threshold logic, as shown in Figure 4. The current sensing circuit has a gain of 0.2V/A, from the P-MOSFET current to the CSA_ output. When the CSA1 output reaches the threshold, the OCP comparator is tripped to turn off the P-MOSFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFETs.

Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the Overcurrent Fault Counter is set to 1 and the Overcurrent Condition Flag is set from LOW to HIGH. If, on the subsequent cycle, another overcurrent condition is detected, the OC Fault Counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shutdown under an Overcurrent Fault Condition. An Overcurrent Fault Condition will result with the regulator attempting to restart in a hiccup mode with the delay between restarts being 8 soft-start periods. At the end of the eighth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away prior to the OC Fault Counter reaching a count of four, the Overcurrent Condition Flag will set back to LOW.

If the negative output current reaches -2.5A, the part enters Negative Overcurrent Protection. At this point, all switching stops and the part enters tri-state mode while the pull-down FET is discharging the output until it reaches normal regulation voltage, then the IC restarts.

PG

There are two independent power-good signals. PG1 monitors the Output Channel 1 and PG2 monitors the Output Channel 2. When powering up, the open-collector Power-on Reset output holds low for about 1ms after V_O reaches the preset voltage. The PG_ output also serves as a 1ms delayed Power-Good signal.

chanhvinh.com

UVLO

When the input voltage is below the undervoltage lock out (UVLO) threshold, the regulator is disabled.

Enable

The enable (EN) input allows the user to control the turning on or off the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference. Then the soft start-up begins.

Soft-start-up

The soft-start-up eliminates the inrush current during the start-up. The soft-start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage speed so that the output voltage rises in a controlled fashion. At the very beginning of the start-up, the output voltage is less than 0.5V; hence the PWM operating frequency is 1/2 of the normal frequency.

When the IC ramps up at start-up, it can't sink current even at PWM mode, behaving like in diode emulated mode for the soft-start time.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs, or the output undervoltage fault latch is set, its output discharges to PGND through an internal 100Ω switch.

Power MOSFETs

The power MOSFETs are optimize for best efficiency. The ON-resistance for the P-MOSFET is typically 50mΩ and the ON-resistance for the N-MOSFET is typical 50mΩ.

100% Duty Cycle

The ISL8036, ISL8036A features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL8036, ISL8036A can no longer maintain the regulation at the output, the regulator completely turns on the P-MOSFET. The maximum drop-out voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-MOSFET.

Thermal Shutdown

The ISL8036, ISL8036A has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shutdown. As the temperature drops to +125°C, the ISL8036, ISL8036A resumes operation by stepping through a soft start-up.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operation, ISL8036, ISL8036A typically uses a 1.5µH output inductor. Higher or lower inductor value can be used to optimize the total converter system performance. For example, for a higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. The inductor ripple current can be expressed in Equation 2:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 2)}$$

The inductor's saturation current rating needs be at least larger than the peak current. The ISL8036, ISL8036A protects the typical peak current 4.8A. The saturation current needs be over 4.8A for maximum output current application.

ISL8036, ISL8036A uses an internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended minimum output capacitor values for the ISL8036, ISL8036A are shown in Table 4.

TABLE 4. OUTPUT CAPACITOR VALUE vs V_{OUT} ISL8036, ISL8036A

V_{OUT} (V)	C_{OUT} (µF)	L (µH)
0.8	2 x 22	1.0~2.2
1.2	2 x 22	1.0~2.2
1.6	2 x 22	1.0~2.2
1.8	2 x 22	1.0~3.3
2.5	2 x 22	1.0~3.3
3.3	2 x 6.8	1.0~4.7
3.6	10	1.0~4.7

In Table 4, the minimum output capacitor value is given for different output voltages to make sure the whole converter system is stable.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider, which is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier. Refer to Figure 2.

The output voltage programming resistor, R_2 (or R_5 in Channel 2), will depend on the desired output voltage of the regulator. The value for the feedback resistor is typically between 0Ω and 750kΩ. Let R_2 = 124kΩ, then R_3 will be:

$$R_3 = \frac{R_2 x 0.8V}{V_{OUT} - 0.8V} \quad \text{(EQ. 3)}$$

For better performance, add 12pF in parallel with R_2. If the output voltage desired is 0.8V, then leave R_3 unpopulated and short R_2.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. One 22µF X5R or X7R ceramic capacitor is a good starting point for the input capacitor selection per channel.

chanhvinh.com

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For ISL8036, ISL8036A, the power loop is composed of the output inductor L's, the output capacitor C_{OUT1} and C_{OUT2}, the LX's pins, and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the LX_ pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The FB network should be as close as possible to its FB pin. SGND should have one single connection to PGND. The input capacitor should be placed as closely as possible to the VIN pin. Also, the ground of the input and output capacitors should be connected as closely as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 5 vias ground connection within the pad for the best thermal relief.

© Copyright Intersil Americas LLC 2010-2012. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

chanhvinh.com

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
July 18, 2012	FN6853.3	page 5 Comments added, COMP pin: COMP pin is NC in dual mode operation, using internal compensation. If SS pin is tied to CSS (without VIN connection), external compensation is automatically used. Connect an external R,C network on COMP pin for parallel mode operation. Comments added, SS pin: When SS pin is tied to VIN, SS time is 1.5ms. SS pin is tied to VIN only in dual mode operation. SS pin is tied to CSS only in parallel mode operation, using only external compensation. page 6 Ordering Information table, added evals: ISL8036ACRSHEVAL1Z, ISL8036ADUALEVAL1Z, ISL8036CRSHEVAL1Z, ISL8036DUALEVAL1Z page 15 Figure 33 title correction: "1.8VIN" on the title of these is changed to "1.8VOUT". Figure 34 title correction: "1.8VIN" on the title of these is changed to "1.8VOUT" Figure 35 title correction: "1.8VIN" on the title of these is changed to "1.8VOUT" page 18, Figure 48, deleted "1.8V" in the title since the condition is mentioned in the page header. page 22 Line 4 in Overcurrent Protection paragraph, instead of "Figure 66" changed to "Figure 4". "with the delay between restarts being 4 soft-start periods" changed to "with the delay between restarts being 8 soft-start periods". "end of the fourth soft-start wait period" to "end of the eighth soft-start wait period"
October 14, 2011	FN6853.2	Added “Related Literature” on page 1. In the “Absolute Maximum Ratings” on page 8, changed: “LX1, LX2....-1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)” to: “LX1, LX2....-3V/(10ns)/-1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)/8.5V(10ns)”
October 12, 2010	FN6853.1	In Table 3 on page 3, corrected F_{SW} for ISL8036 from 1Hz to 1MHz.
September 28, 2010	FN6853.0	Initial release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL8036, ISL8036A

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

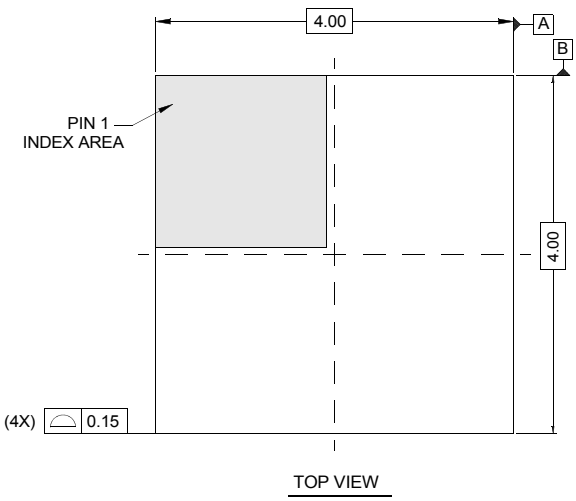
FITs are available from our website at: http://rel.intersil.com/reports/search.php

chanhvinh.com

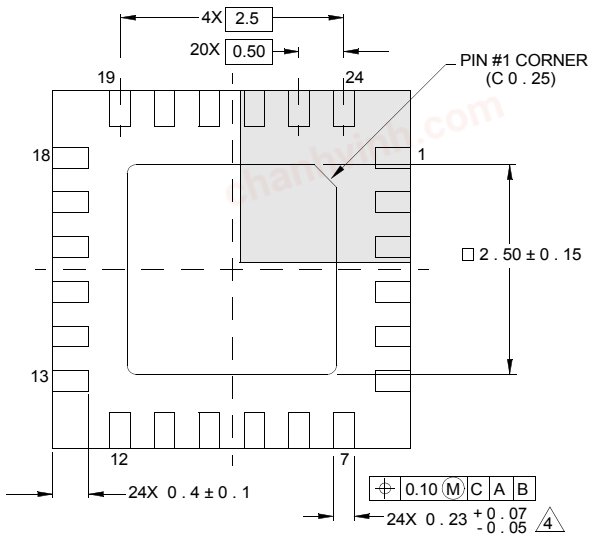
Package Outline Drawing

L24.4x4D

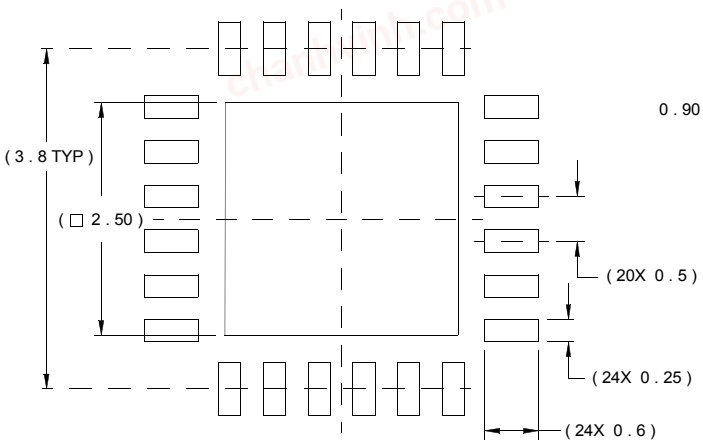
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



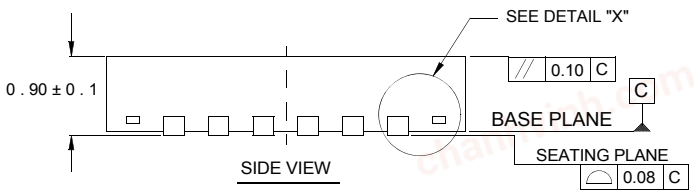
TOP VIEW



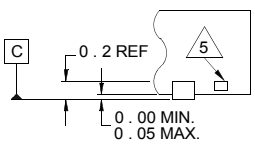
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.