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ISL6262A

Two-Phase Core Controller (Santa Rosa, IMVP-6+)

FN6343
Rev 1.00
December 23, 2008

The ISL6262A is a two-phase buck converter regulator implementing Intel® IMVP-6+ protocol with embedded gate drivers. The two-phase buck converter uses two interleaved channels to effectively double the output voltage ripple frequency, and thereby reduce output voltage ripple amplitude with fewer components; lower component cost; reduced power dissipation; and smaller real estate area.

The heart of the ISL6262A is the patented R^3 Technology™, Intersil's Robust Ripple Regulator modulator. Compared with the traditional multiphase buck regulator, the R^3 Technology™ has the fastest transient response. This is due to the R^3 modulator commanding variable switching frequency during a load transient.

Intel® Mobile Voltage Positioning (IMVP) is a smart voltage regulation technology, which effectively reduces power dissipation in Intel® Pentium processors. To boost battery life, the ISL6262A supports DPRSLPVR (deeper sleep), DPRSTP# and PSI# functions, and maximizes the efficiency via automatically enabling different phase operation modes. At heavy load operation of the active mode, the regulator commands the two phase continuous conduction mode (CCM) operation. While the PSI# is asserted with medium load in active mode, the ISL6262A smoothly disables one phase and operates in one-phase CCM. When the CPU enters deeper sleep mode, the ISL6262A enables diode emulation to maximize the efficiency at light load.

For better system power management of the portable computer, the ISL6262A also provides a CPU power monitor output. The analog output at the power monitor pin can be fed into an A/D converter to report instantaneous or average CPU power.

A 7-bit digital-to-analog converter (DAC) allows dynamic adjustment of the core output voltage from 0.300V to 1.500V. A 0.5% system accuracy of the core output voltage over-temperature is achieved by the ISL6262A.

A unity-gain differential amplifier is provided for remote CPU die sensing. This allows the voltage on the CPU die to be accurately measured and regulated per Intel® IMVP-6+ specifications. Current sensing can be realized using either lossless inductor DCR sensing, or precision resistor sensing. A single NTC thermistor network thermally compensates the gain and the time constant of the DCR variations.

Features

- Precision Two/One-phase CORE Voltage Regulator
  - 0.5% System Accuracy Over-Temperature
  - Enhanced Load Line Accuracy
- Internal Gate Driver with 2A Driving Capability
- Dynamic Phase Adding/Dropping
- Microprocessor Voltage Identification Input
  - 7-Bit VID Input
  - 0.300V to 1.500V in 12.5mV Steps
  - Support VID Change On-the-Fly
- Multiple Current Sensing Schemes Supported
  - Lossless Inductor DCR Current Sensing
  - Precision Resistive Current Sensing
- CPU Power Monitor
- Thermal Monitor
- User Programmable Switching Frequency
- Differential Remote CPU Die Voltage Sensing
- Static and Dynamic Current Sharing
- Overvoltage, Undervoltage, and Overcurrent Protection
- Pb-Free (RoHS Compliant)

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6262ACRZ	ISL6262 ACRZ	-10 to +100	48 Ld 7x7 QFN	L48.7x7
ISL6262ACRZ-T*	ISL6262 ACRZ	-10 to +100	48 Ld 7x7 QFN	L48.7x7
ISL6262AIRZ	ISL6262 AIRZ	-40 to +100	48 Ld 7x7 QFN	L48.7x7
ISL6262AIRZ-T*	ISL6262 AIRZ	-40 to +100	48 Ld 7x7 QFN	L48.7x7

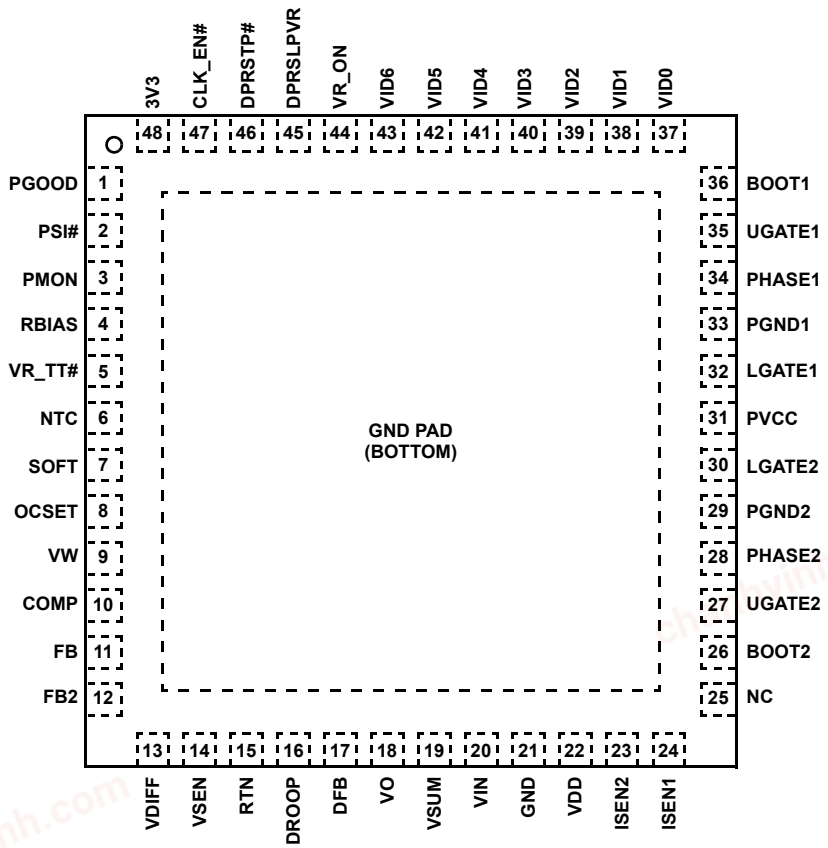
*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

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Pinout

ISL6262A
(48 LD 7x7 QFN)
TOP VIEW



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Absolute Maximum Ratings

Supply Voltage, VDD . . . . . -0.3 to +7V
Battery Voltage, VIN. . . . . +28V
Boot Voltage (BOOT). . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT to PHASE . . . . . -0.3V to +7V (DC)
-0.3V to +9V (<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20nS Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE -0.3V (DC) to BOOT
. . . . . PHASE-5V (<20nS Pulse Width, 10µJ) to BOOT
LGATE Voltage (LGATE) . . . . . -0.3V (DC) to (VDD +0.3V)
. . . . . -2.5V (<20nS Pulse Width, 5µJ) to (VDD +0.3V)
All Other Pins. . . . . -0.3V to (VDD +0.3V)
Open Drain Outputs, PGOOD, VR_TT# . . . . . -0.3 to +7V

Thermal Information

Thermal Resistance (Typical)	θ_{JA}°C/W	θ_{JC}°C/W
QFN Package (Notes 1, 2).	29	4.5

Maximum Storage Temperature Range. . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage, VDD . . . . . +5V ±5%
Battery Voltage, VIN . . . . . +5V to 25V
Ambient Temperature
Commercial . . . . . -10°C to +100°C
Industrial. . . . . -40°C to +100°C
Junction Temperature
Commercial . . . . . -10°C to +125°C
Industrial. . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{DD} = 5V, T_A = -40°C to +100°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	VR_ON = 3.3V		3.6	4.1	mA
		VR_ON = 0V			1	µA
+3.3V Supply Current	I_{3V3}	No load on CLK_EN#			1	µA
Battery Supply Current at VIN pin	I_{VIN}	VR_ON = 0V, VIN = 25V			1	µA
POR (Power-On Reset) Threshold	POR_r	V_{DD} Rising		4.35	4.5	V
	POR_f	V_{DD} Falling	4.0	4.15		V
SYSTEM AND REFERENCES						
System Accuracy	%Error (V_{CC_CORE}) ISL6262ACRZ	No load, closed loop, active mode, T_A = 0°C to +100°C, VID = 0.75 to 1.5V	-0.5		0.5	%
		VID = 0.5 to 0.7375V	-8		8	mV
		VID = 0.3 to 0.4875V	-15		15	mV
System Accuracy	%Error (V_{CC_CORE}) ISL6262AIRZ	No load, closed loop, active mode, T_A = -40°C to +100°C, VID = 0.75 to 1.5V	-0.8		0.8	%
		VID = 0.5 to 0.7375V	-10		10	
		VID = 0.3 to 0.4875V	18		18	mV
Droop Amplifier Offset			0.3		0.3	
R_{BIAS} Voltage	R_{RBIAS}	R_{RBIAS} = 147kΩ	1.45	1.47	1.49	V
Boot Voltage	V_{BOOT}		1.188	1.2	1.212	V
Maximum Output Voltage	V_{CC_CORE} (max)	VID = [0000000]		1.5		V
	V_{CC_CORE} (min)	VID = [1100000]		0.3		V
VID Off State		VID = [1111111]		0		V

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CHANNEL FREQUENCY						
Nominal Channel Frequency	f_{SW}	R_{FSET} = 6.9kΩ, 2 channel operation, V_{COMP} = 2V	285	300	315	kHz
Adjustment Range			100		500	kHz
AMPLIFIERS						
Droop Amplifier Offset			-0.3		0.3	mV
Error Amp DC Gain	A_{V0}			90		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF		18		MHz
Error Amp Slew Rate	SR	C_L = 20pF		5		V/µs
FB Input Current	$I_{IN(FB)}$			10	150	nA
ISEN						
Imbalance Voltage					2	mV
Input Bias Current				20		nA
SOFT-START CURRENT						
Soft-Start Current	I_{SS}		-47	-42	-37	µA
Soft Geyserville Current	I_{GV}	|SOFT - REF|>100mV	±180	±205	±230	µA
Soft Deeper Sleep Entry Current	I_{C4}	DPRSLPVR = 3.3V	-47	-42	-37	µA
Soft Deeper Sleep Exit Current	I_{C4EA}	DPRSLPVR = 3.3V	37	42	47	µA
Soft Deeper Sleep Exit Current	I_{C4EB}	DPRSLPVR = 0V	180	205	230	µA
GATE DRIVER DRIVING CAPABILITY						
UGATE Source Resistance	$R_{SRC(UGATE)}$	500mA Source Current		1	1.5	Ω
UGATE Source Current	$I_{SRC(UGATE)}$	V_{UGATE_PHASE} = 2.5V		2		A
UGATE Sink Resistance	$R_{SNK(UGATE)}$	500mA Sink Current		1	1.5	Ω
UGATE Sink Current	$I_{SNK(UGATE)}$	V_{UGATE_PHASE} = 2.5V		2		A
LGATE Source Resistance	$R_{SRC(LGATE)}$	500mA Source Current		1	1.5	Ω
LGATE Source Current	$I_{SRC(LGATE)}$	V_{LGATE} = 2.5V		2		A
LGATE Sink Resistance	$R_{SNK(LGATE)}$	500mA Sink Current		0.5	0.9	Ω
LGATE Sink Current	$I_{SNK(LGATE)}$	V_{LGATE} = 2.5V		4		A
UGATE to PHASE Resistance	$R_{p(UGATE)}$			1		kΩ
GATE DRIVER SWITCHING TIMING (refer to “ISL6262A Gate Driver Timing Diagram” on page 6)						
UGATE Rise Time	t_{RU}	PV_{CC} = 5V, 3nF Load		8.0		ns
LGATE Rise Time	t_{RL}	PV_{CC} = 5V, 3nF Load		8.0		ns
UGATE Fall Time	t_{FU}	PV_{CC} = 5V, 3nF Load		8.0		ns
LGATE Fall Time	t_{FL}	PV_{CC} = 5V, 3nF Load		4.0		ns
UGATE Turn-on Propagation Delay	t_{PDHU}	PV_{CC} = 5V, Outputs Unloaded		30		ns
LGATE Turn-on Propagation Delay	t_{PDHU}	PV_{CC} = 5V, Outputs Unloaded		15		ns
BOOTSTRAP DIODE						
Forward Voltage		V_{DDP} = 5V, Forward Bias Current = 2mA	0.43	0.58	0.72	V
Leakage		V_R = 16V			1	µA
POWER GOOD and PROTECTION MONITOR						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA		0.26	0.4	V
PGOOD Leakage Current	I_{OH}	P_{GOOD} = 3.3V	-1		1	µA

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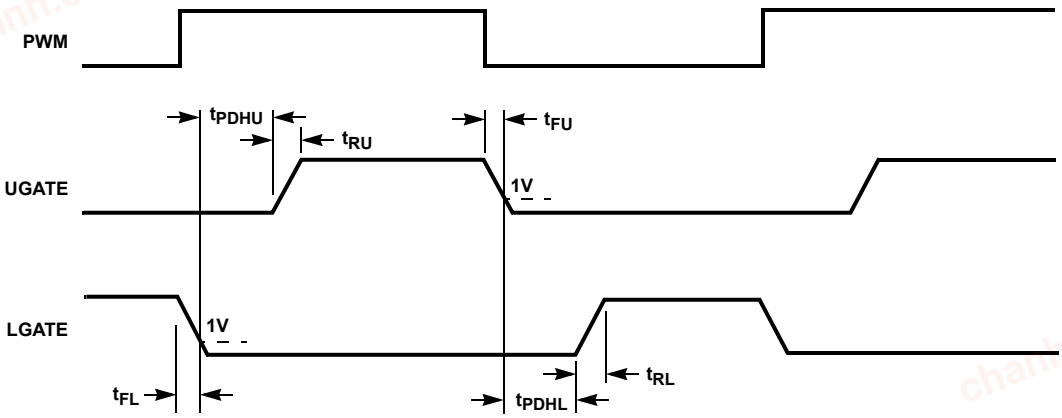
Electrical Specifications

V_{DD} = 5V, T_A = -40°C to +100°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

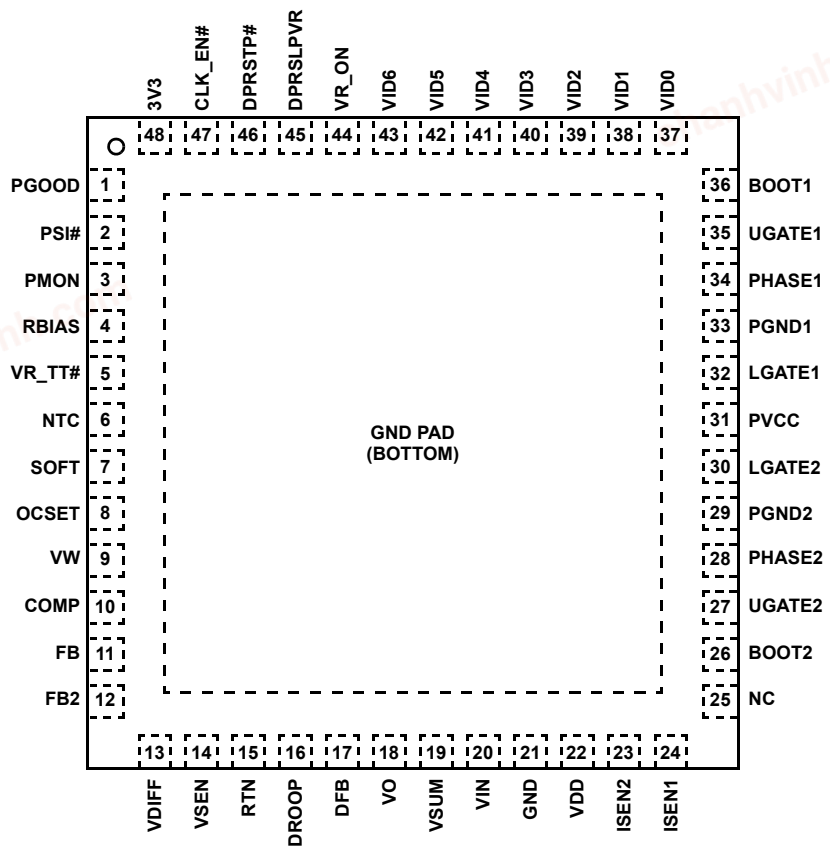
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Delay	t_{pgd}	CLK_EN# Low to PGOOD High	6.3	7.6	8.9	ms
Overvoltage Threshold	O_{VH}	V_O rising above setpoint >1ms	160	200	240	mV
Severe Overvoltage Threshold	O_{VHS}	V_O rising above setpoint >0.5µs	1.675	1.7	1.725	V
OCSET Reference Current		I (R_{BIAS}) = 10µA	9.8	10	10.2	µA
OC Threshold Offset		DROOP rising above OCSET >120µs	-3.5		3.5	mV
Current Imbalance Threshold		Difference between ISEN1 and ISEN2 >1ms		9		mV
Undervoltage Threshold (VDIFF-SOFT)	UV_f	V_O falling below setpoint for >1ms	-360	-300	-240	mV
LOGIC INPUTS						
VR_ON, DPRSLPVR Input Low	$V_{IL(3.3V)}$				1	V
VR_ON, DPRSLPVR Input High	$V_{IH(3.3V)}$		2.3			V
Leakage Current of VR_ON	$I_{IL(3.3V)}$	Logic input is low	-1	0		µA
	$I_{IH(3.3V)}$	Logic input is high at 3.3V		0	1	µA
Leakage Current of DPRSLPVR	$I_{IL_DPRSLP(3.3V)}$	DPRSLPVR input is low	-1	0		µA
	$I_{IH_DPRSLP(3.3V)}$	DPRSLPVR input is high at 3.3V		0.45	1	µA
DAC(VID0-VID6), PSI# and DPRSTP# Input Low	$V_{IL(1V)}$				0.3	V
DAC(VID0-VID6), PSI# and DPRSTP# Input High	$V_{IH(1V)}$		0.7			V
Leakage Current of DAC(VID0-VID6), PSI# and DPRSTP#	$I_{IL(1V)}$	Logic input is low	-1	0		µA
	$I_{IH(1V)}$	Logic input is high at 1V		0.45	1	µA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	53	60	67	µA
Over-Temperature Threshold		V(NTC) falling	1.18	1.2	1.22	V
VR_TT# Low Output Resistance	R_{TT}	I = 20mA		6.5	9	Ω
POWER MONITOR						
PMON Output Voltage Range	V_{pmon}	VSEN = 1.2V, Droop - V_O = 80mV	1.638	1.680	1.722	V
		VSEN = 1V, Droop - V_O = 20mV	0.308	0.350	0.392	V
PMON Maximum Voltage	$V_{pmonmax}$		2.8	3.0		V
PMON Sourcing Current	I_{sc_pmon}	VSEN = 1V, Droop - V_O = 50mV	2			mA
PMON Sinking Current	I_{sk_pmon}	VSEN = 1V, Droop - V_O = 50mV	2			mA
Maximum Current Sinking Capability		(see Figure 31)	PMON/ 250Ω	PMON/ 180Ω	PMON/ 130Ω	A
PMON Impedance		When PMON is within its sourcing/sinking current range (Established by characterization)		7		Ω
CLK_EN# OUTPUT LEVELS						
CLK_EN# High Output Voltage	V_{OH}	3V3 = 3.3V, I = -4mA	2.9	3.1		V
CLK_EN# Low Output Voltage	V_{OL}	$I_{CLK_EN\#}$ = 4mA		0.26	0.4	V

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ISL6262A Gate Driver Timing Diagram



Functional Pin Description



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PGOOD - Power good open-drain output. Connect externally with 680Ω to VCCP or 1.9kΩ to 3.3V.

PSI# - Current indicator input. When asserted low, indicates a reduced load-current condition and initiates single-phase operation.

PMON - Analog output. PMON is proportional to the product of Vsen and droop voltage.

RBIAS - 147k resistor to GND sets internal current reference.

VR_TT# - Thermal overload output indicator with open-drain output. Over-temperature pull-down resistance is 10Ω.

NTC - Thermistor input to VRTT# circuit and a 60µA current source is connected internally to this pin.

SOFT - A capacitor from this pin to GND sets the maximum slew rate of the output voltage. SOFT is the non-inverting input of the error amplifier.

OCSET - Overcurrent set input. A resistor from this pin to VO sets DROOP voltage limit for OC trip. A 10µA current source is connected internally to this pin.

VW - A resistor from this pin to COMP programs the switching frequency (for example, 6.82kΩ ≅ 300kHz).

COMP - This pin is the output of the error amplifier.

FB - This pin is the inverting input of error amplifier.

FB2 - There is a switch between FB2 pin and the FB pin. The switch is closed in single-phase operation and is opened in two phase operation. The components connecting to FB2 are to adjust the compensation in single phase operation to achieve optimum performance.

VDIFF - This pin is the output of the differential amplifier.

VSEN - Remote core voltage sense input.

RTN - Remote core voltage sense return.

DROOP - Output of the droop amplifier. The voltage level on this pin is the sum of V_O and the droop voltage.

DFB - Inverting input to droop amplifier.

VO - An input to the IC that reports the local output voltage.

VSUM - This pin is connected to the summation junction of channel current sensing.

VIN - Battery supply voltage. It is used for input voltage feed-forward to improve input line transient performance.

GND - Signal ground. Connect to local controller ground.

VDD - 5V control power supply.

ISEN2 - Individual current sharing sensing for Channel 2. If ISEN2 is pulled to 5V, phase 2's gate signals are disabled. ISL6262A is then configured in always-1-phase mode.

ISEN1 - Individual current sharing sensing for Channel 1.

N/C - Not connected. Grounding this pin to signal ground in the practical layout.

BOOT2 - This pin is the upper gate driver supply voltage for phase 2. An internal boot strap diode is connected to the PVCC pin.

UGATE2 - Upper MOSFET gate signal for phase 2.

PHASE2 - The phase node of phase 2. Connect this pin to the source of the Channel 2 upper MOSFET.

PGND2 - The return path of the lower gate driver for phase 2.

LGATE2 - Lower-side MOSFET gate signal for phase 2.

PVCC - 5V power supply for gate drivers.

LGATE1 - Lower-side MOSFET gate signal for phase 1.

PGND1 - The return path of the lower gate driver for phase 1.

PHASE1 - The phase node of phase 1. Connect this pin to the source of the Channel 1 upper MOSFET.

UGATE1 - Upper MOSFET gate signal for phase 1.

BOOT1 - This pin is the upper-gate-driver supply voltage for phase 1. An internal boot strap diode is connected to the PVCC pin.

VID0, VID1, VID2, VID3, VID4, VID5, VID6 - VID input with VID0 is the least significant bit (LSB) and VID6 is the most significant bit (MSB).

VR_ON - Digital enable input. A logic high signal on this pin enables the regulator.

DPRSLPVR - Deeper sleep enable signal. A logic high signal on this pin indicates the micro-processor is in deeper-sleep mode and also indicates a slow C4 entry or exit rate with 41µA discharging or charging the SOFT capacitor.

DPRSTP# - Deeper sleep slow wake up signal. A logic low signal on this pin indicates the micro-processor is in deeper-sleep mode.

CLK_EN# - Digital output for system clock. Goes active 13 clks after V_{core} is within 10% of Boot voltage.

3V3 - 3.3V supply voltage for CLK_EN#.

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Functional Block Diagram

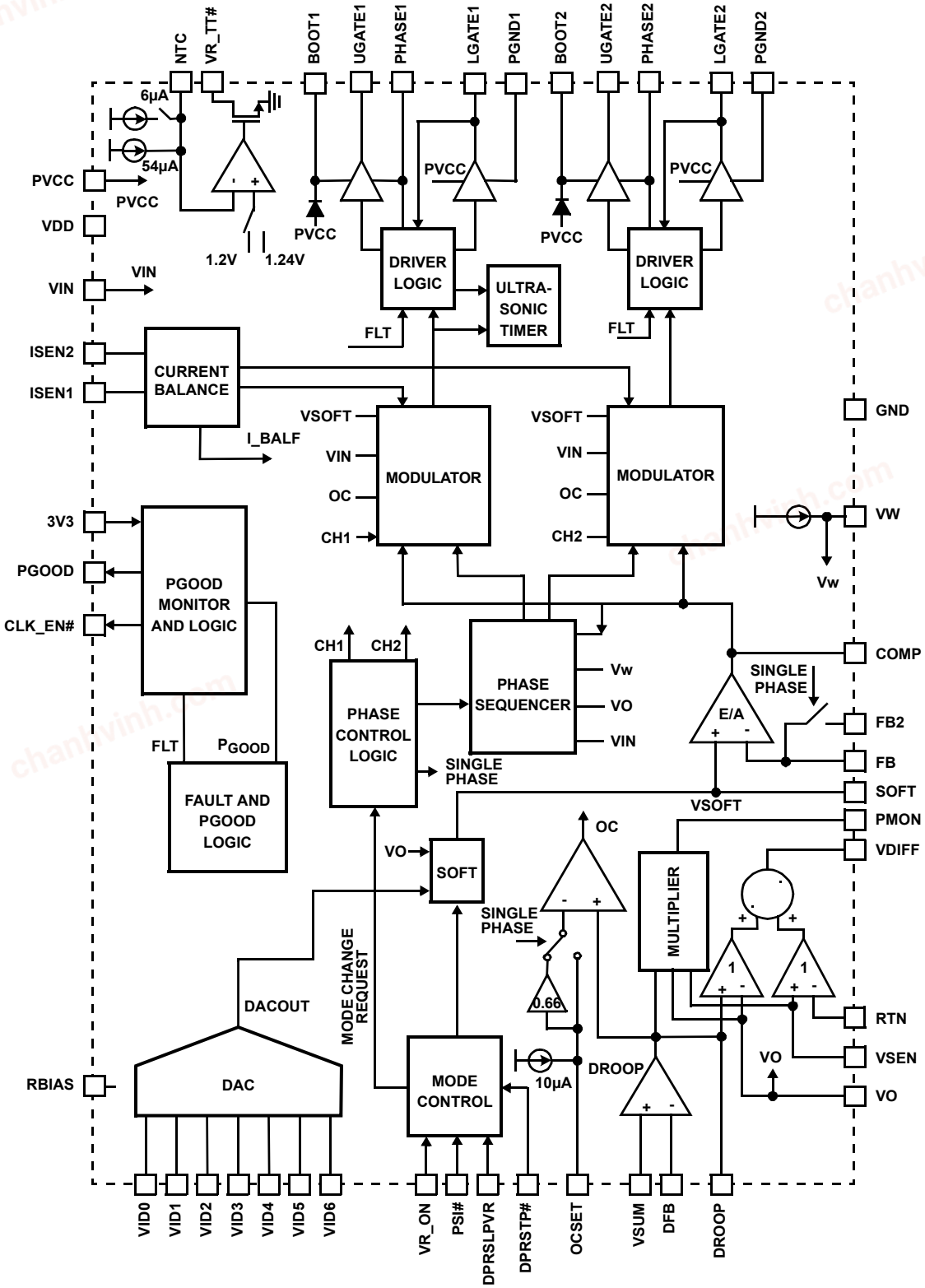


FIGURE 1. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF ISL6262A

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Typical Performance Curves 300kHz Operation, 2xIRF7821 as Upper Devices and 2xIRF7832 as Bottom Devices

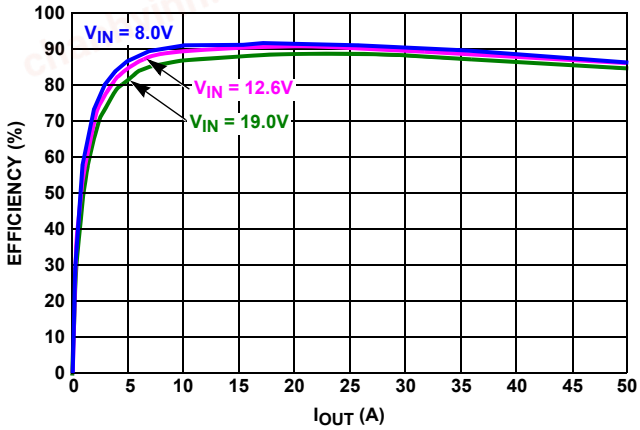


FIGURE 2. ACTIVE MODE EFFICIENCY, 2 PHASE, CCM, PSI# = HIGH, VID = 1.15V

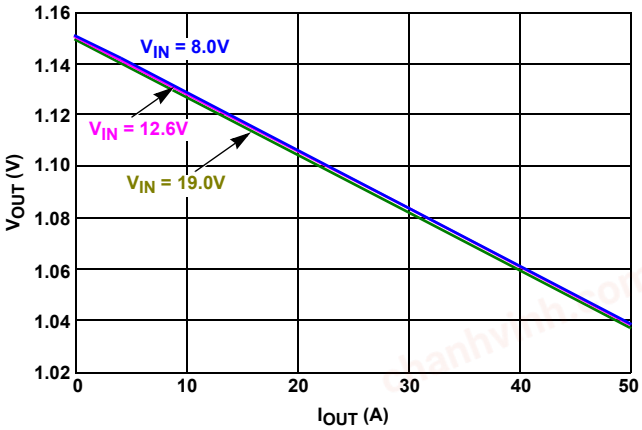


FIGURE 3. ACTIVE MODE LOAD LINE, 2 PHASE, CCM, PSI# = HIGH, VID = 1.15V

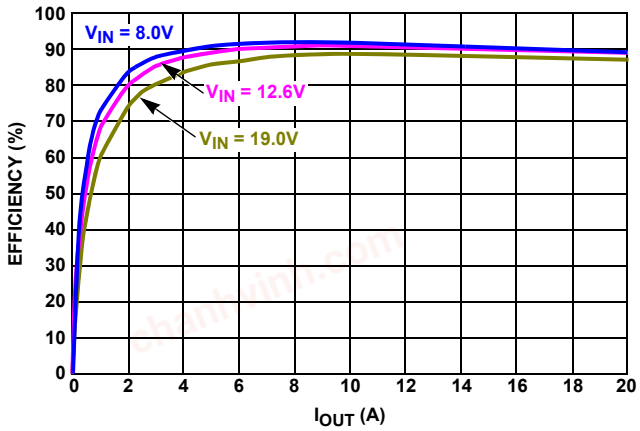


FIGURE 4. ACTIVE MODE EFFICIENCY, 1 PHASE, CCM, PSI# = LOW, VID = 1.15V

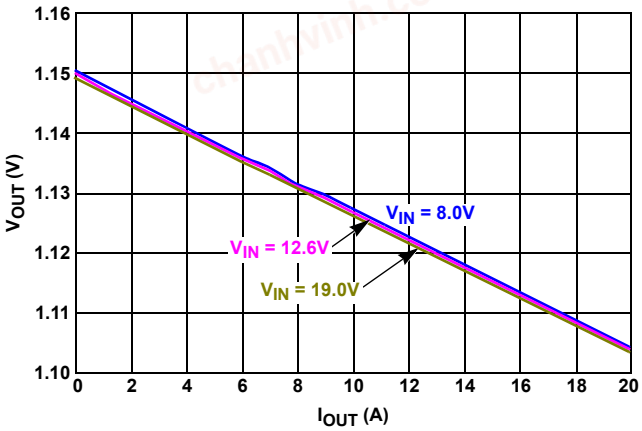


FIGURE 5. ACTIVE MODE LOAD LINE, 1 PHASE, CCM, PSI# = LOW, VID = 1.15V

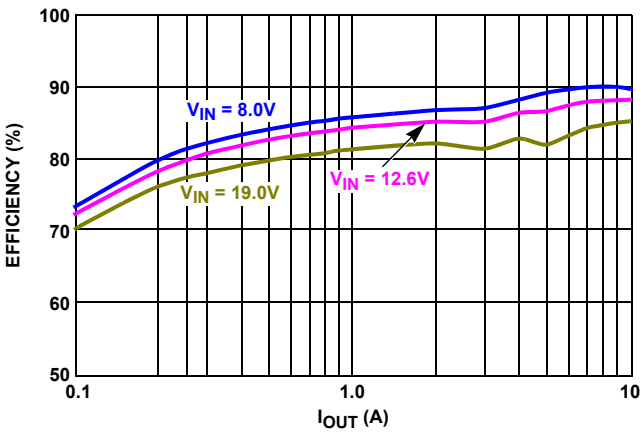


FIGURE 6. DEEPER SLEEP MODE EFFICIENCY

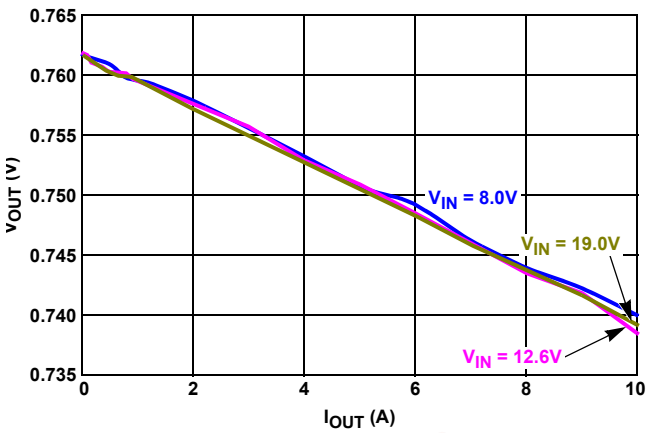


FIGURE 7. DEEPER SLEEP MODE LOAD LINE

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Typical Performance Curves 0.36µH Filter Inductor and 4 x 330µF Output SP Caps and 24 x 22µF Ceramic Caps

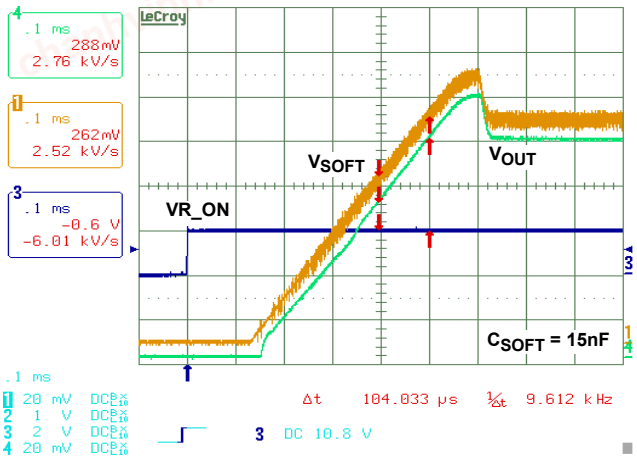


FIGURE 8. SOFT-START WAVEFORM SHOWING SLEW RATE OF 2.5mV/µs AT VID = 1V, I_{LOAD} = 10A

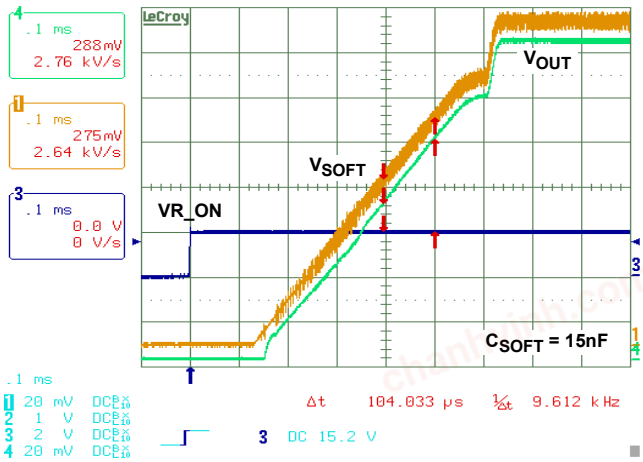


FIGURE 9. SOFT-START WAVEFORM SHOWING SLEW RATE OF 2.5mV/µs AT VID = 1.4375V, I_{LOAD} = 10A

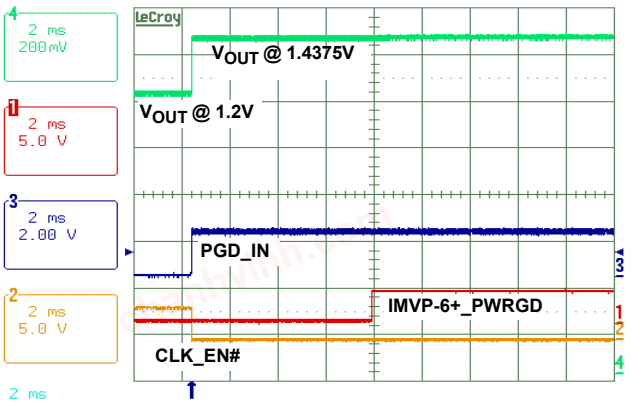


FIGURE 10. SOFT-START WAVEFORM SHOWING CLK_EN# AND IMVP-6+ PGOOD

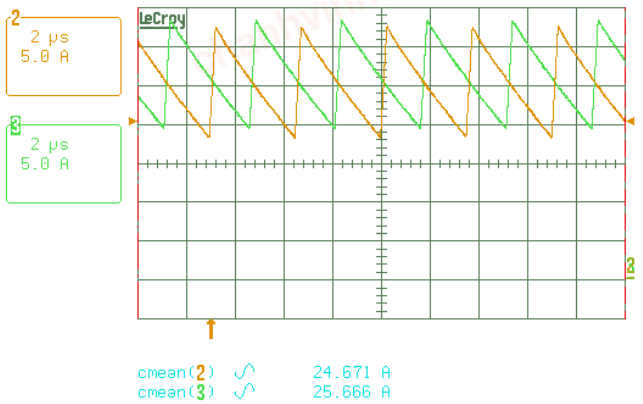


FIGURE 11. 2 PHASE CURRENT BALANCE, FULL LOAD (50A)

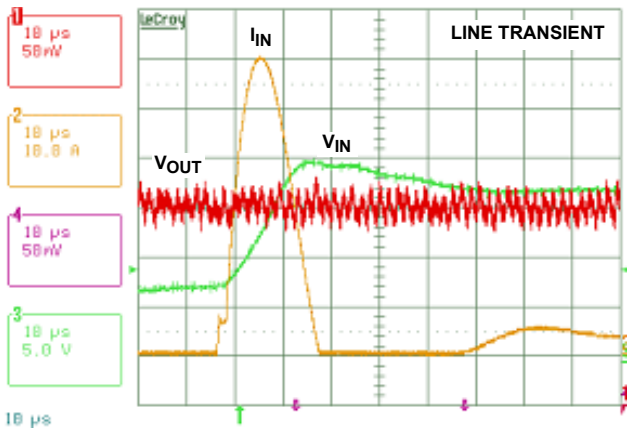


FIGURE 12. 8V-20V INPUT LINE TRANSIENT RESPONSE, C_{IN} = 240µF

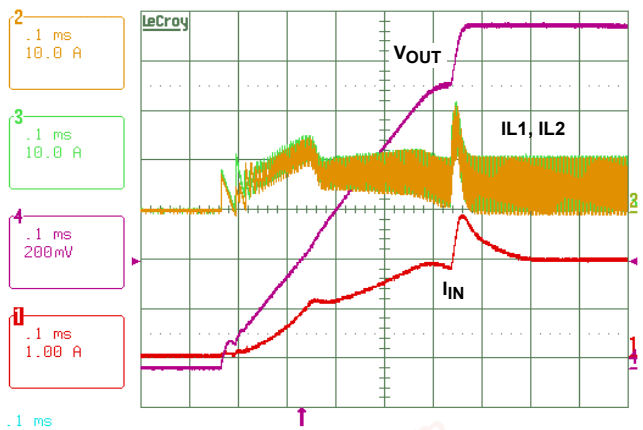


FIGURE 13. INRUSH CURRENT AT START-UP, V_{IN} = 8V, VID = 1.4375V, I_{LOAD} = 10A

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Typical Performance Curves 0.36µH Filter Inductor and 4 x 330µF Output SP Caps and 24 x 22µF Ceramic Caps **(Continued)**

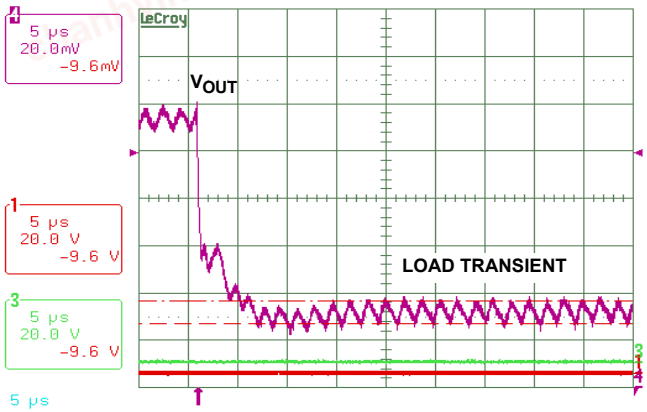


FIGURE 14. LOAD STEP-UP RESPONSE AT THE CPU SOCKET MPGA479, 35A LOAD STEP @ 200A/µs, 2 PHASE CCM

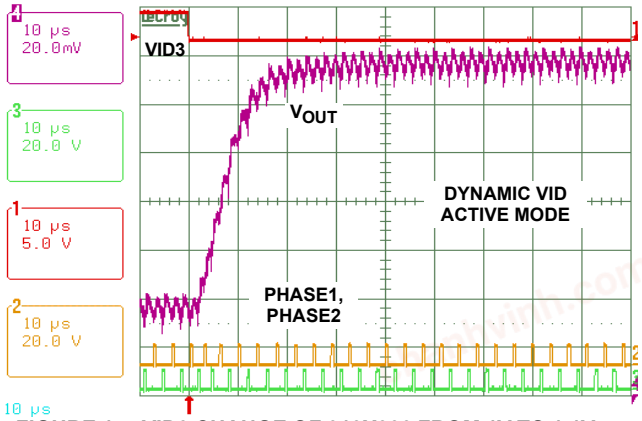


FIGURE 15. VID3 CHANGE OF 010X000 FROM 1V TO 1.1V WITH DPRSLPVR = 0, DPRSTP# = 1, PSI# = 1

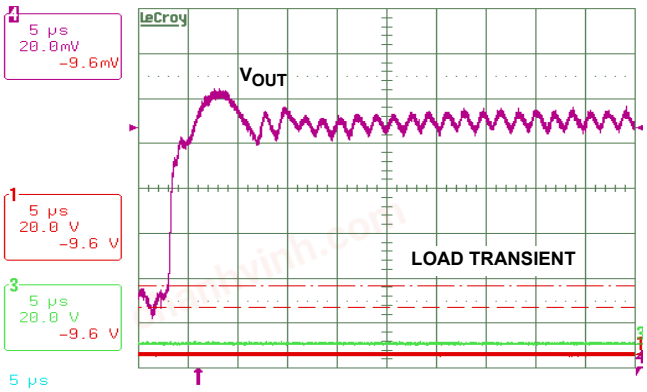


FIGURE 16. LOAD DUMP RESPONSE AT THE CPU SOCKET MPGA479, 35A LOAD STEP @ 200A/µs, 2 PHASE CCM

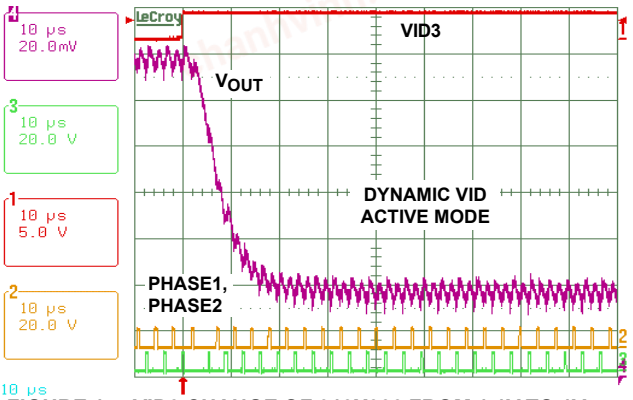


FIGURE 17. VID3 CHANGE OF 010X000 FROM 1.1V TO 1V WITH DPRSLPVR = 0, DPRSTP# = 1, PSI# = 1

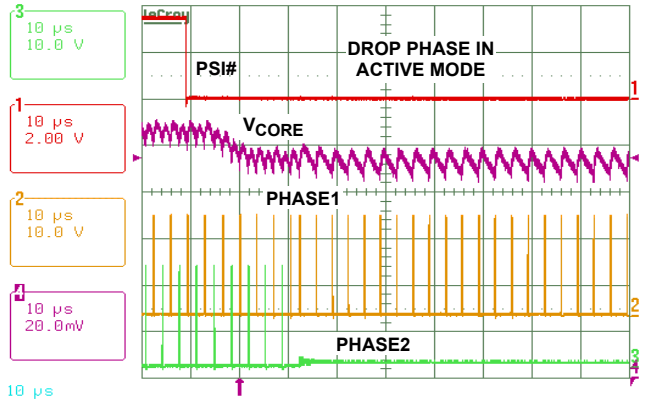


FIGURE 18. 2-CCM TO 1-CCM UPON PSI# ASSERTION WITH VID LSB CHANGE, AT DPRSLPVR = 0, DPRSTP# = 1, I_{LOAD} = 10A

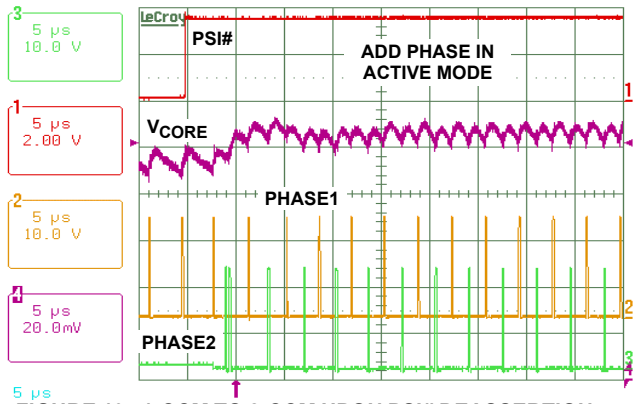


FIGURE 19. 1-CCM TO 2-CCM UPON PSI# DEASSERTION WITH VID LSB CHANGE AT DPRSLPVR = 0, DPRSTP# = 1

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Typical Performance Curves 0.36µH Filter Inductor and 4 x 330µF Output SP Caps and 24 x 22µF Ceramic Caps **(Continued)**

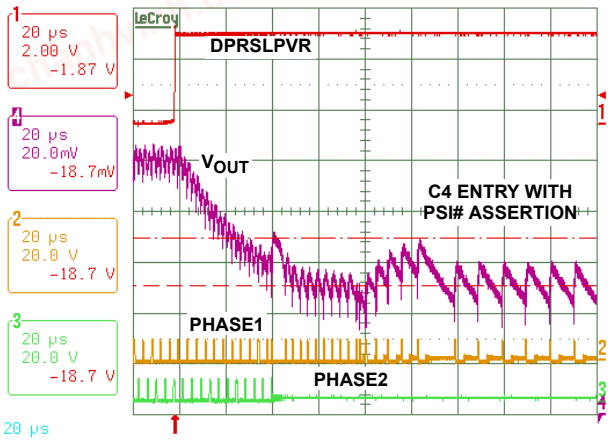


FIGURE 20. C4 ENTRY WITH VID CHANGE 0011X00 FROM 1.2V TO 1.15V, I_{LOAD} = 2A, TRANSITION OF 2-CCM TO 1-DCM, PSI# TOGGLE FROM 1 TO 0 WITH DPRSLPVR FROM 0 TO 1

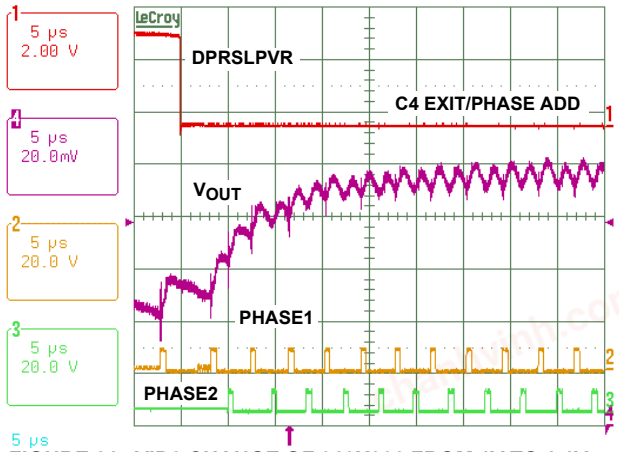


FIGURE 21. VID3 CHANGE OF 010X000 FROM 1V TO 1.1V WITH DPRSLPVR = 0, DPRSTP# = 1, PSI# = 1

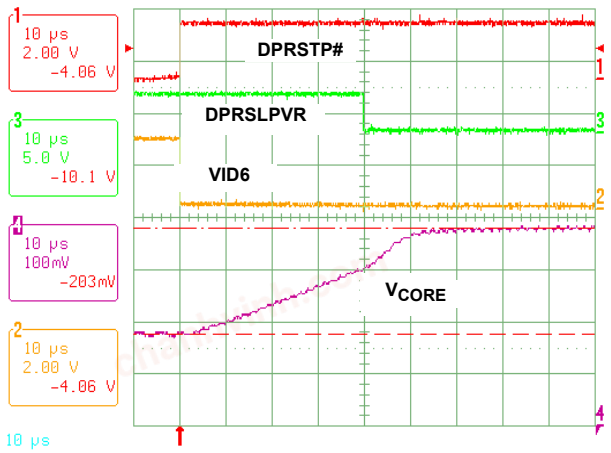


FIGURE 22. SLOW C4 EXIT WITH DELAY OF DPRSLPVR, FROM VID1000000 (0.7V) TO 0110000 (0.9V)

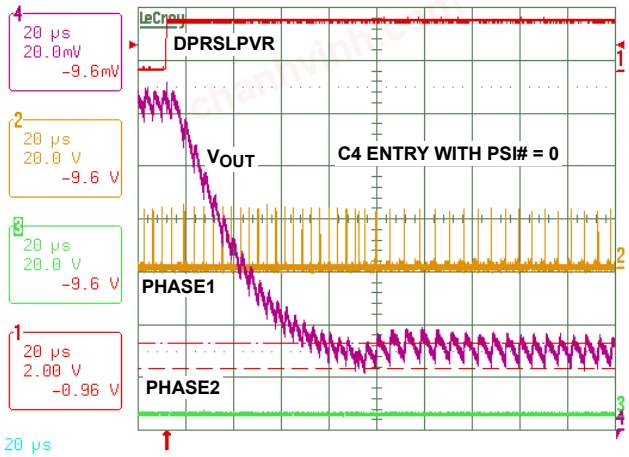


FIGURE 23. C4 ENTRY WITH VID CHANGE OF 011X011 FROM 0.8625V TO 0.7625V, I_{LOAD} = 3A, 1-CCM TO 1-DCM

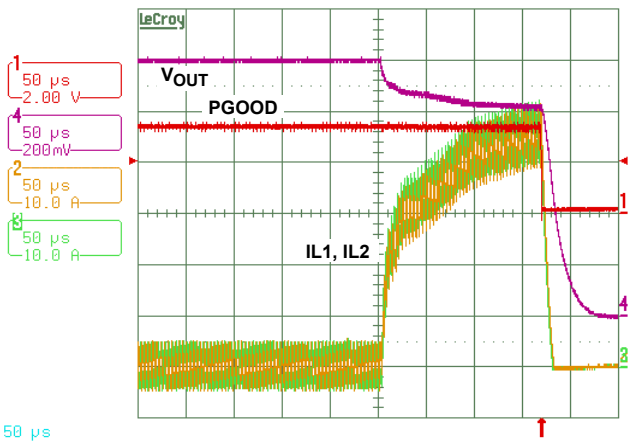


FIGURE 24. OVERCURRENT PROTECTION

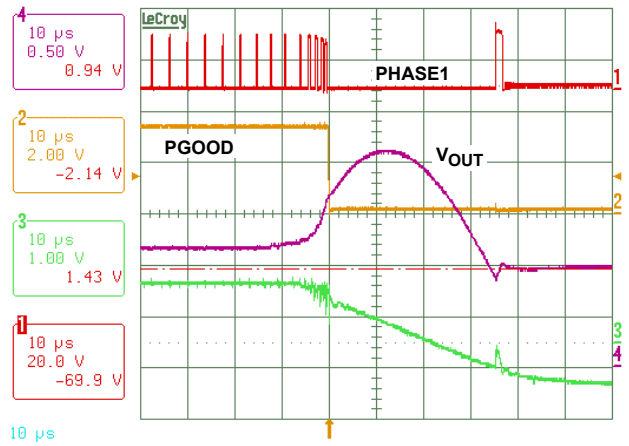


FIGURE 25. 1.7V OVERVOLTAGE PROTECTION SHOWS OUTPUT VOLTAGE PULLED LOW TO 0.9V AND PWM THREE-STATE

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Typical Performance Curves 0.36µH Filter Inductor and 4 x 330µF Output SP Caps and 24 x 22µF Ceramic Caps **(Continued)**

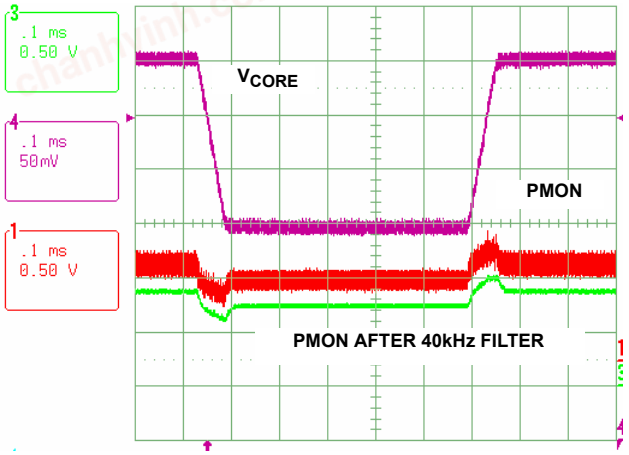


FIGURE 26. VID TRANSITION FROM 1V TO 1.15V I_{LOAD} = 21A, EXTERNAL FILTER 40kΩ AND 100pF AT PMON

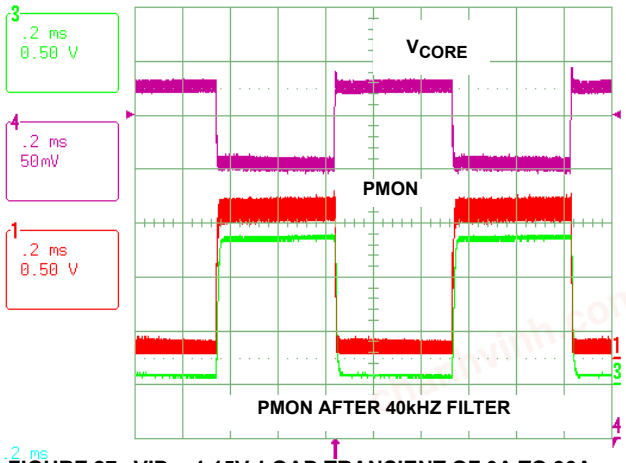


FIGURE 27. VID = 1.15V, LOAD TRANSIENT OF 0A TO 36A WITH INTEL® VTT TOOL, 1kHz REPETITION RATE, 50% DUTY CYCLE, TR = 56

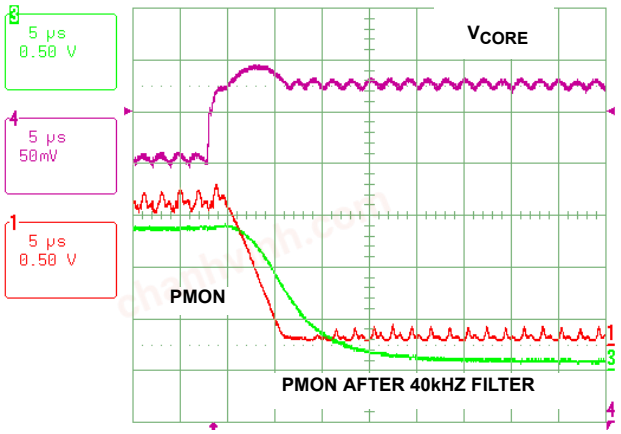


FIGURE 28. VID = 1.15V, LOAD RELEASE FROM 36A TO 0A WITH INTEL® VTT TOOL, 1kHz REPETITION RATE, 50% DUTY CYCLE, TR = 56

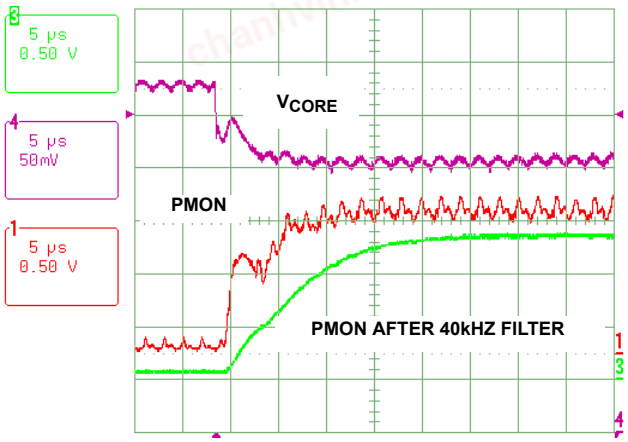


FIGURE 29. VID = 1.15V, LOAD APPLICATION FROM 0A TO 36A WITH INTEL® VTT TOOL, 1kHz REPETITION RATE, 50% DUTY CYCLE, TR = 56

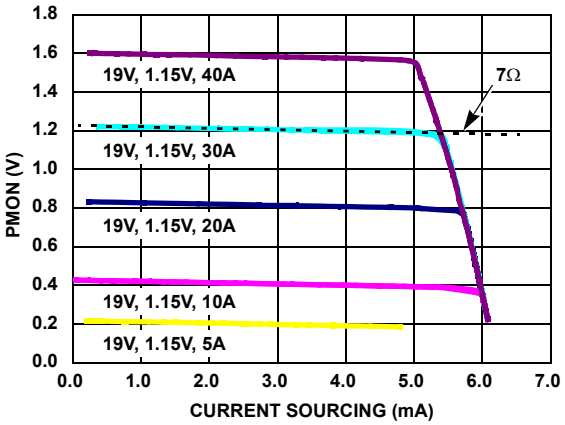


FIGURE 30. POWER MONITOR CURRENT SOURCING CAPABILITY

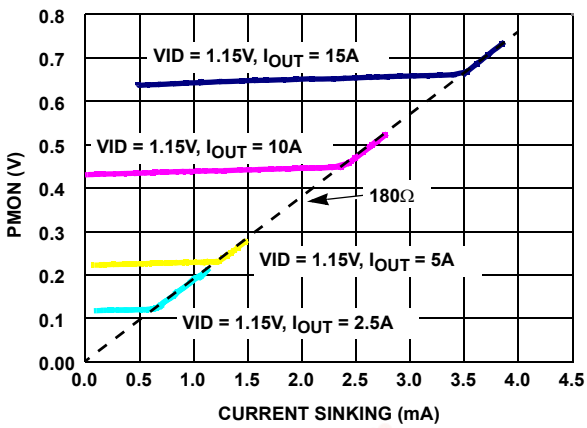


FIGURE 31. POWER MONITOR CURRENT SINKING CAPABILITY

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Simplified Application Circuit for DCR Current Sensing

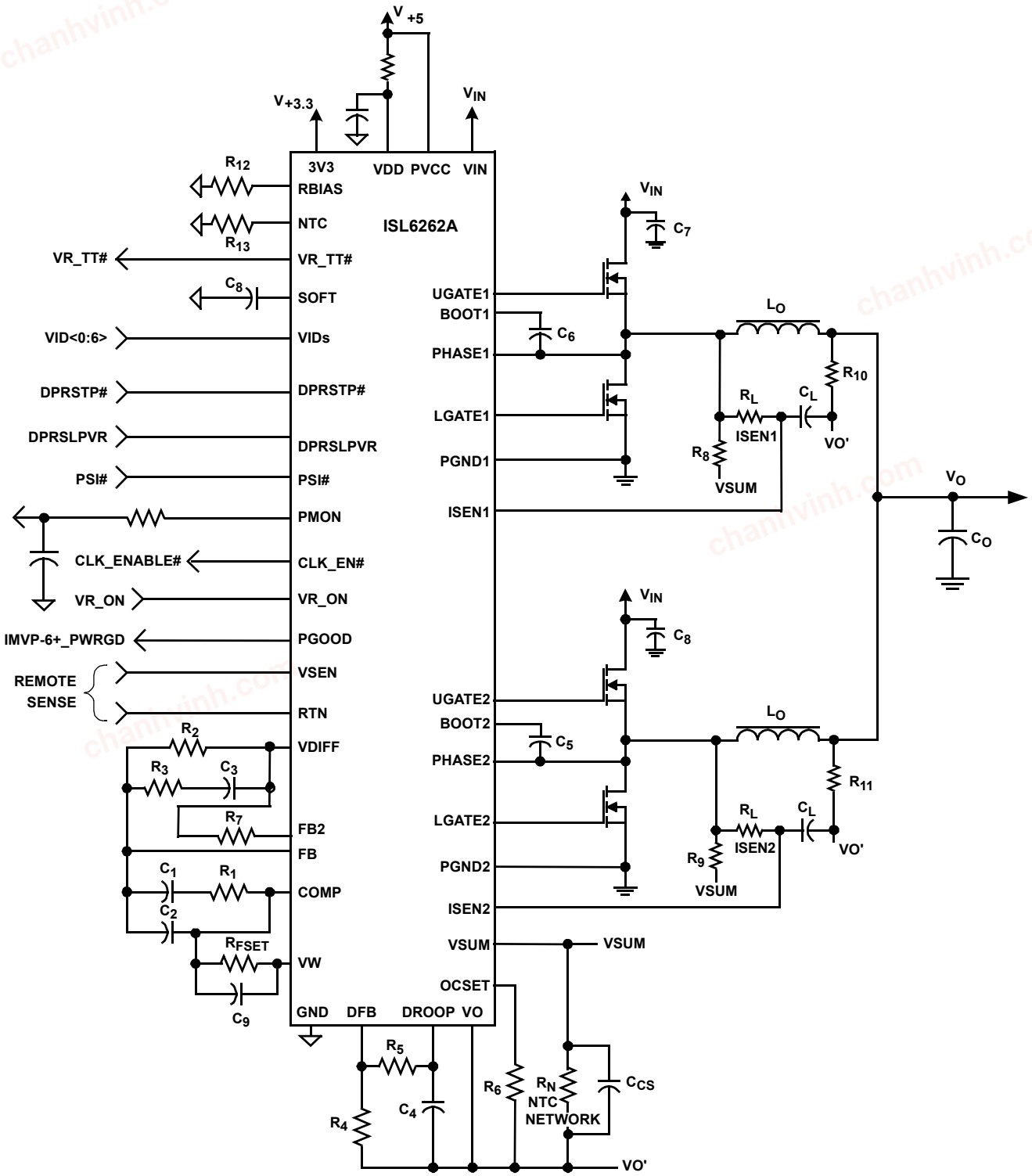


FIGURE 32. ISL6262A BASED TWO-PHASE BUCK CONVERTER WITH INDUCTOR DCR CURRENT SENSING

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Simplified Application Circuit for Resistive Current Sensing

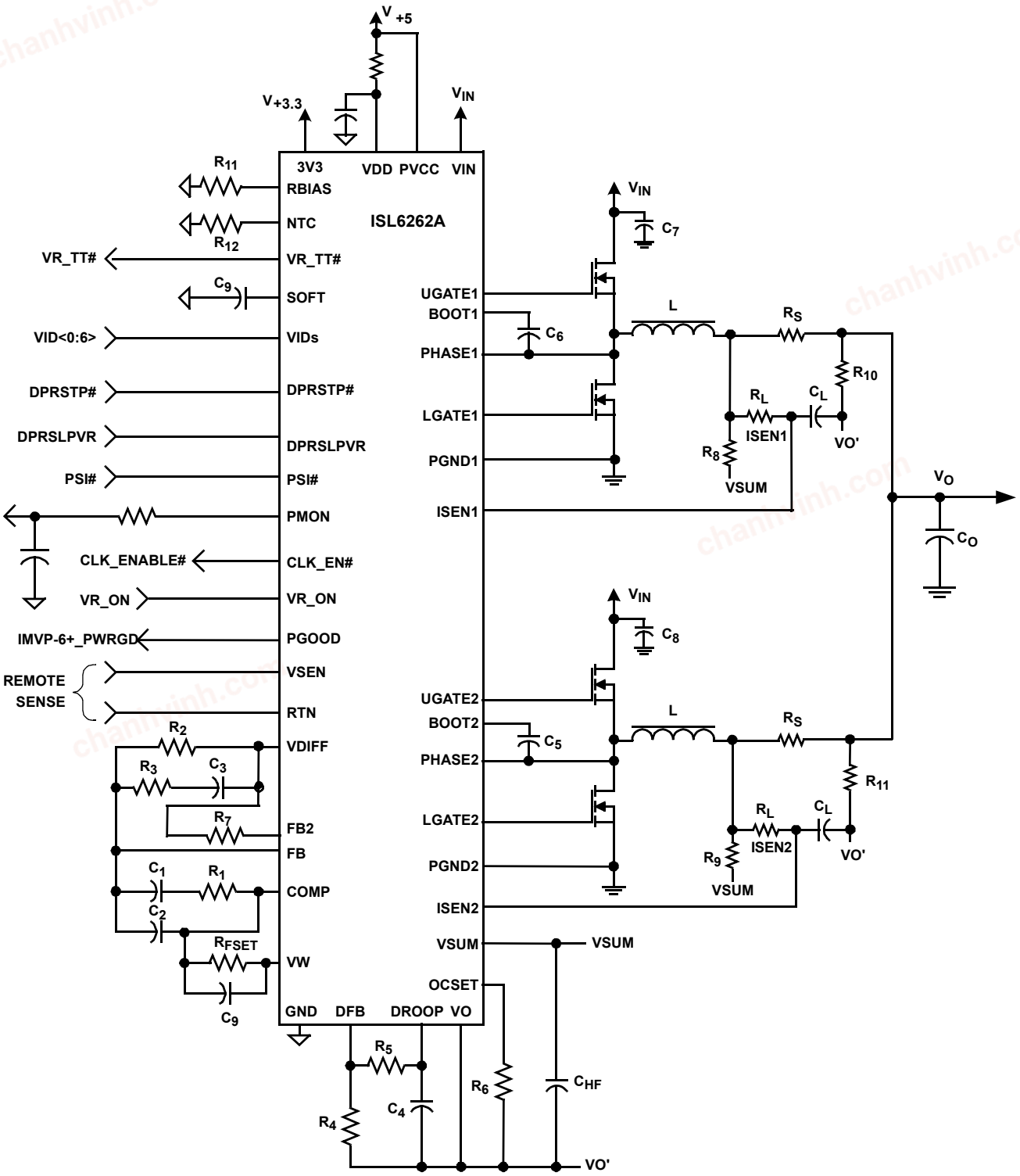


FIGURE 33. ISL6262A BASED TWO-PHASE BUCK CONVERTER WITH RESISTIVE CURRENT SENSING

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Theory of Operation

The ISL6262A is a two-phase regulator implementing Intel IMVP-6+ protocol and includes embedded gate drivers for reduced system cost and board area. The regulator provides optimum steady-state and transient performance for microprocessor core applications up to 50A. System efficiency is enhanced by idling one phase at low-current and implementing automatic DCM-mode operation.

The heart of the ISL6262A is R^3 Technology™, Intersil's Robust Ripple Regulator modulator. The R^3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. The ISL6262A modulator internally synthesizes an analog of the inductor ripple current and uses hysteretic comparators on those signals to establish PWM pulse widths. Operating on these large-amplitude, noise-free synthesized signals allows the ISL6262A to achieve lower output ripple and lower phase jitter than either conventional hysteretic or fixed frequency PWM controllers. Unlike conventional hysteretic converters, the ISL6262A has an error amplifier that allows the controller to maintain a 0.5% voltage regulation accuracy throughout the VID range from 0.75V to 1.5V.

The hysteresis window voltage is relative to the error amplifier output such that load current transients results in increased switching frequency, which gives the R^3 regulator a faster response than conventional fixed frequency PWM controllers. Transient load current is inherently shared between active phases due to the use of a common hysteretic window voltage. Individual average phase voltages are monitored and controlled to equally share the static current among the active phases.

Start-Up Timing

With the controller's +5V VDD voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the 3.3V logic HIGH threshold. Approximately 100µs later, SOFT and VOUT begin ramping to the boot voltage of 1.2V. At start-up, the regulator always operates in a 2-phase CCM mode, regardless of control signal assertion levels. During this internal, the SOFT cap is charged by 41µA current source. If the SOFT capacitor is selected to be 20nF, the SOFT ramp will be at 2mV/µs for a soft-start time of 600µs. Once VOUT is within 10% of the boot voltage for 13 PWM cycles (43µs for frequency = 300kHz), then CLK_EN# is pulled LOW and the SOFT cap is charged/discharged by approximately 200µA. Therefore, VOUT slews at +10mV/µs to the voltage set by the VID pins. Approximately 7ms later, PGOOD is asserted HIGH. Typical start-up timing is shown in Figure 34.

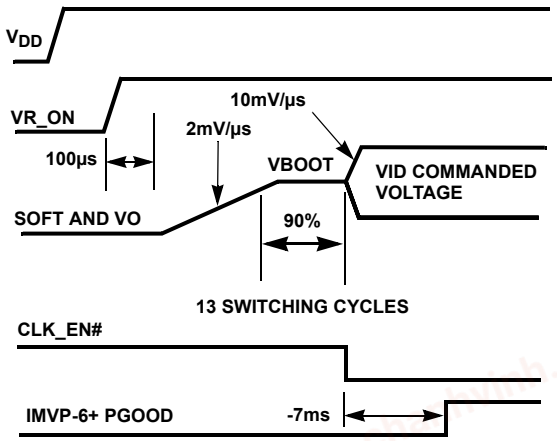


FIGURE 34. SOFT-START WAVEFORMS USING A 20nF SOFT CAPACITOR

Static Operation

After the start sequence, the output voltage will be regulated to the value set by the VID inputs shown in Table 1. The entire VID table is presented in the IntelIMVP-6+ specification. The ISL6262A will control the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.5V.

TABLE 1. TRUNCATED VID TABLE FOR INTEL® IMVP-6+ SPECIFICATION

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOUT (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	1	0	1	1.4375
0	0	1	0	0	0	1	1.2875
0	0	1	1	1	0	0	1.15
0	1	1	0	1	0	1	0.8375
0	1	1	1	0	1	1	0.7625
1	1	0	0	0	0	0	0.3000
1	1	1	1	1	1	1	0.0000

A fully-differential amplifier implements core voltage sensing for precise voltage control at the microprocessor die. The inputs to the amplifier are the VSEN and RTN pins.

As the load current increases from zero, the output voltage will droop from the VID table value by an amount proportional to current to achieve the IMVP-6+ load line. The ISL6262A provides for current to be measured using either resistors in series with the channel inductors as shown in the application circuit of Figure 33, or using the intrinsic series resistance of the inductors as shown in the application circuit of Figure 32. In both cases, signals representing the inductor currents are summed at VSUM, which is the non-inverting input to the DROOP amplifier shown in the "Functional Block Diagram" on page 8 of Figure 1. The voltage at the DROOP pin minus the output voltage, VO´, is a high-bandwidth analog of the total inductor current. This voltage is used as an input to a

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differential amplifier to achieve the IMVP-6+ load line, and also as the input to the overcurrent protection circuit.

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding thus maintaining the load-line accuracy.

In addition to monitoring the total current (used for DROOP and overcurrent protection), the individual channel average currents are also monitored and used for balancing the load between channels. The IBAL circuit will adjust the channel pulse-widths up or down relative to the other channel to cause the voltages presented at the ISEN pins to be equal.

The ISL6262A controller can be configured for two-channel operation, with the channels operating 180° apart. The channel PWM frequency is determined by the value of R_{FSET} connected to pin VW as shown in Figure 32 and Figure 33. Input and output ripple frequencies will be the channel PWM frequency multiplied by the number of active channels.

High Efficiency Operation Mode

The ISL6262A has several operating modes to optimize efficiency. The controller's operational modes are designed to work in conjunction with the Intel® IMVP-6+ control signals to maintain the optimal system configuration for all IMVP-6+ conditions. These operating modes are established by the IMVP-6+ control signal inputs such as PSI#, DPRSLPVR, and DPRSTP# as shown in Table 2. At high current levels, the system will operate with both phases fully active, responding rapidly to transients and deliver the maximum power to the load. At reduced load-current levels, one of the phases may be idled. This configuration will minimize switching losses, while still maintaining transient response capability. At the lowest current levels, the controller automatically configures the system to operate in single-phase automatic-DCM mode, thus achieving the highest possible efficiency. In this mode of operation, the lower MOSFET will be configured to automatically detect and prevent discharge current flowing from the output capacitor through the inductors, and the switching frequency will be proportionately reduced, thus greatly reducing both conduction and switching losses. If ISEN2 is pulled to 5V, the ISL6262A operates at 1-phase-only mode. The ISL6262A always enables the diode emulation mode of phase 1 in always-1-phase configuration.

Smooth mode transitions are facilitated by the R^3 Technology™, which correctly maintains the internally synthesized ripple currents throughout mode transitions. The controller is thus able to deliver the appropriate current to the load throughout mode transitions. The controller contains embedded mode-transition algorithms that maintain voltage-regulation for all control signal input sequences and durations.

Mode-transition sequences often occur in concert with VID changes; therefore the timing of the mode transitions of ISL6262A has been carefully designed to work in concert with VID changes. For example, transitions into single-phase will be delayed until the VID induced voltage ramp is complete. This allows the associated output capacitor charging current to be shared by both inductor paths. While in single-phase automatic-DCM mode, VID changes will initiate an immediate return to two-phase CCM mode. This ensures that both inductor paths share the output capacitor charging current and are fully active for the subsequent load current increases.

The controller contains internal counters that prevent spurious control signal glitches from resulting in unwanted mode transitions. Control signals of less than two switching periods do not result in phase-idling. Signals of less than seven switching periods do not result in implementation of automatic-DCM mode.

While transitioning to single-phase operation, the controller smoothly transitions current from the idling-phase to the active-phase, and detects the idling-phase zero-current condition. During transitions into automatic-DCM or forced-CCM mode, the timing is carefully adjusted to eliminate output voltage excursions. When a phase is added, the current balance between phases is quickly restored.

TABLE 2. CONTROL SIGNAL TRUTH TABLES FOR OPERATION MODES OF ISL6262A IN TWO-PHASE DESIGN

	DPRSLPVR	DPRSTP#	PSI#	PHASE OPERATION MODES	EXPECTED CPU MODE
Intel IMVP-6+ COMPLIANT LOGIC	0	1	1	2-phase CCM	Active mode
	0	1	0	1-phase CCM	Active mode
	1	0	1	1-phase diode emulation	Deeper sleep mode
	1	0	0	1-phase diode emulation	Deeper sleep mode
OTHER LOGIC COMMANDS	0	0	1	2-phase CCM	
	0	0	0	1-phase CCM	
	1	1	1	2-phase CCM	
	1	1	0	1-phase CCM	

While PSI# is high, both phases are switching. If PSI# is asserted low and either DPRSTP# or DPRSLPVR are not asserted, the controller will transition to CCM operation with only phase 1 switching, and both MOSFETs of phase 2 will be

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off. The controller will thus eliminate switching losses associated with the unneeded channel.

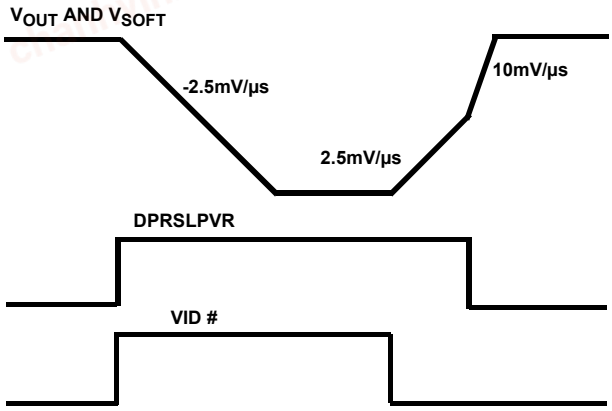


FIGURE 35. DEEPER SLEEP TRANSITION SHOWING DPRSLPVR'S EFFECT ON EXIT SLEW RATE

When PSI#, DPRSTP#, and DPRSLPVR are all asserted, the controller will transition to single-phase DCM mode. In this mode, both MOSFETs associated with phase 2 are off, and the ISL6262A turns off the lower MOSFET of Channel 1 whenever the Channel 1 current decays to zero. As load is further reduced, the phase 1 channel switching frequency decreases to maintain high efficiency.

Dynamic Operation

See Figure 35. The ISL6262A responds to changes in VID command voltage by slewing to new voltages with a dV/dt set by the SOFT capacitor and by the state of DPRSLPVR. With C_{SOFT} = 15nF and DPRSLPVR HIGH, the output voltage will move at ±2.8mV/s for large changes in voltage. For DPRSLPVR LOW, the large signal dV/dt will be ±10mV/s. As the output voltage approaches the VID command value, the dV/dt moderates to prevent overshoot.

Keeping DPRSLPVR HIGH for voltage transitions into and out of Deeper Sleep will result in low dV/dt output voltage changes with resulting minimized audio noise. For fastest recovery from Deeper Sleep to Active mode, holding DPRSLPVR LOW results in maximum dV/dt. Therefore, the ISL6262A is IMVP-6+ compliant for DPRSTP# and DPRSLPVR logic.

Intersil's R^3 Technology™ has intrinsic voltage feedforward. As a result, high-speed input voltage steps do not result in significant output voltage perturbations. In response to load current step increases, the ISL6262A will transiently raise the switching frequency so that response time is decreased and current is shared by two channels.

Protection

The ISL6262A provides overcurrent, overvoltage, under-voltage protection and over-temperature protection as shown in Table 3.

Overcurrent protection is tied to the voltage droop which is determined by the resistors selected as described in “Component Selection and Application” on page 19“. After the load-line is set, the OCSET resistor can be selected to detect overcurrent at any level of droop voltage. An overcurrent fault will occur when the load current exceeds the overcurrent setpoint voltage while the regulator is in a 2-phase mode. While the regulator is in a 1-phase mode of operation, the overcurrent setpoint is automatically reduced to 66% of two-phase overcurrent level. For overcurrents less than 2.5 times the OCSET level, the over-load condition must exist for 120µs in order to trip the OC fault latch. This is shown in Figure 24.

TABLE 3. FAULT-PROTECTION SUMMARY OF ISL6262A

	FAULT DURATION PRIOR TO PROTECTION	PROTECTION ACTIONS	FAULT RESET
Overcurrent fault	120µs	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Way-Overcurrent fault	<2µs	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Overvoltage fault (1.7V)	Immediately	Low-side MOSFET on until Vcore <0.85V, then PWM three-state, PGOOD latched low (OV to 1.7V always)	VDD toggle
Overvoltage fault (+200mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Undervoltage fault (-300mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Unbalance fault (7.5mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Over-temperature fault (NTC <1.18V)	Immediately	VR_TT# goes low	N/A

For overloads exceeding 2.5xthe set level, the PWM outputs will immediately shut off and PGOOD goes low to maximize protection due to hard shorts.

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In addition, excessive phase unbalance (for example, due to gate driver failure) will be detected in two-phase operation and the controller will be shutdown after one millisecond's detection of the excessive phase current unbalance. The phase unbalance is detected by the voltage on the ISEN pins if the difference is greater than 9mV.

Undervoltage protection is independent of the overcurrent limit. If the output voltage is less than the VID set value by 300mV or more, a fault will latch after one millisecond in that condition. The PWM outputs will turn off and PGOOD will go low. Note that most practical core regulators will have the overcurrent set to trip before the -300mV undervoltage limit.

There are two levels of overvoltage protection and response.

1. For output voltage exceeding the set value by +200mV for one millisecond, a fault is declared. All of the above faults have the same action taken: PGOOD is latched low and the upper and lower power MOSFETs are turned off so that inductor current will decay through the MOSFET body diodes. This condition can be reset by bringing VR_ON low or by bringing VDD below 4V. When these inputs are returned to their high operating levels, a soft-start will occur.
2. The second level of overvoltage protection behaves differently (see Figure 25). If the output exceeds 1.7V, an OV fault is immediately declared, PGOOD is latched low and the low-side MOSFETs are turned on. The low-side MOSFETs will remain on until the output voltage is pulled down below about 0.85V, at which time all MOSFETs are turned off. If the output again rises above 1.7V, the protection process is repeated. This offers the maximum amount of protection against a shorted high-side MOSFET while preventing output ringing below ground. The 1.7V OV is not reset with VR_ON, but requires that VDD be lowered to reset. The 1.7V OV detector is active at all times that the controller is enabled including after one of the other faults occurs so that the processor is protected against high-side MOSFET leakage while the MOSFETs are commanded off.

The ISL6262A has a thermal throttling feature. If the voltage on the NTC pin goes below the 1.2V over-temperature threshold, the VR_TT# pin is pulled low indicating the need for thermal throttling to the system oversight processor. No other action is taken within the ISL6262A in response to NTC pin voltage.

Power Monitor

The power monitor signal is an analog output. Its magnitude is proportional to the product of $V_{CCSENSE}$ and the voltage difference between V_{droop} and V_O, which is the programmed voltage droop value, equal to load current multiplied by the load line impedance (for example 2.1mΩ). The output voltage of the PMON pin in two-phase design is given by: $V_{pmon} = V_{CCSENSE} * (V_{droop} - V_O) * 17.5$. In always-single-phase design, the output voltage PMON pin is given by: $V_{pmon} = V_{CCSENSE} * (V_{droop}-V_O) * 35$.

The power consumed by the CPU can be calculated by: $P_{cpu} = V_{pmon} / (17.5 * 0.0021)$ (Watt), where 0.0021 is the typical load line slope. The power monitor load regulation is approximately 7Ω. Within its sourcing/sinking current capability range, when the power monitor loading changes to 1mA, the output of the power monitor will change to 7mV. The 7Ω impedance is associated with the layout and package resistance of PMON inside the IC. In practical applications, compared to the load resistance on the PMON pin, 7Ω output impedance contributes no significant error.

Component Selection and Application

Soft-Start and Mode Change Slew Rates

The ISL6262A uses two slew rates for various modes of operation. The first is a slow slew rate used to reduce in-rush current during start-up. It is also used to reduce audible noise when entering or exiting Deeper Sleep Mode. A faster slew rate is used to exit out of Deeper Sleep and to enhance system performance by achieving active mode regulation more quickly. Note that the SOFT cap current is bidirectional. The current is flowing into the SOFT capacitor when the output voltage is commanded to rise and out of the SOFT capacitor when the output voltage is commanded to fall.

The two slew rates are determined by commanding one of two current sources onto the SOFT pin. As can be seen in Figure 36, the SOFT pin has a capacitance to ground. Also, the SOFT pin is the input to the error amplifier and is, therefore, the commanded system voltage. Depending on the state of the system (that is, Start-Up or Active mode) and the state of the DPRSLPVR pin, one of the two currents shown in Figure 36 will be used to charge or discharge this capacitor, thereby controlling the slew rate of the commanded voltage. These currents can be found under “SOFT-START CURRENT” on page 4 of the Electrical Specifications table.

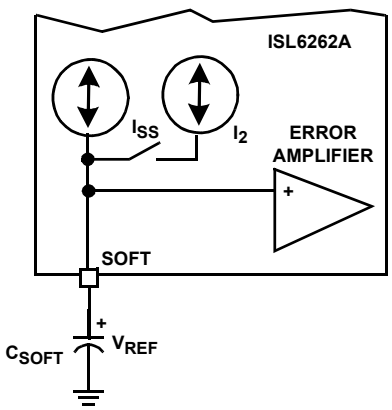


FIGURE 36. SOFT PIN CURRENT SOURCES FOR FAST AND SLOW SLEW RATES

The first current, labeled I_{SS}, is given in the Table Electrical Specifications on page 3 as 42µA. This current is used during soft-start. The second current, I_2 sums with I_{SS} to get the larger of the two currents, labeled I_{GV} in the Table Electrical Specifications on page 3 . This total current is typically 205µA with a minimum of 180µA.

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The IMVP-6+ specification reveals the critical timing associated with regulating the output voltage. The symbol, SLEWRATE, as given in the IMVP-6+ specification will determine the choice of the SOFT capacitor, C_{SOFT}, by Equation 1.

$$C_{SOFT} = \frac{I_{GV}}{SLEWRATE} \quad \text{(EQ. 1)}$$

Using a SLEWRATE of 10mV/µs and the typical I_{GV} value given in the Electrical Specification table of 205µA, C_{SOFT} is as shown in Equation 2.

$$C_{SOFT} = 205\mu A/(10mV/1\mu s) \quad \text{(EQ. 2)}$$

A choice of 0.015µF would guarantee a SLEWRATE of 10mV/µs is met for the minimum I_{GV} value given in the Electrical Specification table. This choice of C_{SOFT} will then control the Start-Up slewrate as well. One should expect the output voltage to slew to the Boot value of 1.2V at a rate given by Equation 3.

$$\frac{dV}{dt} = \frac{I_{SS}}{C_{SOFT}} = \frac{41\mu A}{0.015\mu F} = 2.8mV/\mu s \quad \text{(EQ. 3)}$$

Selecting RBIAS

To properly bias the ISL6262A, a reference current is established by placing a 147kΩ, 1% tolerance resistor from the RBIAS pin to ground. This will provide a highly accurate 10µA current source from which the OCSET reference current can be derived.

Care should be taken in layout that the resistor is placed very close to the RBIAS pin and that a good quality signal ground is connected to the opposite side of the RBIAS resistor. Do not connect any other components to this pin as this would negatively impact performance. Capacitance on this pin would create instabilities and should be avoided.

Start-Up Operation - CLK_EN# and PGOOD

The ISL6262A provides a 3.3V logic output pin for CLK_EN#. The 3V3 pin allows for a system 3.3V source to be connected to separated circuitry inside the ISL6262A, solely devoted to the CLK_EN# function. The output is a 3.3V CMOS signal with 4mA sourcing and sinking capability. This implementation removes the need for an external pull-up resistor on this pin, and due to the normal level of this signal being a low, removes the leakage path from the 3.3V supply to ground through the pull-up resistor. This reduces the 3.3V supply current that would occur under normal operation with a pull-up resistor and prolongs battery life. For noise immunity, the 3.3V supply should be decoupled to digital ground rather than to analog ground.

As mentioned in “Theory of Operation” on page 16, CLK_EN# is logic level high at start-up until approximately 43µs after the V_{CC}-core is in regulation at the Boot level. Approximately 43µs after V_{CC}-core are within regulation, CLK_EN# goes low, triggering an internal timer for the IMVP6_PWRGD signal. This timer allows IMVP-6_PWRGD to go high approximately 6.8ms after CLK_EN# goes low.

Static Mode of Operation - Processor Die Sensing

Die sensing is the ability of the controller to regulate the core output voltage at a remotely sensed point. This allows the voltage regulator to compensate for various resistive drops in the power path and ensure that the voltage seen at the CPU die is the correct level independent of load current.

The VSEN and RTN pins of the ISL6262A are connected to Kelvin sense leads at the die of the processor through the processor socket. These signal names are Vcc_sense and Vss_sense respectively. This allows the voltage regulator to tightly control the processor voltage at the die, independent of layout inconsistencies and voltage drops. This Kelvin sense technique provides for extremely tight load line regulation.

These traces should be laid out as noise sensitive traces. For optimum load line regulation performance, the traces connecting these two pins to the Kelvin sense leads of the processor must be laid out away from rapidly rising voltage nodes, (switching nodes) and other noisy traces. To achieve optimum performance, place common mode and differential mode filters to analog ground on VSEN and RTN as shown in Figure 37.

Intersil recommends the use of the R_{opn1} and R_{opn2} connected to V_{OUT} and ground as shown in Figure 37. These resistors provide voltage feedback in the event that the system is powered up without a processor installed. These resistors typically range from 20 to 100Ω.

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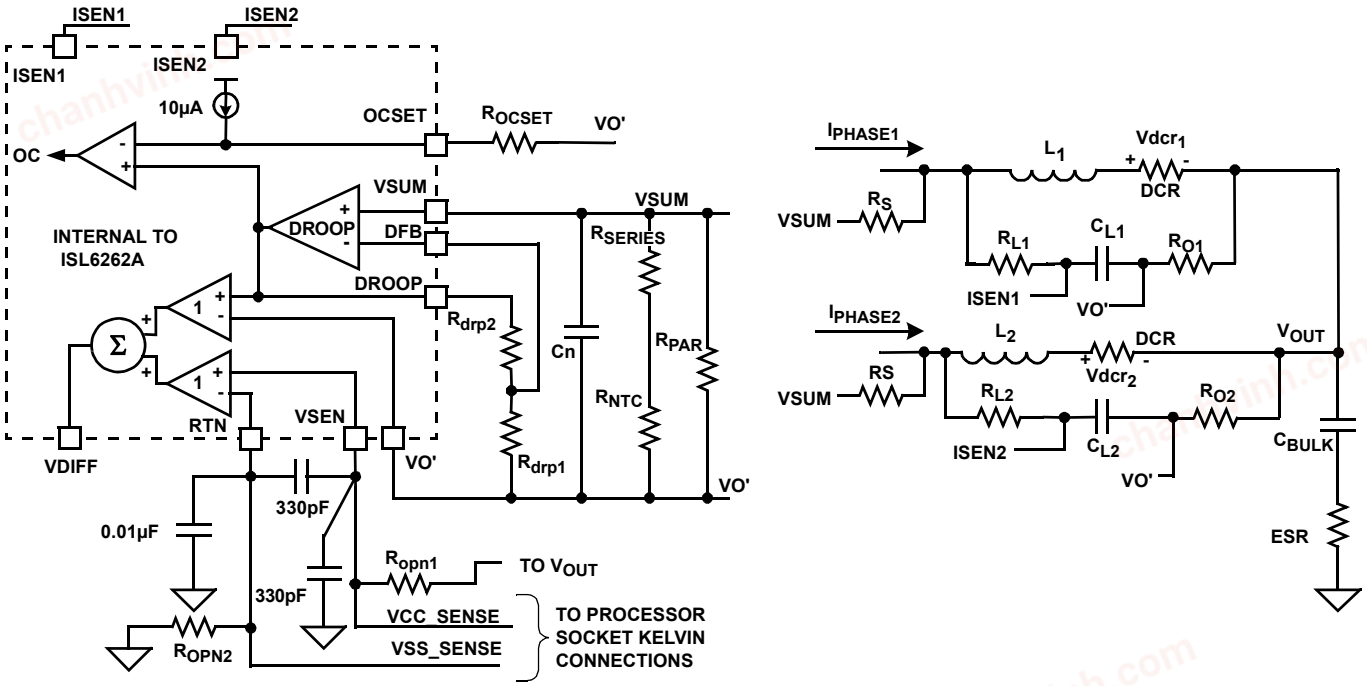


FIGURE 37. SIMPLIFIED SCHEMATIC FOR DROOP AND DIE SENSING WITH INDUCTOR DCR CURRENT SENSING

Setting the Switching Frequency - FSET

The R^3 modulator scheme is not a fixed frequency PWM architecture. The switching frequency can increase during the application of a load to improve transient performance.

It also varies slightly due to changes in input and output voltage and output current, but this variation is normally less than 10% in continuous conduction mode.

The resistor connected between the VW and COMP pins of the ISL6262A adjusts the switching window, and therefore adjusts the switching frequency (Figure 32). The R_{FSET} resistor that sets up the switching frequency of the converter operating in CCM can be determined using Equation 4, where R_{FSET} is in kΩ and the switching period is in µs.

$$R_{FSET}(k\Omega) = (period(\mu s) - 0.29) \bullet 2.33 \quad \text{(EQ. 4)}$$

For 300kHz operation, R_{fset} is suggested to be 6.81kΩ. In discontinuous conduction mode (DCM), the ISL6262A runs in period stretching mode. The switching frequency is dependent on the load current level. In general, the lighter load, the slower switching frequency. Therefore, the switching loss is much reduced for the light load operation, which is important for conserving the battery power in the portable application.

Voltage Regulator Thermal Throttling

Intel® IMVP-6+ technology supports thermal throttling of the processor to prevent catastrophic thermal damage to the voltage regulator. The ISL6262A features a thermal monitor that senses the voltage change across an externally placed negative temperature coefficient (NTC) thermistor.

Proper selection and placement of the NTC thermistor allows for detection of a designated temperature rise by the system.

Figure 38 shows the thermal throttling feature with hysteresis. At low temperature, SW1 is on and SW2 connects to the 1.2V side. The total current going into NTC pin is 60µA. The voltage on the NTC pin is higher than the threshold voltage of 1.2V and the comparator output is low. VR_TT# is pulling up high by the external resistor.

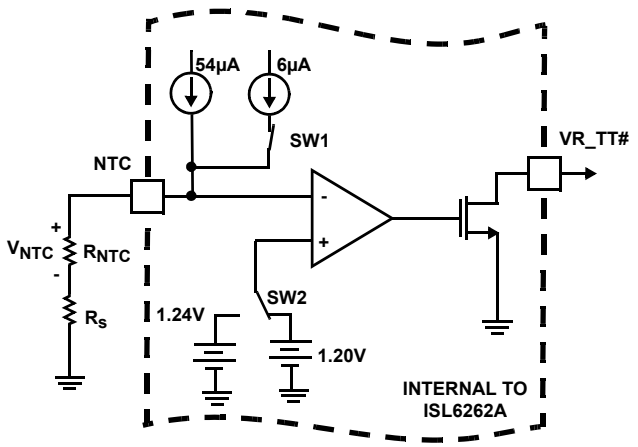


FIGURE 38. CIRCUITRY ASSOCIATED WITH THE THERMAL THROTTLING FEATURE IN ISL6262A

When the temperature increases, the NTC resistor value on the NTC pin decreases. Thus, the voltage on the NTC pin decreases to a level lower than 1.2V. The comparator output changes polarity and turns SW1 off and connects SW2 to 1.24V. This pulls VR_TT# low and sends the signal to start thermal throttle. There is a 6µA current reduction on the NTC pin and 20mV voltage increase on the threshold voltage of the

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comparator in this state. The VR_TT# signal will be used to change the CPU operation and decrease the power consumption. When the temperature goes down, the NTC thermistor voltage will eventually go up. When the NTC pin voltage increases to 1.24V, the comparator output will then be able to flip back. Such a temperature hysteresis feature of VR_TT# is illustrated in Figure 39. T_1 represents the higher temperature point at which the VR_TT# goes from low to high due to the system temperature rise. T_2 represents the lower temperature point at which the VR_TT# goes high from low because the system temperature decreases to the normal level.

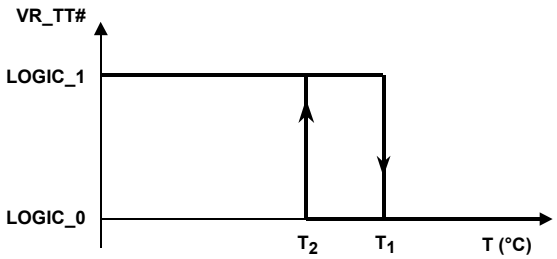


FIGURE 39. TEMPERATURE HYSTERESIS OF VR_TT#

Usually, the NTC thermistor's resistance can be approximated by Equation 5.

$$R_{NTC}(T) = R_{NTCTo} \bullet e^{b \bullet \left(\frac{1}{T+273} - \frac{1}{To+273}\right)} \quad \text{(EQ. 5)}$$

T is the temperature of the NTC thermistor and b is a parameter constant depending on the thermistor material. T_o is the reference temperature in which the approximation is derived. The most common temperature for T_o is +25°C. For example, there are commercial NTC thermistor products with b = 2750k, b = 2600k, b = 4500k or b = 4250k.

From the operation principle of the VR_TT# circuit explained, the NTC resistor satisfies Equation 6 and 8.

$$R_{NTC}(T_1) + R_S = \frac{1.2V}{60\mu A} = 20k\Omega \quad \text{(EQ. 6)}$$

$$R_{NTC}(T_2) + R_S = \frac{1.24V}{54\mu A} = 22.96k\Omega \quad \text{(EQ. 7)}$$

From Equation 6 and Equation 7, Equation 8 can be derived,

$$R_{NTC}(T_2) - R_{NTC}(T_1) = 2.96k\Omega \quad \text{(EQ. 8)}$$

Using Equation 5 into Equation 8, the required nominal NTC resistor value can be obtained by: Equation 9.

$$R_{NTCTo} = \frac{2.96k\Omega \bullet e^{b \bullet \left(\frac{1}{T_o+273}\right)}}{e^{b \bullet \left(\frac{1}{T_2+273}\right)} - e^{b \bullet \left(\frac{1}{T_1+273}\right)}} \quad \text{(EQ. 9)}$$

For those cases where the constant b is not accurate enough to approximate the resistor value, the manufacturer provides the resistor ratio information at different temperatures. The nominal NTC resistor value may be expressed in another way shown in Equation 10.

$$R_{NTCTo} = \frac{2.96k\Omega}{\overset{\Lambda}{R}_{NTC(T_2)} - \overset{\Lambda}{R}_{NTC(T_1)}} \quad \text{(EQ. 10)}$$

where $\overset{\Lambda}{R}_{NTC(T)}$ is the normalized NTC resistance to its nominal value. Most data sheets of the NTC thermistor give the normalized resistor value based on its value at +25°C.

Once the NTC thermistor resistor is determined, the series resistor can be derived by: Equation 11.

$$R_S = \frac{1.2V}{60\mu A} - R_{NTC}(T1) = 20k\Omega - R_{NTC_T_1} \quad \text{(EQ. 11)}$$

Once R_{NTCTo} and R_S is designed, the actual NTC resistance at T_2 and the actual T_2 temperature can be found in: Equations 12, and 13.

$$R_{NTC_T_2} = 2.96k\Omega + R_{NTC_T_1} \quad \text{(EQ. 12)}$$

$$T_{2_actual} = \frac{1}{\frac{1}{b}\ln\left(\frac{R_{NTC_T_2}}{R_{NTCTo}}\right) + 1/(273+To)} - 273 \quad \text{(EQ. 13)}$$

For example, if using Equations 9, 10 and 11 to design a thermal throttling circuit with the temperature hysteresis +100°C to +105°C, since T_1 = +105°C and T_2 = +100°C, and if we use a Panasonic NTC with b = 4700, Equation 9 gives the required NTC nominal resistance as R_{NTC_To} = 459kΩ.

In fact, the data sheet gives the resistor ratio value at +100°C to +105°C, which is 0.03956 and 0.03322 respectively. The b value 4700k in the Panasonic data sheet only covers to +85°C. Therefore, using Equation 10 is more accurate for +100°C design, the required NTC nominal resistance at +25°C is 467kΩ. The closest NTC resistor value from the manufacturer is 467kΩ. So the series resistance is given by Equation 14.

$$R_S = 20k\Omega - R_{NTC_105°C} = 20k\Omega - 15.65k\Omega = 4.35k\Omega \quad \text{(EQ. 14)}$$

The closest standard resistor is 4.42kΩ. Furthermore, the NTC resistance at T_2 is given by Equation 15.

$$R_{NTC_T2} = 2.96k\Omega + R_{NTC_T1} = 18.16k\Omega \quad \text{(EQ. 15)}$$

Therefore, the NTC branch is designed to have a 470k NTC and 4.42k resistor in series. The part number of the NTC thermistor is ERTJ0EV474J. It is a 0402 package. The NTC

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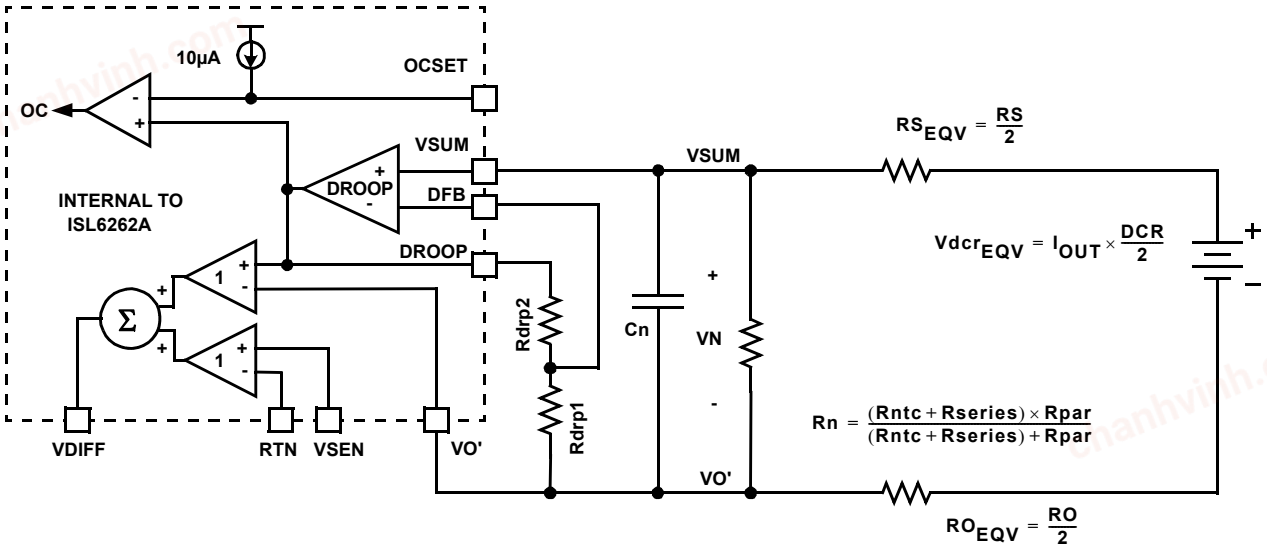


FIGURE 40. EQUIVALENT MODEL FOR DROOP AND DIE SENSING USING DCR SENSING

thermistor should be placed in the spot which gives the best indication of the temperature of voltage regulator circuit.

Static Mode of Operation - Static Droop Using DCR Sensing

As previously mentioned, the ISL6262A has an internal differential amplifier which provides for very accurate voltage regulation at the die of the processor. The load line regulation is also accurate for both two-phase and single-phase operation. The process of selecting the components for the appropriate load line droop is explained here.

For DCR sensing, the process of compensation for DCR resistance variation to achieve the desired load line droop has several steps and is somewhat iterative.

The two-phase solution using DCR sensing is shown in Figure 37. There are two resistors connecting to the terminals of inductor of each phase. These are labeled R_S and R_O. These resistors are used to obtain the DC voltage drop across each inductor. Each inductor will have a certain level of DC current flowing through it, and this current, when multiplied by the DCR of the inductor, creates a small DC voltage drop across the inductor terminal. When this voltage is summed with the other channels DC voltages, the total DC load current can be derived.

R_O is typically 1Ω to 10Ω. This resistor is used to tie the outputs of all channels together and thus create a summed average of the local CORE voltage output. R_S is determined through an understanding of both the DC and transient load currents. This value will be covered in the next section. However, it is important to keep in mind that the output of each of these R_S resistors are tied together to create the VSUM voltage node. With both the outputs of R_O and R_S tied together, the simplified model for the droop circuit can be derived. This is presented in Figure 40.

Figure 40 shows the simplified model of the droop circuitry. Essentially one resistor can replace the R_O resistors of each phase and one R_S resistor can replace the R_S resistors of each phase. The total DCR drop due to load current can be replaced by a DC source, the value of which is given by: Equation 16.

$$V_{DCR_EQU} = \frac{I_{OUT} \bullet DCR}{2} \quad \text{(EQ. 16)}$$

For the convenience of analysis, the NTC network comprised of R_{ntc}, R_{series} and R_{par}, given in Figure 37, is labeled as a single resistor R_n in Figure 40.

The first step in droop load line compensation is to adjust R_n, RO_{EQV} and RS_{EQV} such that sufficient droop voltage exists even at light loads between the VSUM and VO' nodes. As a rule of thumb, we start with the voltage drop across the R_n network, VN, to be 0.5 to 0.8 times V_{DCR_EQU}. This ratio provides for a fairly reasonable amount of light load signal from which to arrive at droop.

The resultant NTC network resistor value is dependent on the temperature and given by Equation 17.

$$R_n(T) = \frac{(R_{series} + R_{ntc}) \bullet R_{par}}{R_{series} + R_{ntc} + R_{par}} \quad \text{(EQ. 17)}$$

For simplicity, the gain of Vn to the V_{dcr_equ} is defined by G1, also dependent on the temperature of the NTC thermistor.

$$G_1(T) \overset{\Delta}{=} \frac{R_n(T)}{R_n(T) + RS_{EQV}} \quad \text{(EQ. 18)}$$

$$DCR(T) = DCR_{25°C} \bullet (1 + 0.00393*(T-25)) \quad \text{(EQ. 19)}$$

Therefore, the output of the droop amplifier divided by the total load current can be expressed as shown in Equation 20, where R_{droop} is the realized load line slope and 0.00393 is the temperature coefficient of the copper.

$$R_{droop} = G_1(T) \bullet \frac{DCR_{25}}{2} \bullet (1 + 0.00393*(T-25)) \bullet k_{droopamp} \quad \text{(EQ. 20)}$$

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To achieve the droop value independent from the temperature of the inductor, it is equivalently expressed by Equation 21.

$$G_1(T) \bullet (1 + 0.00393*(T-25)) \cong G_{1target} \quad \text{(EQ. 21)}$$

The non-inverting droop amplifier circuit has the gain $K_{droopamp}$ expressed as:

$$k_{droopamp} = 1 + \frac{R_{drp2}}{R_{drp1}}$$

$G_{1target}$ is the desired gain of Vn over I_{OUT} • DCR/2. Therefore, the temperature characteristics of gain of Vn is described by Equation 22.

$$G_1(T) = \frac{G_{1target}}{(1 + 0.00393*(T-25))} \quad \text{(EQ. 22)}$$

For the $G_{1target}$ = 0.76:
R_{ntc} = 10kΩ with b = 4300,
R_{series} = 2.61kΩ, and
R_{par} = 11kΩ

RS_{EQV} = 1825Ω generates a desired G1, close to the feature specified in Equation 22.

The actual G1 at +25°C is 0.769. For different G1 and NTC thermistor preferences, the design file to generate the proper value of R_{ntc}, R_{series}, R_{par}, and RS_{EQV} is provided by Intersil.

Then, the individual resistors from each phase to the VSUM node, labeled R_{S1} and R_{S2} in Figure 37, are then given by Equation 23.

$$R_S = 2 \bullet RS_{EQV} \quad \text{(EQ. 23)}$$

So, R_S = 3650Ω. Once we know the attenuation of the R_S and R_N network, we can then determine the droop amplifier gain required to achieve the load line. Setting R_{drp1} = 1k_1%, then R_{drp2} can be found using Equation 24.

$$Rdrp2 = \left(\frac{2 \bullet R_{droop}}{DCR \bullet G1(25°C)} - 1\right) \bullet R_{drp1} \quad \text{(EQ. 24)}$$

Droop Impedance (R_{droop}) = 0.0021 (V/A) as per the Intel IMVP-6+ specification, DCR = 0.0008Ω typical for a 0.36µH inductor, R_{drp1} = 1kΩ and the attenuation gain (G1) = 0.77, R_{drp2} is then given by Equation 25.

$$Rdrp2 = \left(\frac{2 \bullet R_{droop}}{0.0008 \bullet 0.769} - 1\right) \bullet 1k\Omega \approx 5.82k\Omega \quad \text{(EQ. 25)}$$

Note, we choose to ignore the R_O resistors because they do not add significant error.

These designed values in R_n network are very sensitive to the layout and coupling factor of the NTC to the inductor. As only one NTC is required in this application, this NTC should be placed as close to the Channel 1 inductor as possible and PCB traces sensing the inductor voltage should be going directly to the inductor pads.

Once the board has been laid out, some adjustments may be required to adjust the full load droop voltage. This is fairly easy and can be accomplished by allowing the system to achieve thermal equilibrium at full load, and then adjusting R_{drp2} to obtain the appropriate load line slope.

To see whether the NTC has compensated the temperature change of the DCR, the user can apply full load current and wait for the thermal steady state and see how much the output voltage will deviate from the initial voltage reading. A good compensation can limit the drift to 2mV. If the output voltage is decreasing with temperature increase, that ratio between the NTC thermistor value and the rest of the resistor divider network has to be increased. The user should follow the evaluation board value and layout of NTC as much as possible to minimize engineering time.

The 2.1mV/A load line should be adjusted by R_{drp2} based on maximum current, (not based on small current steps like 10A), as the droop gain might vary between each 10A step. Basically, if the max current is 40A, the required droop voltage is 84mV. The user should have 40A load current on and look for 84mV droop. If the drop voltage is less than 84mV, for example 80mV, the new value will be calculated by: using Equation 26.

$$Rdrp2_new = \frac{84mV}{80mV}(Rdrp1 + Rdrp2) - Rdrp1 \quad \text{(EQ. 26)}$$

For the best accuracy, the effective resistance on the DFB and VSUM pins should be identical so that the bias current of the droop amplifier does not cause an offset voltage. In the previous example, the resistance on the DFB pin is R_{drp1} in parallel with R_{drp2}, that is, 1k in parallel with 5.82k or 853Ω. The resistance on the VSUM pin is R_n in parallel with RS_{EQV} or 5.87k in parallel with 1.825k or 1392Ω. The mismatch in the effective resistances is 1404 - 53 = 551Ω. Do not let the mismatch get larger than 600Ω. To reduce the mismatch, multiply both R_{drp1} and R_{drp2} by the appropriate factor. The appropriate factor in the example is 1404/853 = 1.65. In summary, the predicted load line with the designed droop network parameters based on the Intersil design tool is shown in Figure 41

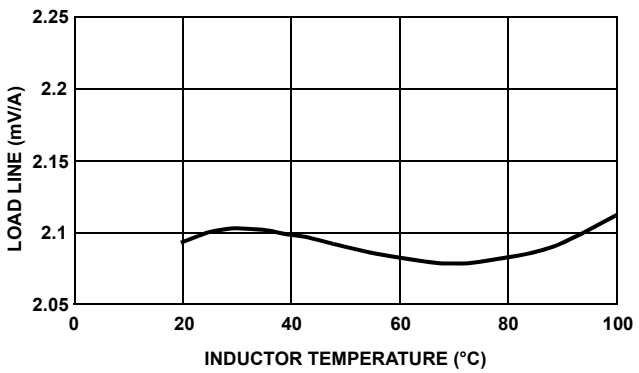


FIGURE 41. LOAD LINE PERFORMANCE WITH NTC THERMAL COMPENSATION

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Dynamic Mode of Operation - Dynamic Droop Using DCR Sensing

Droop is very important for load transient performance. If the system is not compensated correctly, the output voltage could sag excessively upon load application and potentially create a system failure. The output voltage could also take a long period of time to settle to its final value. This could be problematic if a load dump were to occur during this time. This situation would cause the output voltage to rise above the no load setpoint of the converter and could potentially damage the CPU.

The L/DCR time constant of the inductor must be matched to the R_n*C_n time constant as shown in Equation 27.

$$\frac{L}{DCR} = \frac{R_n \bullet RS_{EQV}}{R_n + RS_{EQV}} \bullet C_n \qquad \text{(EQ. 27)}$$

Solving for C_n we now have Equation 28.

$$C_n = \frac{\frac{L}{DCR}}{\frac{R_n \bullet RS_{EQV}}{R_n + RS_{EQV}}} \qquad \text{(EQ. 28)}$$

Note, R_O was neglected. As long as the inductor time constant matches the C_n, R_n and R_s time constants as given previously, the transient performance will be optimum. As in the static droop case, this process may require a slight adjustment to correct for layout inconsistencies. For the example of L = 0.36µH with 0.8mΩ DCR, Cn is calculated in Equation 29.

$$C_n = \frac{\frac{0.36\mu H}{0.0008}}{\text{parallel}(5.823K,\ 1.825K)} \approx 330nF \qquad \text{(EQ. 29)}$$

The value of this capacitor is selected to be 330nF. As the inductors tend to have 20% to 30% tolerances, this cap generally will be tuned on the board by examining the transient voltage. If the output voltage transient has an initial dip, lower than the voltage required by the load line, and slowly increases back to the steady state, the capacitor is too small and vice versa. It is better to have the capacitor value a little bigger to cover the tolerance of the inductor to prevent the output voltage from going lower than the specification. This cap needs to be a high grade capacitor like X7R with low tolerance. There is another consideration in order to achieve better time constant match mentioned previously. The NPO/COG (class-I) capacitors have only 5% tolerance and a very good thermal characteristics. But those capacitors are only available in small capacitance values. In order to use such capacitors, the resistors and thermistors surrounding the droop voltage sensing and droop amplifier has to be resized up to 10X to reduce the capacitance by 10X. But attention has to be paid in balancing the impedance of droop amplifier in this case.

Dynamic Mode of Operation - Compensation Parameters

Considering the voltage regulator as a black box with a voltage source controlled by VID and a series impedance, in order to achieve the 2.1mV/A load line, the impedance needs to be 2.1mΩ. The compensation design has to target the output impedance of the converter to be 2.1mΩ. There is a mathematical calculation file available to the user. The power stage parameters such as L and Cs are needed as the input to calculate the compensation component values. Attention has to be paid to the input resistor to the FB pin. Too high of a resistor will cause an error to the output voltage regulation because of bias current flowing in the FB pin. It is better to keep this resistor below 3k when using this file.

Static Mode of Operation - Current Balance Using DCR or Discrete Resistor Current Sensing

Current Balance is achieved in the ISL6262A through the matching of the voltages present on the ISEN pins. The ISL6262A adjusts the duty cycles of each phase to maintain equal potentials on the ISEN pins. R_L and C_L around each inductor, or around each discrete current resistor, are used to create a rather large time constant such that the ISEN voltages have minimal ripple voltage and represent the DC current flowing through each channel's inductor. For optimum performance, R_L is chosen to be 10kΩ and CL is selected to be 0.22µF. When discrete resistor sensing is used, a capacitor most likely needs to be placed in parallel with R_L to properly compensate the current balance circuit.

ISL6262A uses RC filter to sense the average voltage on phase node and forces the average voltage on the phase node to be equal for current balance. Even though the ISL6262A forces the ISEN voltages to be almost equal, the inductor currents will not be exactly equal. Using DCR current sensing as an example, two errors have to be added to find the total current imbalance.

1. Mismatch of DCR: If the DCR has a 5% tolerance then the resistors could mismatch by 10% worst case. If each phase is carrying 20A then the phase currents mismatch by 20A*10% = 2A.
2. Mismatch of phase voltages/offset voltage of ISEN pins: The phase voltages are within 2mV of each other by current balance circuit. The error current that results is given by 2mV/DCR. If DCR = 1mΩ then the error is 2A.

In the previous example, the two errors add to 4A. For the two phase DC/DC, the currents would be 22A in one phase and 18A in the other phase. In the above analysis, the current balance can be calculated with 2A/20A = 10%. This is the worst case calculation. For example, the actual tolerance of two 10% DCRs is 10%*sqrt(2) = 7%.

There are provisions to correct the current imbalance due to layout or to purposely divert current to certain phase for better thermal management. Customer can put a resistor in parallel with the current sensing capacitor on the phase of interest in order to purposely increase the current in that phase.

If the PC board trace resistance from the inductor to the microprocessor are significantly different between two phases, the current will not be balanced perfectly. Intersil has a

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proprietary method to achieve the perfect current sharing in case of severe unbalanced layout.

When choosing the current sense resistor, both the tolerance of the resistance and the TCR are important. Also, the current sense resistor's combined tolerance at a wide temperature range should be calculated.

Droop Using Discrete Resistor Sensing - Static/ Dynamic Mode of Operation

Figure 42 shows the equivalent circuit of a discrete current sense approach. Figure 33 shows a more detailed schematic of this approach. Droop is solved the same way as the DCR sensing approach with a few slight modifications.

First, because there is no NTC required for thermal compensation, the R_n resistor network in the previous section is not required. Second, because there is no time constant matching required, the C_n component is not matched to the L/DCR time constant. This component does indeed provide noise immunity and therefore is populated with a 39pF capacitor.

The R_S values in the previous section, R_S = 1.5k_1%, are sufficient for this approach.

Now the input to the droop amplifier is essentially the Vrsense voltage. This voltage is given by Equation 30.

$$Vrsense_{EQV} = \frac{R_{sense}}{2} \bullet I_{OUT} \qquad \text{(EQ. 30)}$$

The gain of the droop amplifier, $K_{droopamp}$, must be adjusted for the ratio of the R_{sense} to droop impedance, R_{droop}. We use the Equation 31.

$$K_{droopamp} = \frac{R_{droop}}{R_{sense}} \bullet 2 \qquad \text{(EQ. 31)}$$

Solving for the R_{drp2} value, R_{droop} = 0.0021(V/A) as per the Intel IMVP-6+ specification, R_{sense} = 0.001Ω and R_{drp1} =1kΩ, we obtain in Equation 32.

$$R_{drp2} = (K_{droopamp} - 1) \bullet R_{drp1} = 3.2k\Omega \qquad \text{(EQ. 32)}$$

These values are extremely sensitive to layout. Once the board has been laid out, some tweaking may be required to adjust the full load droop. This is fairly easy and can be accomplished by allowing the system to achieve thermal equilibrium at full load, and then adjusting R_{drp2} to obtain the desired droop value.

Fault Protection - Overcurrent Fault Setting

As previously described, the overcurrent protection of the ISL6262A is related to the droop voltage. Previously we have calculated that the droop voltage = ILoad*R_{droop}, where R_{droop} is the load line slope specified as 0.0021 (V/A) in the Intel IMVP-6+ specification. Knowing this relationship, the overcurrent protection threshold can be set up as a voltage droop level. Knowing this voltage droop level, one can program in the appropriate drop across the R_{OC} resistor. This voltage drop will be referred to as Voc. Once the droop voltage is greater than Voc, the PWM drives will turn off and PGOOD will go low.

The selection of R_{OC} is given in Equation 33. Assuming we desire an overcurrent trip level, I_{OC}, of 55A, and knowing from the Intel Specification that the load line slope, R_{droop} is 0.0021 (V/A), we can then calculate for R_{OC} as shown in Equation 33.

$$R_{OC} = \frac{I_{OC} \bullet R_{droop}}{10\mu A} = \frac{55 \bullet 0.0021}{10 \bullet 10^{-6}} = 11.5k\Omega \qquad \text{(EQ. 33)}$$

Note: If the droop load line slope is not -0.0021 (V/A) in the application, the overcurrent setpoint will differ from predicted.

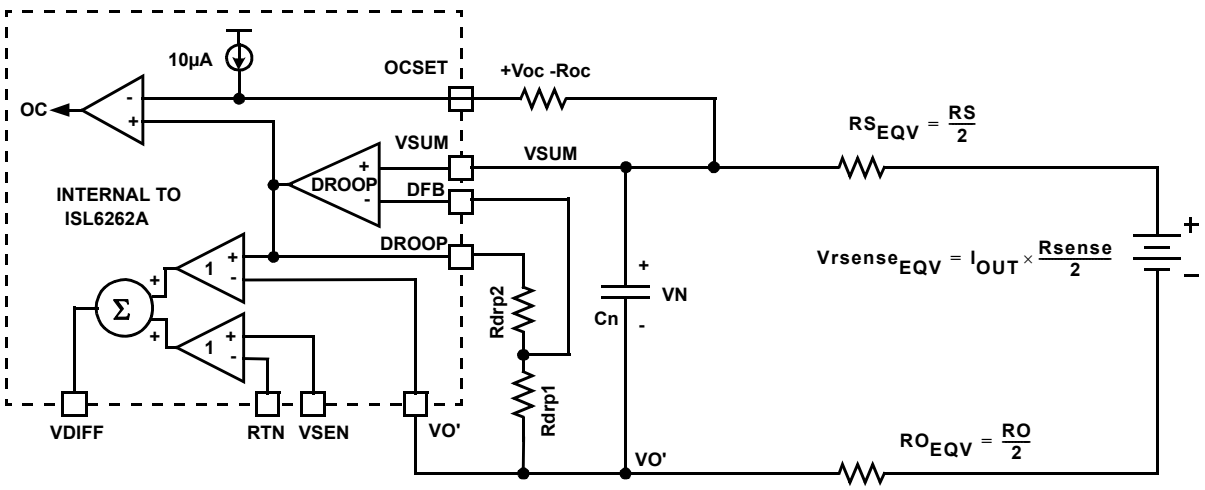


FIGURE 42. EQUIVALENT MODEL FOR DROOP AND DIE SENSING USING DISCRETE RESISTOR SENSING

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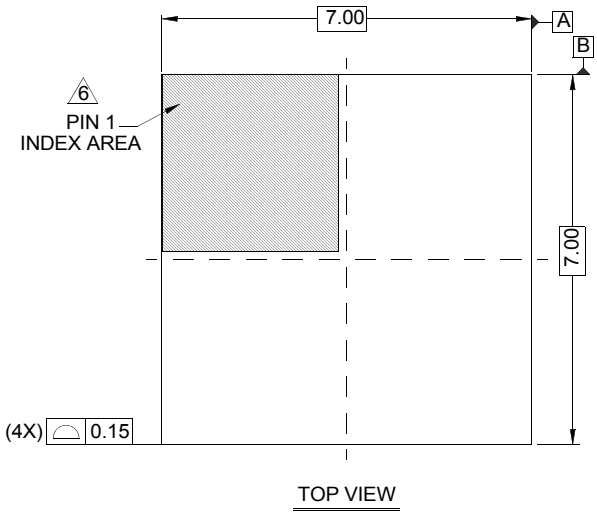
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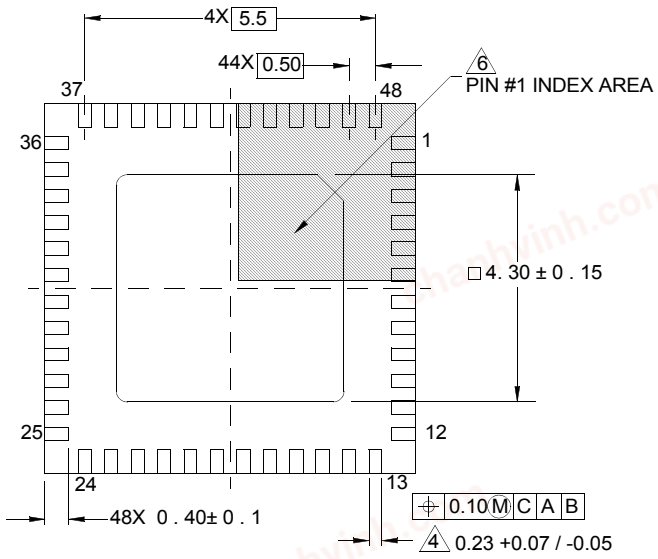
Package Outline Drawing

L48.7x7

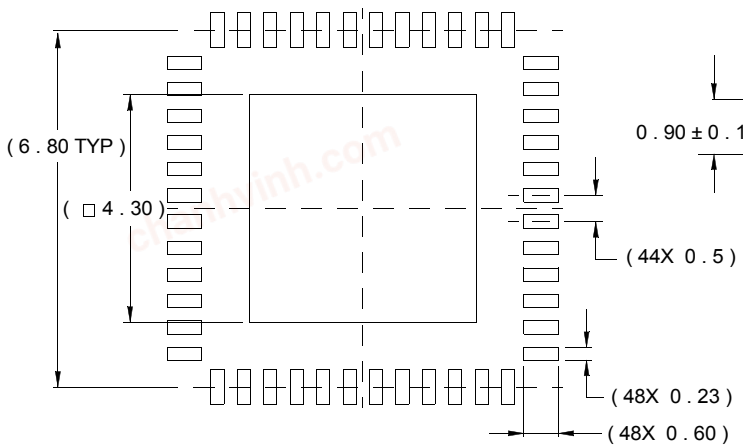
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



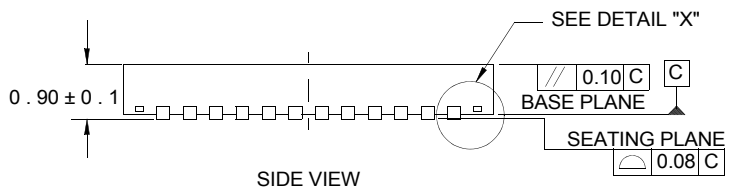
TOP VIEW



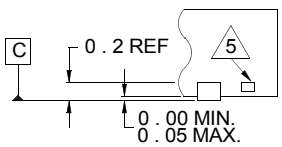
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.