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MegaQ™: An Automatic Composite Video Equalizer, Fully-Adaptive to 1 Mile (1600m)

ISL59601, ISL59602, ISL59603, ISL59604, ISL59605

The ISL59601, ISL59602, ISL59603, ISL59604, and ISL59605 (the "MegaQ™" product family) are single-channel adaptive equalizers designed to automatically compensate for long runs of Cat 5/6 or RG-59 cable, producing high quality video output with no user interaction. The ISL59601 equalizes Cat 5/6 up to a distance of 1000 feet (300 meters), while the ISL59605 equalizes up to 5300 feet (1600 meters).

MegaQ™ compensates for high frequency cable losses of up to 60dB (ISL59605) at 5MHz as well as source amplitude variations up to ±3dB.

The ISL59601, ISL59602, ISL59603, ISL59604, and ISL59605 operate from a single +5V supply. Inputs are AC-coupled and internally DC-restored. The output can drive $2V_{P-P}$ into two source-terminated 75Ω loads (AC-coupled or DC-coupled).

Related Literature

- AN1780 "ISL59605-Catx-EVZ Evaluation Board Operation" (Stand-Alone Evaluation Board)
- AN1776 "ISL59603-Coax-EVZ Evaluation Board Operation" (Stand-Alone Evaluation Board)
- AN1775 "ISL59605-SPI-EVALZ Evaluation Board (with Serial Interface) Operation" (Evaluation Board with USB Serial Interface)

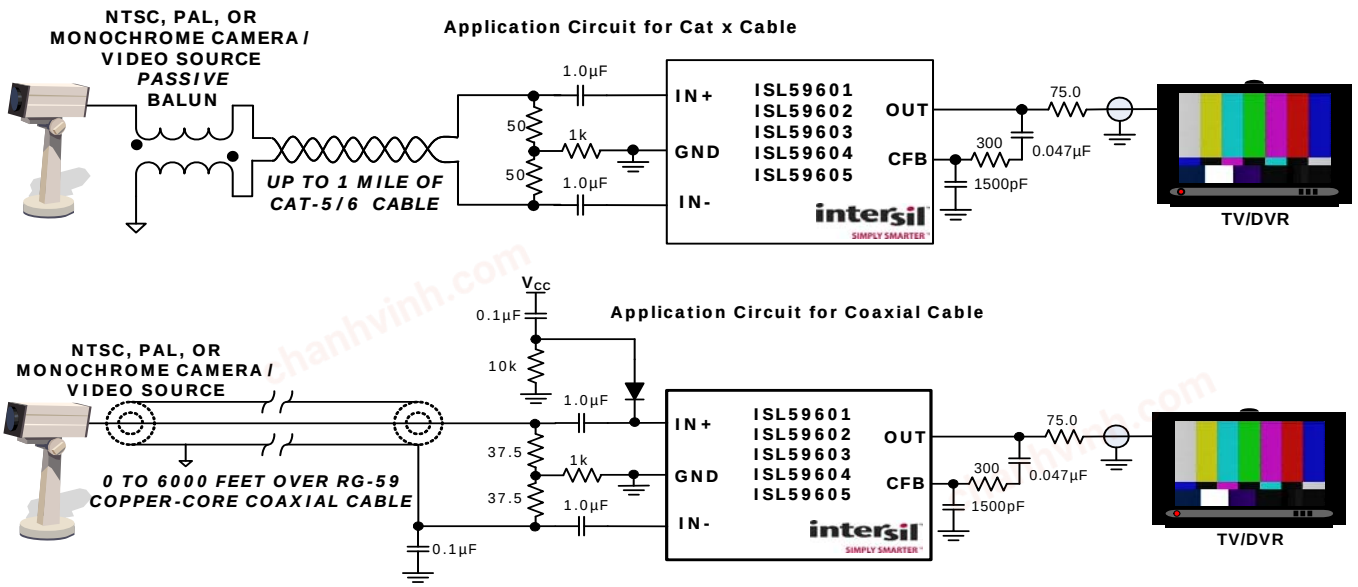
Features

- ISL59605 Equalizes Up to 1 Mile (1600m) of Cat 5/6 and Up to 6000 Feet (1800m) of RG-59
- Fully Automatic, Stand-Alone Operation - No User Adjustment Required
- ±8kV ESD Protection on All Inputs
- Automatic Cable Type Compensation
- Compatible with Color or Monochrome, NTSC or PAL Signals
- Automatic Polarity Detection and Inversion
- Compensates for ±3dB Source Variation (in Addition to Cable Losses)
- Optional Serial Interface Adds Additional Functionality
- 5MHz -3dB Bandwidth
- Works with Single-Ended or Differential Inputs
- Output Drives Up to Two 150Ω Video Loads

Applications

- Surveillance Video
- Video Distribution

Typical Application

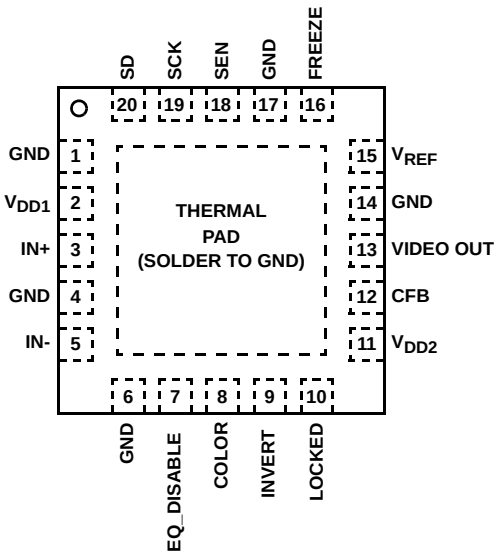


CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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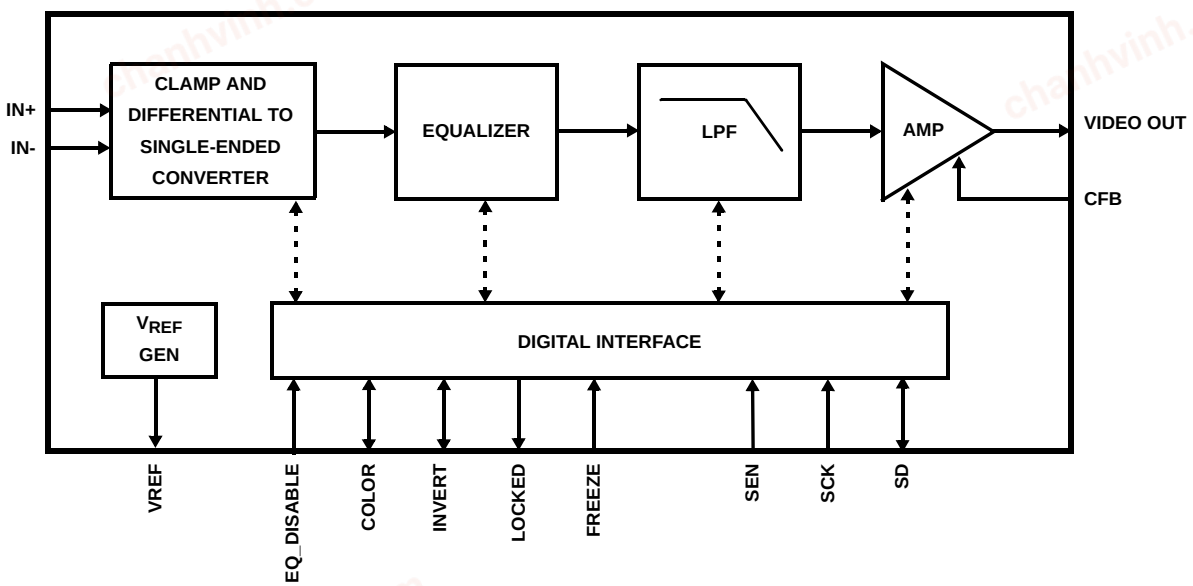
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Pin Configuration

ISL59601, ISL59602, ISL59603, ISL59604, ISL59605
(20 LD QFN)
TOP VIEW



Block Diagram



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Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
INPUTS		
3	IN+	High impedance analog input. This is the positive differential video input. Input signals are externally AC-coupled with an external 1.0µF capacitor. See Applications Information section for information regarding input network for Cat x and coax cables.
5	IN-	High impedance analog input. This is the negative differential video input. Input signals are externally AC-coupled with an external 1.0µF capacitor. See Applications Information section for information regarding input network for Cat x and coax cables.
12	CFB	Analog input. Bypass to ground with a 1500pF capacitor and connect to VIDEO OUT via a 0.047µF capacitor in series with a 300Ω resistor.
OUTPUTS		
13	VIDEO OUT	Single-ended video output. The internal AGC sets this level to $2V_{P-P}$ for a nominal $1V_{P-P}$ (pre-cable) video source.
DIGITAL I/O		
7	EQ_DISABLE	Digital Input. Equalizer Disable. 0: Normal Operation 1: Disables the equalizer to allow for insertion of upstream data onto the signal path, e.g. RS-485. This pin must be asserted high or low. Do not float this pin.
8	COLOR	Digital I/O. Color Indicator/Override. 0: Monochrome 1: Color When used as an output, this pin indicates whether the incoming signal does or does not have a colorburst. When used as an input, this pin forces the state machine to into monochrome or color mode. See Figure 49 and associated text for more information on functionality. When COLOR is not externally driven, it is an output pin with a 13k (typical) output impedance. It is capable of driving 5V, high-impedance CMOS logic. Note: The COLOR indicator may be invalid for monochrome signals over greater than ~4800 feet. The device will still equalize properly if this occurs.
9	INVERT	Digital I/O. Polarity Indicator/Override. 0: Nominal Polarity. 1: Inverted Polarity. When used as an output, this pin indicates the polarity of the incoming signal. When used as an input, this pin controls whether or not the input signal is inverted in the signal chain. See Figure 48 and associated text for more information on functionality. When INVERT is not externally driven, it is an output pin with a 13k (typical) output impedance. It is capable of driving 5V, high-impedance CMOS logic. In stand-alone mode, toggling this pin high-low-high or low-high-low will make the equalizer reacquire the signal.
10	LOCKED	Digital Output. 0: Signal is not equalized (or not present). 1: Signal is equalized and settled. Note: The LOCKED indicator may be invalid for monochrome signals over greater than ~4800 feet. The device will still equalize properly if this occurs.
16	FREEZE	Digital Input. Freezes equalizer in its current EQ state. 0: Continuous Update 1: Freeze EQ in current state. For stand-alone operations, connect FREEZE to the LOCKED pin to enter the recommended **Lock Until Reset** mode. Tie this pin low if unused.
SERIAL INTERFACE		
18	SEN	Digital Input. Serial Interface Enable. This pin should be tied to ground when not in use.
19	SCK	Digital Input. Serial Interface Clock Signal. This pin should be tied to ground when not in use.
20	SD	Digital I/O. Serial Interface Data Signal. This pin should be tied to ground when not in use.
POWER		
2	V_{DD1}	+5V power supply for analog equalizer. Isolate from +5V source with a ferrite bead and bypass to ground with a 0.1µF capacitor in parallel with a 4.7µF capacitor.

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Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
11	V_{DD2}	+5V power supply for output amplifier. Bypass to ground with a 0.1µF capacitor.
15	V_{REF}	Internally generated 2.5V reference. Bypass to ground with a low-ESR 0.47µF capacitor. Do not attach anything else to this pin.
1, 4, 6, 14, 17	GND	Ground
THERMAL PAD		
EP	PAD	Solder the exposed thermal PAD to ground for best thermal and electrical performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	MAX EQ LENGTH	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL59601IRZ	596 01IRZ	1000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59601IRZ-T7	596 01IRZ	1000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59601IRZ-T7A	596 01IRZ	1000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59602IRZ	596 02IRZ	2000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59602IRZ-T7	596 02IRZ	2000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59602IRZ-T7A	596 02IRZ	2000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59603IRZ	596 03IRZ	3000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59603IRZ-T7	596 03IRZ	3000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59603IRZ-T7A	596 03IRZ	3000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59604IRZ	596 04IRZ	4000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59604IRZ-T7	596 04IRZ	4000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59604IRZ-T7A	596 04IRZ	4000 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59605IRZ	596 05IRZ	5300 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59605IRZ-T7	596 05IRZ	5300 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59605IRZ-T7A	596 05IRZ	5300 feet	-40 to +85	20 Ld QFN (4x4mm)	L20.4x4C
ISL59605-Catx-EVZ	Stand-alone (no USB I/O) evaluation board				
ISL59603-Coax-EVZ	Stand-alone (no USB I/O) evaluation board				
ISL59605-SPI-EVALZ	Evaluation board with serial interface				

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL59601, ISL59602, ISL59603, ISL59604, ISL59605. For more information on MSL please see techbrief TB363.

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Table of Contents

Absolute Maximum Ratings . . . 6
Thermal Information . . . 6
Electrical Specifications . . . 6
Serial Timing . . . 7
Serial Timing Diagram . . . 8
Typical Performance Over 1000 Feet of Cat 5 . . . 9
Typical Performance Over 2000 Feet of Cat 5 . . . 10
Typical Performance Over 3000 Feet of Cat 5 . . . 11
Typical Performance Over 4000 Feet of Cat 5 . . . 12
Typical Performance Over 5200 Feet of Cat 5 . . . 13
Typical Performance Over 1000 Feet of Copper-Core RG-59 . . . 14
Typical Performance Over 2000 Feet of Copper-Core RG-59 . . . 15
Typical Performance Over 3000 Feet of Copper-Core RG-59 . . . 16
Typical Performance Over 4000 Feet of Copper-Core RG-59 . . . 17
Typical Performance Over 5000 Feet of Copper-Core RG-59 . . . 18
Typical Performance Over 6000 Feet of Copper-Core RG-59 . . . 19
Functional Description . . . 20
- MegaQ™ Overview . . . 20
- Equalization for Various Cable Types . . . 20

Application Information . . . 21
- Unshielded Twisted Pair (UTP) App Circuit . . . 21
- Coax Input Circuit . . . 21
- Dual UTP/Coax Input Circuit . . . 21
- Input Multiplexing . . . 21
- Stand-Alone Operation and Configuration . . . 21
  - Lock Until RESET . . . 21
  - Continuous Update . . . 22
- Polarity Detection and Correction . . . 22
- The COLOR Pin . . . 22
- Monochrome Video Signals . . . 22
- Security Cameras . . . 22
- Additional Equalization Modes Available With the Serial Interface . . . 22
  - Continuous Update . . . 22
  - Lock Until RESET . . . 23
  - Lock Until Signal Loss . . . 23
  - Manual Length . . . 23
- Serial Interface Protocol . . . 23
  - Write Operation . . . 23
  - Read Operation . . . 23

Register Listing . . . 24
Bypassing and Layout Considerations . . . 26
- General PowerPAD Design Considerations . . . 26
- Power Dissipation . . . 26

Revision History . . . 27
Products . . . 27
Package Outline Drawing . . . 28

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Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_{DD} and GND 5.75V
Maximum Continuous Output Current 50mA
Maximum Voltage on any Pin . . . . . GND - 0.3V to V_{DD} + 0.3V
ESD Rating
Human Body Model (tested per JESD22-A114) 8,000V
Machine Model (Tested per JESD22-A115). 600V
CDM Model (Tested per JESD22-C101) 2,000V
Latch Up (Tested per JESD78; Class II, Level A). 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld QFN Package (Notes 4, 5)	40	3.7

Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Die Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{DD} = V_{DD1} = V_{DD2} = +5V, source video amplitude before any cable loss = 1V_{P-P}, cable type = Cat 5, cable length = 0 feet, R_L = 150Ω (75Ω series + 75Ω load to ground), T_A = +25°C, exposed die plate = 0V, unless otherwise specified. Max cable length = 1000 feet for ISL59601, 2000 feet for ISL59602, 3000 feet for ISL59603, 4000 feet for ISL59604, and 5300 feet for ISL59605.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SUPPLY						
V_{DD}	V_{DD} Operating Range		4.5	5.0	5.5	V
I_{S1}	V_{DD1} Supply Current			40	60	mA
I_{S2}	V_{DD2} Supply Current			30	45	mA
$PSRR_{DC}$	Power Supply Rejection Ratio			60		dB
AC PERFORMANCE						
BW	-3dB Bandwidth	Full power		5		MHz
DG	Differential Gain	Cable length = max, 20IRE Sub Carrier on 100% ramp		1		%
DP	Differential Phase	Cable length = max, 20IRE Sub Carrier on 100% ramp		1		°
DC PERFORMANCE						
V_{BL}	Output Blanking/Backporch Level	Measured at VIDEO OUT pin	0.82	0.95	1.05	V
INPUT CHARACTERISTICS						
V_{INDIFF_MIN}	Minimum Correctable Peak-to-Peak Signal Swing	Measured at the source-end of cable, before cable losses		0.7		V_{P-P}
V_{INDIFF_MAX}	Maximum Correctable Peak-to-Peak Signal Swing	Measured at the source-end of cable, before cable losses		1.4		V_{P-P}
V_{CM-MIN}	Min Common Mode Input Voltage			1		V
V_{CM-MAX}	Max Common Mode Input Voltage			4		V
SNR	Signal-to-Noise Ratio, NTC-7 weighted filter	EQ = 0 feet		-67		dB rms
		EQ = 1,000 feet		-67		dB rms
		EQ = 2,000 feet		-65		dB rms
		EQ = 3,000 feet		-64		dB rms
		EQ = 4,000 feet		-61		dB rms
		EQ = 5,300 feet		-54		dB rms

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Electrical Specifications

$V_{DD} = V_{DD1} = V_{DD2}$ = +5V, source video amplitude before any cable loss = $1V_{P-P}$, cable type = Cat 5, cable length = 0 feet, R_L = 150Ω (75Ω series + 75Ω load to ground), T_A = +25°C, exposed die plate = 0V, unless otherwise specified. Max cable length = 1000 feet for ISL59601, 2000 feet for ISL59602, 3000 feet for ISL59603, 4000 feet for ISL59604, and 5300 feet for ISL59605. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
CMRR	Common-mode Rejection Ratio at f_{IN} = 100kHz	0 feet cable		-50		dB
		2,500 feet cable		-35		dB
I_{Clamp}	Input Clamp Current			25		µA
OUTPUT CHARACTERISTICS						
A_{GC-ACC}	AGC Accuracy	Accuracy of sync tip amplitude relative to 600mV		±0.5		dB
I_{OUT}	Output Drive Current			40		mA
t_{EN-EQ}	Enable-to-Equalization On Time			500		ns
t_{DIS-EQ}	Disable-to-Equalization Off Time			500		ns
LOGIC CONTROL PINS						
V_{IH}	Logic High Level		2.0			V
V_{IL}	Logic Low Level				0.8	V
I_{LOGIC}	Logic Input Current	EQ_DISABLE, FREEZE, SD, SCK, SEN		±10		µA
		INVERT, COLOR		±500		µA

Serial Timing

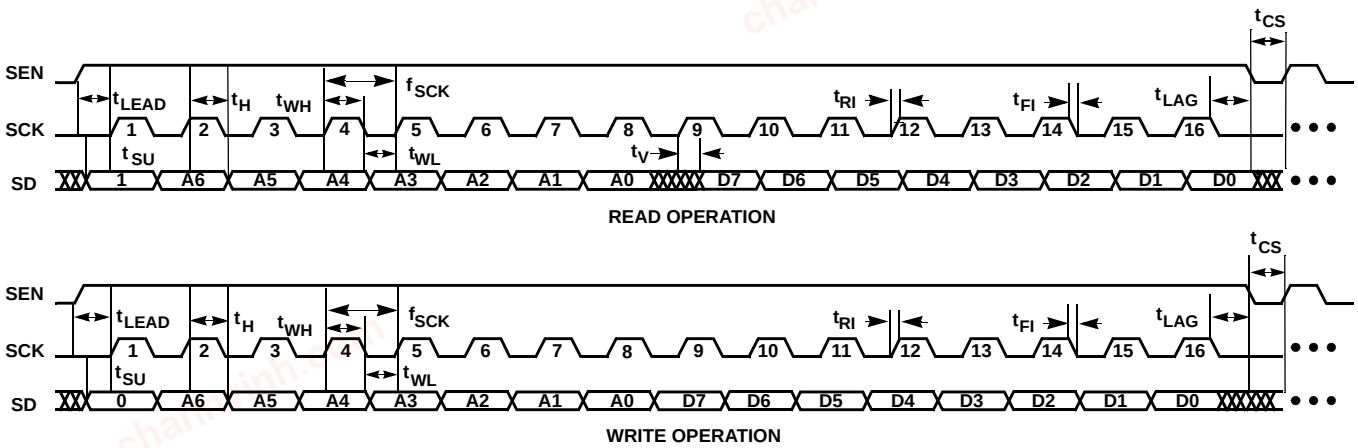
PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
t_{CS}	Serial Enable Deselect Time		10			ns
t_{LEAD}	Lead Time		10			ns
t_{SU}	SD, SCK Setup Time		10			ns
t_H	SD, SEN, SCK Hold Time		10			ns
t_{WH}	SCK High Time		100			ns
t_{WL}	SCK Low Time		100			ns
t_{RI}	SD, SEN, SCK Rise Time		10			ns
t_{FI}	SD, SEN, SCK Fall Time		10			ns
t_{LAG}	Lag Time		10			ns
t_V	SCK Rising Edge to SD Data Valid	Read Operation			10	ns
f_{SCK}	SCK Frequency				5	MHz

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

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Serial Timing Diagram



READ OPERATION

WRITE OPERATION

A6:A0 = REGISTER ADDRESS, D7:D0 = DATA TO BE READ/WRITTEN

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Typical Performance Over 1000 Feet of Cat 5



FIGURE 1. TEST PATTERN IMAGE AFTER 1000 FEET OF UNCOMPENSATED CAT 5



FIGURE 2. TEST PATTERN IMAGE AFTER 1000 FEET OF CAT 5 WITH ISL59601 (OR BETTER)

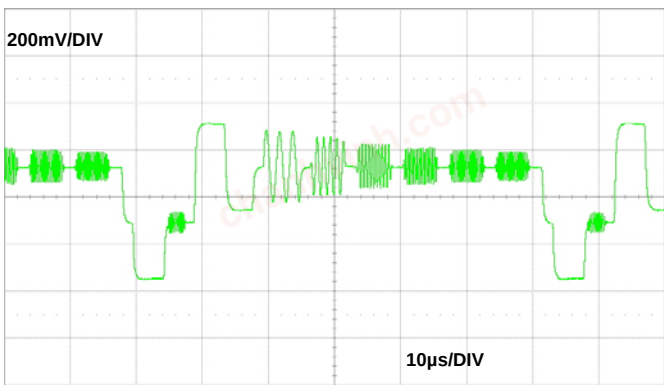


FIGURE 3. MULTIBURST WAVEFORM AFTER 1000 FEET OF UNCOMPENSATED CAT 5

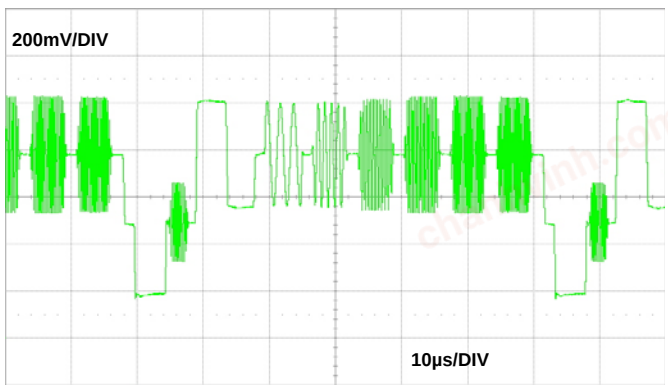


FIGURE 4. MULTIBURST WAVEFORM AFTER 1000 FEET OF CAT 5 WITH ISL59601 (OR BETTER)

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Typical Performance Over 2000 Feet of Cat 5



FIGURE 5. TEST PATTERN IMAGE AFTER 2000 FEET OF UNCOMPENSATED CAT 5



FIGURE 6. TEST PATTERN IMAGE AFTER 2000 FEET OF CAT 5 WITH ISL59602 (OR BETTER)

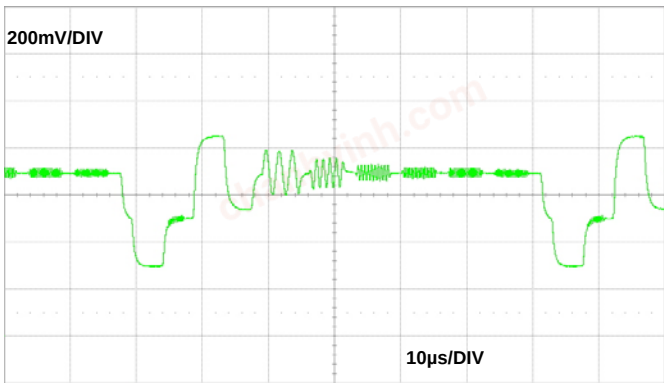


FIGURE 7. MULTIBURST WAVEFORM AFTER 2000 FEET OF UNCOMPENSATED CAT 5

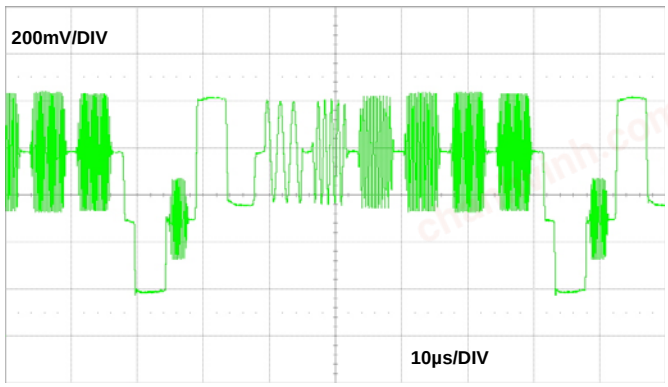


FIGURE 8. MULTIBURST WAVEFORM AFTER 2000 FEET OF CAT 5 WITH ISL59602 (OR BETTER)

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Typical Performance Over 3000 Feet of Cat 5



FIGURE 9. TEST PATTERN IMAGE AFTER 3000 FEET OF UNCOMPENSATED CAT 5



FIGURE 10. TEST PATTERN IMAGE AFTER 3000 FEET OF CAT 5 WITH ISL59603 (OR BETTER)

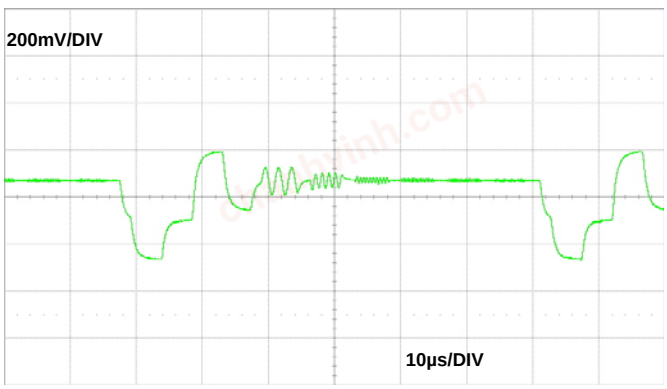


FIGURE 11. MULTIBURST WAVEFORM AFTER 3000 FEET OF UNCOMPENSATED CAT 5

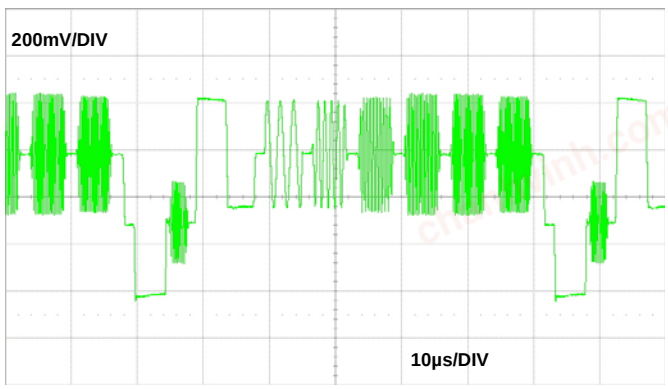


FIGURE 12. MULTIBURST WAVEFORM AFTER 3000 FEET OF CAT 5 WITH ISL59603 (OR BETTER)

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Typical Performance Over 4000 Feet of Cat 5

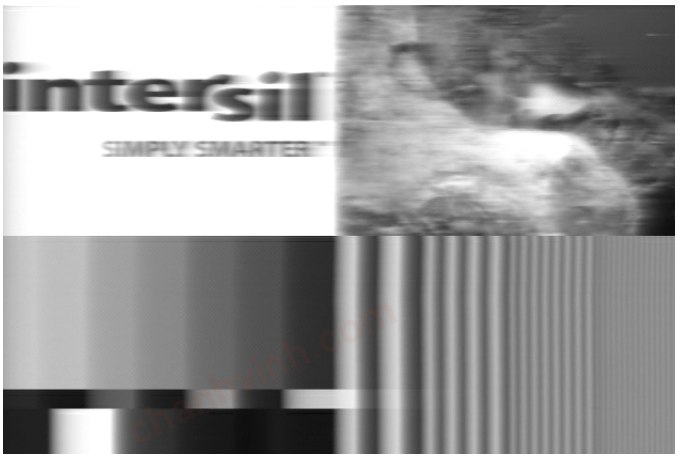


FIGURE 13. TEST PATTERN IMAGE AFTER 4000 FEET OF UNCOMPENSATED CAT 5



FIGURE 14. TEST PATTERN IMAGE AFTER 4000 FEET OF CAT 5 WITH ISL59604 (OR BETTER)

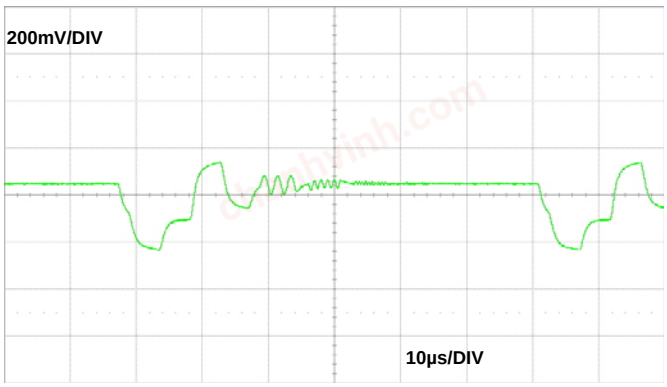


FIGURE 15. MULTIBURST WAVEFORM AFTER 4000 FEET OF UNCOMPENSATED CAT 5

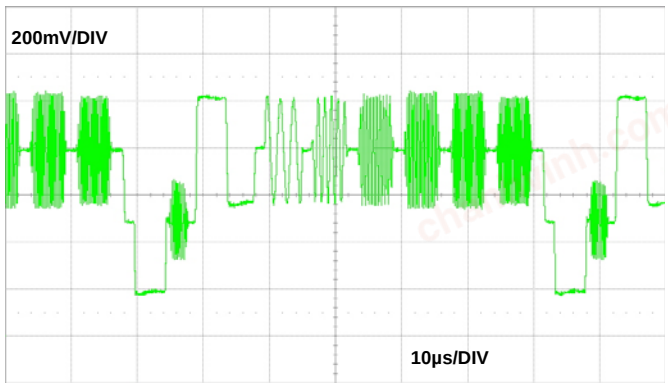


FIGURE 16. MULTIBURST WAVEFORM AFTER 4000 FEET OF CAT 5 WITH ISL59604 (OR BETTER)

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Typical Performance Over 5200 Feet of Cat 5



FIGURE 17. TEST PATTERN IMAGE AFTER 5200 FEET OF UNCOMPENSATED CAT 5



FIGURE 18. TEST PATTERN IMAGE AFTER 5200 FEET OF CAT 5 WITH ISL59605

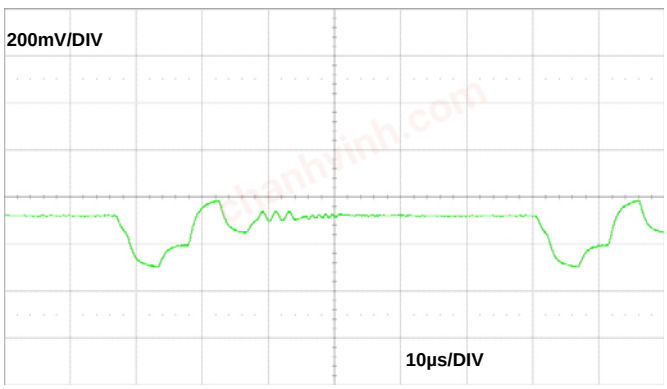


FIGURE 19. MULTIBURST WAVEFORM AFTER 5200 FEET OF UNCOMPENSATED CAT 5

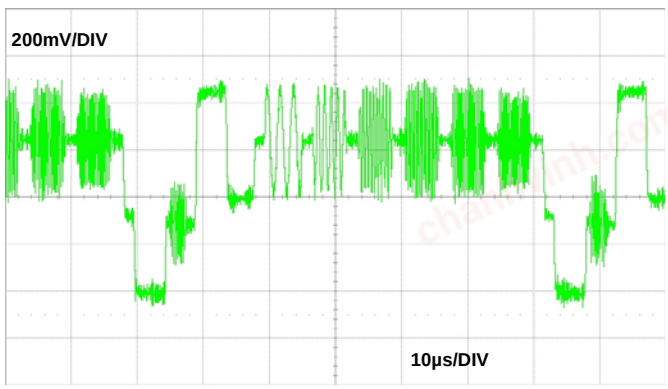


FIGURE 20. MULTIBURST WAVEFORM AFTER 5200 FEET OF CAT 5 WITH ISL59605

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Typical Performance Over 1000 Feet of Copper-Core RG-59



FIGURE 21. TEST PATTERN IMAGE AFTER 1000 FEET OF UNCOMPENSATED RG-59 COAX



FIGURE 22. TEST PATTERN IMAGE AFTER 1000 FEET OF RG-59 COAX WITH ISL59601 (OR BETTER)

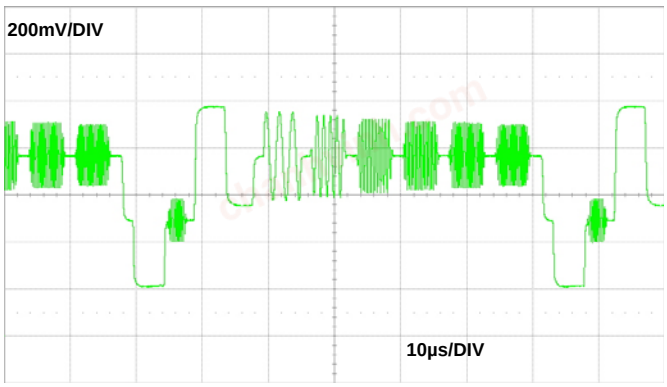


FIGURE 23. MULTIBURST WAVEFORM AFTER 1000 FEET OF UNCOMPENSATED RG-59 COAX

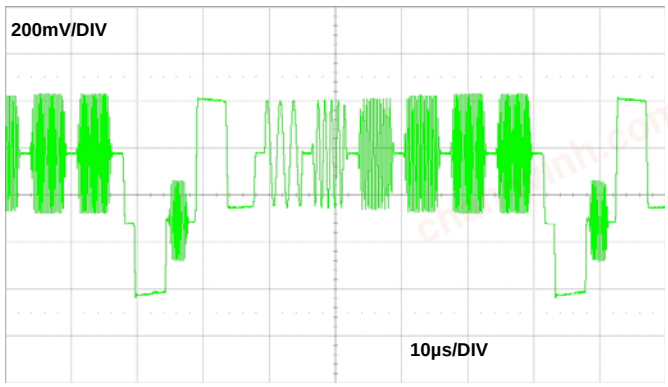


FIGURE 24. MULTIBURST WAVEFORM AFTER 1000 FEET OF RG-59 COAX WITH ISL59601 (OR BETTER)

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Typical Performance Over 2000 Feet of Copper-Core RG-59



FIGURE 25. TEST PATTERN IMAGE AFTER 2000 FEET OF UNCOMPENSATED RG-59 COAX



FIGURE 26. TEST PATTERN IMAGE AFTER 2000 FEET OF RG-59 COAX WITH ISL59602 (OR BETTER)

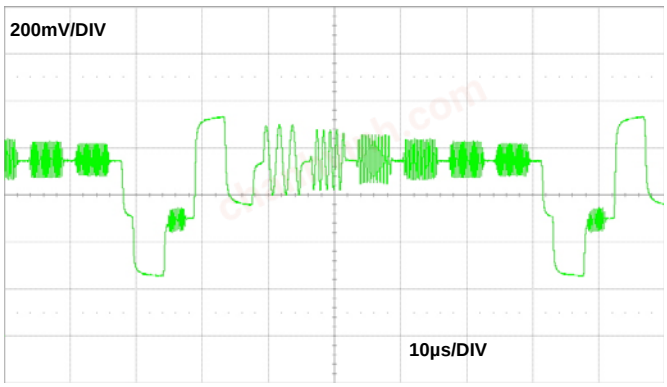


FIGURE 27. MULTIBURST WAVEFORM AFTER 2000 FEET OF UNCOMPENSATED RG-59 COAX

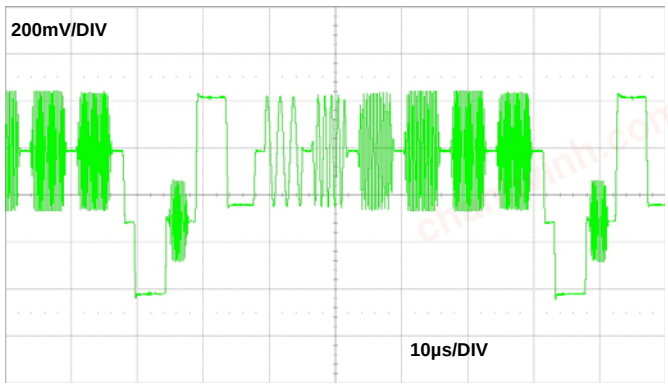


FIGURE 28. MULTIBURST WAVEFORM AFTER 2000 FEET OF RG-59 COAX WITH ISL59602 (OR BETTER)

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Typical Performance Over 3000 Feet of Copper-Core RG-59



FIGURE 29. TEST PATTERN IMAGE AFTER 3000 FEET OF UNCOMPENSATED RG-59 COAX



FIGURE 30. TEST PATTERN IMAGE AFTER 3000 FEET OF RG-59 COAX WITH ISL59602 (OR BETTER)

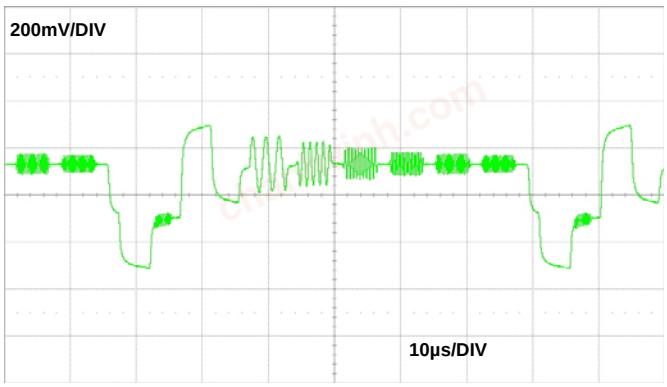


FIGURE 31. MULTIBURST WAVEFORM AFTER 3000 FEET OF UNCOMPENSATED RG-59 COAX

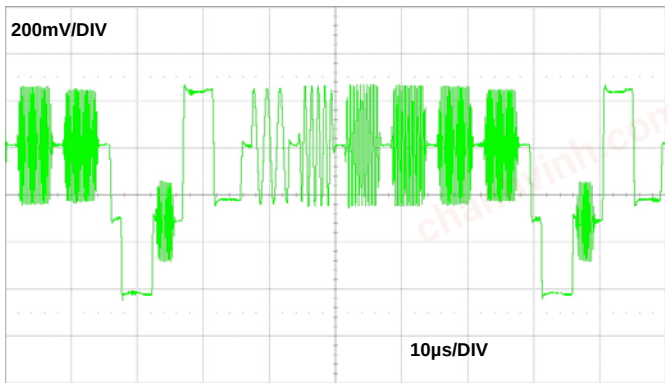


FIGURE 32. MULTIBURST WAVEFORM AFTER 3000 FEET OF RG-59 COAX WITH ISL59602 (OR BETTER)

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Typical Performance Over 4000 Feet of Copper-Core RG-59



FIGURE 33. TEST PATTERN IMAGE AFTER 4000 FEET OF UNCOMPENSATED RG-59 COAX



FIGURE 34. TEST PATTERN IMAGE AFTER 4000 FEET OF RG-59 COAX WITH ISL59602 (OR BETTER)

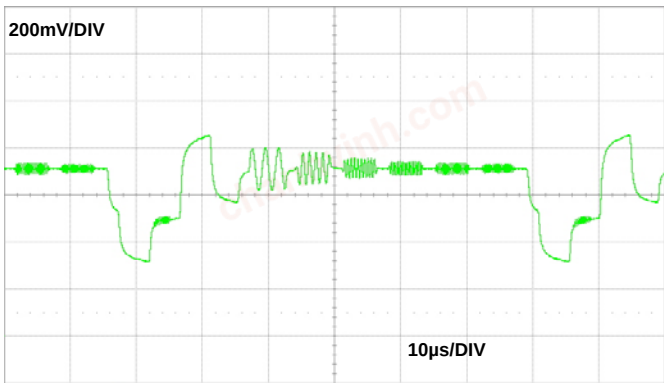


FIGURE 35. MULTIBURST WAVEFORM AFTER 4000 FEET OF UNCOMPENSATED RG-59 COAX

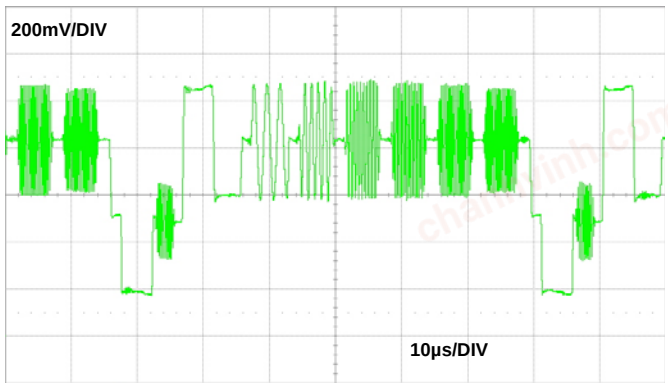


FIGURE 36. MULTIBURST WAVEFORM AFTER 4000 FEET OF RG-59 COAX WITH ISL59602 (OR BETTER)

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Typical Performance Over 5000 Feet of Copper-Core RG-59



FIGURE 37. TEST PATTERN IMAGE AFTER 5000 FEET OF UNCOMPENSATED RG-59 COAX



FIGURE 38. TEST PATTERN IMAGE AFTER 5000 FEET OF RG-59 COAX WITH ISL59603 (OR BETTER)

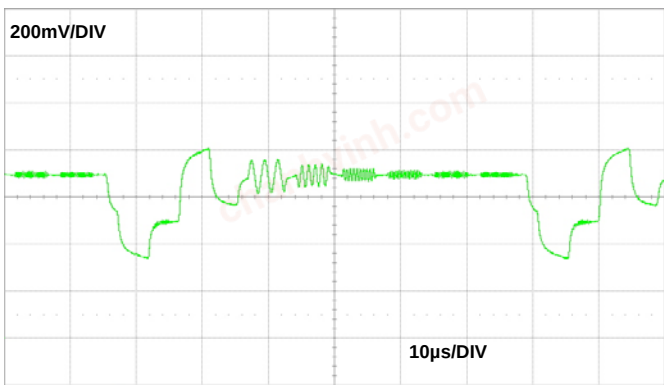


FIGURE 39. MULTIBURST WAVEFORM AFTER 5000 FEET OF UNCOMPENSATED RG-59 COAX

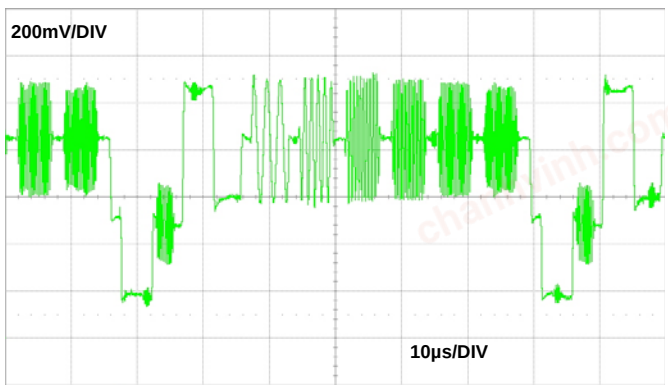


FIGURE 40. MULTIBURST WAVEFORM AFTER 5000 FEET OF RG-59 COAX WITH ISL59603 (OR BETTER)

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Typical Performance Over 6000 Feet of Copper-Core RG-59



FIGURE 41. TEST PATTERN IMAGE AFTER 6000 FEET OF UNCOMPENSATED RG-59 COAX



FIGURE 42. TEST PATTERN IMAGE AFTER 6000 FEET OF RG-59 COAX WITH ISL59603 (OR BETTER)

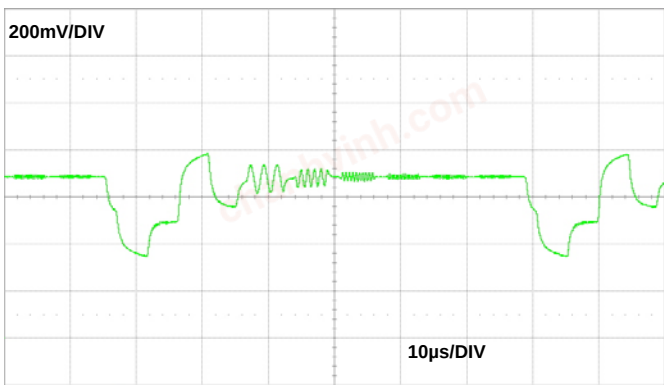


FIGURE 43. MULTIBURST WAVEFORM AFTER 6000 FEET OF UNCOMPENSATED RG-59 COAX

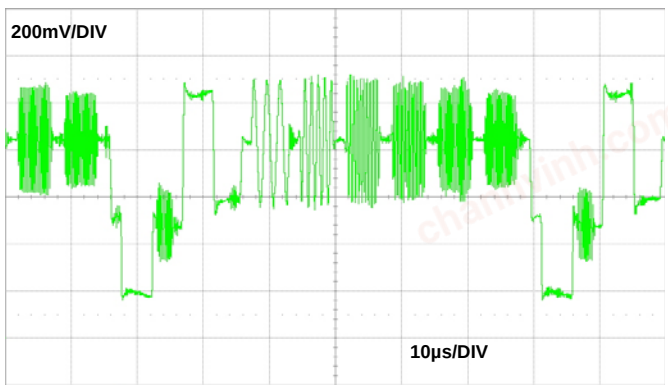


FIGURE 44. MULTIBURST WAVEFORM AFTER 6000 FEET OF RG-59 COAX WITH ISL59603 (OR BETTER)

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Functional Description

MegaQ™ Overview

MegaQ™ is a fully automated, stand-alone equalizer for composite video transmitted over UTP (Unshielded Twisted Pair, i.e. Cat 5, Cat 6, etc.) or coaxial (RG-59) cables.

Differential video signals sent over long distances of twisted pair wire exhibit large high frequency attenuation, resulting in loss of high frequency detail/blurring. The exact loss characteristic is a complex function of wire gauge, length, composition, and coupling to adjacent conductors.

The video signal can be restored by applying a filter with the exact inverse transfer function to the far end signal. MegaQ™ is designed to compensate for the losses due to long cables, and incorporates the functionality and flexibility to match a wide variety of cable types and loss characteristics.

While MegaQ™ was designed and optimized for stand-alone operation, with no need for any external control of any kind, it has an optional SPI serial interface with some additional features. See “Additional Equalization Modes Available With the Serial Interface” on page 22 for more information on the features and operation of the serial interface.

Equalization for Various Cable Types

TABLE 1. CABLE TYPES AND LENGTHS

CABLE TYPE	MAXIMUM LENGTH SUPPORTED
Copper-Core	
CAT5/CAT5e	5300 feet
CAT6	5600 feet
Coaxial - RG-59	6000 feet
CAT2/CAT3 (telephone wire)	3000 feet
Belden IMSA Spec 39-2 581718 (3-pair traffic light cable)	5300 feet
Non-Copper-Core*	
CAT5/CAT5e CCA (Copper-Coated Aluminum Core)	2000 feet
Coaxial - RG-59 CCS (Copper-Coated Steel Core)	1500 feet

*Image quality will be significantly improved over unequalized cable, but there will still be some image smearing due to the high resistance of the core material.

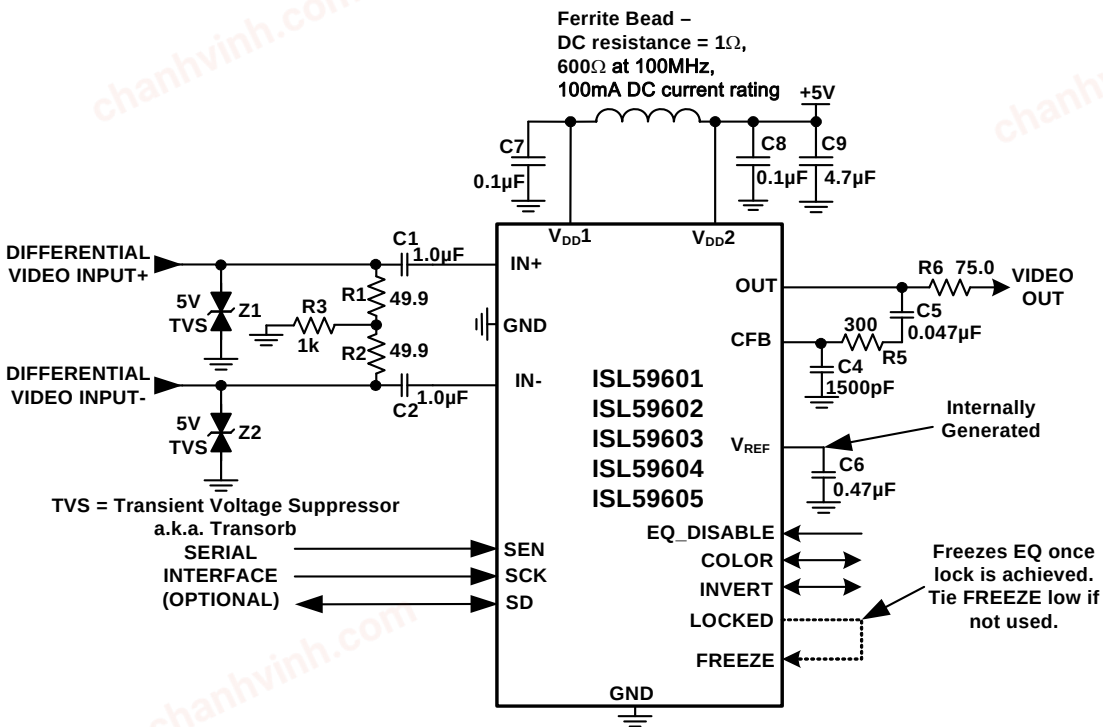


FIGURE 45. APPLICATION CIRCUIT FOR UTP CABLE

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Application Information

Unshielded Twisted Pair (UTP) App Circuit

Figure 45 shows the complete schematic for a MegaQ™ equalizer configured for unshielded twisted pair (UTP) cable. The input signal is terminated into the network formed by R1, R2, and R3. C1 and C2 AC-couple the signal into MegaQ™. To protect the front-end circuitry, 5V transorbs (Z1 and Z2) should be used instead of diodes because the signals on either differential input may swing far enough below ground to turn on a diode and distort the video.

On the output side, C5, R5, and C4 form a compensation network, while R6 provides 75Ω source-termination for the video output. MegaQ™ has an native gain of 6dB, so when VIDEO OUT is terminated into 75Ω (the input to a DVR, TV, etc.), R6 and the 75Ω terminator form a 2:1 divider, producing standard video amplitude across the 75Ω terminator.

Coax Input Circuit

Figure 46 shows the input termination recommended for coaxial cables. The differential termination resistance is now 75Ω to match the characteristic impedance of the RG-59 coax cable. C3 bypasses high-frequency noise on the *coax* ground line to system ground. This allows the coax ground to be independent of the system at low frequencies (DC to 50/60Hz) to accommodate differences in the ground potential of the remote video source(s). The coax startup network (D1, R4, C4) prevents a rare start-up condition that can occur when a high average-picture-level (e.g. white screen) video signal is present on the inputs before the power has been applied.

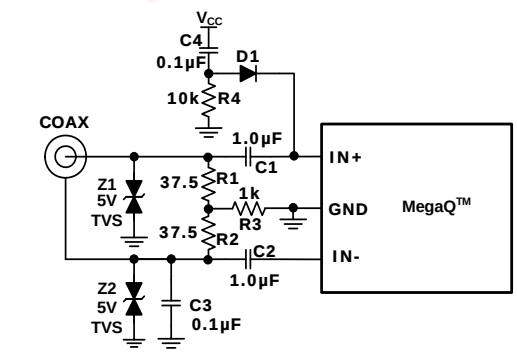


FIGURE 46. APPLICATION CIRCUIT FOR COAX CABLE

Dual UTP/Coax Input Circuit

If desired, it is also possible to support both UTP and coax cables with the same PCB layout using two SPST switches that are closed when in coax mode (Figure 47). Since UTP requires a 100Ω termination network while coax requires 75Ω, a switch to introduce a shunt 300Ω resistor when in coax mode will change the termination from 100Ω to 75Ω. A second switch is required to engage C3. The addition of the coax startup circuit (D1, R4, C4) can unbalance the capacitance of the differential pair and degrade the CMRR in UTP applications. This in turn could cause excess noise at long lengths of UTP. In UTP applications, if the output signal is too noisy at long distances, an optional capacitor Cx may be used to balance the capacitance of the differential inputs. The value of Cx should be determined by calculating how much trace capacitance is added by the coax startup circuit. A typical value for a good layout is ~5pF. Note that only coax *or* UTP should be connected at any one time - this circuit does not multiplex between them.

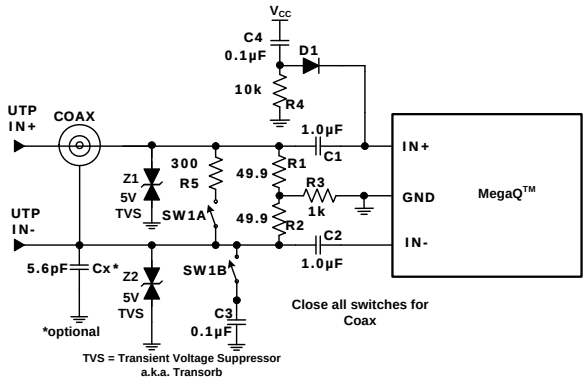


FIGURE 47. APPLICATION CIRCUIT FOR UTP/COAX CABLE

Input Multiplexing

Placing a semiconductor multiplexer in front of this part may increase high frequency attenuation and noise. However a low-capacitance mechanical relay may be acceptable. Note that changing from one channel to another in **Lock Until Reset** mode will require a reset (INVERT toggle) to trigger equalization of the new channel (see “Lock Until RESET” on page 21).

For best performance, do not multiplex the inputs to the equalizer - this can further degrade the signal. Instead, multiplex at the output after equalization has been performed.

Stand-Alone Operation and Configuration

In its default stand-alone configuration, MegaQ™ features two modes of automatic cable equalization: **Lock Until Reset** and **Continuous Update**. **Lock Until Reset** is the recommended mode for most applications.

LOCK UNTIL RESET

In the **Lock Until Reset** mode, once MegaQ™ finds the optimum equalization and the LOCKED signal goes high, the equalization is frozen and will not change until either the power is cycled or the INVERT signal is toggled, which initiates a re-equalization of the input signal. Re-equalization is usually only necessary during device/system evaluation - in normal operation MegaQ™ powers-up, acquires and equalizes the signal, and continues to equalize until/unless it is powered-down. If the signal is lost in **Lock Until Reset** mode, the LOCKED pin will not go low until/unless the device is reset by toggling the INVERT pin. A reset should only be necessary if the length or type of cable was changed without cycling power.

To enable the **Lock Until Reset** mode, tie the LOCKED output pin to the FREEZE input pin as shown in Figure 45 on page 20.

To generate a reset (and trigger a re-equalization), toggle the external INVERT pin to its opposite state for at least 1ms. Depending on the initial state of INVERT, this would be a high-low-high or low-high-low sequence.

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CONTINUOUS UPDATE

In the **Continuous Update** mode, MegaQ™ will continuously try to find the optimum equalization solution. When the equalization has settled for 100 sequential video lines with no changes, the LOCKED pin will go high. However once lock is achieved, noise and average-picture-level changes may cause the device to unlock, causing some image perturbation while MegaQ™ re-equalizes.

The **Continuous Update** mode is enabled whenever the FREEZE pin is set to a logic low (grounded).

Polarity Detection and Correction

MegaQ™ features polarity detection and correction, automatically detecting incorrectly-wired input signals and inverting the signal inside the IC as necessary. The detected polarity is indicated by the state of the INVERT pin.

The INVERT pin has 2 modes of operation. It is typically used to indicate whether or not the incoming signal is inverted (the "+" signal on the "-" input and vice-versa). The state of the invert signal is then used to tell the signal processing logic whether or not to invert the signal in the signal path.

A logic high on INVERT indicates that the positive differential input signal is on IN- (pin 5) and the negative differential input signal is on IN+ (pin 3). A logic low indicates nominal polarity.

However the unique design of the INVERT I/O pin (Figure 48) also allows MegaQ™'s internal inversion detector to be overdriven externally, forcing MegaQ™ to invert or not invert the signal regardless of the state of the inversion detection function. This is not necessary in normal operation, but it may improve performance in particularly noisy environments when the polarity of the signal is guaranteed to be correct.

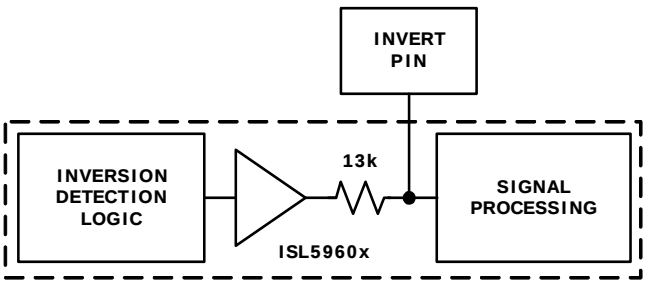


FIGURE 48. INVERT PIN STRUCTURE

The COLOR Pin

The color pin has 2 modes of operation. It is typically used to indicate whether or not the incoming signal has a colorburst or not. The state of the color signal is then used to tell the signal processing logic whether or not it can rely on the presence of a colorburst signal. A logic high indicates a color signal; a logic low indicates monochrome.

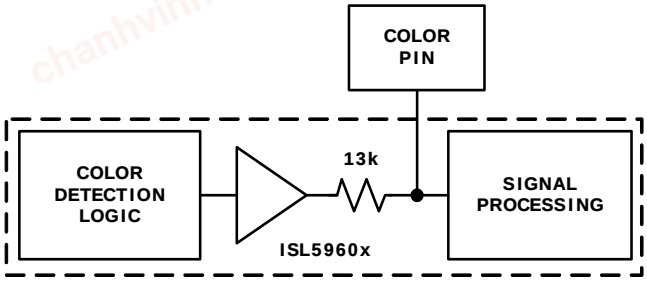


FIGURE 49. COLOR PIN STRUCTURE

However the unique design of the COLOR I/O pin (Figure 49) also allows MegaQ™'s internal color detector to be overdriven externally. This is not necessary in normal operation, but it may improve performance in particularly noisy environments when the signal type is predetermined.

Monochrome Video Signals

MegaQ™ will equalize monochrome signals to the same distance as color signals. However due to the high level of noise past ~4800 feet, the COLOR and LOCKED indicators may become invalid for monochrome signals. The device will still equalize properly if this occurs.

Security Cameras

MegaQ™ is ideal for security camera installations.

The automatic adaptive equalizer doesn't need any active silicon on the transmit side of the cable, enabling upgrading of older installations without having to touch the installed camera base, including older monochrome cameras.

MegaQ™ automatically adjusts for wiring polarity errors as well as adjusts for optimum image quality. These features eliminates the need for the installer to make any adjustments.

With an extended equalization range of 5300ft, the ISL59605 enables cameras to be placed in even more remote locations, enabling coverage of up to three square miles from a single monitoring station.

Additional Equalization Modes Available With the Serial Interface

In addition to the **Lock Until Reset** and **Continuous Update** modes, software control of MegaQ™ through the SPI interface adds a **Lock Until Signal Loss** mode and a **Manual Equalization** mode.

Note: When controlling MegaQ™ through the SPI interface, the external FREEZE pin must be tied to ground (logic low). Failure to keep FREEZE at a logic low will prevent the software controls from working properly.

All of the equalization modes are selected via the two "Locking Mode/Manual Length Enable" register bits, 0x05[1:0].

CONTINUOUS UPDATE

Continuous Update mode is entered by setting address 0x05[1:0] = 00b. **Continuous Update** behavior is the same as described in the stand-alone mode.

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LOCK UNTIL RESET

Lock Until Reset mode is entered by setting address 0x05[1:0] = 10b. **Lock Until Reset** behavior is the same as described in the stand-alone mode, with the exception of how to generate a reset.

To generate a reset via software, select **Continuous Update** mode and then return to **Lock Until Reset** mode (register 0x05[1:0] = 00b then 10b). Toggling INVERT (either the hardware pin or the software bit) will *not* cause a reset/re-equalization event.

LOCK UNTIL SIGNAL LOSS

Lock Until Signal Loss mode is entered by setting address 0x05[1:0] = 01b. **Lock Until Signal Loss** can only be enabled via the SPI interface.

In the **Lock Until Signal Loss** mode, MegaQ™ will freeze the equalization once the LOCKED pin goes high (in the same way as **Lock Until Reset**). Unlike the "Settled" state in the **Continuous Update** mode, only a signal loss lasting more than 1ms (typical) will cause MegaQ™ to re-equalize the signal when it returns. In this sense, the **Lock Until Signal Loss** mode can be considered as halfway between the **Continuous Update** mode and the **Lock Until Reset** mode. The **Lock Until Signal Loss** mode is useful, for example, when testing or demonstrating a system by plugging in multiple different length cables - it eliminates the need to also generate a reset. To prevent potentially undesired re-equalization, signal losses lasting less than 1ms (typical) do not trigger a re-equalization.

MANUAL LENGTH

Manual Length mode is entered by setting address 0x05[1:0] = 11b. **Manual Length** mode allows the forcing of specific cable lengths, cable type, DC gains, etc. (see the Register Listing on the next page). The "Cable Type" bit (0x05 [4]) allows selection between the two most common cable types for security video: Cat 5/6 or steel core RG-59 coaxial. However since many of MegaQ™'s automatic functions and adjustments are disabled in **Manual Length** mode, performance is almost always worse than what is achieved in any of the automatic modes. For example, automatic polarity correction is disabled so the polarity must be manually set using the INVERT bit. There is no practical reason to ever use **Manual Length** mode in normal operation.

Serial Interface Protocol

While MegaQ™ is designed to work as a stand-alone equalizer, it does have a serial interface that can be used to control it and monitor its state.

The serial interface is used to read and write the configuration registers. It uses three signals (SCK, SD, and SEN) for programming. The serial clock can operate up to 5MHz (5Mbits/s). The "Serial Timing Diagram" on page 8 shows the timing of serial I/O.

A transaction begins when the host microcontroller takes SEN (serial enable) high. The first 8 bits on the SD (serial data) pin are latched by MegaQ™ on the rising edge of SCK (serial clock) to form the address byte. The MSB of the address byte indicates whether the operation is a read (1) or a write (0), and the next seven bits indicate which register is to be read from or written to. Each read and write operation consists of 16 bits: 8 bits for an address byte followed by 8 bits of data. See the "Serial Timing Diagram" on page 8 for more details on using the SPI interface.

TABLE 2. ADDRESS BYTE FORMAT

0 = Write 1 = Read	A6	A5	A4	A3	A2	A1	A0
(MSB)							(LSB)

WRITE OPERATION

After the address byte is clocked in, the next 8 bits should contain the data to be sent to the register identified in the address byte.

READ OPERATION

After the rising edge of the 8th clock after the address byte is clocked in, the microcontroller should tristate the SD line so MegaQ™ can begin to output data on the SD pin (from the register identified in the address byte), beginning on the 9th rising edge of SCK. The data should be latched on the *falling* edge of SCK to allow enough time for the data to settle. See ""Serial Timing Diagram" on page 8 for more details on how to read from the registers.

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Register Listing

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x00	Device ID (0x31)	3:0	Device Revision	0 = initial silicon, 1 = first revision, etc.
		7:4	Device ID	0x3
0x01	Signal Status (N/A)	0	Signal Present	0: A signal is not present at the input 1: A signal is present at the input
		1	DLL Locked	0: DLL is not locked 1: DLL is locked
		2	Signal Polarity	0: Inverted Polarity 1: Nominal Polarity This bit is only valid if the INVERT pin is connected as an output. If INVERT is overdriven, this value may not reflect the polarity of the input signal.
		3	Color Detected	0: Signal is monochrome 1: Signal has a colorburst
		4	Signal Overloaded	0: Signal (if present) is within normal range 1: Signal appears to be overloaded
		5	Settled	0: EQ is not settled, though DLL may be locked. 1: EQ has stabilized and equalization achieved.
0x02	Manual Length(0x00)	5:0	Manual Length	Manual Length Control; 0x0 through 0x3F, 84 feet per bit. 0x0: 0 feet. 0x3F: 5300 feet (Cat 5 mode) This register sets the EQ setting when MegaQ™ is in manual length mode (reg 0x05[1:0] = 11). Note that the length in this register is for Cat 5 cable when “Cable Type” (reg 0x05[4]) equals 0. When “Cable Type” is set to 1 (coax mode), then the length is for steel core coax. In coax mode, the maximum length is 0x14 (~1200 feet) and setting the register higher than this value does not provide any increase in equalization.

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Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x03	Manual DC Gain (0x20)	5:0	Manual DC Gain	0x00: Maximum DC Gain (+3dB) 0x20: Mid-Scale 0dB 0x3F: Minimum DC Gain (-3dB) This register sets the DC Gain when the device is in manual length mode (reg 0x05[1:0] = 11).
0x04	Pin Overrides (0x00)	0	Freeze Select	0: Use value of FREEZE pin. 1: Use value in “Freeze Value” bit
		1	Freeze Value	If Freeze Select = 1, then: 0: Equalization is not frozen 1: Equalization is frozen at current setting. If Freeze Select = 0, then this bit is ignored.
		2	Eq-Disable Select	0: Use value of EQ_DISABLE pin. 1: Use value in “Eq-Disable Value” bit
		3	Eq-Disable Value	If Eq-Disable Select = 1, then: 0: Equalizer is enabled 1: Equalizer is disabled (allows data to be sent upstream over cable pair connected to inputs) If Eq-Disable Select = 0, then this bit is ignored.
		4	Color Select	0: Use value of COLOR pin 1: Use value in “Color Value” bit
		5	Color Value	If Color Select = 1, then 0: Monochrome Mode 1: Color Mode If Color Select = 0, then this bit is ignored.
		6	Invert Select	0: Use value of INVERT pin. 1: Use value in “Invert Value” bit
		7	Invert Value	If Invert Select = 1, then 0: Incoming signal is not inverted 1: Incoming signal is inverted If Invert Select = 0, then this bit is ignored.
0x05	Equalization Control (0x00)	1:0	Locking Mode/Manual Length Enable	00 = **Continuous Monitoring** 01 = **Lock Until Signal Loss*** 10 = **Lock Until Reset** 11 = **Manual Length**** *Signal must be missing for at least 1ms in order to trigger a re-equalization. ** In **Manual Length** mode the polarity corrector is disabled and the polarity must be set using the INVERT bit or pin. Note: The FREEZE pin must be tied to ground/a logic low for this function to work correctly.
		3:2	Noise Filter	00: No Noise Filtering 01: Min Noise Filtering 10 or 11: Max Noise Filtering Note: Noise Filtering is only available on the ISL59605
		4	Cable Type	0: CAT5/6 Mode 1: Steel Core Coax Mode This bit is ignored in all modes except **Manual Length** (reg 0x05[1:0] = 11). Set to 1 if using copper-coated steel-core coaxial cable and you are in **Manual Length**.

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Bypassing and Layout Considerations

MegaQ™ requires a dedicated ground plane in order to function properly. For 2-layer boards, pour a quarter-inch ground plane extending around the device on both the top and bottom layers. Ensure that the ground plane on the bottom layer is a **solid** plane with no traces cutting through it. Bypass capacitors must be placed as close as possible to the device in order to ensure good performance at longer lengths of equalization. Ensure that the ground connections for the bypass capacitors connect **directly** to the same uniform ground plane described previously.

General PowerPAD Design Considerations

The thermal pad must be connected to the ground plane for heat dissipation. Figure 50 is an example of how to use vias to remove heat from the IC.

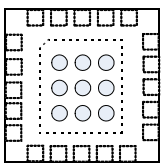


FIGURE 50. PCB VIA PATTERN

The thermal pad is electrically connected to GND through the high resistance IC substrate. We recommend you fill the thermal pad area with vias. The via array should be centered in the thermal pad and placed such that the center on center spacing is 3x the via radius. Vias should be small, but large enough to allow solder wicking during reflow. Connect all vias to ground. It is important the vias have a low thermal resistance for efficient heat transfer. Do not use “thermal relief” patterns. It is important to have a solid connection of the plated-through hole to each plane.

Power Dissipation

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing use Equation 2:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L} \quad \text{(EQ. 2)}$$

for sinking use Equation 3:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT} - V_S) \times I_{LOAD} \quad \text{(EQ. 3)}$$

Where:

V_S = Supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

I_{LOAD} = Load current

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
August 6, 2012	FN6739.2	Typical applications circuit diagrams and corresponding text updated to reflect more optimal setup for the device.
February 4, 2011		Converted to Updated Intersil Template page 1 - Updated Related Literature by changing titles to match released application notes Added standard Reference to MIN and MAX columns and Note to Electrical Specifications and Serial Timing Spec Tables: "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." page 4 - Updated ordering information by naming Evaluation boards to match Intrepid. CHANGED I2C to SPI as follows: page 22 first paragraph and 2nd Note paragraph under "Additional Equalization Modes Available with the Serial Interface" section from "...MegaQ through the I2C interface..." to "...MegaQ through the SPI interface..." page 23 "Under Lock Until Signal Loss" section 1st paragraph last sentence "...via the I2C interface." To: "...via the SPI interface."
November 19, 2010	FN6739.1	Modified both "Typical Application" drawings on page 1 to reflect recommended new termination network. Modified Figures 45, 46, and 47 to reflect recommended new termination network. Modified text in "UTP Application Circuit" and "Coax Input Circuit" sections to mention changes to termination network. Added "Dual UTP/Coax Input Circuit" heading
October 21, 2010		Added superscript TM to all MegaQ and trademark statement, pg 1. Added ±8kV ESD protection to the Features list Pg24, Register 0x04 of the Register Listing: Fixed Select and Value locations (were swapped for each pin). Last two rows should say "Invert", not "INVERT", EXCEPT for "Use the value of INVERT pin Pg25, address 0x05 of Register listing, 3:2 Noise filter row, change from: 00: No Noise Filtering 01: Min Noise Filtering 1X: Max Noise Filtering to: 00: No Noise Filtering 01: Min Noise Filtering 10 or 11: Max Noise Filtering Note: Noise Filtering is only available on the ISL59605
October 8, 2010	FN6739.0	Initial Release.

Products

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For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL59601, ISL59602, ISL59603, ISL59604, ISL59605.

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

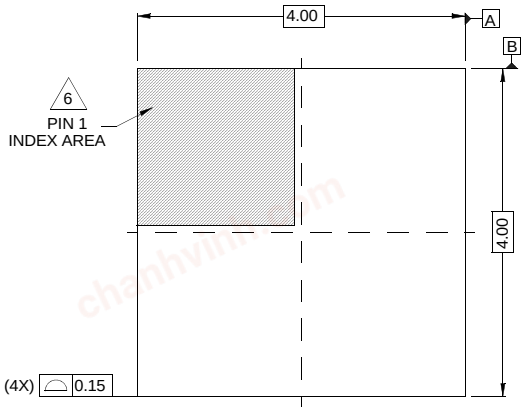
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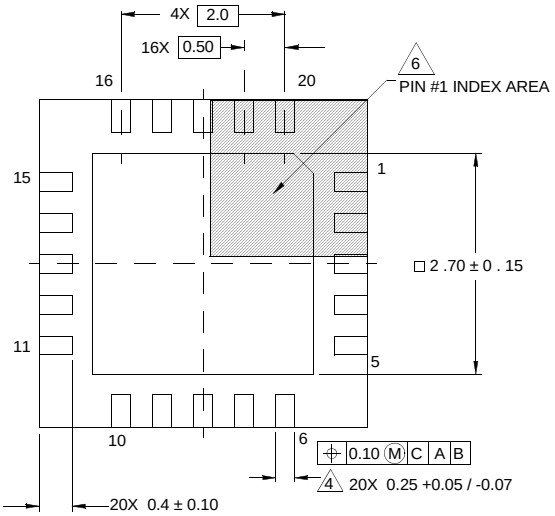
Package Outline Drawing

L20.4x4C

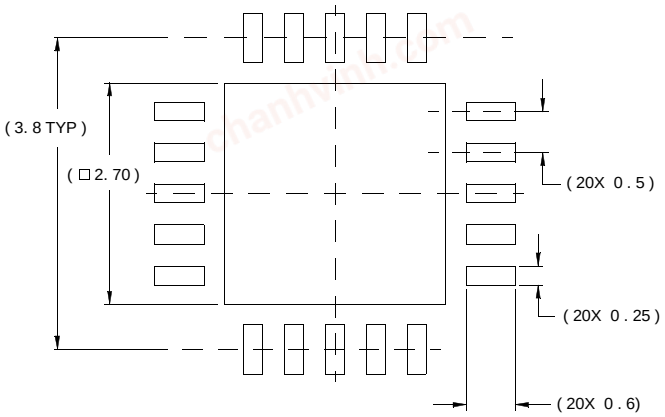
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 11/06



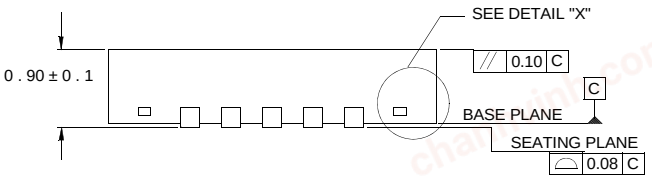
TOP VIEW



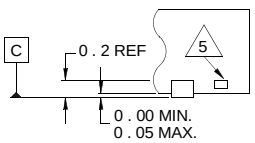
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.