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DATASHEET

ISL43240

Low-Voltage, Single and Dual Supply, Quad SPDT, High Performance Analog Switch

FN6036
Rev 3.00
Dec 15, 2014

The Intersil ISL43240 device is a CMOS, precision, quad SPDT analog switch designed to operate from a single +2V to +12V supply or from a ±2V to ±6V supply. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (5µW), low leakage currents (5nA max), and fast switching speeds (t_{ON} = 52ns, t_{OFF} = 40ns). A 5Ω maximum r_{ON} flatness ensures signal fidelity, while channel-to-channel mismatch is guaranteed to be less than 2Ω.

The ISL43240 is a quad single-pole/double-throw (SPDT) device and can be used as a quad SPDT, a quad 2:1 multiplexer, a single 4:1 multiplexer or a dual 2-channel differential multiplexer.

Table 1 summarizes the performance of this family.

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	QUAD SPDT
±4.5V r_{ON}	18Ω
±4.5V t_{ON}/t_{OFF}	52ns/40ns
10.8V r_{ON}	14Ω
10.8V t_{ON}/t_{OFF}	40ns/27ns
4.5V r_{ON}	30Ω
4.5V t_{ON}/t_{OFF}	64ns/29ns
3V r_{ON}	51Ω
3V t_{ON}/t_{OFF}	120ns/50ns
Packages	20 Ld SSOP, 20 Ld QFN 4x4

Related Literature

- TB363, "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- AN557, "Recommended Test Procedures for Analog Switches"

Features

- Fully specified for 10% tolerances at V_S = ±5V and V+ = 12V, 5V and 3.3V
- Four separately controlled SPDT switches
- ON-resistance (r_{ON}) 18Ω
- r_{ON} matching between channels . . . . . <1Ω
- Low charge injection . . . . . 5pC (Max)
- Low power consumption (P_D) . . . . . <5µW
- Low off leakage current (max at +85°C) 2.5nA
- Fast switching action
  - t_{ON} 52ns
  - t_{OFF} 40ns
- Guaranteed break-before-make
- Minimum 2000V ESD protection per Method 3015.7
- TTL, CMOS compatible
- Pb-free (RoHS compliant)

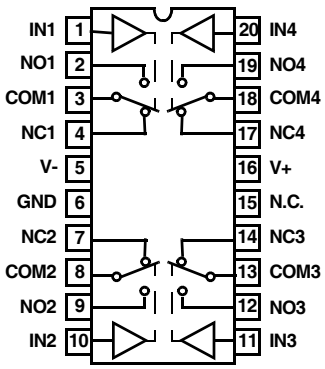
Applications

- Battery powered, handheld, and portable equipment
  - Barcode scanners
  - Laptops, notebooks, palmtops
- Communications systems
  - Radios
  - XDSL and PBX/PABX
  - RF "Tee" switches
  - Base stations
- Test equipment
  - Medical ultrasound
  - Electrocardiograph
  - ATE
- Audio and video switching
- General purpose circuits
  - +3V/+5V DACs and ADCs
  - Digital filters
  - Operational amplifier gain switching networks
  - High frequency analog switching
  - High speed multiplexing

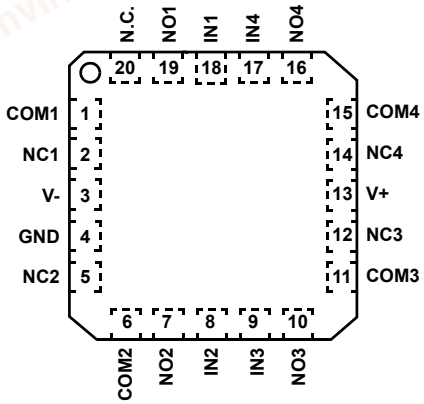
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Pin Configurations (Note 1)

ISL43240 (SSOP)
TOP VIEW



ISL43240 (QFN)
TOP VIEW



NOTE:
1. Switches shown for Logic “0” input.

Truth Table

LOGIC	ISL43240 NO SW	ISL43240 NC SW
0	OFF	ON
1	ON	OFF

NOTE: Logic “0” ≤ 0.8V. Logic “1” ≥2.4V.

Pin Descriptions

PIN	FUNCTION
V+	Positive Power Supply Input
V-	Negative Power Supply Input. Connect to GND for Single Supply Configurations.
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Internal Connection

Ordering Information

PART NO. (Notes 2, 3, 4)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL43240IAZ	43240 IAZ	-40 to 85	20 Ld SSOP	M20.209
ISL43240IRZ	43240IRZ	-40 to 85	20 Ld QFN	L20.4x4

NOTES:
2. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see product information page for ISL43240. For more information on MSL, please see tech brief TB363.

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Absolute Maximum Ratings

V+ to V- . . . . . -0.3 to15V
V+ to GND . . . . . -0.3 to15V
V- to GND . . . . . -15 to 0.3V
All Other Pins (Note 5) . . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
Continuous Current (Any Terminal) 30mA
Peak Current, IN, NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 100mA
ESD Rating (Per MIL-STD-883 Method 3015) . . . . . >2kV

Operating Conditions

Temperature Range
ISL43240IX . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
20 Ld SSOP Package (Note 6)	150
20 Ld QFN Package (Note 7)	75

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Moisture Sensitivity (See TB363)
All Packages . . . . . Level 1
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(SSOP - Lead Tips Only)
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
6. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications ±5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 7), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	V-	-	V+	V
ON Resistance, r_{ON}	V_S = ±4.5V, I_{COM} = 10mA, V_{NO} or V_{NC} = ±3.5V, See Figure 5	25	-	18	25	Ω
		Full	-	-	30	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_S = ±4.5V, I_{COM} = 10mA, V_{NO} or V_{NC} = ±3V	25	-	0.5	2	Ω
		Full	-	-	4	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V_S = ±4.5V, I_{COM} = 10mA, V_{NO} or V_{NC} = 0V, ±3V, Note 10	25	-	-	5	Ω
		Full	-	-	5	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V, Note 9	25	-0.2	-	0.2	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V, Note 9	25	-0.4	-	0.4	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.4	1.6	-	V
Input Voltage Low, V_{INL}		Full	-	1.5	0.8	V
Input Current, I_{INH}, I_{INL}	V_S = ±5.5V, V_{IN} = 0V or V+	Full	-1	-	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	52	65	ns
		Full	-	-	75	ns
Turn-OFF Time, t_{OFF}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	40	50	ns
		Full	-	-	55	ns
Break-before-make Time Delay, t_D	V_S = ±5.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 3	Full	10	19	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	-	5	pC
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	30	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$, See Figures 4 and 6	25	-	71	-	dB
Crosstalk, Note 11		25	-	-92	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	59	-	dB

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Electrical Specifications ±5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 7), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	±2	-	±6	V
Positive Supply Current, I+	V_S = ±5.5V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.01	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.01	1	µA
		Full	-1	-	1	µA

NOTES:

8. V_{IN} = Input voltage to perform proper function.
9. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
10. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at +25°C.
11. Flatness is defined as the delta between the maximum and minimum r_{ON} values over the specified voltage range.
12. Between any two switches.

Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 7), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-resistance, r_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V, See Figure 5	25	-	30	40	Ω
		Full	-	-	50	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V	25	-	0.5	3	Ω
		Full	-	-	4	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 5.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V, Note 10	25	-	4.4	6	Ω
		Full	-	-	8	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V, Note 9	25	-0.2	-	0.2	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 1V, 4.5V Note 9	25	-0.4	-	0.4	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.4	1.5	-	V
Input Voltage Low, V_{INL}		Full	-	1.4	0.8	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	Full	-1	-	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	64	80	ns
		Full	-	-	90	ns
Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	29	40	ns
		Full	-	-	45	ns
Break-before-make Time Delay, t_D	V+ = 5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 3	Full	15	39	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	1.2	2	pC
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	30	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$, See Figures 4 and 6	25	-	71	-	dB
Crosstalk, Note 11		25	-	-92	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	59	-	dB

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Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 7), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 5.5V, V- = 0V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.01	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.01	1	µA
		Full	-1	-	1	µA

Electrical Specifications 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 7), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, r_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V, See Figure 5	25	-	51	60	Ω
		Full	-	-	70	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V	25	-	0.5	3	Ω
		Full	-	-	4	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 0.5V, 1.5V, Note 10	25	-	12	17	Ω
		Full	-	-	17	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 1V, 3V, V_{NO} or V_{NC} = 3V, 1V, Note 9	25	-0.2	-	0.2	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 1V, 3V, V_{NO} or V_{NC} = 1V, 3V, Note 9	25	-0.4	-	0.4	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.4	1.0	-	V
Input Voltage Low, V_{INL}		Full	-	0.9	0.8	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	-1	-	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	120	138	ns
		Full	-	-	160	ns
Turn-OFF Time, t_{OFF}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	50	60	ns
		Full	-	-	65	ns
Break-before-make Time Delay, t_D	V+ = 3.6V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 3	Full	30	60	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	1	2	pC
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	30	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$, See Figures 4 and 6	25	-	71	-	dB
Crosstalk, Note 11		25	-	-92	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	59	-	dB
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V- = 0V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.01	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.01	1	µA
		Full	-1	-	1	µA

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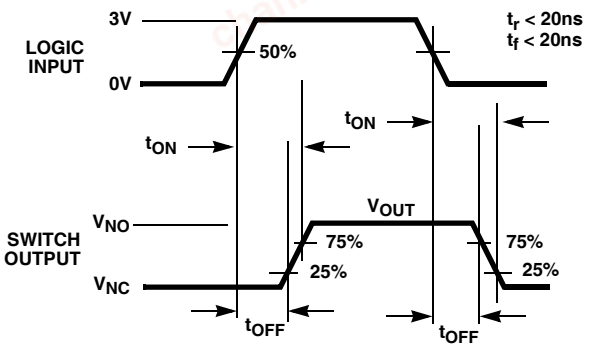
Electrical Specifications 12V Supply

Test Conditions: V+ = +10.8V to +13.2V, V- = GND = 0V, V_{INH} = 3.0V, V_{INL} = 0.8V (Note 7), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-resistance, r_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V, See Figure 5	25	-	14	20	Ω
		Full	-	-	30	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V	25	-	0.3	2	Ω
		Full	-	-	4	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 13.2V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, 6V, 9V, Note 10	25	-	1.7	2	Ω
		Full	-	-	3	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 13V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 12V, 1V, Note 9	25	-0.2	-	0.2	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 13V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 1V, 12V Note 9	25	-0.4	-	0.4	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	3.0	2.8	-	V
Input Voltage Low, V_{INL}		Full	-	2.2	0.8	V
Input Current, I_{INH}, I_{INL}	V+ = 13.2V, V_{IN} = 0V or V+	Full	-1	-	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	40	50	ns
		Full	-	-	83	ns
Turn-OFF Time, t_{OFF}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	27	35	ns
		Full	-	-	40	ns
Break-before-make Time Delay, t_D	V+ = 13.2V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 3	Full	5	20	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	12	14	pC
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	30	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$, See Figures 4 and 6	25	-	71	-	dB
Crosstalk, Note 11		25	-	-92	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	59	-	dB
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.01	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.01	1	µA
		Full	-1	-	1	µA

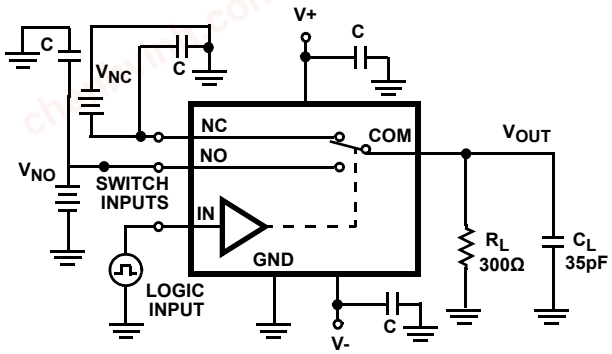
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Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

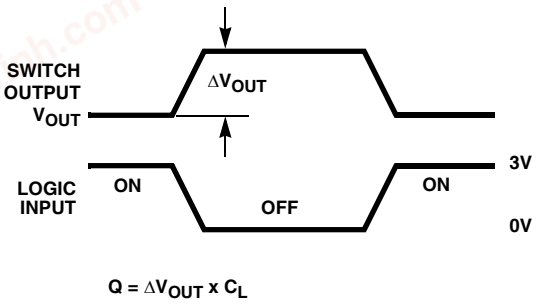


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

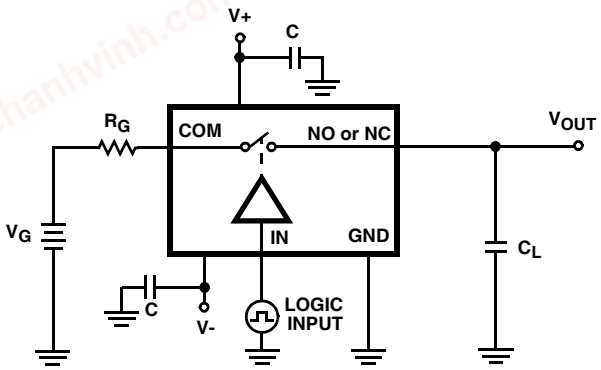
FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

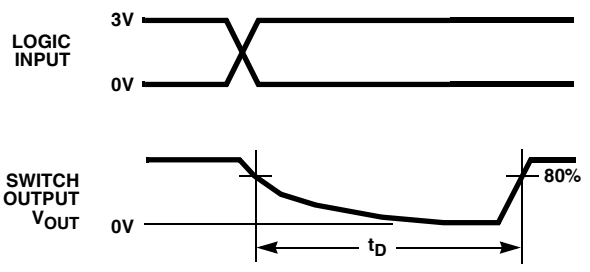
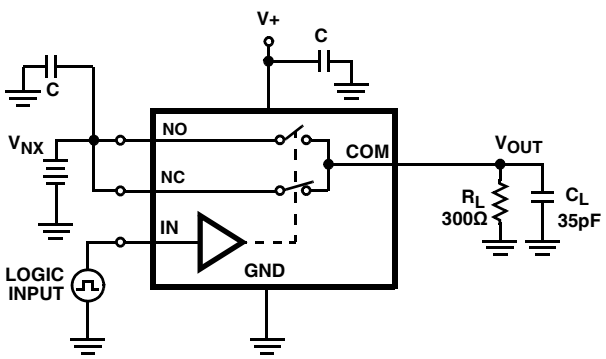


FIGURE 3A. MEASUREMENT POINTS



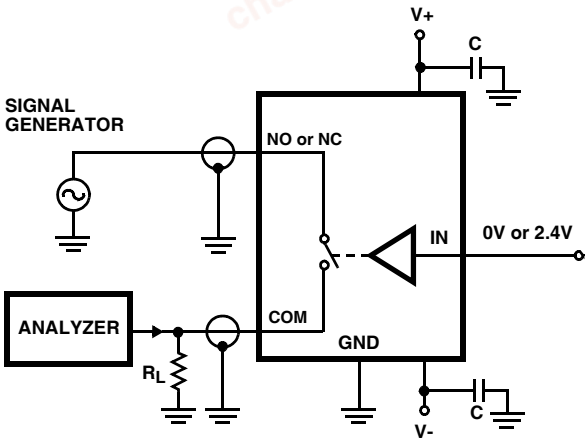
Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

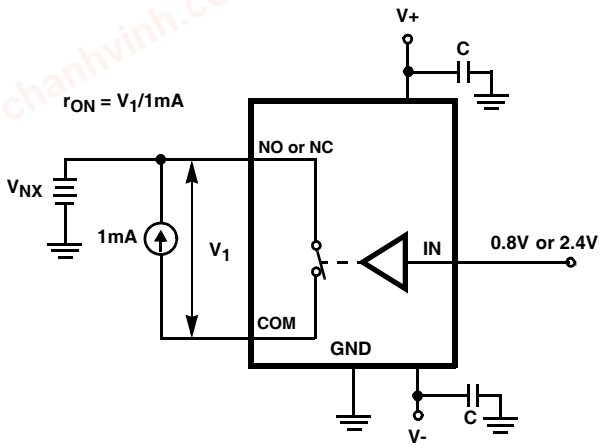
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Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 4. OFF ISOLATION TEST CIRCUIT



Repeat test for all switches.

FIGURE 5. R_{ON} TEST CIRCUIT

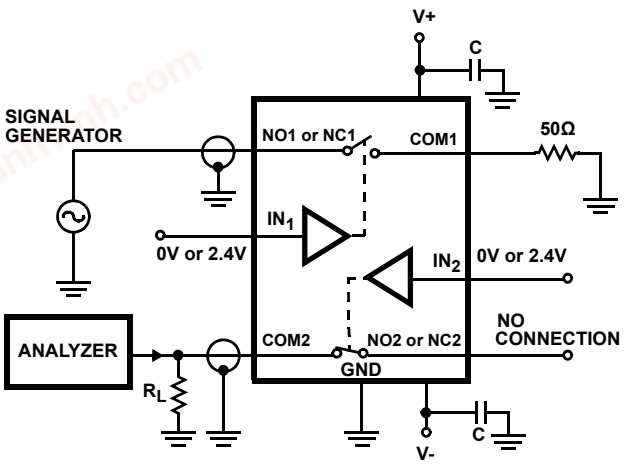


FIGURE 6. CROSSTALK TEST CIRCUIT

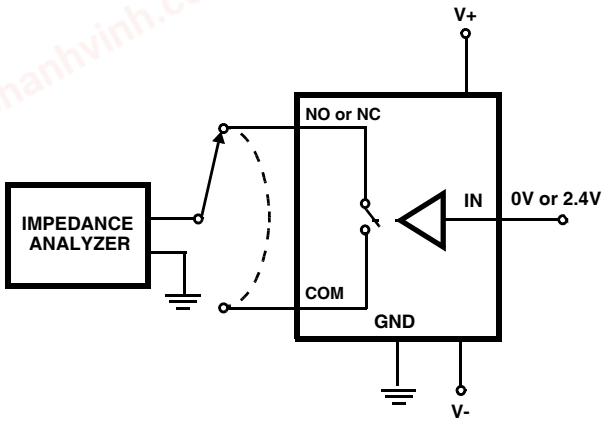


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43240 quad analog switches offer precise switching capability from a bipolar ±2V to ±6V or a single 2V to 12V supply with low on-resistance (18Ω) and high speed operation (t_{ON} = 52ns, t_{OFF} = 40ns). The devices are especially well suited for portable battery powered equipment thanks to the low operating supply voltage (2V), low power consumption (5µW), low leakage currents (5nA max). High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 8). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above V-.

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The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

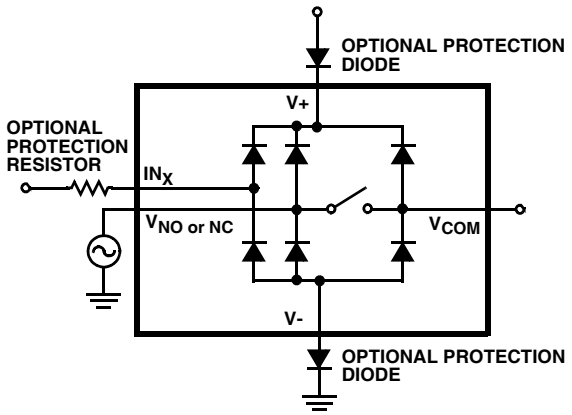


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43240 construction is typical of most CMOS analog switches, in that they have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL43240 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies (±6V or 12V single supply), as well as room for overshoot and noise spikes.

This family of switches performs equally well when operated with bipolar or single voltage supplies. The minimum recommended supply voltage is 2V or ±2V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables starting on page 3 and Typical Performance curves on page 10 for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

Logic-Level Thresholds

V+ and GND power the internal logic stages, so V- has no affect on logic thresholds. This switch family is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.5V to 10V (see Figure 17). At 12V the V_{IH} level is about 2.8V. For best results with a 12V supply, use a logic family that provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails (see Figure 18). Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL43240 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 3V logic (0V to 3V) while operating with dual or single 5V supplies the device draws only 10µA of current (see Figure 18 for V_{IN} = 3V). Similar devices of competitors can draw 8 times this amount of current.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 200MHz (see Figure 19). Figure 19 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An off switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed-through from a switch's input to its output. Off Isolation is the resistance to this feed-through, while Crosstalk indicates the amount of feed-through from one switch to another. Figure 20 details the high Off Isolation and Crosstalk rejection provided by this switch. At 10MHz, off isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

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Typical Performance Curves $T_A = 25°C$, Unless Otherwise Specified

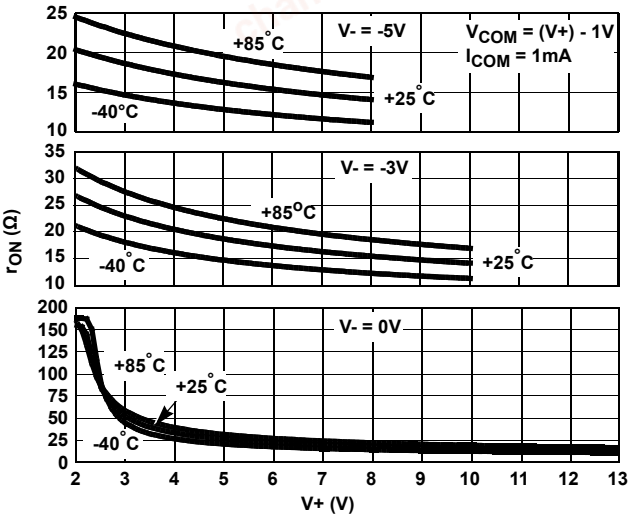


FIGURE 9. ON RESISTANCE vs POSITIVE SUPPLY VOLTAGE

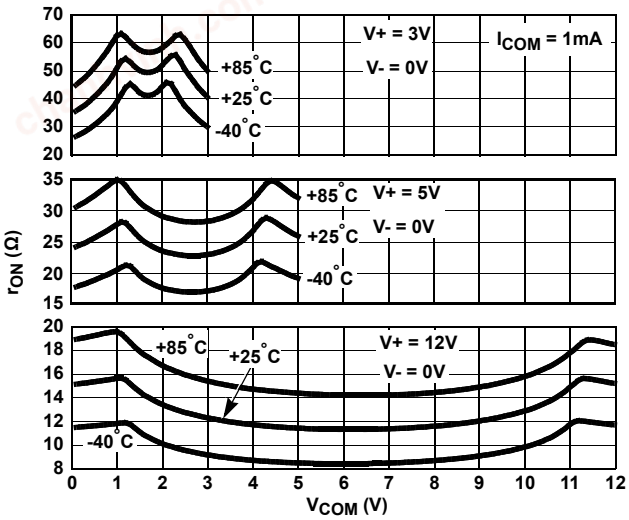


FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

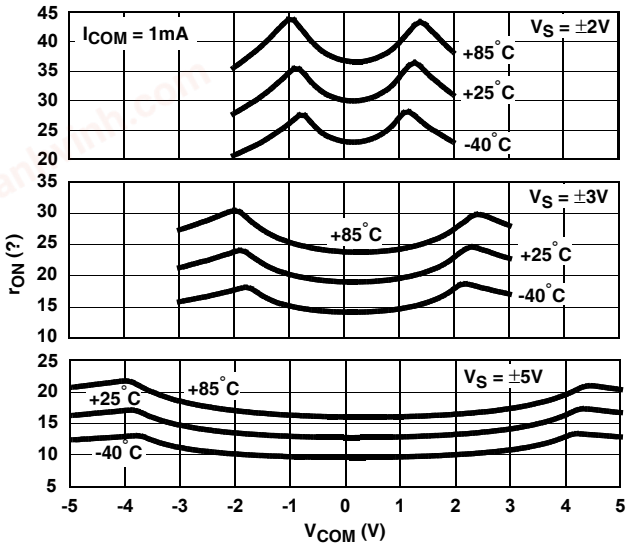


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

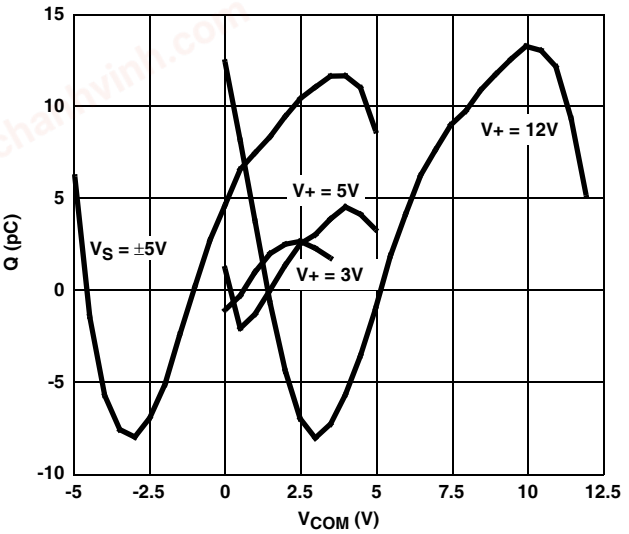


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

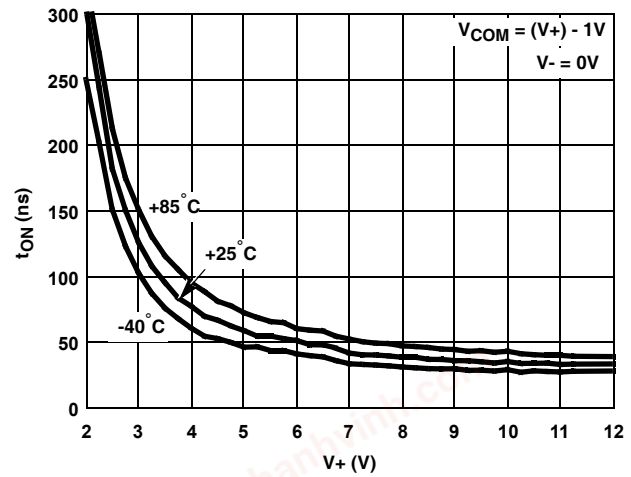


FIGURE 13. TURN - ON TIME vs POSITIVE SUPPLY VOLTAGE

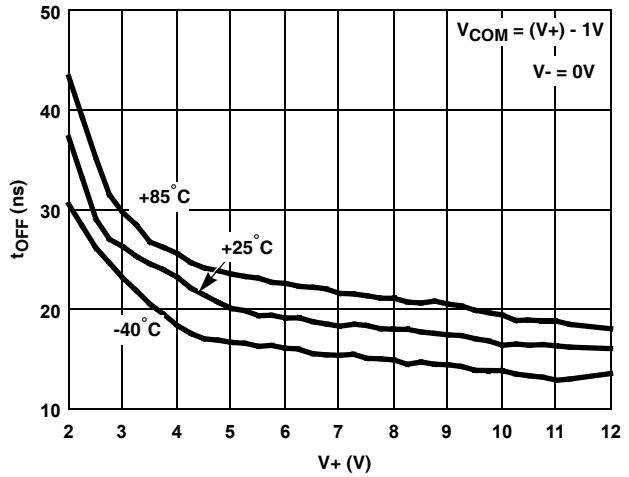


FIGURE 14. TURN - OFF TIME vs POSITIVE SUPPLY VOLTAGE

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Typical Performance Curves $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

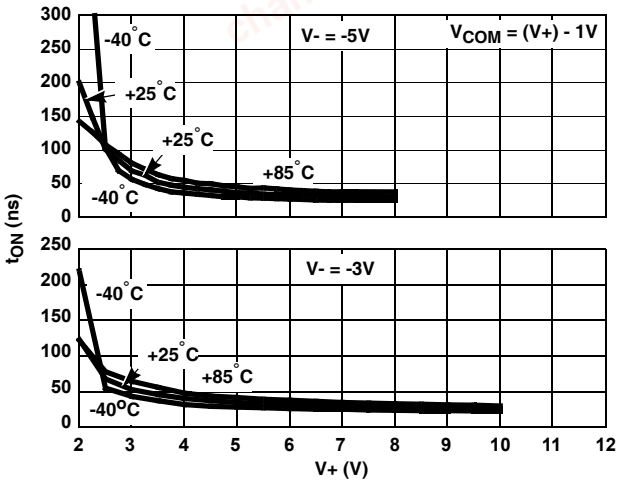


FIGURE 15. TURN - ON TIME vs POSITIVE SUPPLY VOLTAGE

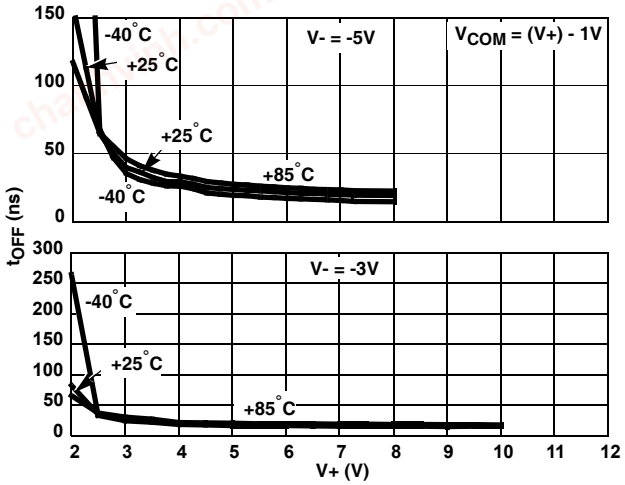


FIGURE 16. TURN - OFF TIME vs POSITIVE SUPPLY VOLTAGE

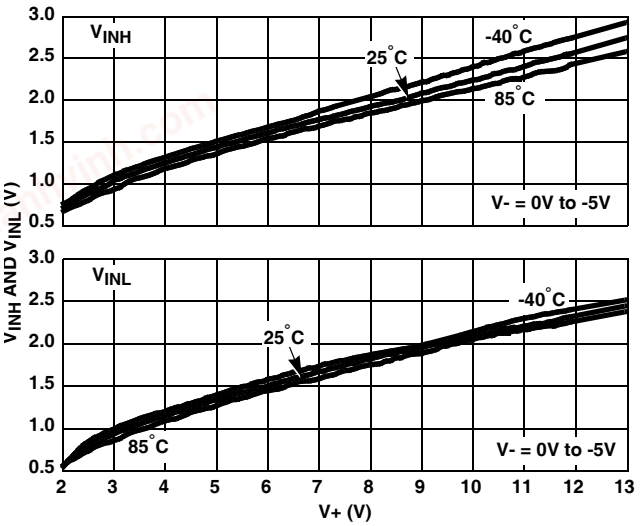


FIGURE 17. DIGITAL SWITCHING POINT vs POSITIVE SUPPLY VOLTAGE

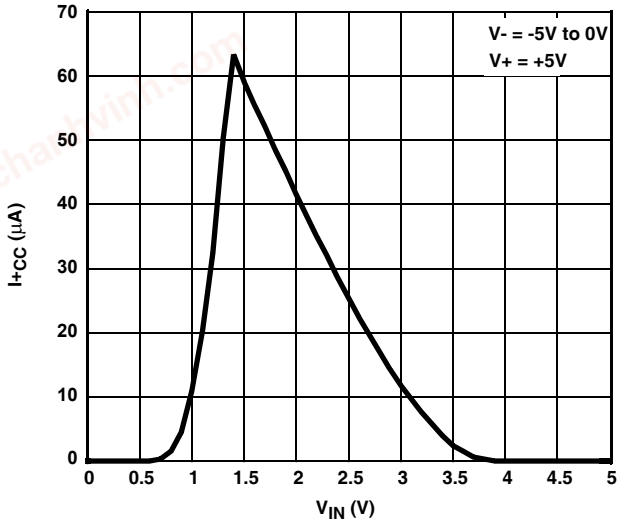


FIGURE 18. POSITIVE SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE

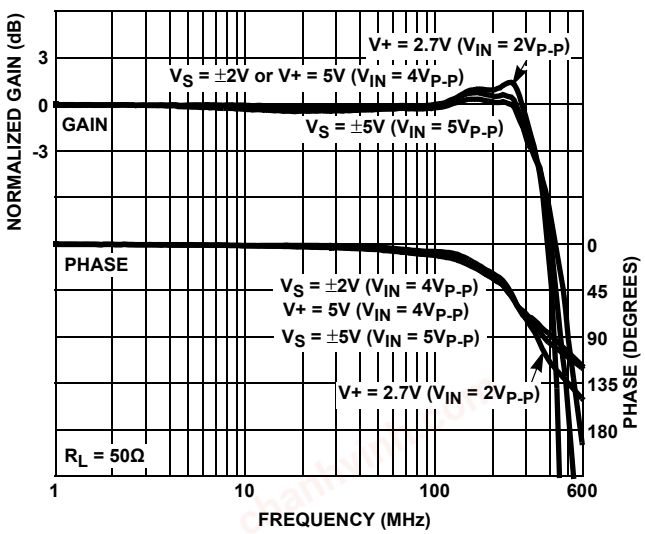


FIGURE 19. FREQUENCY RESPONSE

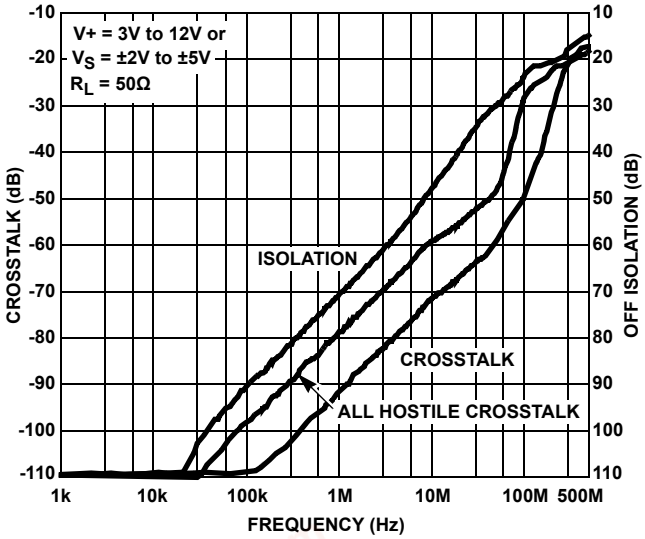


FIGURE 20. CROSSTALK AND OFF ISOLATION

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Typical Performance Curves T_A = 25°C, Unless Otherwise Specified (Continued)

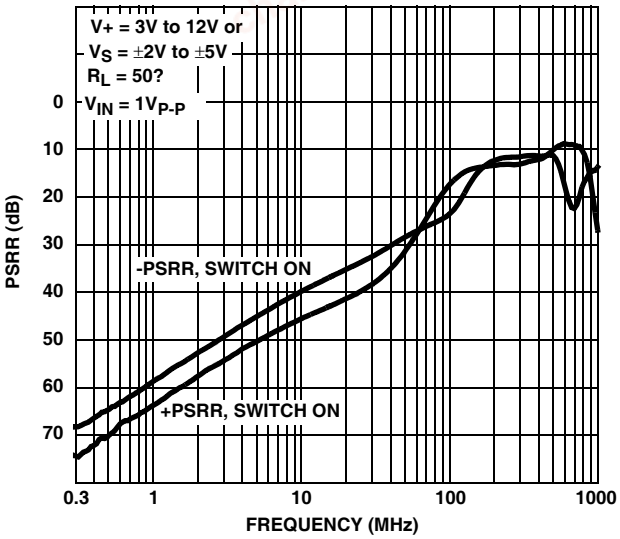


FIGURE 21. ±PSRR vs FREQUENCY

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

V-

TRANSISTOR COUNT:

ISL43240: 418

PROCESS:

Si Gate CMOS

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 15, 2014	FN6036.3	Made updates throughout datasheet to Intersil Standard. On page 2, updated the Ordering Information table to standard. -Removed Obsolete products (ISL43240IA, ISL43240IA, ISL43240IR and ISL43240IR-T). -Added Note 2, “Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.” -Added Note 4, “For Moisture Sensitivity Level (MSL), please see product information page for ISL43240. For more information on MSL, please see tech brief TB363” Added Revision History and About Intersil sections. Updated the L20.4x4 Package Outline Drawing on page 15 to the latest revision: Rev 1 to Rev 2 change: Change to Issue to "I" Change A1 to add 0.02 to Nominal Change A2 to add 0.65 to Nominal Change "b" Nominal to 0.25 Change D2 and E2, min to 1.95, nominal to 2.10 Change "L" min to 0.35, nominal to 0.60, max to 0.75 delete "L1" line and note 10 Change "k" min to 0.20 Remove the "5" from the "Ne" line under the min column Change Rev to Rev. 2 11/04 Rev 2 to Rev 3 change: Updated to new POD format by removing table listing dimensions and moving dimensions onto drawing. Added Typical Recommended Land Pattern.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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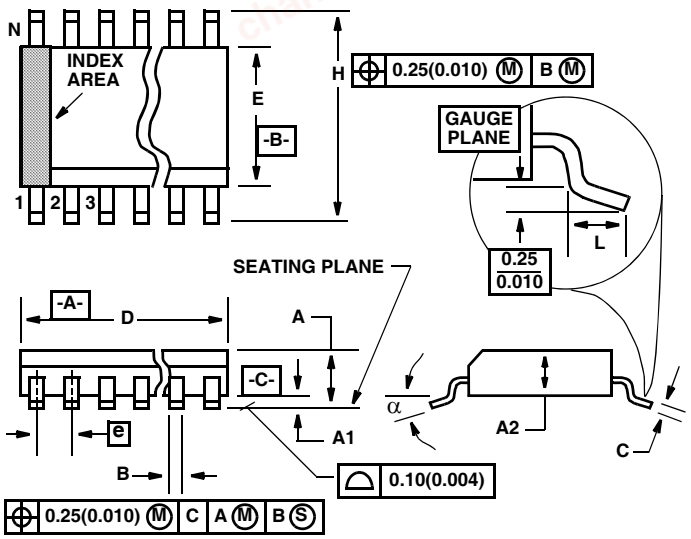
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Shrink Small Outline Plastic Packages (SSOP)



M20.209 (JEDEC MO-150-AE ISSUE B)
20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.068	0.078	1.73	1.99	
A1	0.002	0.008’	0.05	0.21	
A2	0.066	0.070’	1.68	1.78	
B	0.010’	0.015	0.25	0.38	9
C	0.004	0.008	0.09	0.20’	
D	0.278	0.289	7.07	7.33	3
E	0.205	0.212	5.20’	5.38	4
e	0.026 BSC		0.65 BSC		
H	0.301	0.311	7.65	7.90’	
L	0.025	0.037	0.63	0.95	6
N	20		20		7
α	0 deg.	8 deg.	0 deg.	8 deg.	

Rev. 3 11/02

NOTES:

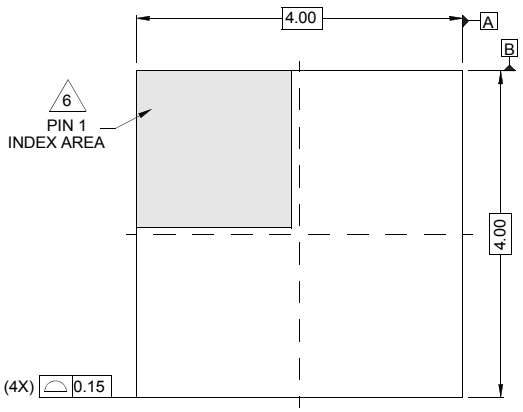
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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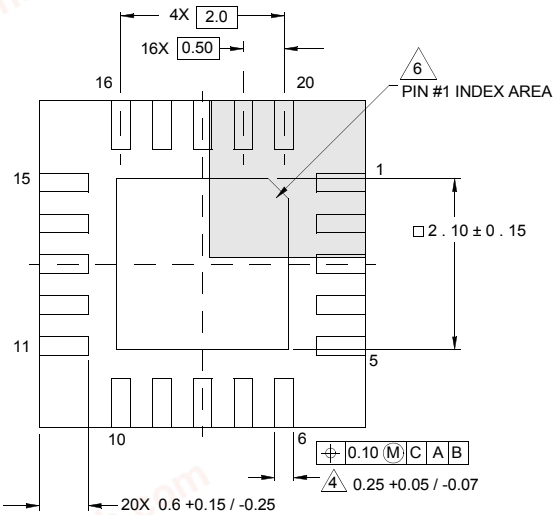
Package Outline Drawing

L20.4x4

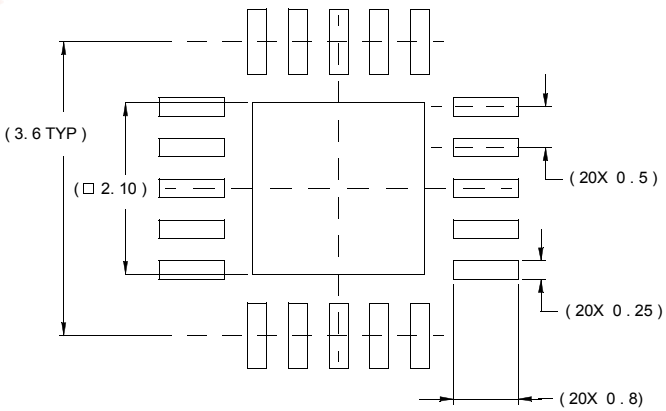
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 11/06



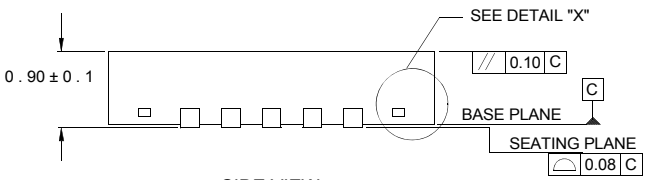
TOP VIEW



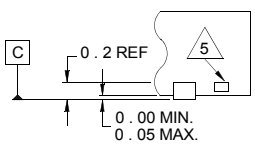
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.