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ISL3280E, ISL3281E, ISL3282E, ISL3283E, ISL3284E

±16.5kV ESD Protected, +125°C, 3.0V to 5.5V, SOT-23/TDFN Packaged, 20Mbps, Full Fail-safe, Low Power, RS-485/RS-422 Receivers

FN6543
Rev 4.01
Mar 31, 2022

The ISL3280E, ISL3281E, ISL3282E, ISL3283E, and ISL3284E are ±16.5kV IEC61000 ESD Protected, 3.0V to 5.5V powered, single receivers that meet both the RS-485 and RS-422 standards for balanced communication. These receivers have very low bus currents (+125µA/-100µA), so they present a true "1/8 unit load" to the RS-485 bus. This allows up to 256 receivers on the network without violating the RS-485 specification's 32 unit load maximum and without using repeaters.

Receiver inputs feature a "Full Fail-Safe" design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or terminated but undriven.

The ISL3280E and ISL3284E feature an always enabled Rx; the ISL3281E features an active high Rx enable pin and the ISL3282E and ISL3283E include an active low enable pin. All versions are offered in Industrial and Extended Industrial (-40°C to +125°C) temperature ranges.

A 26% smaller footprint is available with the ISL3282E TDFN package. These devices, plus the ISL3284E, also feature a logic supply pin (V_L) that sets the V_{OH} level of the RO output (and the switching points of the RE/$\overline{RE}$ input) to be compatible with another supply voltage in mixed voltage systems.

For companion single RS-485 transmitters in micro packages, see the *ISL3295E, ISL3298E datasheet.*

Features

- IEC61000 ESD protection on RS-485 inputs . . . . . ±16.5kV
  - Class 3 ESD level on all other pins . . . . . >5kV HBM
- Pb-free (RoHS compliant)
- Wide supply range . . . . . 3.0V to 5.5V
- Specified for +125°C operation
- Logic supply pin (V_L) eases operation in mixed supply systems (ISL3282E, ISL3284E only)
- Full fail-safe (open, short, terminated/undriven)
- True 1/8 unit load allows up to 256 devices on the bus
- High data rates. . . . . up to 20Mbps
- Low quiescent supply current. . . . . 500µA (max)
  - Very low shutdown supply current . . . . . 20µA (max)
- -7V to +12V common mode input voltage range
- Tri-statable Rx available (active low or high EN input)
- 5V tolerant logic inputs when VCC ≤ 5V

Applications

- Clock distribution
- High node count systems
- Space constrained systems
- Security camera networks
- Building environmental control/lighting systems
- Industrial/process control networks

TABLE 1. SUMMARY OF FEATURES

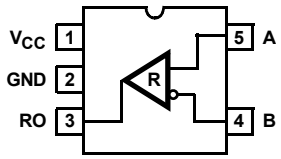
PART NUMBER	FUNCTION	DATA RATE (Mbps)	# DEVICES ON BUS	RX ENABLE?	V_L PIN?	QUIESCENT I_{CC} (µA)	LOW POWER SHUTDOWN?	LEAD COUNT
ISL3280E	1 Rx	20	256	NO	NO	350	NO	5-SOT
ISL3281E	1 Rx	20	256	ACTIVE HIGH	NO	350	YES	6-SOT
ISL3282E	1 Rx	20	256	ACTIVE LOW	YES	350	YES	8-TDFN
ISL3283E	1 Rx	20	256	ACTIVE LOW	NO	350	YES	6-SOT
ISL3284E	1 Rx	20	256	NO	YES	350	NO	6-SOT

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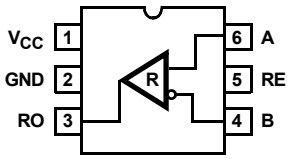
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Pin Configurations

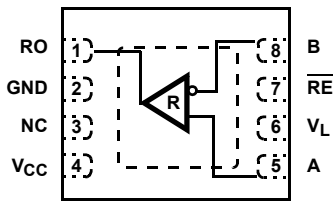
ISL3280E
(5 LD SOT-23)
TOP VIEW



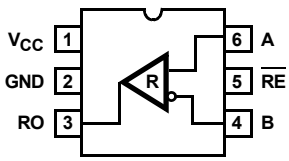
ISL3281E
(6 LD SOT-23)
TOP VIEW



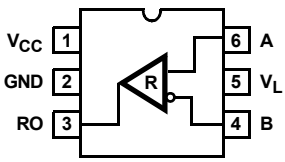
ISL3282E
(8 LD TDFN)
TOP VIEW



ISL3283E
(6 LD SOT-23)
TOP VIEW



ISL3284E
(6 LD SOT-23)
TOP VIEW



Pin Descriptions

PIN NAME	FUNCTION
RO	Receiver output: If A - B ≥ -50mV, RO is high; If A - B ≤ -200mV, RO is low; RO = High if A and B are unconnected (floating) or shorted.
RE, $\overline{RE}$	Receiver output enable. RO is enabled when RE is high, or $\overline{RE}$ is low; RO is high impedance when RE is low, or $\overline{RE}$ is high. If the Rx enable function is not used, connect $\overline{RE}$ directly to GND, or connect RE through a 1kΩ, or greater, resistor to V_{CC}. RE is internally pulled high, and $\overline{RE}$ is internally pulled low.
GND	Ground connection. This is also the potential of the TDFN thermal pad.
A	±16.5kV IEC61000 ESD protected RS-485, RS-422 level, noninverting receiver input.
B	±16.5kV IEC61000 ESD protected RS-485, RS-422 level, inverting receiver input.
V_{CC}	System power supply input (3.0V to 5.5V). On devices with a V_L pin powered from a separate supply, power-up V_{CC} first.
V_L	Logic-level supply, which sets the V_{IL} / V_{IH} levels for the $\overline{RE}$ (ISL3282E only) pin and sets the V_{OH} level of the RO output (ISL3282E, ISL3284E). If V_L and V_{CC} are different supplies, power-up this supply after V_{CC} and keep $V_L \leq V_{CC}$.
NC	No Connection.

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Truth Table

RECEIVING		
INPUTS		OUTPUT
RE, $\overline{RE}$	A - B	RO
1, 0	≥ -0.05V	1
1, 0	≤ -0.2V	0
1, 0	Inputs Open/Shorted	1
0, 1	X	High-Z*

NOTE: *Shutdown Mode, except for ISL3280E, ISL3284E

Ordering Information

PART NUMBER (Notes 1, 3)	PART MARKING (Note 4)	PACKAGE (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 2)	TEMP. RANGE
ISL3280EFHZ-T	280F	5 Ld SOT-23	P5.064	Reel, 3k	-40 to +125°C
ISL3280EFHZ-T7A				Reel, 250	
ISL3280EIHZ-T	280I	5 Ld SOT-23	P5.064	Reel, 3k	-40 to +85°C
ISL3280EIHZ-T7A				Reel, 250	
ISL3281EFHZ-T	281F	6 Ld SOT-23	P6.064	Reel, 3k	-40 to +125°C
ISL3281EFHZ-T7A				Reel, 250	
ISL3281EIHZ-T	281I	6 Ld SOT-23	P6.064	Reel, 3k	-40 to +85°C
ISL3281EIHZ-T7A				Reel, 250	
ISL3282EFRTZ-T	82F	8 Ld TDFN	L8.2x3A	Reel, 6k	-40 to +125°C
ISL3282EIRTZ-T	82I	8 Ld TDFN	L8.2x3A	Reel, 6k	-40 to +85°C
ISL3283EFHZ-T	283F	6 Ld SOT-23	P6.064	Reel, 3k	-40 to +125°C
ISL3283EFHZ-T7A				Reel, 250	
ISL3283EIHZ-T	283I	6 Ld SOT-23	P6.064	Reel, 3k	-40 to +85°C
ISL3283EIHZ-T7A				Reel, 250	
ISL3284EFHZ-T	284F	6 Ld SOT-23	P6.064	Reel, 3k	-40 to +125°C
ISL3284EIHZ-T	284I	6 Ld SOT-23	P6.064	Reel, 3k	-40 to +85°C

NOTES:

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. See TB347 for details about reel specifications.
3. For Moisture Sensitivity Level (MSL), see the ISL3280E, ISL3281E, ISL3282E, ISL3283E, ISL3284E product information pages. For more information about MSL, see TB363.
4. SOT-23 “PART MARKING” is branded on the bottom side.

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Typical Operating Circuits

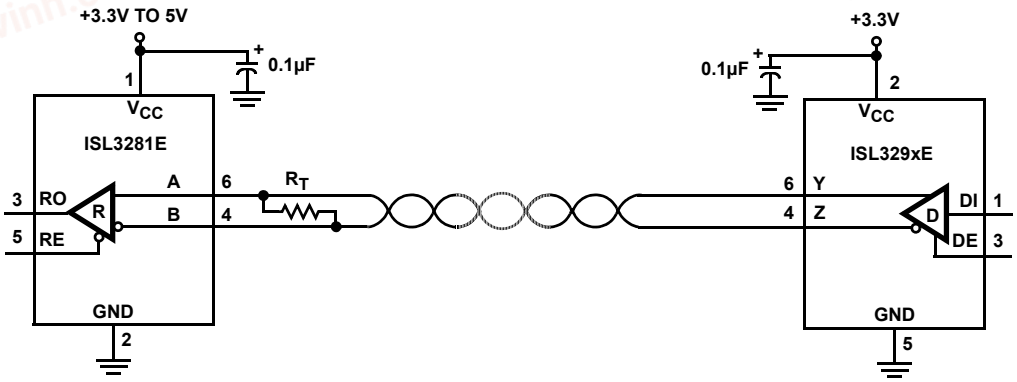


FIGURE 1. NETWORK WITH ENABLES

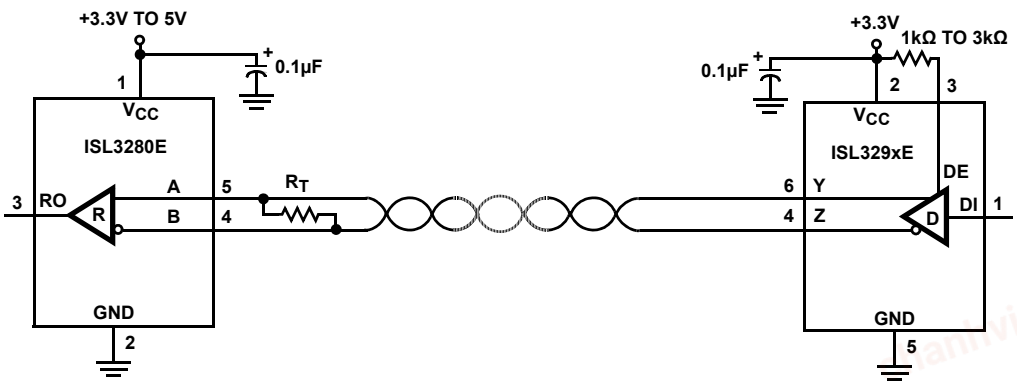


FIGURE 2. NETWORK WITHOUT ENABLES

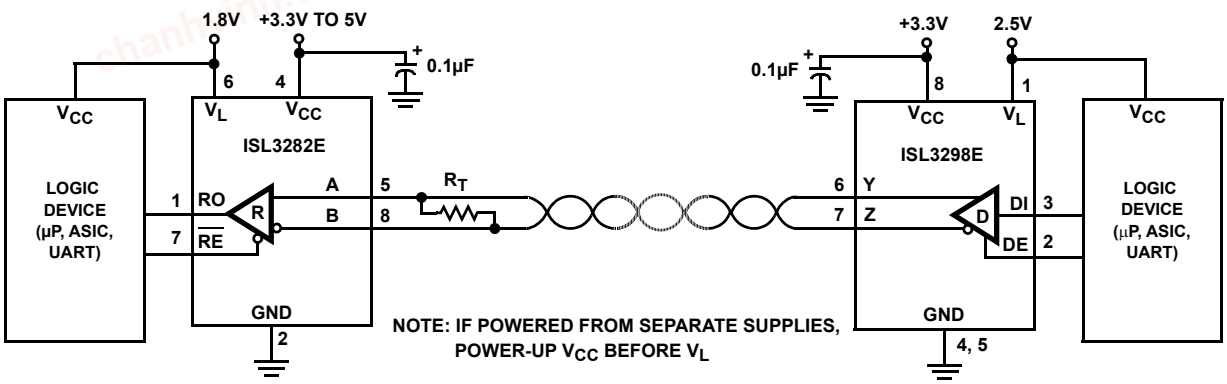


FIGURE 3. NETWORK WITH V_L PIN FOR INTERFACE TO LOWER VOLTAGE LOGIC DEVICES

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Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to 7V
V_L to GND (ISL3282E, ISL3284E Only) ..... -0.3V to (V_{CC} +0.3V)
Input Voltages
RE, $\overline{RE}$ ..... -0.3V to 7V
Input/Output Voltages
A, B ..... -8V to +13V
RO (Not ISL3282E, ISL3284E) ..... -0.3V to (V_{CC} +0.3V)
RO (ISL3282E, ISL3284E) ..... -0.3V to (V_L +0.3V)
Short-circuit Duration
RO ..... Indefinite
ESD Rating ..... See Specification Table

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld SOT-23 Package (Note 5)	190	N/A
6 Ld SOT-23 Package (Note 5)	177	N/A
8 Ld TDFN Package (Notes 6, 7)	65	8

Maximum Junction Temperature (Plastic Package) ..... +150°C
Maximum Storage Temperature Range ..... -65°C to +150°C
Pb-free Reflow Profile ..... see TB493

Operating Conditions

Temperature Range
F Suffix ..... -40°C to +125°C
I Suffix ..... -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
7. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 5.5V; V_L = V_{CC} (ISL3282E, ISL3284E only); Typicals are at T_A = +25°C (Note 12); Unless Otherwise Specified (Note 8).

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 11)	TYP (Note 12)	MAX (Note 11)	UNIT
DC CHARACTERISTICS								
Input High Voltage (RE, $\overline{RE}$) (Notes 9, 10)	V_{IH1}	V_L = V_{CC} if ISL3282E	$V_{CC} \le 3.6V$	Full	2	-	-	V
	V_{IH2}		$V_{CC} \le 5.5V$	Full	2.4	-	-	V
	V_{IH3}	2.7V ≤ V_L < 3.0V	ISL3282E	Full	1.7	-	-	V
	V_{IH4}	2.3V ≤ V_L < 2.7V		Full	1.6	-	-	V
	V_{IH5}	1.6V ≤ V_L < 2.3V		Full	0.72*V_L	-	-	V
	V_{IH6}	1.35V ≤ V_L < 1.6V		25	-	0.5*V_L	-	V
Input Low Voltage (RE, $\overline{RE}$) (Notes 9, 10)	V_{IL1}	V_L = V_{CC} if ISL3282E		Full	-	-	0.7	V
	V_{IL2}	$V_L \ge 2.7V$	ISL3282E	Full	-	-	0.7	V
	V_{IL3}	2.3V ≤ V_L < 2.7V		Full	-	-	0.6	V
	V_{IL4}	1.6V ≤ V_L < 2.3V		Full	-	-	0.25*V_L	V
	V_{IL5}	1.35V ≤ V_L < 1.6V		25	-	0.33*V_L	-	V
Logic Input Current (Note 9)	I_{IN1}	RE = $\overline{RE}$ = 0V or V_{CC}		Full	-15	±9	15	µA
Input Current (A, B)	I_{IN2}	V_{CC} = 0V, 3.6V, or 5.5V	V_{IN} = 12V	Full	-	80	125	µA
			V_{IN} = -7V	Full	-100	-50	-	µA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25	-	15	-	mV
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	-	150	-	kΩ
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	±7	±30	±85	mA
Receiver Output High Voltage	V_{OH1}	I_O = -3.5mA, V_{ID} = -50mV (V_L = V_{CC} if ISL3282E, ISL3284E)		Full	V_{CC} - 0.4	-	-	V
	V_{OH2}	I_O = -1mA, $V_L \ge 1.6V$	ISL3282E, ISL3284E	Full	V_L - 0.4	-	-	V
	V_{OH3}	I_O = -500µA, V_L = 1.5V		Full	1.2	-	-	V
	V_{OH4}	I_O = -150µA, V_L = 1.35V		Full	1.15	-	-	V
	V_{OH5}	I_O = -100µA, $V_L \ge 1.35V$		Full	V_L - 0.1	-	-	V

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Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 5.5V; V_L = V_{CC} (ISL3282E, ISL3284E only); Typicals are at T_A = +25°C (Note 12); Unless Otherwise Specified (Note 8). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 11)	TYP (Note 12)	MAX (Note 11)	UNIT
Receiver Output Low Voltage	V_{OL1}	I_O = 4mA, V_{ID} = -200mV, $V_L \geq$ 2.2V if ISL3282E, ISL3284E		Full	-	0.2	0.4	V
	V_{OL2}	I_O = 2mA, $V_L \geq$ 1.5V	ISL3282E, ISL3284E	Full	-	0.2	0.4	V
	V_{OL3}	I_O = 1mA, $V_L \geq$ 1.35V		Full	-	0.1	0.4	V
	V_{OL4}	I_O = 500µA, $V_L \geq$ 1.35V		25	-	0.1	-	V
Three-state (high impedance) Receiver Output Current (Notes 9, 10)	I_{OZR}	0V ≤ V_O ≤ V_{CC}		Full	-1	0.015	1	µA
SUPPLY CURRENT								
No-Load Supply Current	I_{CC}	RE/$\overline{RE}$ = V_{CC}/0V		Full	-	400	500	µA
Shutdown Supply Current (Note 9)	I_{SHDN}	RE/$\overline{RE}$ = 0V/V_{CC}		Full	-	-	20	µA
ESD PERFORMANCE								
RS-485 Pins (A, B)		IEC61000-4-2, Air-Gap Discharge Method		25	-	±16.5	-	kV
		IEC61000-4-2, Contact Discharge Method		25	-	±9	-	kV
		Human Body Model, from bus pins to GND		25	-	±16.5	-	kV
All Pins		HBM, per MIL-STD-883 Method 3015		25	-	±5	-	kV
		MM		25	-	±250	-	V
RECEIVER SWITCHING CHARACTERISTICS								
Maximum Data Rate	f_{MAX}	V_{ID} = ±2V, V_{CM} = 0V (Figure 4 and Table 2) (Note 12)		Full	20	30, 24	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	V_{ID} = ±2V, V_{CM} = 0V (Figure 4)		Full	20	36	60	ns
		$V_L \geq$ 1.5V (Figure 4)	ISL3282E, ISL3284E	25	-	44	-	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SK1}	V_{CC} = 3.3V ±10% (Figure 4)	V_L = V_{CC} if ISL3282E, ISL3284E	Full	-	1	5.5	ns
	t_{SK2}	V_{CC} = 5V ±10% (Figure 4)		Full	-	2	7.5	ns
	t_{SK3}	$V_L \geq$ 1.8V (Figure 4)	ISL3282E, ISL3284E	25	-	2	-	ns
	t_{SK4}	V_L = 1.5V (Figure 4)		25	-	4	-	ns
Receiver Enable to Output High (Note 9)	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 5)	(Note 12)	Full	-	240, 90	500	ns
			$V_L \geq$ 1.5V (Note 12)	25	-	250, 120	-	ns
Receiver Enable to Output Low (Note 9)	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 5)	(Note 12)	Full	-	240, 90	500	ns
			$V_L \geq$ 1.5V (Note 12)	25	-	250, 120	-	ns
Receiver Disable from Output High (Note 9)	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 5)		Full	-	10	20	ns
			$V_L \geq$ 1.5V (Note 12)	25	-	24, 20	-	ns
Receiver Disable from Output Low (Note 9)	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 5)		Full	-	10	20	ns
			$V_L \geq$ 1.5V (Note 12)	25	-	24, 20	-	ns

NOTES:

8. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
9. Does not apply to the ISL3280E or ISL3284E.
10. If the Rx enable function isn't needed, connect the enable pin to the appropriate supply, as described in the Pin Descriptions table on page 2
11. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.
12. Typical values are at 3.3V, 5V. Parameters with a single entry in the "TYP" column apply to 3.3V and 5V.

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Test Circuits and Waveforms

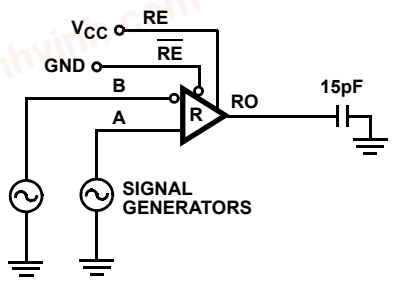


FIGURE 4A. TEST CIRCUIT

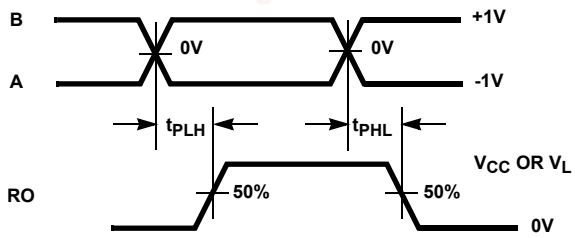
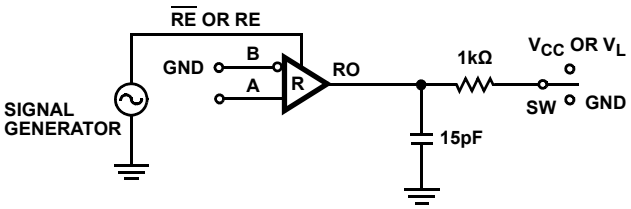


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	A	SW
t_{HZ}	+1.5V	GND
t_{LZ}	-1.5V	V_{CC} OR V_L
t_{ZH}	+1.5V	GND
t_{ZL}	-1.5V	V_{CC} OR V_L

FIGURE 5A. TEST CIRCUIT

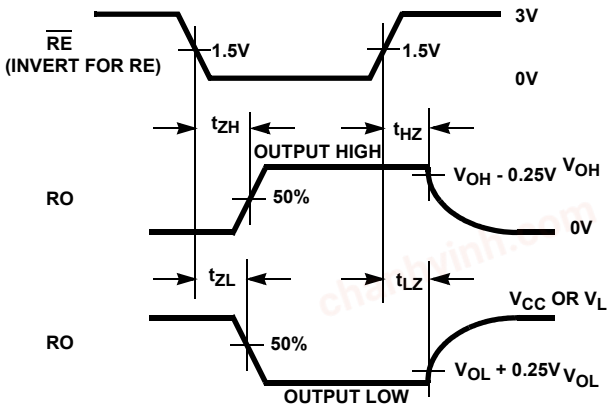


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER ENABLE AND DISABLE TIMES (EXCEPT ISL3280E AND ISL3284E)

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus.

Another important advantage of RS-485 is the extended Common Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

These devices utilize a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is better than ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input resistance of 96kΩ surpasses the RS-422 specification of 4kΩ and is eight times the RS-485 "Unit Load (UL)" requirement of 12kΩ minimum. Thus, these products are known as "one-eighth UL" transceivers and there can be up to 256 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common mode voltages as great as +9V/-7V outside the power supplies (i.e., +12V and -7V), making them ideal for long networks where induced voltages and ground potential differences are realistic concerns.

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All the receivers include a “full fail-safe” function that guarantees a high level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated but undriven bus. Fail-safe with shorted inputs is achieved by setting the Rx upper switching point to -50mV, thereby ensuring that the Rx sees 0V differential as a high input level.

All receivers easily support a 20Mbps data rate and all receiver outputs (except on the ISL3280E and ISL3284E) are tri-statable via the active low $\overline{RE}$ input or by the active high RE input.

TABLE 2. V_{IH}, V_{IL} AND DATA RATE vs V_L FOR V_{CC} = 3.3V OR 5V

V_L (V)	V_{IH} (V)	V_{IL} (V)	DATA RATE (Mbps)
1.35	0.55	0.5	11
1.6	0.7	0.6	16
1.8	0.8	0.7	23
2.3	1	0.9	27
2.7	1.1	1	30
3.3	1.3	1.2	30
5.5 (i.e., V_{CC})	2	1.8	24

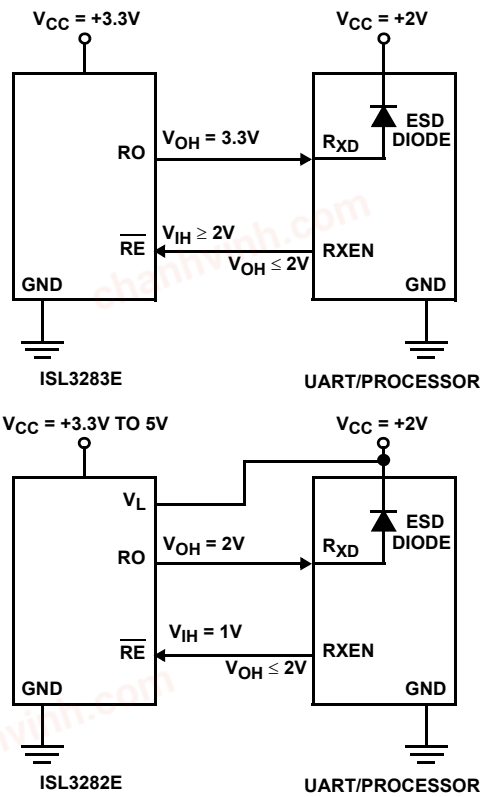


FIGURE 6. USING V_L PIN TO ADJUST LOGIC LEVELS

Wide Supply Range

The ISL3280E, ISL3281E, ISL3282E, ISL3283E, ISL3284E are designed to operate with a wide range of supply voltages from 3.0V to 5.5V. These devices meet the RS-422 and RS-485 specifications over this full range.

Logic Supply (V_L Pin, ISL3282E, ISL3284E)

Note: If powered from separate supplies, power-up V_{CC} before powering up the V_L supply and keep $V_L \leq V_{CC}$.

The ISL3282E, ISL3284E include a V_L pin that powers the logic input ($\overline{RE}$ or RE) and/or the Rx output. These pins interface with “logic” devices such as UARTs, ASICs, and microcontrollers and today most of these devices use power supplies significantly lower than 3.3V. Thus, a 3.3V output level from a 3.3V powered RS-485 IC might seriously overdrive and damage the logic device input. Similarly, the logic device’s low V_{OH} might not exceed the V_{IH} of a 3.3V or 5V powered $\overline{RE}$ input. Connecting the V_L pin to the power supply of the logic device (as shown in Figure 6) limits the ISL3282E, ISL3284E’s Rx output V_{OH} to V_L (see Figures 9 through 13) and reduces the $\overline{RE}$/RE input switching point to a value compatible with the logic device’s output levels. Tailoring the logic pin input switching point and output levels to the supply voltage of the UART, ASIC, or microcontroller eliminates the need for a level shifter/translator between the two ICs.

V_L can be anywhere from V_{CC} down to 1.35V, but the input switching points may not provide enough noise margin when V_L < 1.6V. Table 2 indicates typical V_{IH}, V_{IL} and data rate values for various V_L settings so the user can ascertain whether or not a particular V_L voltage meets his/her needs.

The quiescent, RO unloaded, V_L supply current (I_L) is typically less than 60µA for $V_L \leq$ 3.3V, as shown in Figure 8.

ESD Protection

All pins on these devices include class 3 (>4kV) Human Body Model (HBM) ESD protection structures, but the RS-485 pins (receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±16.5kV HBM and ±16.5kV IEC61000. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (e.g., transient suppression diodes) and the associated, undesirable capacitive load they present.

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IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case) and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-485 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-485 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The A and B RS-485 pins withstand ±16.5kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±9kV. The ISL3280E, ISL3281E, ISL3282E, ISL3283E, and ISL3284E survive ±9kV contact discharges on the RS-485 pins.

Data Rate, Cables and Terminations

RS-485, RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Networks operating at 20Mbps are limited to lengths less than 100', while a 250kbps network that uses slew rate limited transmitters can operate at that data rate over lengths of several thousand feet.

Twisted pair is the cable of choice for RS-485, RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receiver in these ICs.

To minimize reflections, proper termination is imperative for high data rate networks. Short networks using slew rate limited transmitters need not be terminated, but terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transmitter or receiver to the main cable should be kept as short as possible.

Low Power Shutdown Mode

These BiCMOS receivers all use a fraction of the power required by their bipolar counterparts and the versions with output enable functions include a shutdown feature that reduces the already low quiescent I_{CC} to a 20µA trickle. These versions enter shutdown whenever the receiver disables ($\overline{RE}$ = V_{CC} or RE = GND).

Typical Performance Curves

C_L = 15pF, T_A = +25°C; unless otherwise specified.

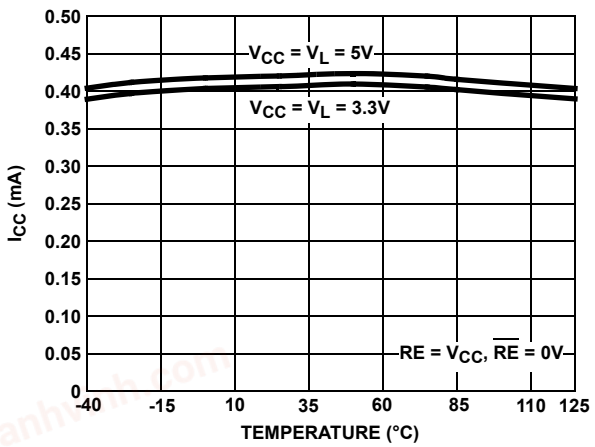


FIGURE 7. SUPPLY CURRENT vs TEMPERATURE

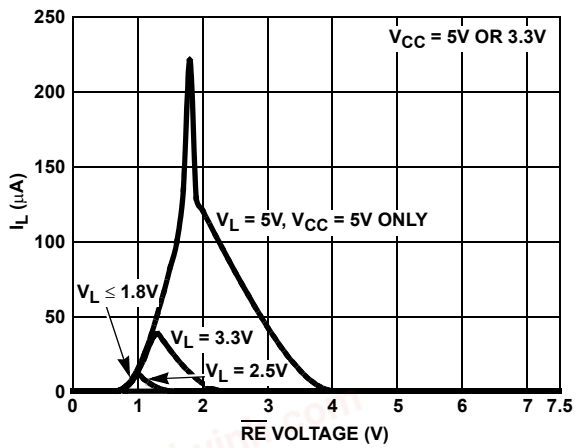


FIGURE 8. V_L SUPPLY CURRENT vs ENABLE PIN VOLTAGE

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Typical Performance Curves

C_L = 15pF, T_A = +25°C; unless otherwise specified. **(Continued)**

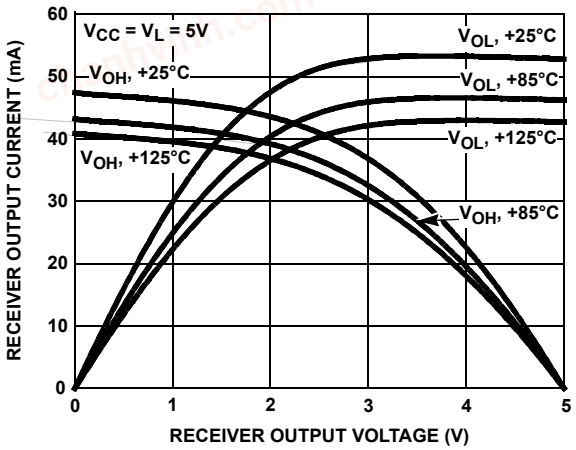


FIGURE 9. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

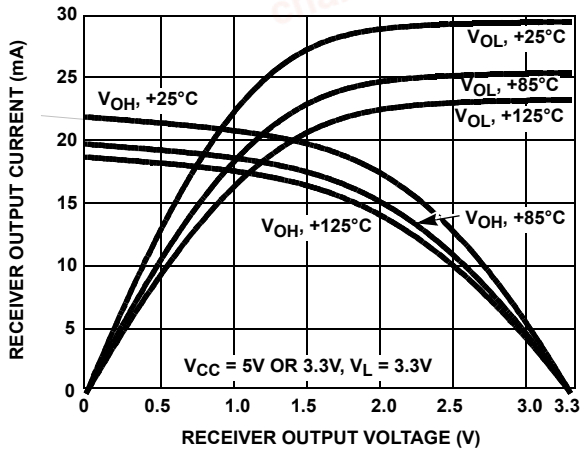


FIGURE 10. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

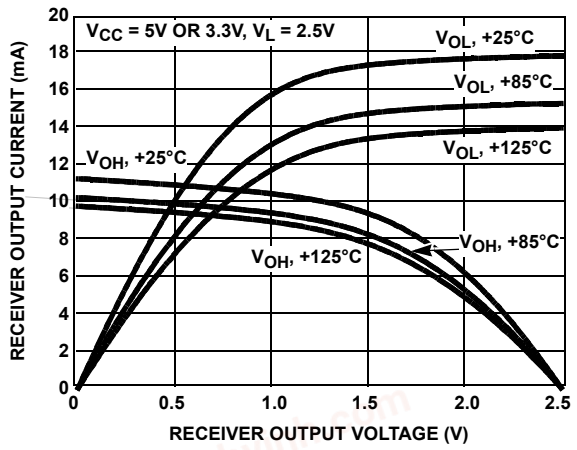


FIGURE 11. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

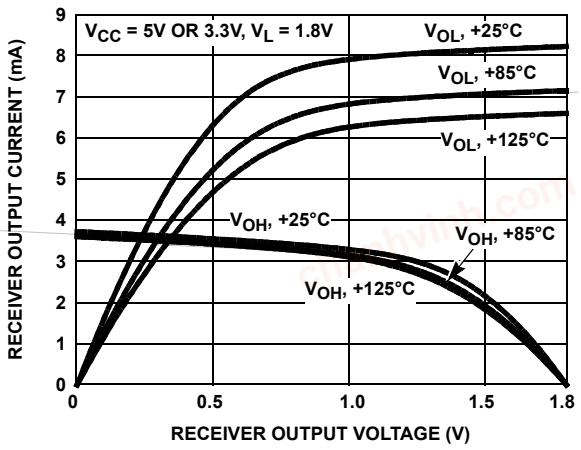


FIGURE 12. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

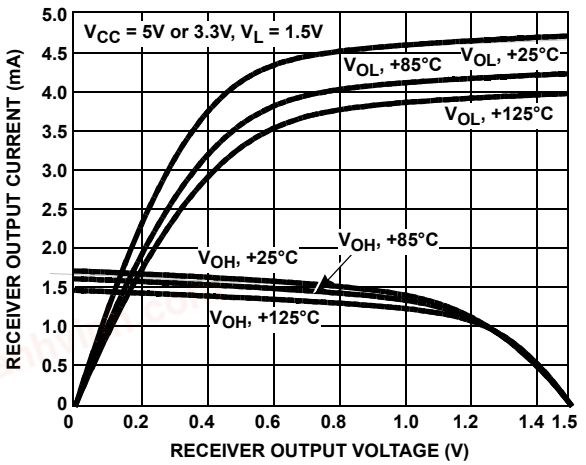


FIGURE 13. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

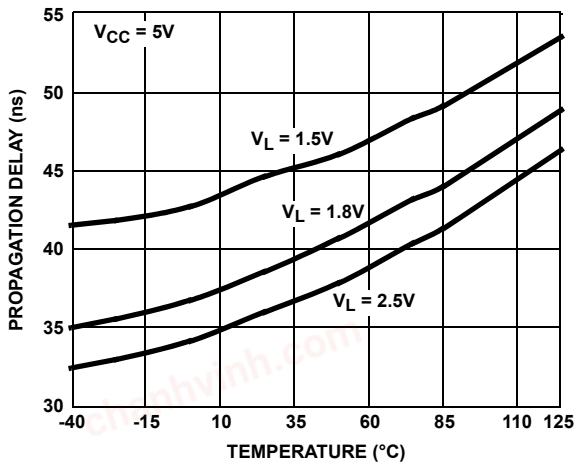


FIGURE 14. RECEIVER PROPAGATION DELAY vs TEMPERATURE

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Typical Performance Curves

C_L = 15pF, T_A = +25°C; unless otherwise specified. **(Continued)**

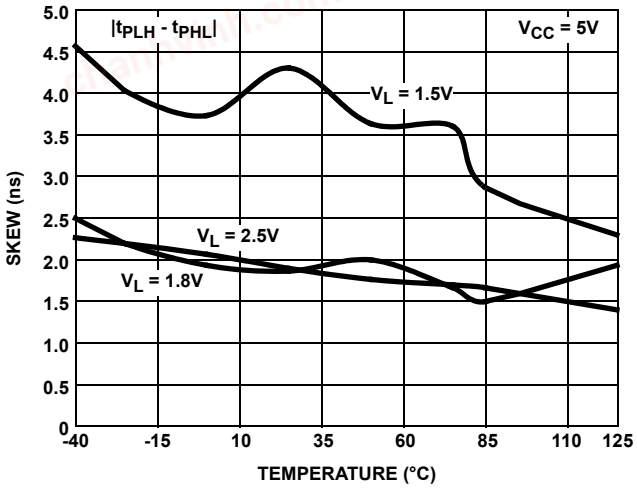


FIGURE 15. RECEIVER SKEW vs TEMPERATURE

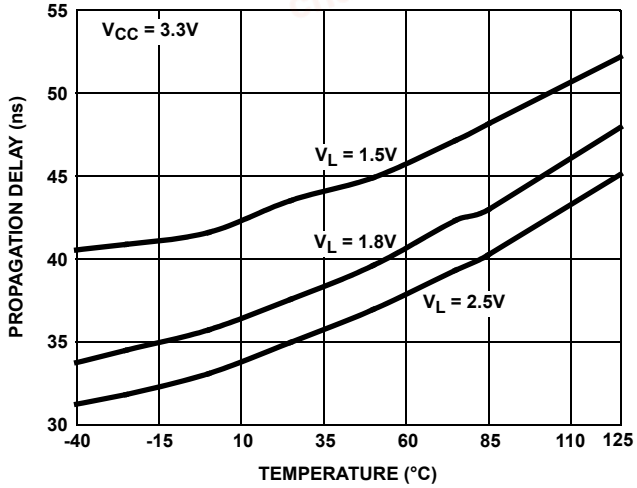


FIGURE 16. RECEIVER PROPAGATION DELAY vs TEMPERATURE

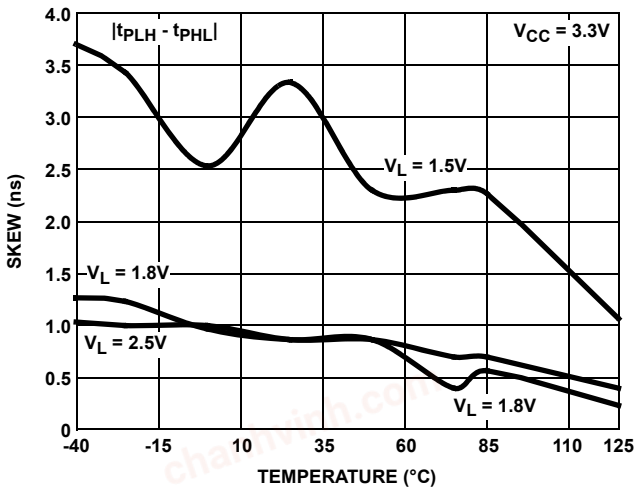


FIGURE 17. RECEIVER SKEW vs TEMPERATURE

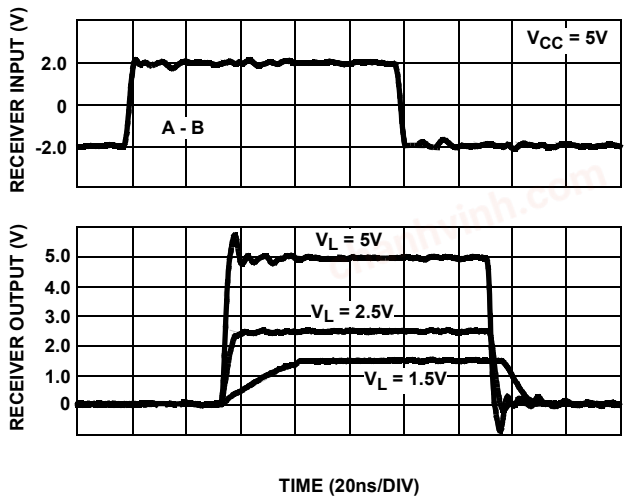


FIGURE 18. RECEIVER WAVEFORMS

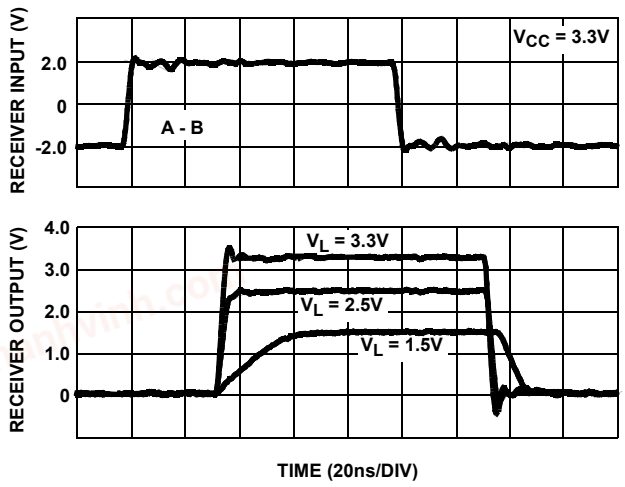


FIGURE 19. RECEIVER WAVEFORMS

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

140

PROCESS:

Si Gate BiCMOS

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

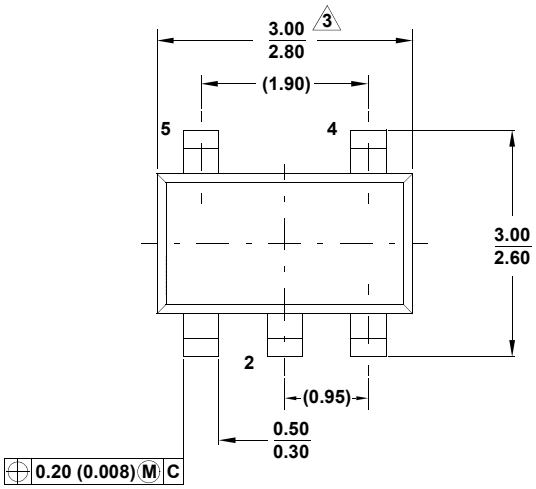
DATE	REVISION	CHANGE
Mar 31, 2022	4.01	Removed ISL3285E information throughout. Updated Ordering Information table formatting. Removed About Intersil section.
Jul 27, 2015	4.00	- Added “No longer available or supported” statement to ISL3285E in Table 1, Ordering Information table and ISL3285E pin configuration section. Replaced L8.2x3A package outline drawing with the newest revision. Changes from revision 1 to revision 2: Tiebar Note updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
Dec 4, 2014	3.00	-Updated datasheet to Intersil new standard. -Added text in several places to clarify that VL can be connected to Vcc. -Ordering information table on page 3: Added MSL note. -Electrical spec table on page 5 under "Logic Input Current": Updated note reference. -Electrical spec table on page 6 under "Shutdown Supply Current": Updated note reference. -Electrical spec table on page 6 under "RECEIVER SWITCHING CHARACTERISTICS : Updated all the note references. -Updated POD P5.064 to new format: Moved dimensions from table onto drawing and added land pattern. -Updated POD P6.064 to new format: Same dimensions, added land pattern and moved dimensions from table onto drawing. - Updated POD L8.2X3A to new format: Added recommended land pattern. -Added revision history.

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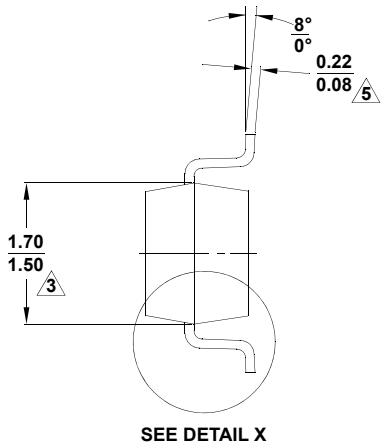
Package Outline Drawings

For the most recent package outline drawing, see P5.064.

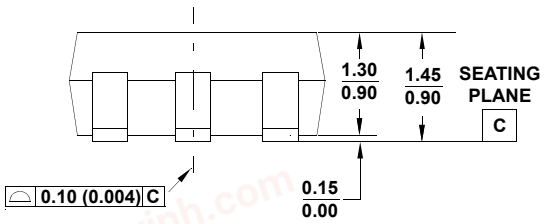
P5.064
5 Lead Small Outline Transistor Plastic Package
Rev 3, 4/11



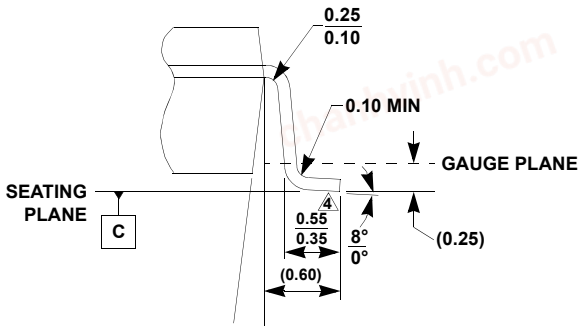
TOP VIEW



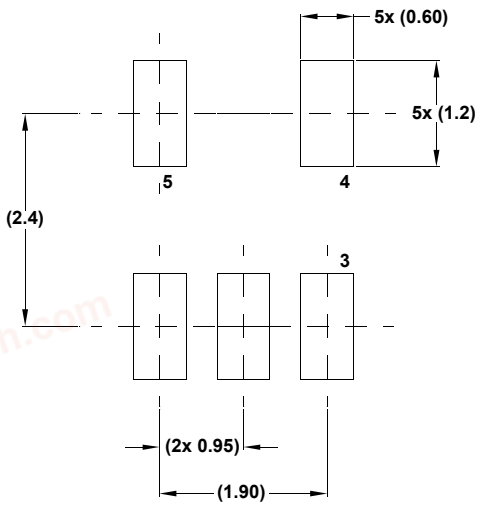
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

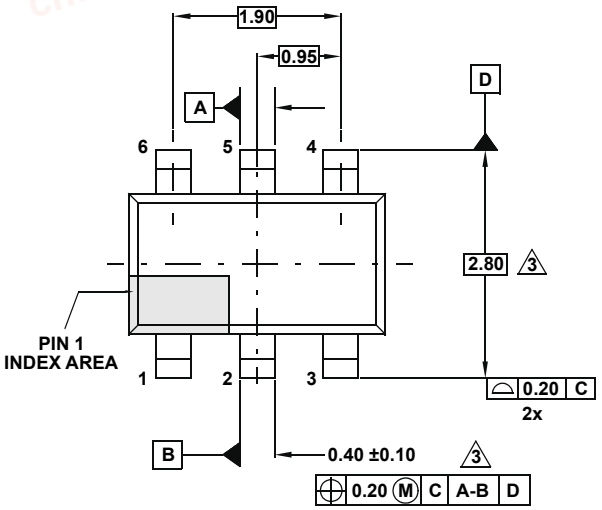
NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Package length and width are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER. Dimensions in ( ) for reference only.

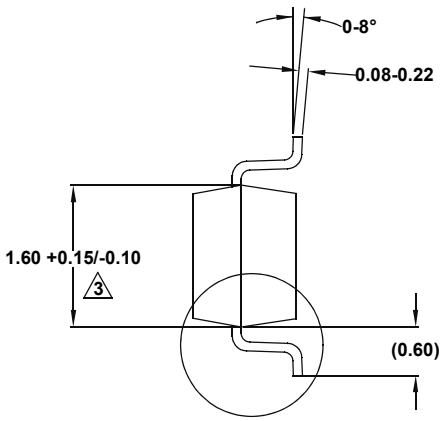
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For the most recent package outline drawing, see P6.064.

P6.064
6 Lead Small Outline Transistor Plastic Package
Rev 4, 2/10

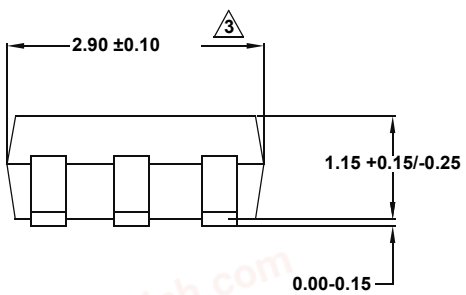


TOP VIEW

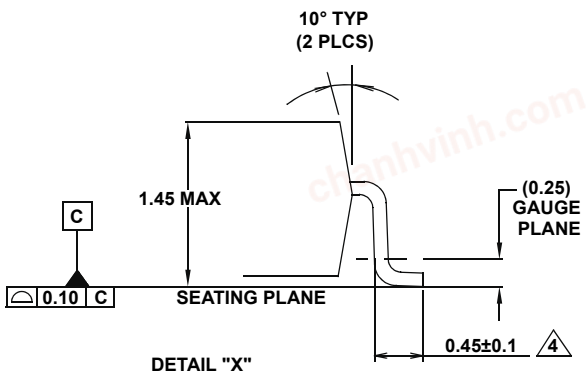


SEE DETAIL X

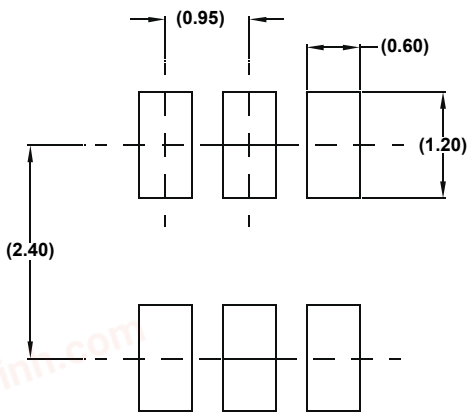
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

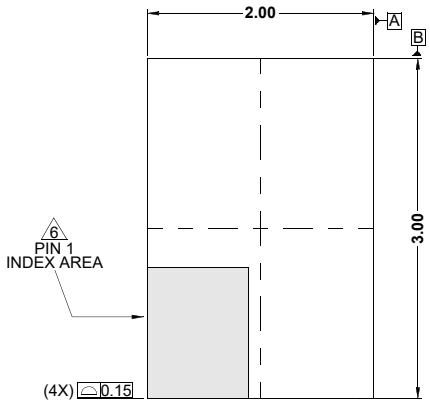
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. Package conforms to JEDEC MO-178AB.

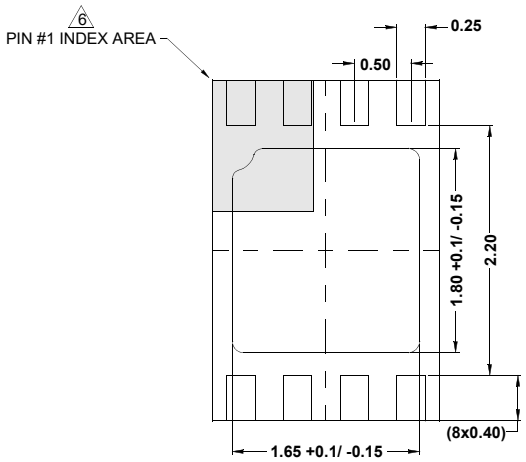
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For the most recent package outline drawing, see L8.2x3A.

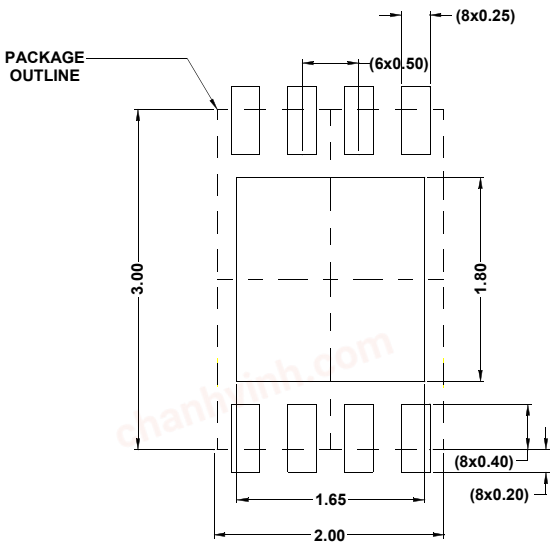
L8.2x3A
8 Lead Thin Dual Flat No-Lead Plastic Package with E-PAD
Rev 2, 05/15



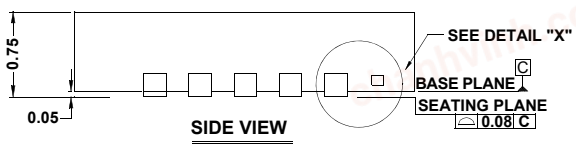
TOP VIEW



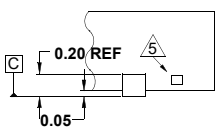
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.20mm and 0.32mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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(Rev.1.0 Mar 2020)

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