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DATASHEET

ISL32600E, ISL32601E, ISL32602E, ISL32603E

1.8V to 3.3V, Micro-Power, ±15kV ESD, +125 °C, Slew Rate Limited RS-485/RS-422 Transceivers

FN7967
Rev.3.0
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The ISL32600E, ISL32601E, ISL32602E, and ISL32603E are ±15kV IEC61000 ESD protected, micro-power, wide supply range transceivers for differential communication. The ISL32600E and ISL32601E operate with V_{CC} ≥ 2.7V and have maximum supply currents as low as 100µA with both the transmitter (Tx) and receiver (Rx) enabled. The ISL32602E and ISL32603E operate with supply voltages as low as 1.8V. These transceivers have very low bus currents, so they present less than a 1/8 unit load to the bus. This allows more than 256 transmitters on the network without violating the RS-485 specification's 32 unit load maximum.

The Rx inputs feature symmetrical switching thresholds and up to 65mV of hysteresis to improve noise immunity and to reduce duty cycle distortion in the presence of slow moving input signals (see Figure 39 on page 18). The Rx input common-mode range is the full -7V to +12V RS-485 range for supply voltages ≥ 3V.

Hot plug circuitry ensures that the Tx and Rx outputs remain in a high impedance state while the power supply stabilizes.

This transceiver family uses slew rate limited drivers, which reduce EMI, and minimize reflections from improperly terminated transmission lines or from unterminated stubs in multidrop and multipoint applications.

The ISL32600E and ISL32602E are configured for full duplex (separate Rx input and Tx output pins) applications. The ISL32601E and ISL32603E are half duplex versions that multiplex the Rx inputs and Tx outputs to allow transceivers with output disable functions in 8 Ld packages. Table 1 on page 3 provides a summary of each device's features.

Features

- Single 1.8V, 3V, or 3.3V supply
- Low supply currents
  - ISL32601E . . . . . 100µA (maximum) at 3V
  - ISL32603E . . . . . 150µA (maximum) at 1.8V
- Ultra low shutdown supply current. 10nA
- IEC61000 ESD protection on RS-485 I/O pins. . . . . ±15kV
  - Class 3 ESD levels on all other pins. . . . . >8kV HBM
- Symmetrical switching thresholds for less duty cycle distortion (see Figure 39 on page 18)
- Up to 65mV hysteresis for improved noise immunity
- Data rates from 128kbps to 460kbps
- Specified for +125°C operation
- 1/8 unit load allows up to 256 devices on the bus
- -7V to +12V common-mode input/output voltage range (V_{CC} ≥ 3V)
- Half and full duplex pinouts; three state Rx and Tx outputs
- 5V tolerant logic inputs
- Tiny MSOP packages consume 50% less board space

Applications

- Differential sensor interfaces
- Process control networks
- Security camera networks
- Building environmental control/lighting systems

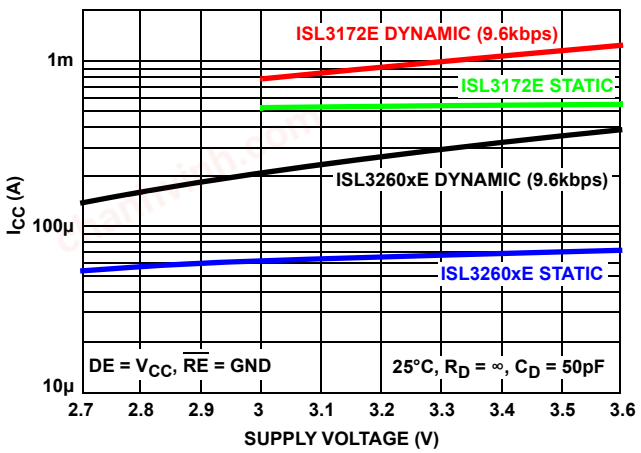


FIGURE 1. THE ISL32600E AND ISL32601E HAVE A 9.6kbps OPERATING I_{CC} LOWER THAN THE STATIC I_{CC} OF MANY EXISTING 3V TRANSCEIVERS

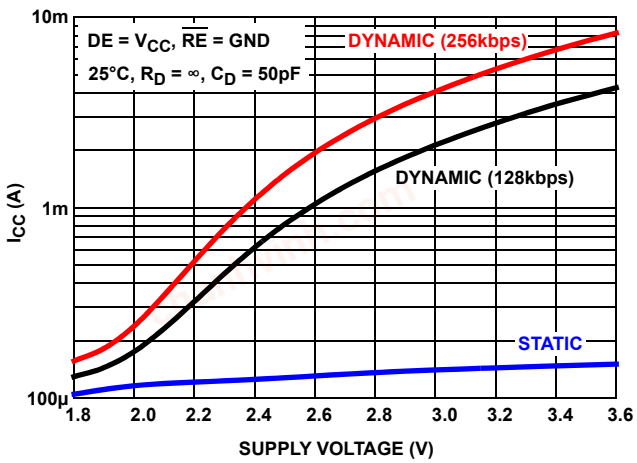


FIGURE 2. THE ISL32602E AND ISL32603E WITH V_{CC} = 1.8V REDUCE OPERATING I_{CC} BY A FACTOR OF 25 TO 40, COMPARED WITH I_{CC} AT V_{CC} = 3.3V

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Typical Operating Circuits

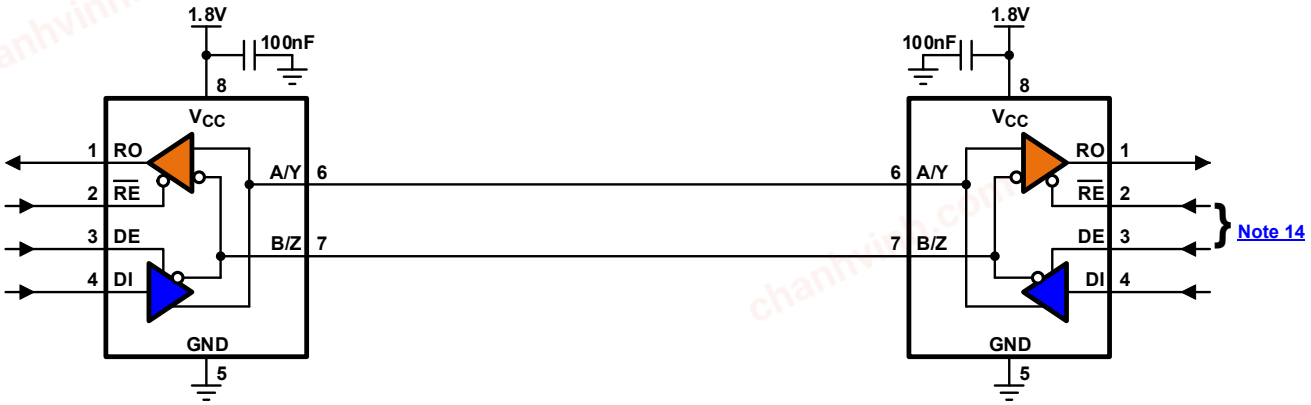


FIGURE 3. HALF DUPLEX NETWORK USING ISL32603E

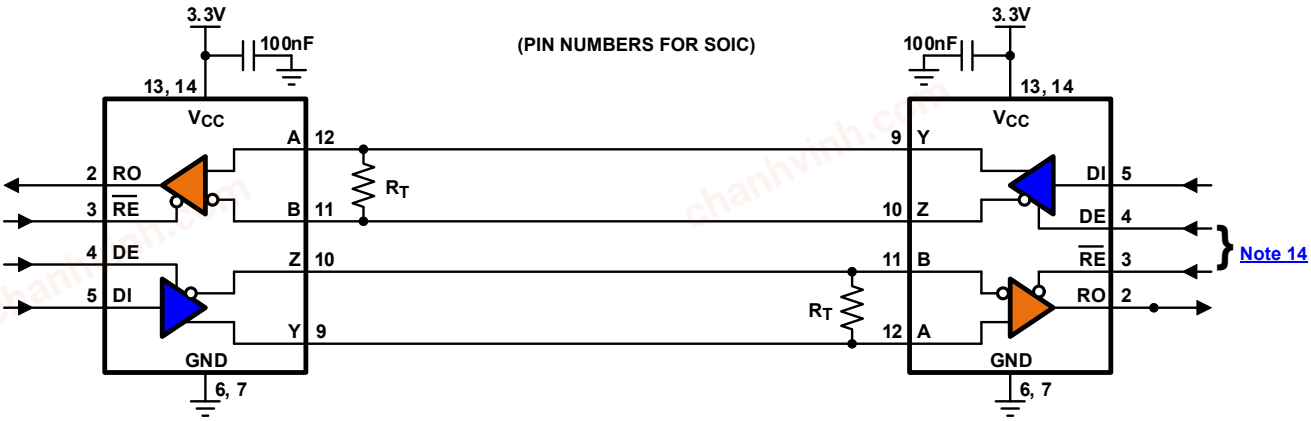


FIGURE 4. FULL DUPLEX NETWORK USING ISL32600E

NOTE: For calculating the resistor values see TB509, "Detecting Bus Signals Correctly with Failsafe Biased RS-485 Receivers".

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Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	CARRIER TYPE (Note 1)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	TEMP. RANGE
ISL32600EFBZ	32600EFBZ	Tube	14 Ld SOIC	M14.15	-40 to +125°C
ISL32600EFBZ-T		Reel, 2.5k			
ISL32600EFBZ-T7A		Reel, 250			
ISL32600EFUZ	32600	Tube	10 Ld MSOP	M10.118	
ISL32600EFUZ-T		Reel, 2.5k			
ISL32600EFUZ-T7A		Reel, 250			
ISL32601EFBZ	32601 EFBZ	Tube	8 Ld SOIC	M8.15	
ISL32601EFBZ-T		Reel, 2.5k			
ISL32601EFBZ-T7A		Reel, 250			
ISL32601EFUZ	32601	Tube	8 Ld MSOP	M8.118	
ISL32601EFUZ-T		Reel, 2.5k			
ISL32601EFUZ-T7A		Reel, 250			
ISL32602EFBZ	32602EFBZ	Tube	14 Ld SOIC	M14.15	
ISL32602EFBZ-T		Reel, 2.5k			
ISL32602EFBZ-T7A		Reel, 250			
ISL32602EFUZ	32602	Tube	10 Ld MSOP	M10.118	
ISL32602EFUZ-T		Reel, 2.5k			
ISL32602EFUZ-T7A		Reel, 250			
ISL32603EFBZ	32603 EFBZ	Tube	8 Ld SOIC	M8.15	
ISL32603EFBZ-T		Reel, 2.5k			
ISL32603EFBZ-T7A		Reel, 250			
ISL32603EFUZ	32603	Tube	8 Ld MSOP	M8.118	
ISL32603EFUZ-T		Reel, 2.5k			
ISL32603EFUZ-T7A		Reel, 250			

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL32600E, ISL32601E, ISL32602E, and ISL32603E device information pages. For more information about MSL, see TB363.

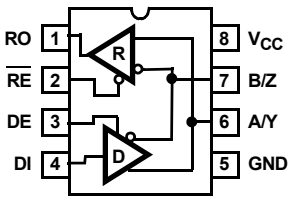
TABLE 1. SUMMARY OF FEATURES

PART NUMBER	SUPPLY RANGE (V)	HALF/FULL DUPLEX	DATA RATE (kbps)	SLEW-RATE LIMITED?	HOT PLUG?	# DEVICES ON BUS	RX/TX ENABLE?	QUIESCENT I_{CC} (µA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL32600E	2.7 to 3.6	FULL	128 - 256	YES	YES	256	YES	60 at 3V	YES	10, 14
ISL32601E	2.7 to 3.6	HALF	128 - 256	YES	YES	256	YES	60 at 3V	YES	8
ISL32602E	1.8 to 3.6	FULL	256 - 460	YES	YES	256	YES	105 at 1.8V	YES	10, 14
ISL32603E	1.8 to 3.6	HALF	256 - 460	YES	YES	256	YES	105 at 1.8V	YES	8

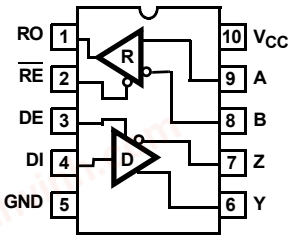
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Pin Assignments

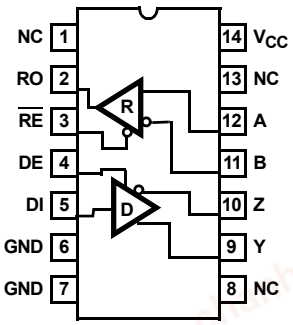
ISL32601E, ISL32603E
(8 LD MSOP, SOIC)
TOP VIEW



ISL32600E, ISL32602E
(10 LD MSOP)
TOP VIEW



ISL32600E, ISL32602E
(14 LD SOIC)
TOP VIEW



Pin Descriptions

PIN	8 LD PACKAGE	10 LD PACKAGE	14 LD PACKAGE	FUNCTION
RO	1	1	2	Receiver output: If A-B ≥ 200mV, RO is high; if A-B ≤ -200mV, RO is low; if A and B are unconnected (floating), RO = high.
$\overline{RE}$	2	2	3	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If the Rx enable function is not required, connect $\overline{RE}$ directly to GND.
DE	3	3	4	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and are high impedance when DE is low. If the Tx enable function is not required, connect DE to V_{CC}.
DI	4	4	5	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	5	5	6, 7	Ground connection.
A/Y	6	-	-	±15kV IEC61000 ESD protected RS-485/422 level, noninverting receiver input and noninverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
B/Z	7	-	-	±15kV IEC61000 ESD protected RS-485/422 level, inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
A	-	9	12	±15kV IEC61000 ESD protected RS-485/422 level, noninverting receiver input.
B	-	8	11	±15kV IEC61000 ESD protected RS-485/422 level, inverting receiver input.
Y	-	6	9	±15kV IEC61000 ESD protected RS-485/422 level, noninverting driver output.
Z	-	7	10	±15kV IEC61000 ESD protected RS-485/422 level, inverting driver output.
V_{CC}	8	10	14	System power supply input (2.7V to 3.6V for the ISL32600E and ISL32601E; 1.8V to 3.6V for the ISL32602E and ISL32603E).
NC	-	-	1, 8, 13	No internal connection.

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Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z *	High-Z *

NOTE: *Shutdown Mode (See Note 11).

Truth Tables (continued)

RECEIVING				
INPUTS				OUTPUT
$\overline{RE}$	DE Half Duplex	DE Full Duplex	A-B	RO
0	0	X	$V_{AB} \geq 0.2V$	1
0	0	X	$0.2V > V_{AB} > -0.2V$	Undetermined
0	0	X	$V_{AB} \leq -0.2V$	0
0	0	X	Inputs Open	1
1	0	0	X	High-Z *
1	1	1	X	High-Z

NOTE: *Shutdown Mode (See Note 11).

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Absolute Maximum Ratings

V_{CC} to GND 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . . -0.3V to 7V
Input/Output Voltages
A, B, ... -8V to +13V
A/Y, B/Z, Y, Z (V_{CC} = 0V or ≥ 3V) . . . . . -8V to +13V
A/Y, B/Z, Y, Z (1.8V ≤ V_{CC} < 3V) . . . . . -8V to +11V
RO . . . . . -0.3V to (V_{CC} +0.3V)
Short-Circuit Duration
Y, Z . . . . . Indeterminate
ESD Rating . . . . . See Specification Table
Latch-Up (per JESD78, Level 2, Class A) . . . . . +125°C

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package	105	47
8 Ld MSOP Package	140	40
10 Ld MSOP Package	160	59
14 Ld SOIC Package	128	39

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Supply Voltage Range
ISL32600E, ISL32601E . . . . . 3V to 3.3V
ISL32602E, ISL32603E . . . . . 1.8V to 3.3V
Differential Load Resistance
ISL32600E, ISL32601E . . . . . 60Ω or 120Ω
ISL32602E, ISL32603E . . . . . ≥10kΩ at 1.8V; 120Ω at 3.3V
Common-Mode Range
ISL32600E, ISL32601E . . . . . -7V to +12V
ISL32602E, ISL32603E
V_{CC} = 1.8V . . . . . -2V to +2V
V_{CC} = 3.3V . . . . . -7V to +12V
Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
5. For θ_{JC}, the case temperature location is taken at the package top center.

ISL32600E, ISL32601E Electrical Specifications

Test Conditions: V_{CC} = 2.7V to 3.6V; typical values are at V_{CC} = 3V, T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range.** (Note 6)

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 15)	TYP	MAX (Note 15)	UNIT
DC CHARACTERISTICS								
Driver Differential V_{OUT}	V_{OD}	R_L = 100Ω (RS-422) (Figure 5A, V_{CC} ≥ 3.15V)		Full	**1.95**	2.1	-	V
		R_L = 54Ω (RS-485) (Figure 5A)	V_{CC} = 2.7V	Full	**1.2**	1.5	V_{CC}	V
			V_{CC} ≥ 3V	Full	**1.4**	1.7	V_{CC}	V
		No Load		Full	-	-	V_{CC}	V
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 5B, V_{CC} ≥ 3V)		Full	**1.3**	-	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 5A)		Full	-	0.01	**0.2**	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 54Ω or 100Ω (Figure 5A)		Full	-	-	**3**	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 5A)		Full	-	0.01	**0.2**	V
Output Leakage Current (Y, Z) (Full Duplex Versions Only)	I_{OZD}	DE = 0V, V_{CC} = 0V (-7V ≤ V_{IN} ≤ 12V) or 2.7V ≤ V_{CC} ≤ 3.6V	V_{IN} = 12V (V_{CC} ≥ 3V)	Full	-	3	**60**	µA
			V_{IN} = 10V (V_{CC} = 2.7V)	Full	-	3	**60**	µA
			V_{IN} = -7V	Full	**-30**	-10	-	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V (Note 8)		Full	-	-	**±250**	mA
Logic Input High Voltage	V_{IH}	DI, DE, $\overline{RE}$		Full	**2**	-	-	V
Logic Input Low Voltage	V_{IL}	DI, DE, $\overline{RE}$		Full	-	-	**0.7**	V

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ISL32600E, ISL32601E Electrical Specifications

Test Conditions: V_{CC} = 2.7V to 3.6V; typical values are at V_{CC} = 3V, T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range.** (Note 6) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 15)	TYP	MAX (Note 15)	UNIT
Logic Input Current	I_{IN1}	DI = DE = $\overline{RE}$ = 0V or V_{CC} (Note 14)		Full	**-1**	-	**1**	µA
Input Current (A, B, A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V (-7V ≤ V_{IN} ≤ 12V) or 2.7V ≤ V_{CC} ≤ 3.6V	V_{IN} = 12V (V_{CC} ≥ 2.7V for A, B)	Full	-	80	**125**	µA
			V_{IN} = 12V (V_{CC} ≥ 3V for A/Y, B/Z)	Full	-	80	**125**	µA
			V_{IN} = 10V (V_{CC} = 2.7V for A/Y, B/Z)	Full	-	80	**125**	µA
			V_{IN} = -7V	Full	**-100**	-50	-	µA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	**-200**	0	**200**	mV
Receiver Input Hysteresis	ΔV_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-	40	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		Full	**V_{CC} - 0.5**	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV		Full	-	-	**0.4**	V
Three-State (High Impedance) Receiver Output Current	I_{OZR}	0V ≤ V_O ≤ V_{CC}, $\overline{RE}$ = V_{CC}		Full	**-1**	-	**1**	µA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	-	30	**±60**	mA
SUPPLY CURRENT								
No-Load Supply Current (Note 7)	I_{CC}	DI = 0V or V_{CC}, DE = V_{CC}, $\overline{RE}$ = 0V or V_{CC}	V_{CC} = 3V	Full	-	60	**100**	µA
			V_{CC} = 3.6V	Full	-	70	**120**	µA
		DI = 0V or V_{CC}, Rx Only (DE = 0V, $\overline{RE}$ = 0V)	V_{CC} = 3V	Full	-	42	**65**	µA
			V_{CC} = 3.6V	Full	-	46	**80**	µA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	0.01	**1**	µA
ESD PERFORMANCE								
RS-485 Pins (A, Y, B, Z, A/Y, B/Z)		IEC61000-4-2, Air-Gap Discharge Method		25	-	±15	-	kV
		IEC61000-4-2, Contact Discharge Method		25	-	±8	-	kV
		Human Body Model, from Bus Pins to GND		25	-	±15	-	kV
All Pins		HBM, per MIL-STD-883 Method 3015		25	-	±8	-	kV
		Machine Model		25	-	400	-	V
SWITCHING CHARACTERISTICS								
Maximum Data Rate	f_{MAX}	R_{DIFF} = 54Ω, (Figures 8, 9)	V_{CC} = 2.7V	Full	**128**	-	-	kbps
			V_{CC} ≥ 3V	Full	**256**	-	-	kbps
Driver Differential Output Delay	t_{DD}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)		Full	-	340	**600**	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)		Full	-	1	**30**	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)		Full	**200**	400	**1000**	ns
Driver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 50pF, SW = GND (Figure 7), (Note 9)		Full	-	-	**1000**	ns
Driver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 50pF, SW = V_{CC} (Figure 7), (Note 9)		Full	-	-	**1000**	ns
Driver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 50pF, SW = GND (Figure 7)		Full	-	-	**150**	ns
Driver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 50pF, SW = V_{CC} (Figure 7)		Full	-	-	**150**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 50pF, SW = GND (Figure 7), (Notes 11, 12)		Full	-	-	**10**	µs

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ISL32600E, ISL32601E Electrical Specifications

Test Conditions: V_{CC} = 2.7V to 3.6V; typical values are at V_{CC} = 3V, T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range.** (Note 6) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 15)	TYP	MAX (Note 15)	UNIT
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 50pF, SW = V_{CC} (Figure 7), (Notes 11, 12)	Full	-	-	**10**	µs
Time to Shutdown	t_{SHDN}	(Note 11)	Full	**50**	-	**600**	ns
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 9)	Full	-	750	**1300**	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 9)	Full	-	115	**300**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 10), (Note 10)	Full	-	-	**50**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 10), (Note 10)	Full	-	-	**50**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 10)	Full	-	12	**50**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 10)	Full	-	13	**50**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 10), (Notes 11, 13)	Full	-	-	**12**	µs
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 10), (Notes 11, 13)	Full	-	-	**12**	µs

ISL32602E, ISL32603E Electrical Specifications

Test Conditions: V_{CC} = 1.8V to 3.6V; Typical values are at V_{CC} = 1.8V, T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range.** (Note 6)

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 15)	TYP	MAX (Note 15)	UNIT
DC CHARACTERISTICS								
Driver Differential V_{OUT}	V_{OD}	R_L = 100Ω (RS-422) (Figure 5A)	V_{CC} = 1.8V	Full	**0.8**	0.9	-	V
			V_{CC} ≥ 3.15V	Full	**1.95**	2.25	-	V
		No Load, V_{CC} = 1.8V		Full	**1.1**	1.4	**V_{CC}**	
		R_L = 54Ω (RS-485) (Figure 5A, V_{CC} ≥ 3V)		Full	**1.5**	1.95	-	V
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 5B, V_{CC} ≥ 3V)		Full	**1.3**	-	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 100Ω (Figure 5A)		Full	-	0.01	**0.2**	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 100Ω (Figure 5A)		Full	-	-	**3**	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 100Ω (Figure 5A)		Full	-	0.01	**0.2**	V
Output Leakage Current (Y, Z) (Full Duplex Versions Only)	I_{OZD}	DE = 0V, V_{CC} = 0V (-7V ≤ V_{IN} ≤ 12V) or 1.8V or 3V ≤ V_{CC} ≤ 3.6V	V_{OUT} = 12V (V_{CC} ≥ 3V)	Full	-	1	**60**	µA
			V_{OUT} = 10V (V_{CC} = 1.8V)	Full	-	1	**60**	µA
			V_{OUT} = -7V	Full	**-30**	-10	-	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V (3.0V ≤ V_{CC} ≤ 3.6V) or -7V ≤ V_Y or V_Z ≤ 10V (V_{CC} = 1.8V) (Note 8)		Full	-	-	**±250**	mA
Logic Input High Voltage	V_{IH}	DI, DE, $\overline{RE}$	V_{CC} ≥ 1.8V	Full	**1.26**	-	-	V
			V_{CC} ≥ 3V	Full	**2**	-	-	V
Logic Input Low Voltage	V_{IL}	DI, DE, $\overline{RE}$	V_{CC} ≥ 1.8V	Full	-	-	**0.4**	V
			V_{CC} ≥ 3V	Full	-	-	**0.8**	V
Logic Input Current	I_{IN1}	DI = DE = $\overline{RE}$ = 0V or V_{CC} (Note 14)		Full	**-1**	-	**1**	µA

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ISL32602E, ISL32603E Electrical Specifications

Test Conditions: V_{CC} = 1.8V to 3.6V; Typical values are at V_{CC} = 1.8V, T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range.** (Note 6) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 15)	TYP	MAX (Note 15)	UNIT
Input Current (A, B, A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V (-7V ≤ V_{IN} ≤ 12V) or 1.8V or 3V ≤ V_{CC} ≤ 3.6V	V_{IN} = 12V (A, B Only)	Full	-	80	**125**	µA
			V_{IN} = 12V (V_{CC} ≥ 3V for A/Y, B/Z)	Full	-	80	**125**	µA
			V_{IN} = 10V (V_{CC} = 1.8V for A/Y, B/Z)	Full	-	80	**125**	µA
			V_{IN} = -7V	Full	**-100**	-50	-	µA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_Y or V_Z ≤ 2V at V_{CC} = 1.8V or -7V ≤ V_Y or V_Z ≤ 12V at V_{CC} ≥ 3V		Full	**-200**	0	**200**	mV
Receiver Input Hysteresis	ΔV_{TH}	-7V ≤ V_Y or V_Z ≤ 2V at V_{CC} = 1.8V or -7V ≤ V_Y or V_Z ≤ 12V at V_{CC} ≥ 3V		Full	-	65	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -1mA, V_{ID} = 200mV		Full	**V_{CC} - 0.4**	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = 2.2mA, V_{ID} = -200mV		Full	-	-	**0.4**	V
Three-State (High Impedance) Receiver Output Current	I_{OZR}	0V ≤ V_O ≤ V_{CC}, $\overline{RE}$ = V_{CC}		Full	**-1**	-	**1**	µA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	-	-	**±60**	mA
SUPPLY CURRENT								
No-Load Supply Current (Note 7)	I_{CC}	DI = 0V or V_{CC}, DE = V_{CC}, $\overline{RE}$ = 0V or V_{CC}	V_{CC} = 1.8V	Full	-	105	**150**	µA
			V_{CC} = 3.6V	Full	-	150	**350**	µA
		DI = 0V or V_{CC}, Rx Only (DE = 0V, $\overline{RE}$ = 0V)	V_{CC} = 1.8V	Full	-	90	**115**	µA
			V_{CC} = 3.6V	Full	-	125	**260**	µA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	-	**1**	µA
ESD PERFORMANCE								
RS-485 Pins (A, Y, B, Z, A/Y, B/Z)		IEC61000-4-2, Air-Gap Discharge Method		25	-	±15	-	kV
		IEC61000-4-2, Contact Discharge Method		25	-	±8	-	kV
		Human Body Model, from Bus Pins to GND		25	-	±15	-	kV
All Pins		HBM, per MIL-STD-883 Method 3015		25	-	±8	-	kV
		Machine Model		25	-	400	-	V
SWITCHING CHARACTERISTICS								
Maximum Data Rate	f_{MAX}	(Figure 8, 9)	V_{CC} = 1.8V, R_{DIFF} = ∞	Full	**256**	-	-	kbps
			V_{CC} ≥ 3V, R_{DIFF} = 54Ω	Full	**460**	-	-	kbps
Driver Differential Output Delay	t_{DD}	C_D = 50pF (Figure 6)	V_{CC} = 1.8V, R_{DIFF} = ∞	Full	-	750	**2600**	ns
			V_{CC} ≥ 3V, R_{DIFF} = 54Ω	Full	-	350	**1500**	ns
Driver Differential Output Skew	t_{SKEW}	C_D = 50pF (Figure 6)	V_{CC} = 1.8V, R_{DIFF} = ∞	Full	-	120	**220**	ns
			V_{CC} ≥ 3V, R_{DIFF} = 54Ω	Full	-	2	**100**	ns
Driver Differential Rise or Fall Time	t_R, t_F	C_D = 50pF (Figure 6)	V_{CC} = 1.8V, R_{DIFF} = ∞	Full	**150**	1700	**4500**	ns
			V_{CC} ≥ 3V, R_{DIFF} = 54Ω	Full	**200**	400	**900**	ns
Driver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 50pF, SW = GND (Figure 7), (Note 9)		Full	-	-	**3000**	ns
Driver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 50pF, SW = V_{CC} (Figure 7), (Note 9)		Full	-	-	**3000**	ns
Driver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 50pF, SW = GND (Figure 7)		Full	-	-	**250**	ns
Driver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 50pF, SW = V_{CC} (Figure 7)		Full	-	-	**250**	ns

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ISL32602E, ISL32603E Electrical Specifications

Test Conditions: V_{CC} = 1.8V to 3.6V; Typical values are at V_{CC} = 1.8V, T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range.** (Note 6) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 15)	TYP	MAX (Note 15)	UNIT
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 50pF, SW = GND (Figure 7), (Notes 11, 12)	Full	-	-	3000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 50pF, SW = V_{CC} (Figure 7), (Notes 11, 12)	Full	-	-	3000	ns
Time to Shutdown	t_{SHDN}	(Note 11)	Full	50	500	1200	ns
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 9)	Full	-	180	1000	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 9)	Full	-	35	250	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 10), (Note 10)	Full	-	-	100	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 10), (Note 10)	Full	-	-	100	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 10)	Full	-	-	75	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 10)	Full	-	-	75	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 10), (Notes 11, 13)	Full	-	-	5500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 10), (Notes 11, 13)	Full	-	-	5500	ns

NOTES:

6. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
7. Supply current specification is valid for loaded drivers when DE = 0V.
8. Applies to peak current. See "Typical Performance Curves" starting on page 13 for more information.
9. When testing this parameter, keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
10. When testing this parameter, the $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
11. Devices are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are assured not to enter shutdown. If the inputs are in this state for at least 600ns (1200ns if V_{CC} = 1.8V), the parts are assured to have entered shutdown. See "Low Power Shutdown Mode" on page 19.
12. Keep $\overline{RE}$ = V_{CC}, and set the DE signal low time >600ns (1200ns if V_{CC} = 1.8V) to ensure that the device enters SHDN.
13. Set the $\overline{RE}$ signal high time >600ns (1200ns if V_{CC} = 1.8V) to ensure that the device enters SHDN.
14. If the Tx or Rx enable function is not needed, connect the enable pin to the appropriate supply (see "Pin Descriptions" on page 4).
15. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

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Test Circuits and Waveforms

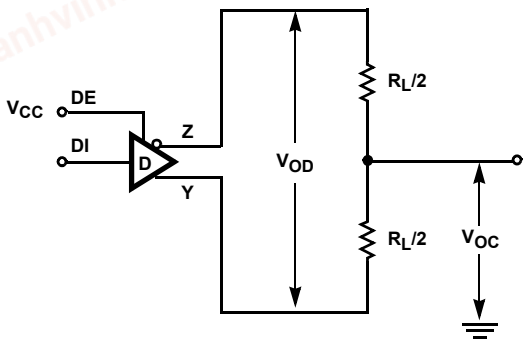


FIGURE 5A. V_{OD} AND V_{OC}

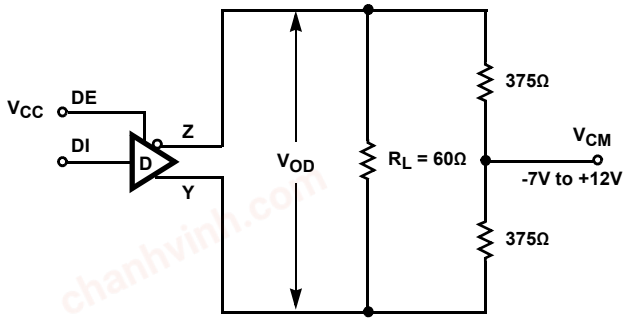


FIGURE 5B. V_{OD} WITH COMMON MODE LOAD

FIGURE 5. DC DRIVER TEST CIRCUITS

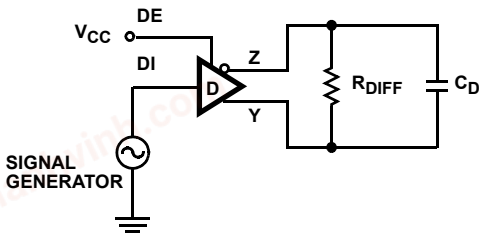


FIGURE 6A. TEST CIRCUIT

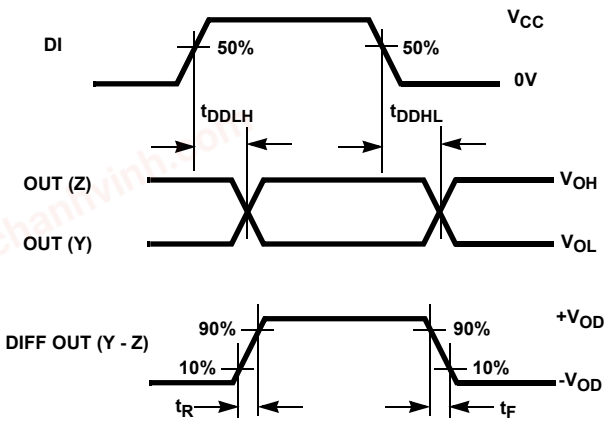
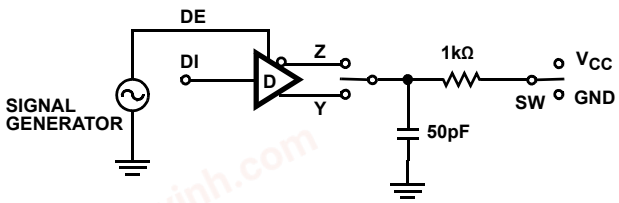


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW
t_{HZ}	Y/Z	X	1/0	GND
t_{LZ}	Y/Z	X	0/1	V_{CC}
t_{ZH}	Y/Z	0 (Note 9)	1/0	GND
t_{ZL}	Y/Z	0 (Note 9)	0/1	V_{CC}
$t_{ZH(SHDN)}$	Y/Z	1 (Note 12)	1/0	GND
$t_{ZL(SHDN)}$	Y/Z	1 (Note 12)	0/1	V_{CC}

FIGURE 7A. TEST CIRCUIT

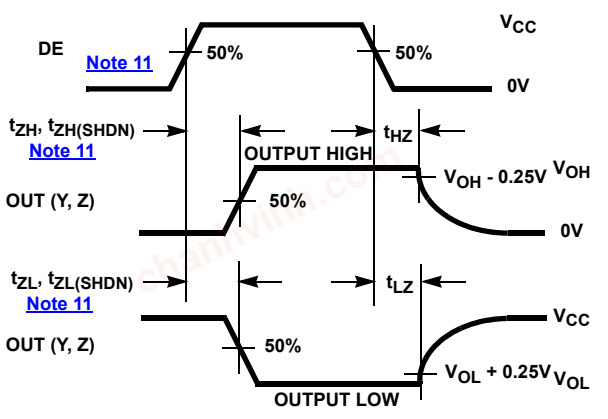


FIGURE 7B. MEASUREMENT POINTS

FIGURE 7. DRIVER ENABLE AND DISABLE TIMES

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Test Circuits and Waveforms (Continued)

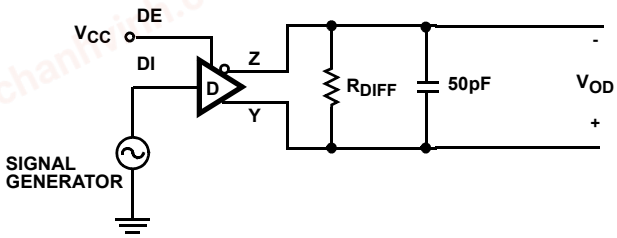


FIGURE 8A. TEST CIRCUIT

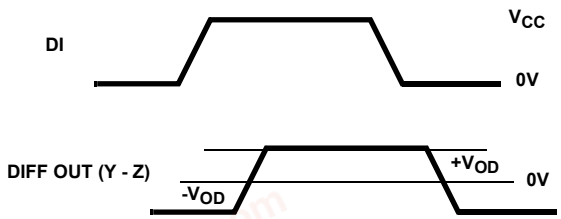


FIGURE 8B. MEASUREMENT POINTS

FIGURE 8. DRIVER DATA RATE

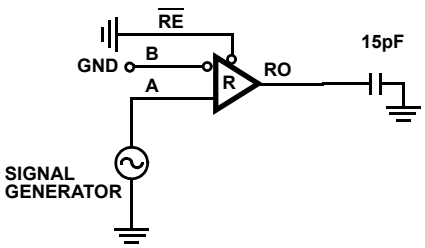


FIGURE 9A. TEST CIRCUIT

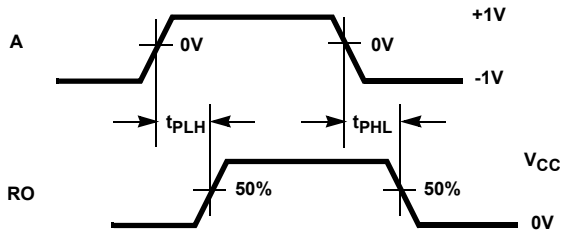
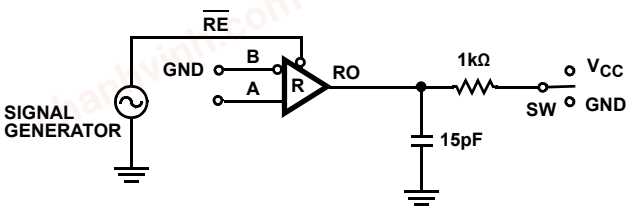


FIGURE 9B. MEASUREMENT POINTS

FIGURE 9. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	DE	A	SW
t_{HZ}	X	+1.5V	GND
t_{LZ}	X	-1.5V	V_{CC}
t_{ZH} (Note 10)	0	+1.5V	GND
t_{ZL} (Note 10)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 13)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 11)	0	-1.5V	V_{CC}

FIGURE 10A. TEST CIRCUIT

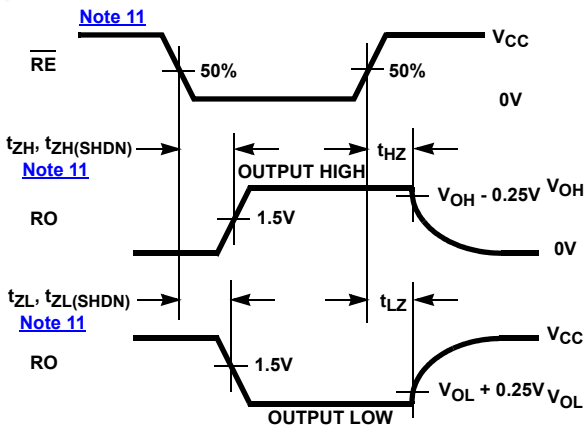


FIGURE 10B. MEASUREMENT POINTS

FIGURE 10. RECEIVER ENABLE AND DISABLE TIMES

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Typical Performance Curves

V_{CC} = 3V (ISL32600E, ISL32601E) or 1.8V (ISL32602E, ISL32603E), T_A = +25°C; unless otherwise specified

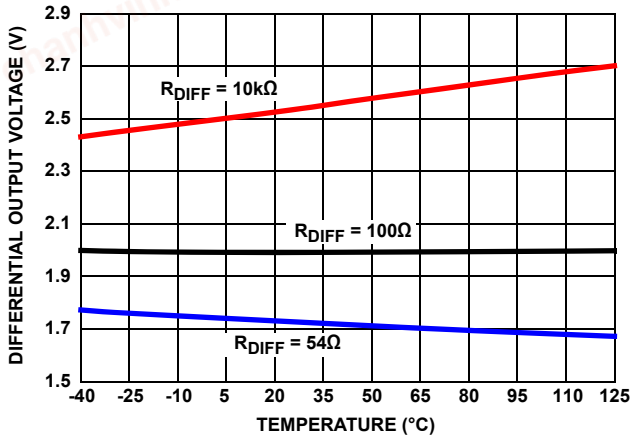


FIGURE 11. ISL32600E, ISL32601E DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

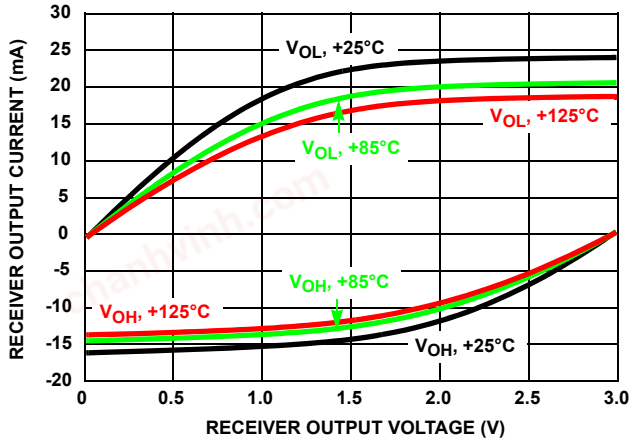


FIGURE 12. ISL32600E, ISL32601E RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

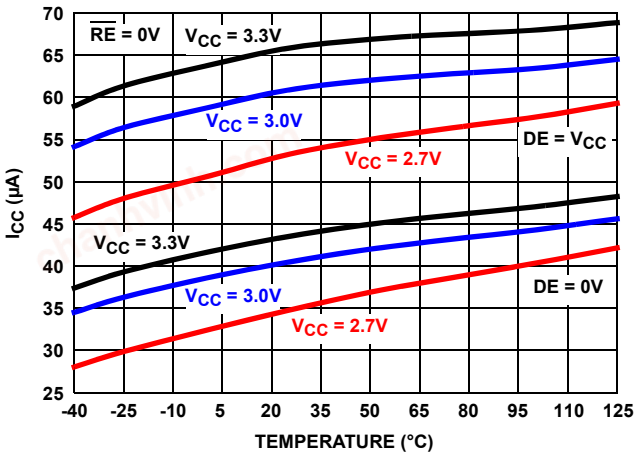


FIGURE 13. ISL32600E, ISL32601E STATIC SUPPLY CURRENT vs TEMPERATURE

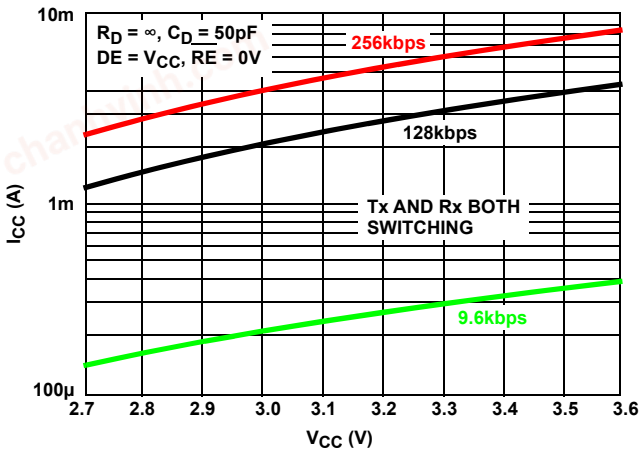


FIGURE 14. ISL32600E, ISL32601E DYNAMIC SUPPLY CURRENT vs SUPPLY VOLTAGE AT DIFFERENT DATA RATES

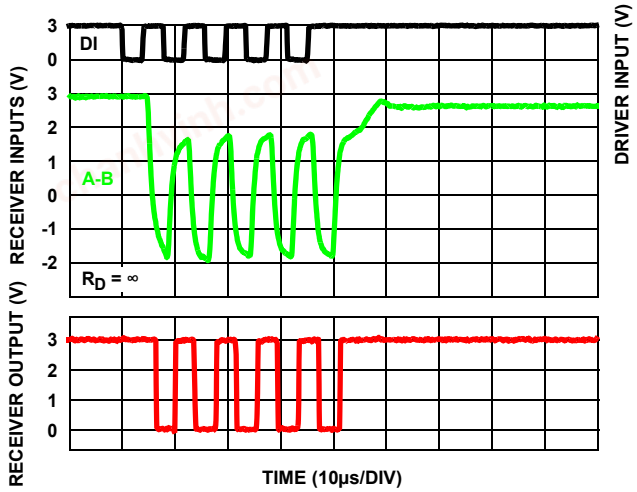


FIGURE 15. ISL32600E, ISL32601E PERFORMANCE WITH V_{CC} = 3V, 256kbps, 3000ft (915m) CAT 5 CABLE

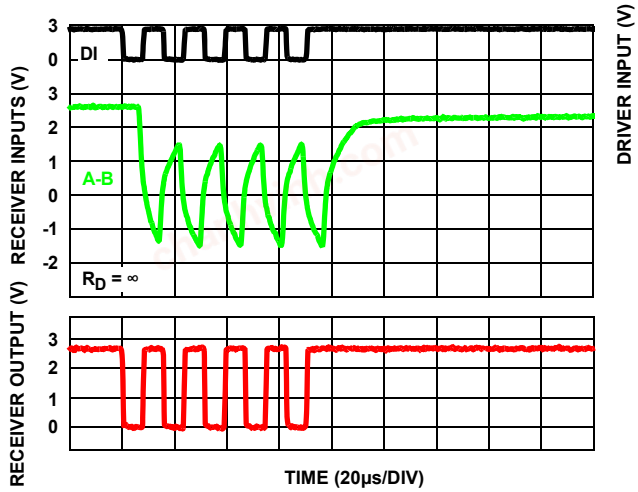


FIGURE 16. ISL32600E, ISL32601E PERFORMANCE WITH V_{CC} = 2.7V, 128kbps, 4000ft (1220m) CAT 5 CABLE

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Typical Performance Curves V_{CC} = 3V (ISL32600E, ISL32601E) or 1.8V (ISL32602E, ISL32603E), T_A = +25°C; unless otherwise specified (Continued)

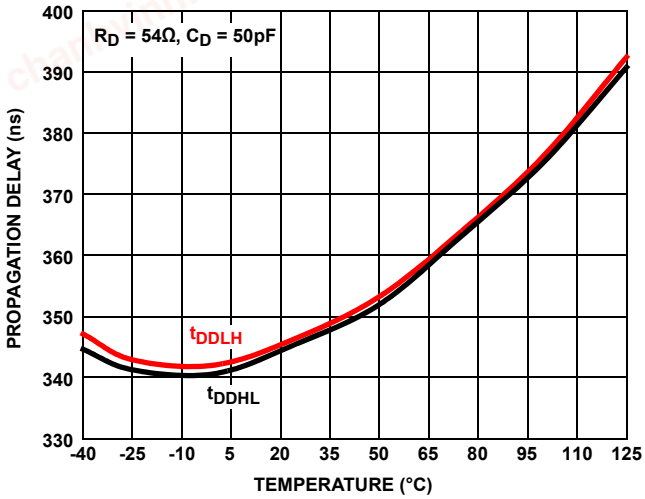


FIGURE 17. ISL32600E, ISL32601E DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE

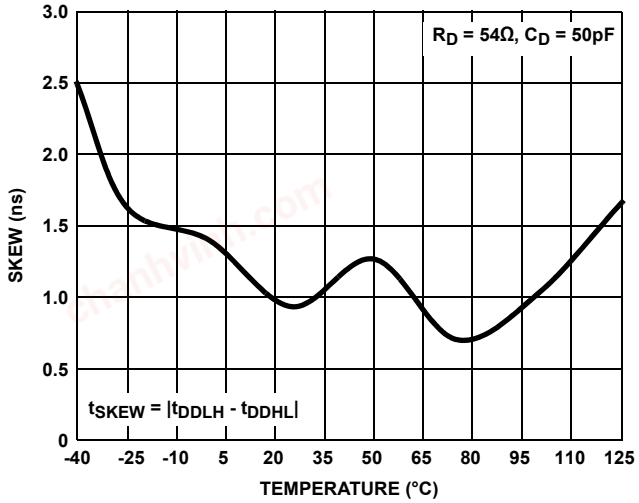


FIGURE 18. ISL32600E, ISL32601E DRIVER DIFFERENTIAL SKEW vs TEMPERATURE

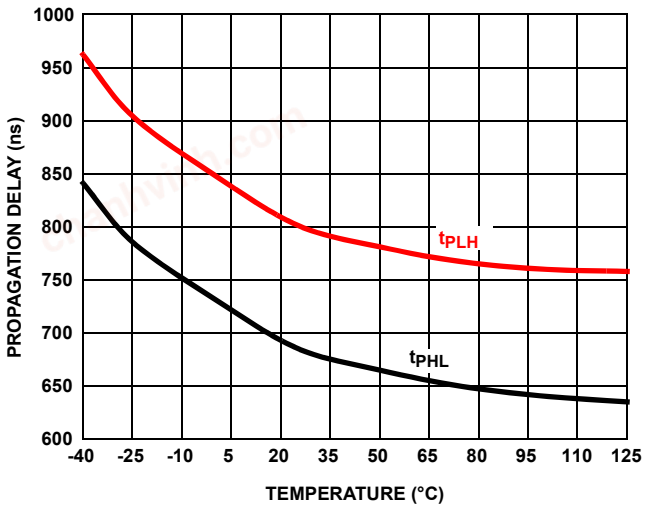


FIGURE 19. ISL32600E, ISL32601E RECEIVER PROPAGATION DELAY vs TEMPERATURE

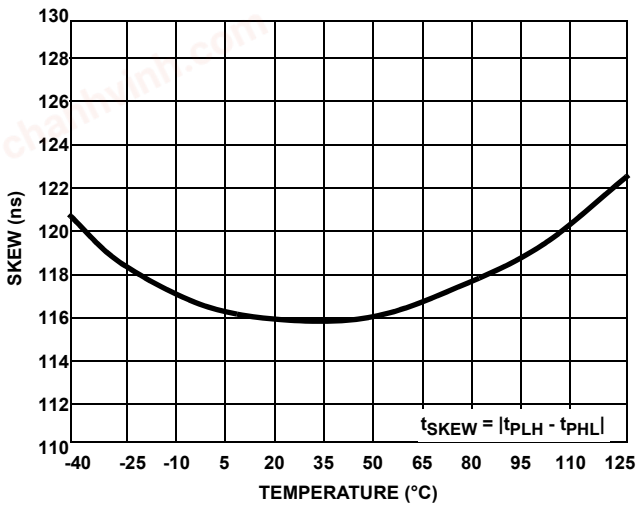


FIGURE 20. ISL32600E, ISL32601E RECEIVER SKEW vs TEMPERATURE

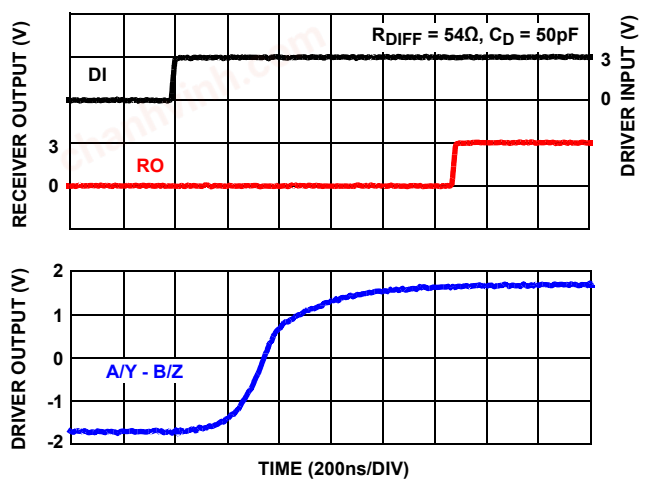


FIGURE 21. ISL32600E, ISL32601E DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH

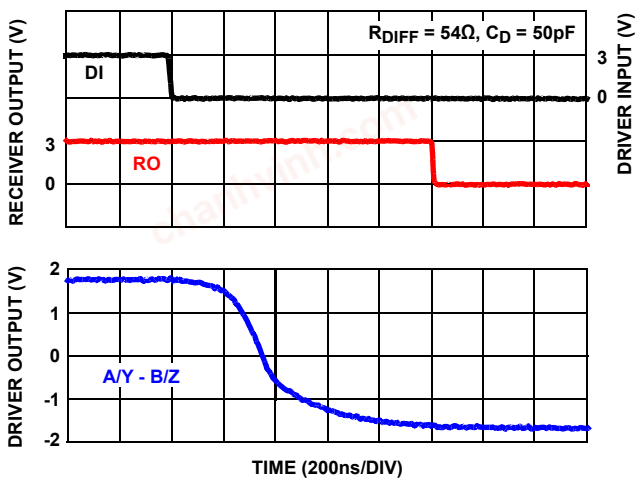


FIGURE 22. ISL32600E, ISL32601E DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW

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Typical Performance Curves V_{CC} = 3V (ISL32600E, ISL32601E) or 1.8V (ISL32602E, ISL32603E), T_A = +25°C; unless otherwise specified (Continued)

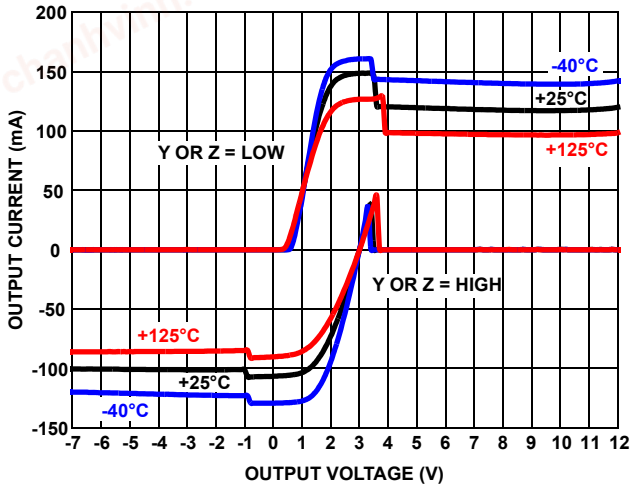


FIGURE 23. ISL32600E, ISL32601E DRIVER OUTPUT CURRENT vs SHORT-CIRCUIT VOLTAGE

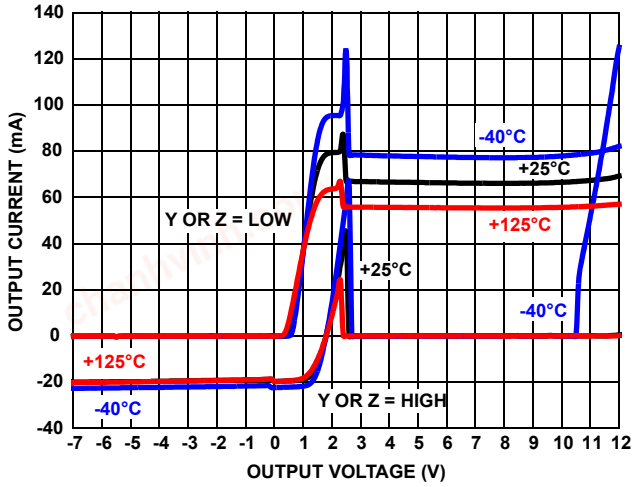


FIGURE 24. ISL32602E, ISL32603E DRIVER OUTPUT CURRENT vs SHORT-CIRCUIT VOLTAGE

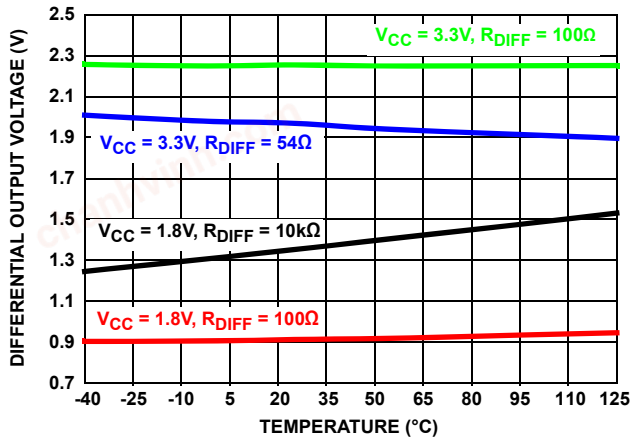


FIGURE 25. ISL32602E, ISL32603E DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

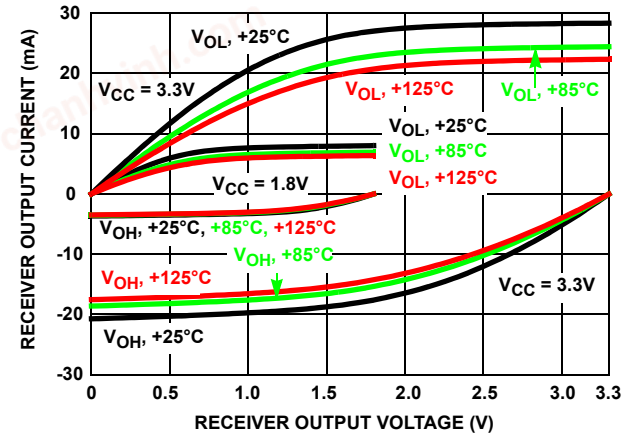


FIGURE 26. ISL32602E, ISL32603E RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

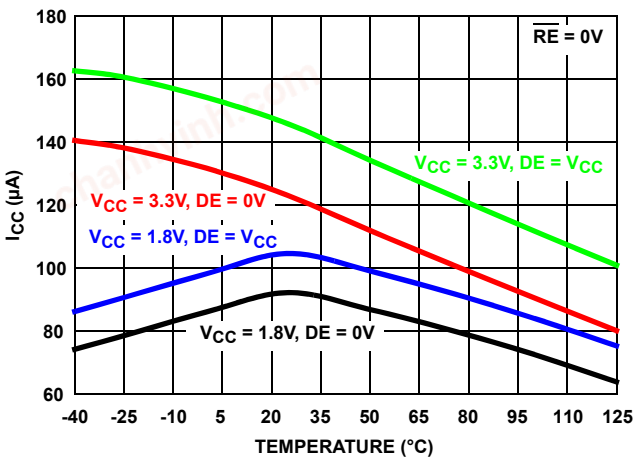


FIGURE 27. ISL32602E, ISL32603E STATIC SUPPLY CURRENT vs TEMPERATURE

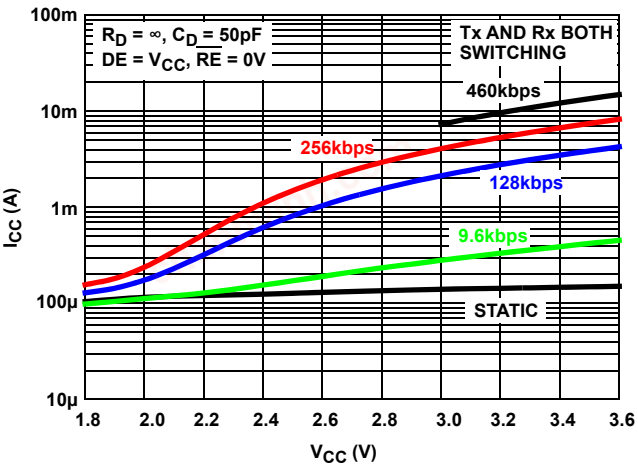


FIGURE 28. ISL32602E, ISL32603E DYNAMIC SUPPLY CURRENT vs SUPPLY VOLTAGE AT DIFFERENT DATA RATES

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Typical Performance Curves V_{CC} = 3V (ISL32600E, ISL32601E) or 1.8V (ISL32602E, ISL32603E), T_A = +25°C; unless otherwise specified (Continued)

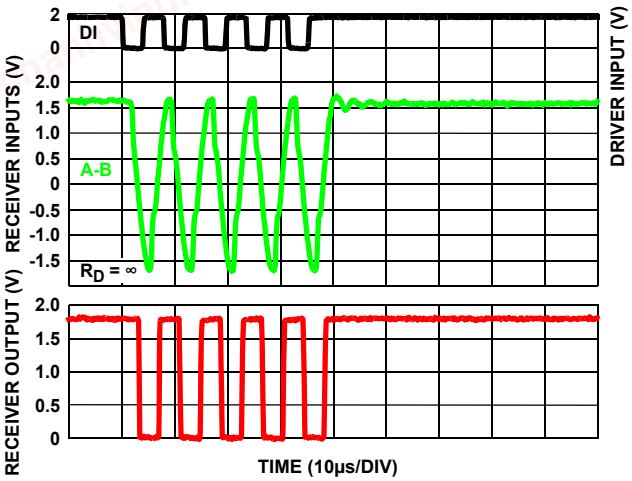


FIGURE 29. ISL32602E, ISL32603E PERFORMANCE WITH V_{CC} = 1.8V, 256kbps, 1000ft (305m) CAT 5 CABLE

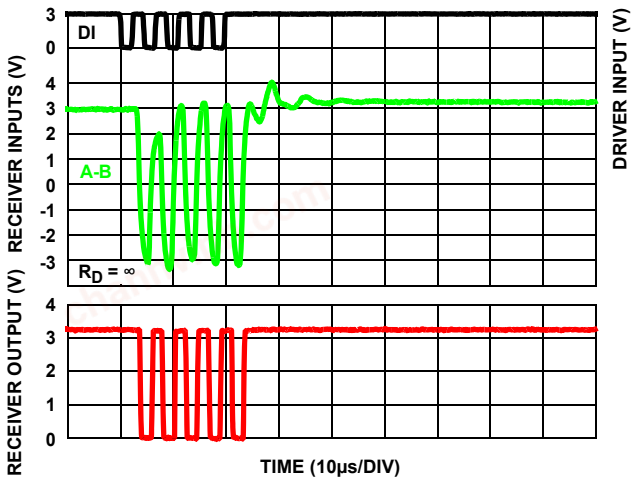


FIGURE 30. ISL32602E, ISL32603E PERFORMANCE WITH V_{CC} = 3.3V, 460kbps, 2000ft (610m) CAT 5 CABLE

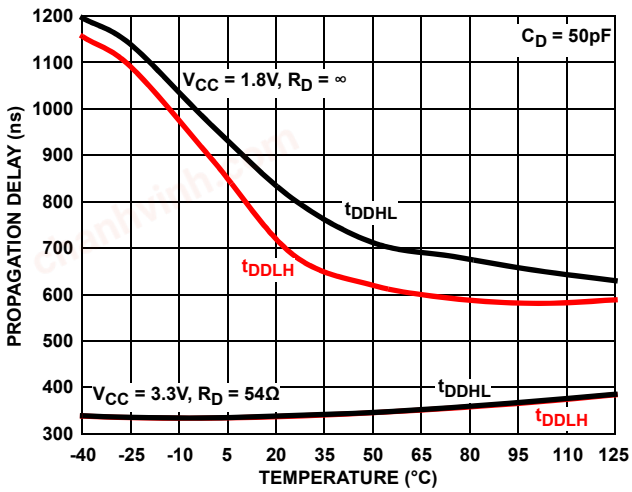


FIGURE 31. ISL32602E, ISL32603E DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE

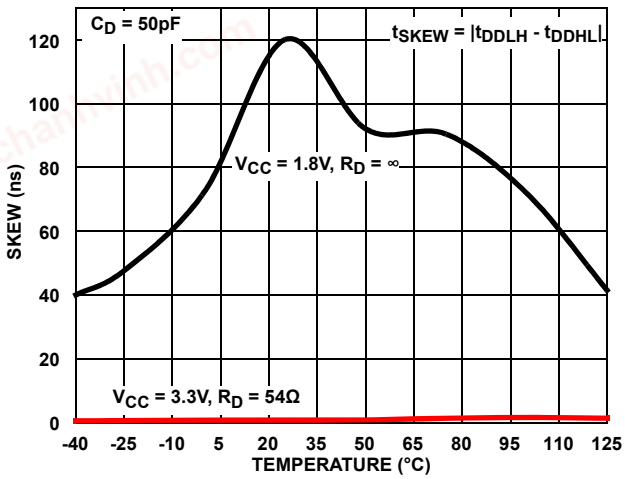


FIGURE 32. ISL32602E, ISL32603E DRIVER DIFFERENTIAL SKEW vs TEMPERATURE

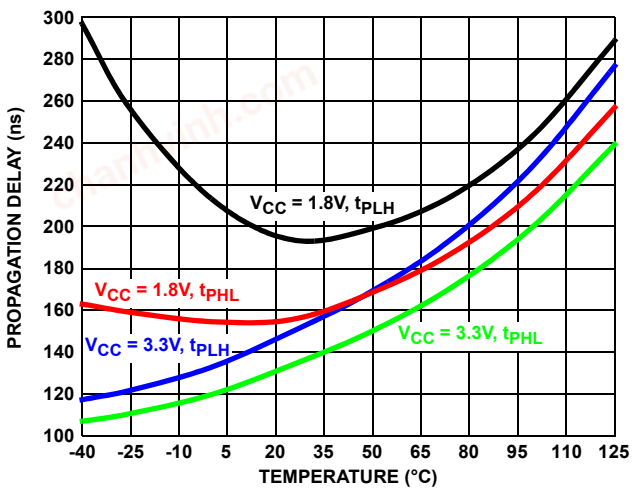


FIGURE 33. ISL32602E, ISL32603E RECEIVER PROPAGATION DELAY vs TEMPERATURE

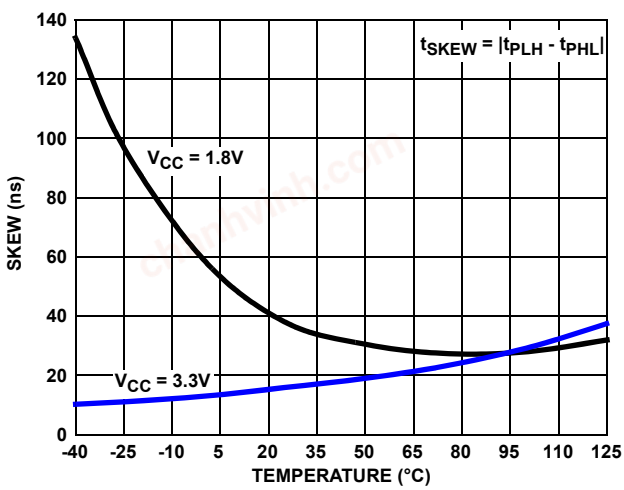


FIGURE 34. ISL32602E, ISL32603E RECEIVER SKEW vs TEMPERATURE

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Typical Performance Curves V_{CC} = 3V (ISL32600E, ISL32601E) or 1.8V (ISL32602E, ISL32603E), T_A = +25°C; unless otherwise specified **(Continued)**

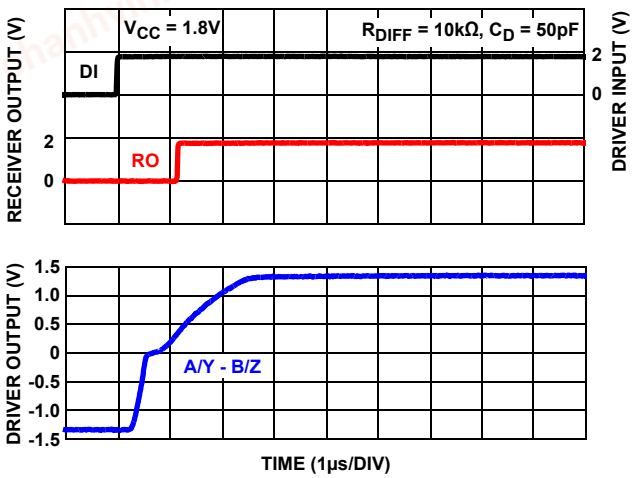


FIGURE 35. ISL32602E, ISL32603E DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH

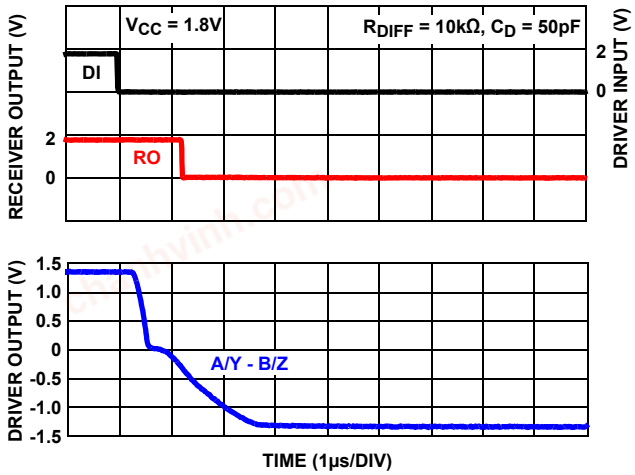


FIGURE 36. ISL32602E, ISL32603E DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW

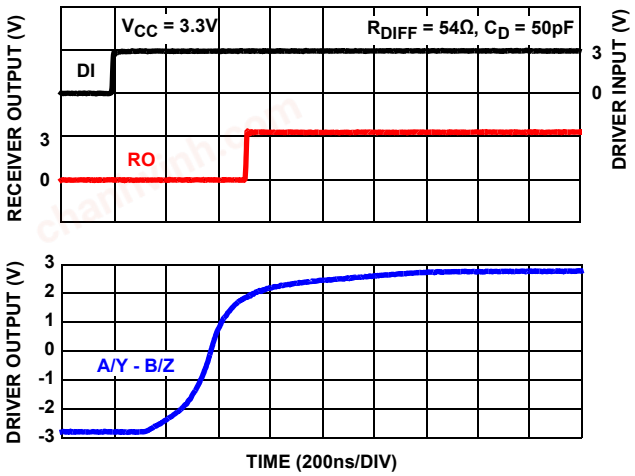


FIGURE 37. ISL32602E, ISL32603E DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH

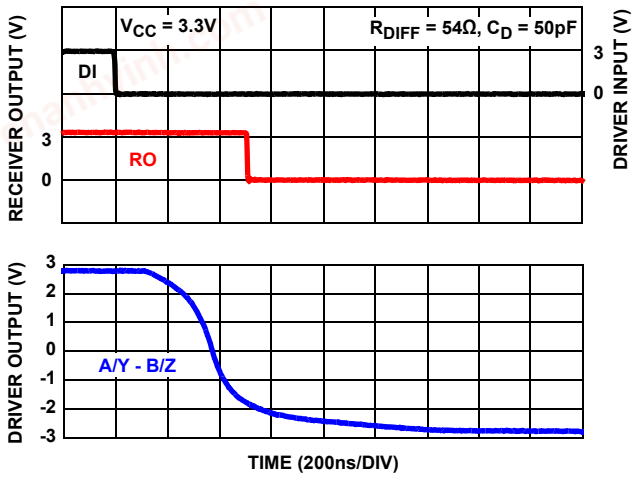


FIGURE 38. ISL32602E, ISL32603E DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

PROCESS:

Si Gate BiCMOS

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 receivers on each bus, assuming one unit load devices. RS-485 is a true multipoint standard, which allows up to 32 one-unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

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Another important advantage of RS-485 is the extended Common-Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from -7V to +12V. RS-422 and RS-485 are intended for runs as long as 4000ft, so the wide CMR is necessary to handle ground potential differences and voltages induced in the cable by external fields.

Receiver Features

The ISL3260xE devices use a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is greater than ±200mV, as required by the RS-422 and RS-485 specifications. The symmetrical ±200mV switching thresholds eliminate the duty cycle distortion that occurs on receivers with Full Fail Safe (FFS) functionality and with slowly transitioning input signals (see Figure 39). FFS receiver switching points have a negative offset, so the RO high time is naturally longer than the low time. The ISL3260xE's larger receiver input sensitivity range enables an increase of the receiver input hysteresis. The 40mV to 65mV receiver hysteresis increases the noise immunity, which is an advantage for noisy networks or networks with slow bus transitions.

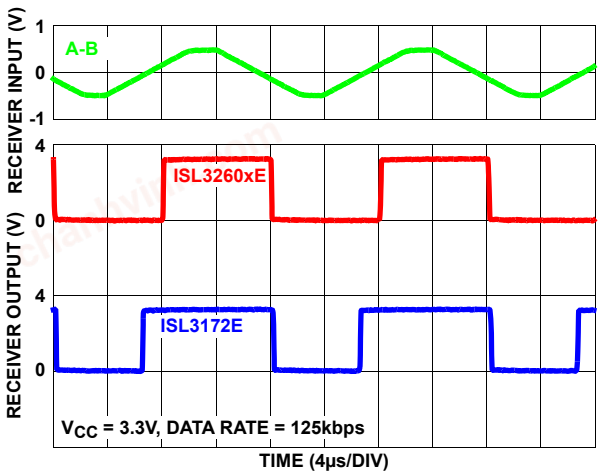


FIGURE 39. COMPARED WITH A FULL-FAILSAFE ISL3172E RECEIVER, THE SYMMETRICAL RX THRESHOLDS OF THE ISL3260xE DELIVER LESS OUTPUT DUTY CYCLE DISTORTION WHEN DRIVEN WITH SLOW INPUT SIGNALS

The receiver input resistance of 96kΩ surpasses the RS-422 specification of 4kΩ and is eight times the RS-485 Unit Load (UL) requirement of 12kΩ minimum. Therefore, these products are known as "one-eighth UL" transceivers and there can be up to 256 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common-mode voltages as great as +9V/-7V outside the power supplies (that is, +12V and -7V) at V_{CC} = 3V, making them ideal for long networks where induced voltages and ground potential differences are realistic concerns. The positive CMR is limited to +2V when the ISL32602E or ISL32603E is operated with V_{CC} = 1.8V.

All the receivers include a "fail-safe if open" function that assures a high level receiver output if the receiver inputs are unconnected (floating). Because the Rx is not FFS, terminated networks may require bus biasing resistors (pull-up on noninverting input, pull-down on inverting input) to preserve the bus idle state when the bus is not actively driven.

Receivers operate at data rates from 128kbps to 460kbps depending on the supply voltage, and all receiver outputs are tri-statable using the active low $\overline{RE}$ input. There are no parasitic diodes nor ESD diodes to V_{CC} on the $\overline{RE}$ input, so $\overline{RE}$ is tolerant of input voltages up to 5.5V, even with the ISL3260xE powered down (V_{CC} = 0V).

Driver Features

The ISL3260xE drivers are differential output devices that deliver at least 1.4V with $V_{CC} \geq 3V$ across a 54Ω load (RS-485) and at least 1.95V with $V_{CC} \geq 3.15V$ across a 100Ω load (RS-422). The 1.8V transmitters deliver a 1.1V unloaded, differential level. Drivers operate at data rates from 128kbps to 460kbps depending on the supply voltage, and they feature low propagation delay skews to maximize bit width. Driver outputs are slew rate limited to minimize EMI and to reduce reflections in unterminated or improperly terminated networks.

All drivers are tri-statable using the active high DE input. There are no parasitic diodes nor ESD diodes to V_{CC} on the DI and DE inputs, so these inputs are tolerant of input voltages up to 5.5V, even with the ISL3260xE powered down (V_{CC} = 0V).

1.8V Operation

The ISL32602E and ISL32603E are specifically designed to operate with supply voltages as low as 1.8V. Avoid termination resistors at this operating condition, and the unterminated driver is assured to deliver a healthy 1.1V differential output voltage. This low supply voltage limits the +CMR to +2V, but the CMR increases as V_{CC} increases.

For proper 1.8V operation, the ISL32602E and ISL32603E must run at a higher operating current. Therefore, their I_{CC} with V_{CC} = 3.3V is considerably higher than the I_{CC} of the ISL32600E and ISL32601E, which are optimized for low I_{CC} at 3.3V (see Figures 1 and 2).

Hot Plug Function

When a piece of equipment powers up, a period of time when the processor or ASIC driving the RS-485 control lines (DE, $\overline{RE}$) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the ISL3260xE devices incorporate a hot plug function. During power-up, circuitry monitoring V_{CC} ensures that the Tx and Rx outputs remain disabled for a period of time, regardless of the state of DE and $\overline{RE}$. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

ESD Protection

All pins on the ISL3260xE devices include Class 3 (>8kV) Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM and ±15kV IEC61000. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Touching the port pins, or connecting a cable, can cause an ESD event that can destroy unprotected ICs. The new ESD structures protect the device

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whether or not it is powered up without degrading the transceiver's CMR. The built-in ESD protection eliminates the need for board level protection structures such as transient suppression diodes and the associated undesirable capacitive load they present.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case), the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-485 pins allows the design of equipment meeting Level 4 criteria without the need for additional board level protection on the RS-485 port.

AIR-GAP DISCHARGE TEST METHOD

For the air-gap discharge test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc. so it is difficult to obtain repeatable results. The ISL3260xE RS-485 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, and eliminates the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. The ISL3260xE devices survive ±8kV contact discharges on the RS-485 pins.

Data Rate, Cables, and Terminations

RS-485/422 are intended for network lengths up to 4000ft (1220m), but the maximum system data rate decreases as the transmission length increases. The ISL32600E and ISL32601E operate at data rates up to 128kbps at the maximum (4000ft) distance, or at data rates of 256kbps for cable lengths less than 3000ft (915m). The ISL32602E and ISL32603E, with V_{CC} = 1.8V, are limited to 1000ft (305m) at 256kbps, or 2000ft (610m) at 128kbps. With V_{CC} = 3.3V, the ISL32602E and ISL32603E deliver 460kbps over 2000ft, 256kbps over 3000ft, or 128kbps over 4000ft cables.

Twisted pair is the cable of choice for RS-485 and RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals that are effectively rejected by the differential receivers in these ICs.

Short networks using these transceivers need not be terminated, but terminations are recommended for 2.7V to 3.6V powered networks unless power dissipation is an overriding concern. Terminations are not recommended for 1.8V applications due to the low drive available from those transmitters.

In point-to-point, or point-to-multipoint (single driver on bus) networks, terminate the main cable in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, keep stubs connecting receivers to the main cable as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Keep stubs connecting a transceiver to the main cable as short as possible.

Terminated networks using the ISL3260xE may require bus biasing resistors (pull-up on noninverting input, pull-down on inverting input) to preserve the bus idle state when the bus is not actively driven. Without bus biasing, the termination resistor collapses the undriven, differential bus voltage to 0V, which is an undefined level to the ISL3260xE Rx. Bus biasing forces a few hundred mV positive differential voltage on the undriven bus, which all RS-485 and RS-422 Rx interpret as a valid logic high.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. These devices meet this requirement using driver output short-circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry that ensures that the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes. Additionally, these devices use a foldback circuit which reduces the short-circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short-circuit condition, the ISL3260xE's thermal shutdown feature disables the drivers whenever the die temperature becomes excessive. Thermal shutdown eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops by about 20°C. If the condition persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers remain operational during thermal shutdown.

Low Power Shutdown Mode

These micro-power transceivers all use a fraction of the power required by their counterparts, but they also include a shutdown feature that reduces the already low quiescent I_{CC} to a 10nA trickle. These devices enter shutdown whenever the receiver and driver are *simultaneously* disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns (1200ns at V_{CC} = 1.8V). Disabling both the driver and the receiver for fewer than 50ns assures that the transceiver does not enter shutdown.

Note that most receiver and driver enable times increase when the transceiver enables from shutdown. See Notes 9 through 13 on page 10 for more information.

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

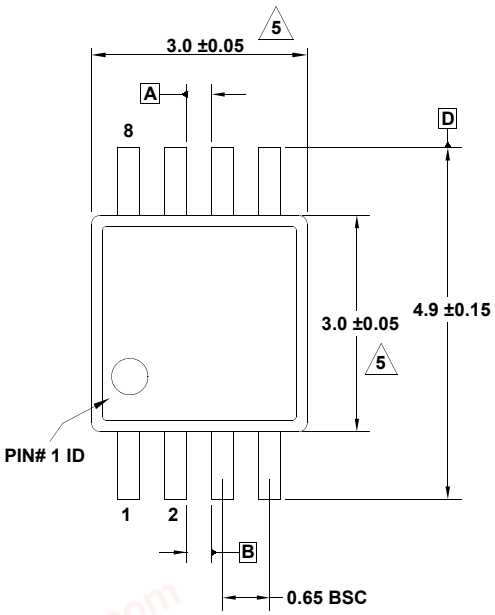
DATE	REVISION	CHANGE
May 28, 2021	3.0	Removed Related Literature section. Updated Ordering Information formatting. Updated Figures 3 and 4. Updated POD M8.118 to the latest revision, changes are as follows: -Corrected typo in the side view 1 updating package thickness tolerance from ±010 to ±0.10. Updated POD M8.15 to the latest revision, changes are as follows: -Added the coplanarity spec into the drawing. Updated POD M10.118 to the latest revision, changes are as follows: -Corrected typo in the side view 1 updating package thickness tolerance from ±010 to ±0.10. Updated POD M14.15 to the latest revision, changes are as follows: -In Side View B and Detail A Added lead length dimension (1.27 – 0.40) and Changed angle of the lead to 0-8 degrees.
Jan 31, 2019	2.0	Updated Figures 3 and 4. Updated ordering information table by adding all tape and reel parts and information and updating notes. Updated links throughout document. Removed About Intersil section. Updated disclaimer.
Oct 20, 2017	1.0	Added the Related Literature section. Updated the Truth Table on page 3. Applied Intersil A Renesas Company template.
June 22, 2012	0.0	Initial Release.

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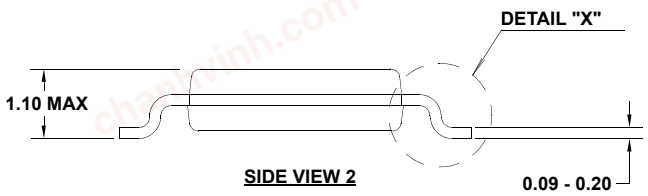
Package Outline Drawings

For the most recent package outline drawing, see M8.118.

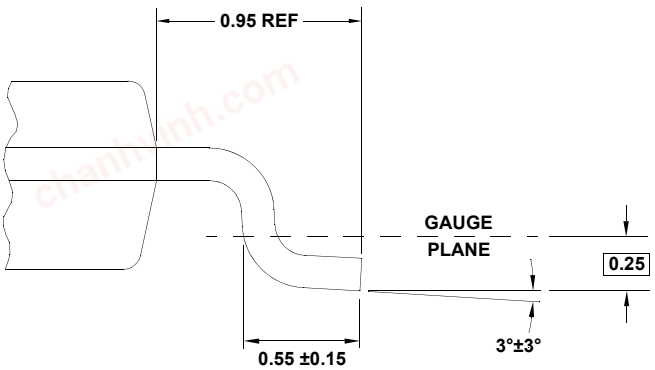
M8.118
8 Lead Mini Small Outline Plastic Package
Rev 5, 5/2021



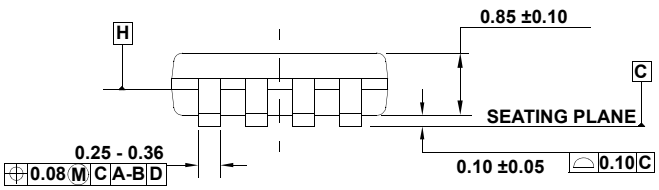
TOP VIEW



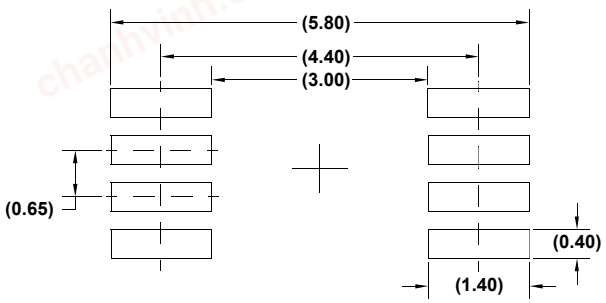
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

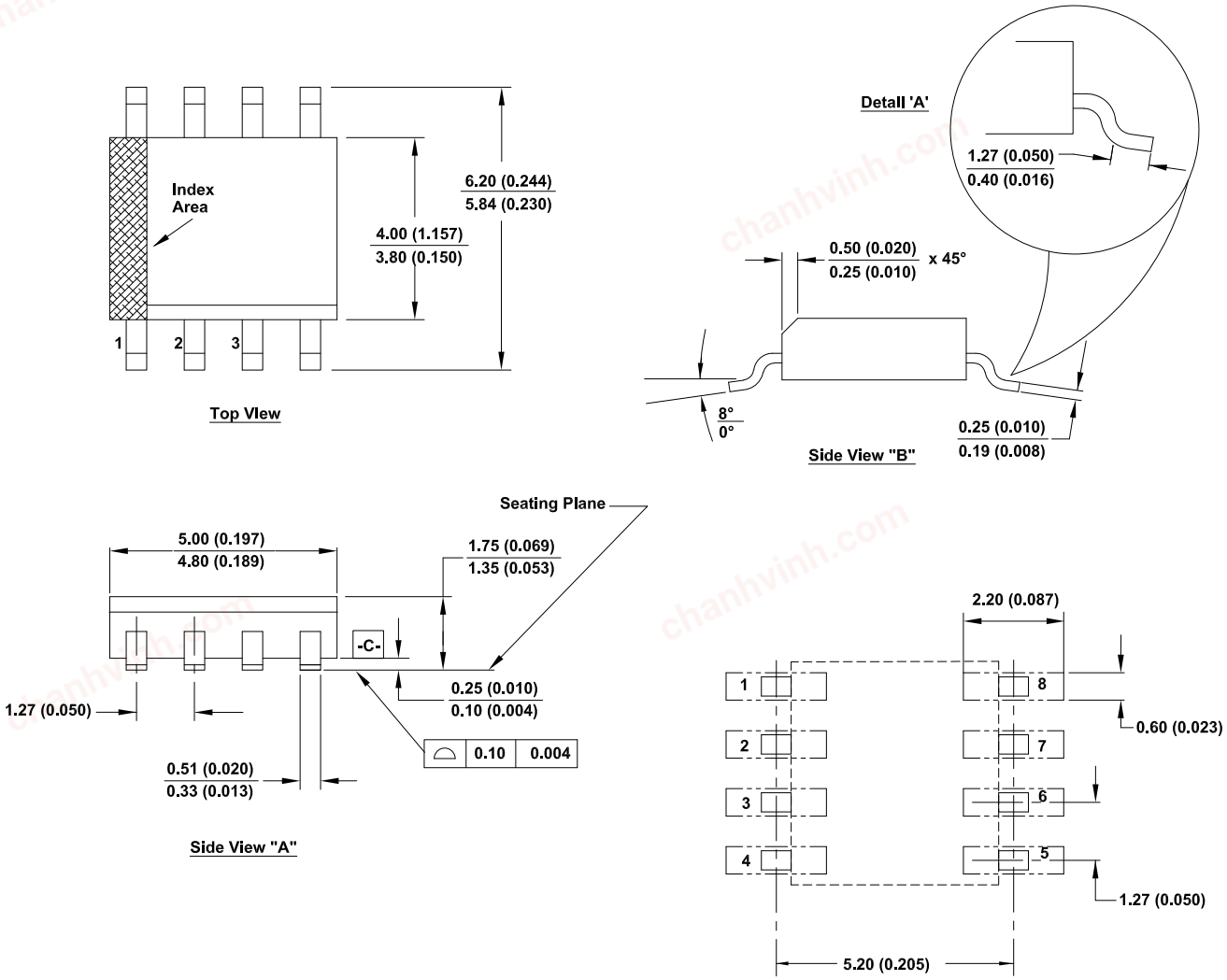
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

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For the most recent package outline drawing, see M8.15.

M8.15
8 Lead Narrow Body Small Outline Plastic Package
Rev 5, 4/2021



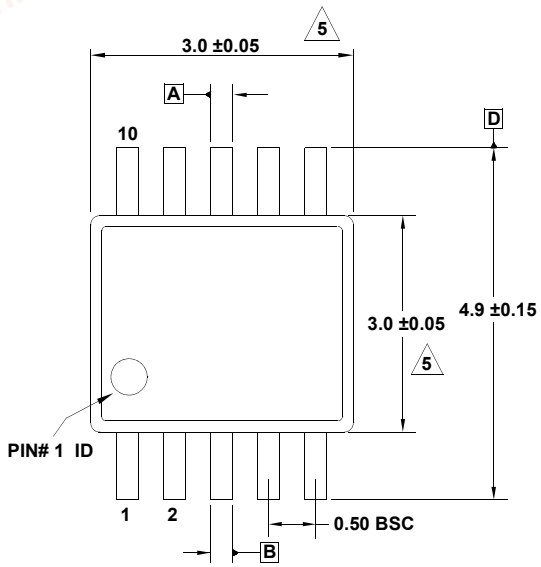
NOTES:

1. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
2. Package length does not include mold flash, protrustion or gate burrs. Mold flash, protrustion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrustions. Interlead flash and protrustions shallnot exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

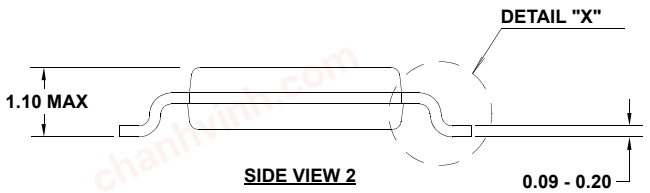
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For the most recent package outline drawing, see M10.118.

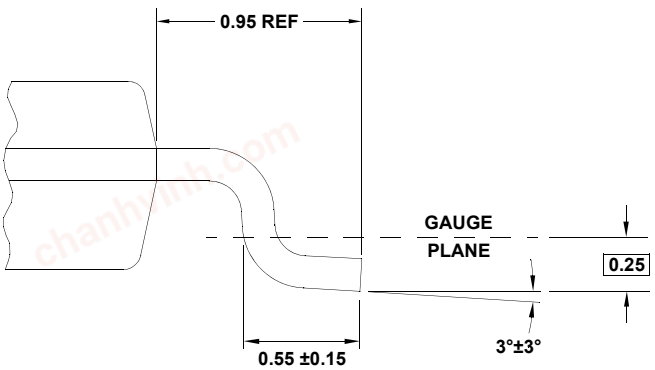
M10.118
10 Lead Mini Small Outline Plastic Package
Rev 2, 5/2021



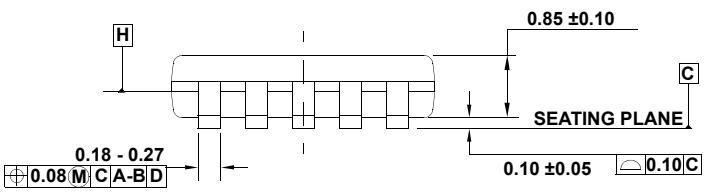
TOP VIEW



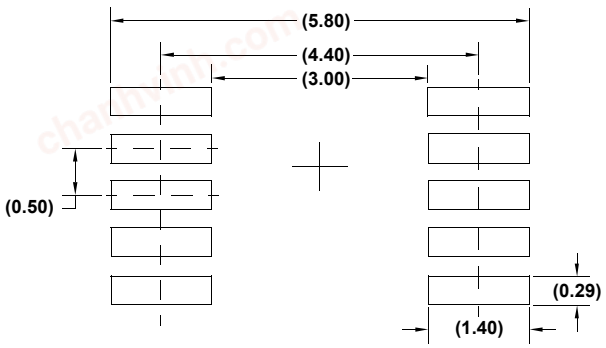
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

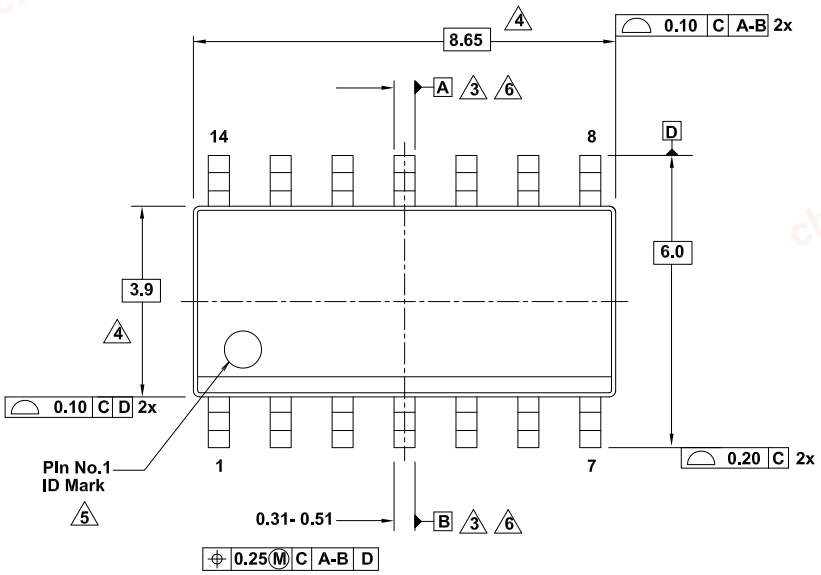
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

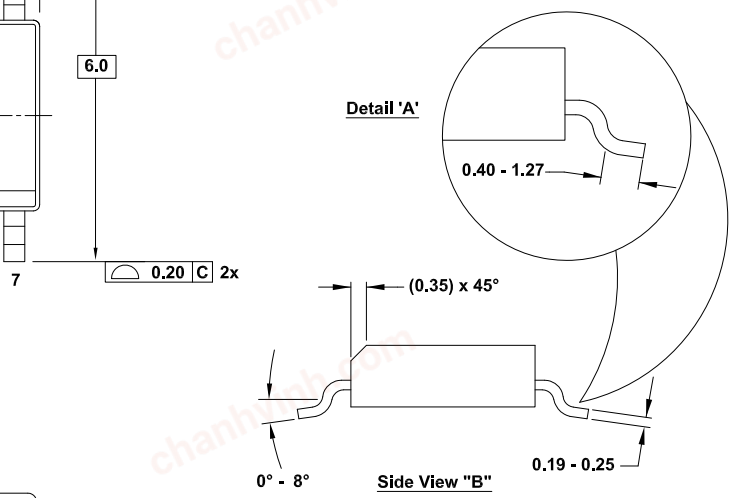
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For the most recent package outline drawing, see M14.15.

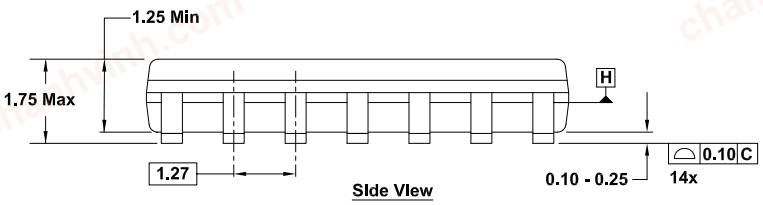
M14.15
14 Lead Narrow Body Small Outline Plastic Package
Rev 2, 6/20



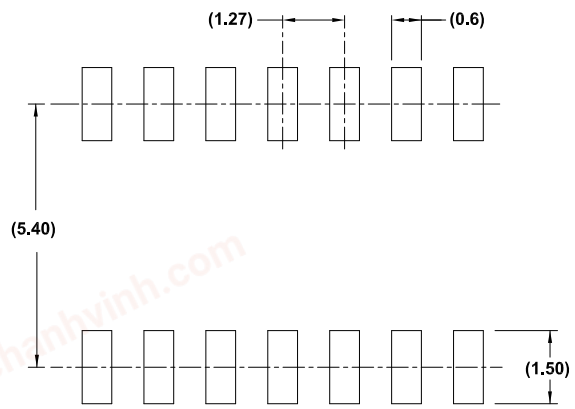
Top View



Side View "B"



Side View



Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Datums A and B are determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier can be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

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