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ISL32172E, ISL32272E, ISL32174E, ISL32179E

QUAD, ±16.5kV ESD Protected, 3.0V to 5.5V, Low Power, RS-422 Transmitters

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The ISL32172E, ISL32272E, ISL32174E, and ISL32179E are ±16.5kV IEC61000-4-2 ESD protected, 3.0V to 5.5V powered, QUAD transmitters for balanced communication using the RS-422 standard. These drivers have very low output leakage currents (±10µA), so they present a low load to the RS-422 bus.

The driver (Tx) outputs are tri-statable and incorporate a hot plug feature to keep them disabled during power-up and power-down. The ISL32172E and ISL32272E have a common EN/$\overline{EN}$, the ISL32174E has a two channel EN12/EN34, and the ISL32179E has a versatile combination of individual and group channel enables (see Table 1).

Only the ISL32179E driver can be slew-rate limited, and only at the data rate of 0.46Mbps. Drivers on the other versions are not limited, so they can achieve 10Mbps or 32Mbps data rates. All versions are offered in industrial and extended industrial (-40°C to +125°C) temperature ranges.

The ISL32179E's QFN package has a 50% smaller footprint compared to the TSSOP. The ISL32179E also features a logic supply pin (V_L) that sets the switching points of the enable and DI inputs to be compatible with a lower supply voltage in mixed voltage systems. Two speed select pins allow the ISL32179E to be configured for 460kbps, 10Mbps, or 32Mbps data rates. Individual channel and group enable pins increase the ISL32179E's flexibility.

Related Literature

For a full list of related documents, visit our website:

- ISL32172E, ISL32272E, ISL32174E, and ISL32179E device pages

Features

- IEC61000 ESD protection on RS-422 outputs . . . . ±16.5kV
  - Class 3 ESD level on all other pins . . . . . .12kV HBM
  - High machine model ESD level on all pins 700V
- Wide supply range . . . . . 3.0V to 5.5V
- Specified for +125°C operation
- Available in industry standard pinouts (ISL32172E, ISL32272E, ISL32174E) or in a space saving QFN (ISL32179E) with added features
- Logic supply pin (V_L) eases operation in mixed supply systems (ISL32179E only)
- User-selectable data rate (ISL32179E only)
- Hot plug Tx outputs remain tri-stated during power-up and power-down
- Low Tx leakage allows > 256 devices on the bus
- High data rates. . . . . up to 32Mbps
- Low quiescent supply current. . . . . 0.8mA (maximum)
  - Low shutdown supply current. 60µA
- Current limiting and thermal shutdown for driver overload protection
- Tri-statable Tx outputs
- 5V tolerant logic inputs when $V_{CC} \leq 5V$
- Pb-free (RoHS compliant)

Applications

- Telecom equipment
- Motor controllers/encoders
- Programmable logic controllers
- Industrial/process control networks

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	FUNCTION	DATA RATE (Mbps)	SLEW RATE LIMITED?	HOT PLUG?	V_L PIN?	TX ENABLE TYPE	QUIESCENT I_{CC} (mA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL32172E	4 Tx	32	NO	YES	NO	EN, $\overline{EN}$	<1	NO	16
ISL32272E	4 Tx	10	NO	YES	NO	EN, $\overline{EN}$	<1	NO	16
ISL32174E	4 Tx	32	NO	YES	NO	EN12, EN34	<1	NO	16
ISL32179E	4 Tx	32, 10, 0.46	SELECTABLE	YES	YES	Individual and group enables	<1	YES	24

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Typical Operating Circuits (1 of 4 Channels Shown)

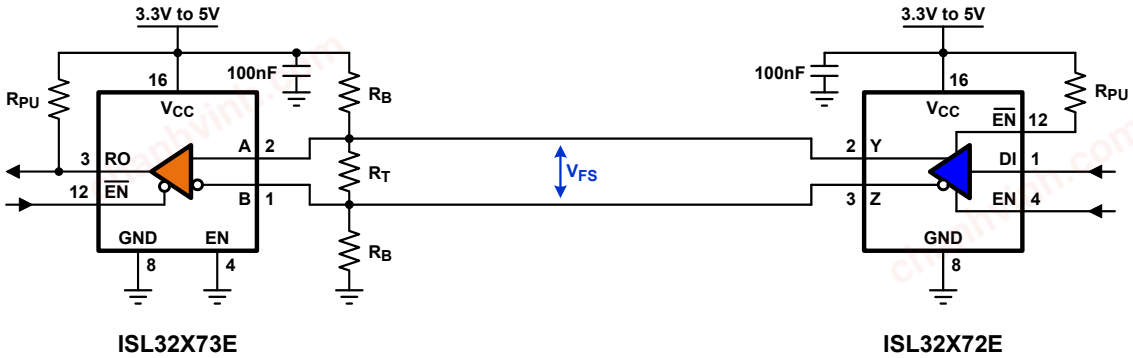


FIGURE 1. NETWORK USING GROUP ENABLES

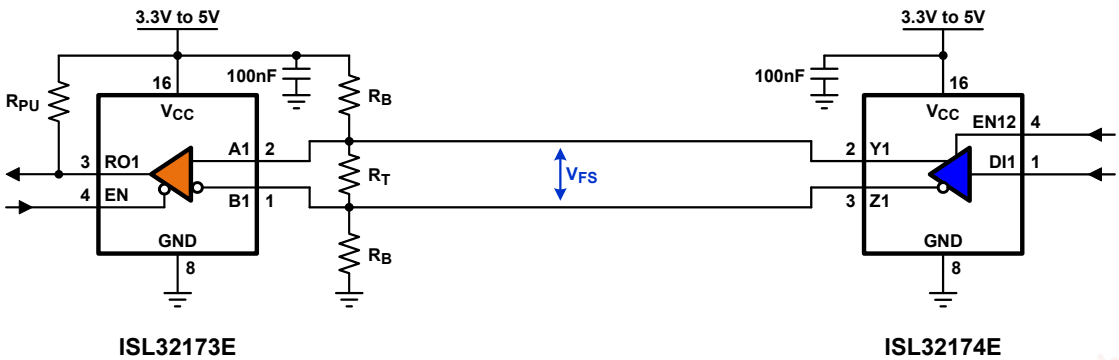
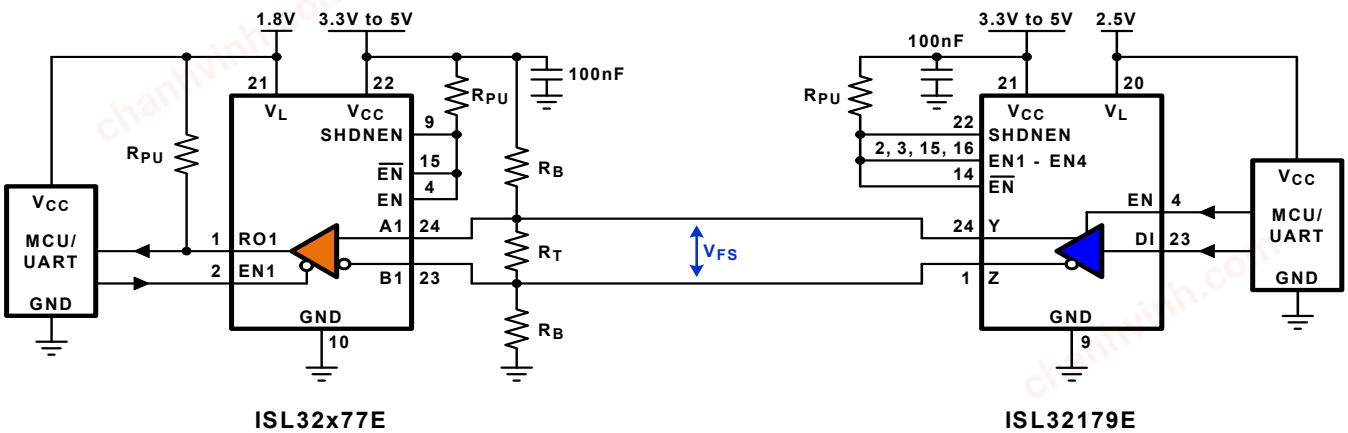


FIGURE 2. NETWORK USING PAIRED ENABLES



Using individual channel enable pins and configured for lowest shutdown supply current

Note: When using separate supplies, V_{CC} must be powered up before V_L

Using active group enable pins and configured for lowest shutdown supply current

Note: When using separate supplies, V_{CC} must be powered up before V_L

FIGURE 3. NETWORK WITH V_L PIN FOR INTERFACING TO LOWER VOLTAGE LOGIC DEVICES

Note: To calculate the resistor values, see TB509.

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Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL32172EFBZ	ISL32172 EFBZ	-40 to +125	-	16 Ld SOIC	M16.15
ISL32172EFBZ-T	ISL32172 EFBZ	-40 to +125	2.5k	16 Ld SOIC	M16.15
ISL32172EFVZ	32172 EFVZ	-40 to +125	-	16 Ld TSSOP	MDP0044
ISL32172EFVZ-T	32172 EFVZ	-40 to +125	2.5k	16 Ld TSSOP	MDP0044
ISL32172EIBZ	ISL32172 EIBZ	-40 to +85	-	16 Ld SOIC	M16.15
ISL32172EIBZ-T	ISL32172 EIBZ	-40 to +85	2.5k	16 Ld SOIC	M16.15
ISL32172EIVZ	32172 EIVZ	-40 to +85	-	16 Ld TSSOP	MDP0044
ISL32172EIVZ-T	32172 EIVZ	-40 to +85	2.5k	16 Ld TSSOP	MDP0044
ISL32174EFVZ	32174 EFVZ	-40 to +125	-	16 Ld TSSOP	MDP0044
ISL32174EFVZ-T	32174 EFVZ	-40 to +125	2.5k	16 Ld TSSOP	MDP0044
ISL32174EIBZ	ISL32174 EIBZ	-40 to +85	-	16 Ld SOIC	M16.15
ISL32174EIBZ-T	ISL32174 EIBZ	-40 to +85	2.5k	16 Ld SOIC	M16.15
ISL32179EFRZ	321 79EFRZ	-40 to +125	-	24 Ld QFN	L24.4x4C
ISL32179EFRZ-T	321 79EFRZ	-40 to +125	6k	24 Ld QFN	L24.4x4C
ISL32179EIRZ	321 79EIRZ	-40 to +85	-	24 Ld QFN	L24.4x4C
ISL32179EIRZ-T	321 79EIRZ	-40 to +85	6k	24 Ld QFN	L24.4x4C
ISL32272EFBZ	ISL32272 EFBZ	-40 to +125	-	16 Ld SOIC	M16.15
ISL32272EFBZ-T	ISL32272 EFBZ	-40 to +125	2.5k	16 Ld SOIC	M16.15
ISL32272EFVZ	32272 EFVZ	-40 to +125	-	16 Ld TSSOP	MDP0044
ISL32272EFVZ-T	32272 EFVZ	-40 to +125	2.5k	16 Ld TSSOP	MDP0044

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL32172E, ISL32272E, ISL32174E, and ISL32179E device pages. For more information about MSL, see TB363.

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Truth Tables

ISL32172E and ISL32272E				
INPUTS			OUTPUTS	
EN	$\overline{EN}$	DIX	ZX	YX
X	0	1/0	0/1	1/0
1	X	0/1	1/0	0/1
0	1	X	Z	Z

NOTE: Z = Tri-state

ISL32174E										
INPUTS			OUTPUTS							
EN12	EN34	DIX	Z1	Y1	Z2	Y2	Z3	Y3	Z4	Y4
0	0	X	Z	Z	Z	Z	Z	Z	Z	Z
0	1	1/0	Z	Z	Z	Z	0/1	1/0	0/1	1/0
1	0	1/0	0/1	1/0	0/1	1/0	Z	Z	Z	Z
1	1	1/0	0/1	1/0	0/1	1/0	0/1	1/0	0/1	1/0

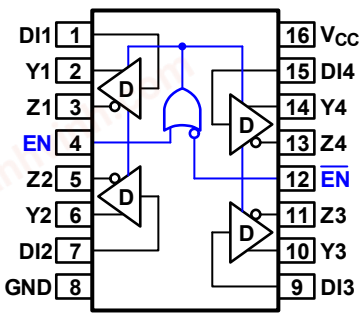
NOTE: Z = Tri-state

ISL32179E								
INPUTS						OUTPUTS		
ENX	EN	$\overline{EN}$	DIX	SPA	SPB	ZX	YX	COMMENTS
0	X	X	X	X	X	Z	Z	Ch X outputs disabled
X	0	1	X	X	X	Z	Z	All outputs disabled
1	X	0	1/0	1	1	0/1	1/0	Individual ENX controls Ch X (32Mbps)
1	1	X	0/1	1	1	1/0	0/1	
1	X	0	1/0	0	1	0/1	1/0	Individual ENX controls Ch X (10Mbps)
1	1	X	0/1	0	1	1/0	0/1	
1	X	0	1/0	X*	0	0/1	1/0	Individual ENX controls Ch X (460kbps)
1	1	X	0/1	X*	0	1/0	0/1	

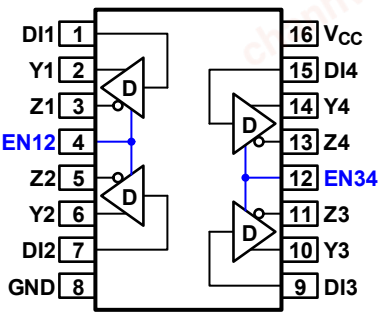
NOTE: *Keep SPA = 1 for lowest current in SHDN. If using individual channel enables and the SHDN mode, connect EN and $\overline{EN}$ to V_{CC} for the lowest SHDN current. The ISL32179E enters SHDN when SHDNEN = 1 and all channels are disabled. Z = Tri-state.

Pin Configurations

ISL32172E, ISL32272E
(16 LD N-SOIC, TSSOP)
TOP VIEWS



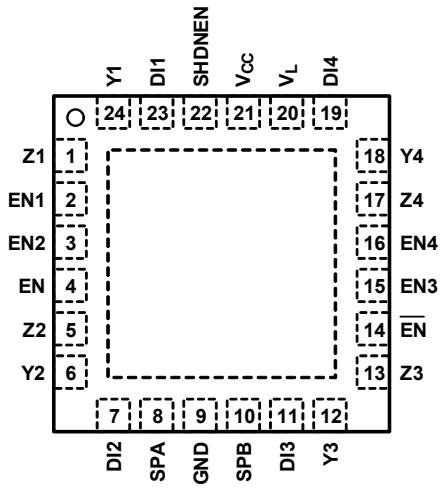
ISL32174E
(16 LD N-SOIC, TSSOP)
TOP VIEWS



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Pin Configurations (Continued)

ISL32179E
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
EN, $\overline{EN}$	Group driver output enables that are internally pulled high to V_{CC}. All ISL32x72E driver outputs, Y and Z, are enabled by driving EN high OR $\overline{EN}$ low. The outputs are high impedance when EN is low AND $\overline{EN}$ is high (for example, if using only the active high EN, connect $\overline{EN}$ directly to V_{CC} or V_L; if using only the active low $\overline{EN}$, connect EN directly to GND). To use group enable on the ISL32179E, connect all the ENX pins to V_{CC} or V_L and use the EN or $\overline{EN}$ pin as previously described. If the group driver enable function is not required (see Note 4), connect EN to V_{CC}, or connect $\overline{EN}$ to GND (ISL32x72E and ISL32179E only).
EN12, EN34	Paired driver output enables that are internally pulled high to V_{CC}. Driving EN12 (EN34) high enables the Channel 1 and 2 (3 and 4) outputs (Y and Z). Driving EN12 (EN34) low disables Channel 1 and 2 (3 and 4) outputs. If the driver enable function is not required (see Note 4), connect EN12 and EN34 to V_{CC} (ISL32174E only).
ENx	Individual driver output enables that are internally pulled high to V_{CC}. Forcing ENx high with EN high OR $\overline{EN}$ low enables the channel X outputs (Y and Z). Driving ENX low disables the Channel X outputs regardless of the states of EN and $\overline{EN}$. Connect both EN and $\overline{EN}$ to V_{CC} for the lowest SHDN current if using SHDN mode (see SHDNEN below). If the individual driver enable function is not required (see Note 4), connect ENX to V_{CC} (ISL32179E only).
SHDNEN	Low power SHDN mode enable. A high level allows the ISL32179E to enter a low power mode when all channels are disabled. A low level prevents the device from entering the low power mode (ISL32179E only).
DIx	Driver input. A low on DI forces the corresponding channel's output Y low and output Z high. A high on DI forces output Y high and output Z low.
SPA, SPB	Speed select inputs that are internally pulled high. See the ISL32179E truth table on page 4 (ISL32179E only).
GND	Ground connection. This is also the potential of the QFN thermal pad.
Yx	±16.5kV IEC61000-4-2 ESD protected RS-422 level and a noninverting transmitter output.
Zx	±16.5kV IEC61000-4-2 ESD protected RS-422 level and an inverting transmitter output.
V_{CC}	System power supply input (3.0V to 5.5V). Power up V_{CC} first on devices with a V_L pin powered from a separate supply.
V_L	Logic power supply input. Connecting the V_L pin to the lower voltage power supply of a logic device (such as a UART or microcontroller) interfacing with the ISL32179E configures its logic pin (DI, EN (all varieties), SHDNEN, and SP) V_{IL}/V_{IH} levels to values compatible with the lower supply voltage. If V_L and V_{CC} are different supplies, power up this supply after V_{CC} and keep $V_L \leq V_{CC}$. (ISL32179E only)
EP	Thermal pad. Connect EP to GND (ISL32179E only).

NOTE:

4. Tie unused EN pins with a 1k resistor to V_{CC}.

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Absolute Maximum Ratings

V_{CC} to GND 7V
V_L to GND (ISL32179E Only)..... -0.3V to (V_{CC} +0.3V)
Input Voltages
DI, EN (all varieties) ..... -0.3V to 7V
Output Voltages
Y, Z ..... -0.5V to 7V
Output Current
Y, Z (per output, continuous, $T_J \le 125°C$)..... 100mA
ESD Rating ..... See Electrical Specifications Table on page 7

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld SOIC Package (Note 5).....	80	N/A
16 Ld TSSOP Package (Note 5)	105	N/A
24 Ld QFN Package (Notes 6, 7)	42	5

Maximum Junction Temperature (Plastic Package) .... +150°C
Maximum Storage Temperature Range .....-65°C to +150°C
Pb-free Reflow Profile ..... see TB493

Operating Conditions

Temperature Range
ISL32x7xEF .....-40°C to +125°C
ISL32x7xEI .....-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379 for details.
7. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V; $V_L = V_{CC}$ (ISL32179E only); Typicals are at V_{CC} = 3.3V or V_{CC} = 5V, T_A = +25°C unless otherwise specified (Notes 8, 12).

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
DC CHARACTERISTICS								
Differential V_{OUT}	V_{OD}	No load		Full	2.5	-	V_{CC}	V
		R_L = 100Ω (RS-422) (see Figure 4)	$V_{CC} \ge 3V$	Full	2	2.6	-	V
			$V_{CC} \ge 4.5V$	Full	3	4	-	V
Single-Ended V_{OUT} (Y or Z)	V_O	I_O = -20mA, V_{OH}		Full	2.4	2.7	-	V
		I_O = 20mA, V_{OL}		Full	-	0.2	0.4	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 100Ω (see Figure 4)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 100Ω (see Figure 4)		Full	-	2.6	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 100Ω (see Figure 4)		Full	-	0.01	0.2	V
Input High Voltage (Logic Pins, Note 16)	V_{IH1}	All Transmitters and ISL32179E, if $V_L = V_{CC}$	3.0V ≤ VCC ≤ 3.6V, DI and ENs	Full	2.2	-	-	V
	V_{IH2}		4.5V≤V_{CC} ≤ 5.5V, DI	Full	2.7	-	-	V
	V_{IH2E}		4.5V≤V_{CC} ≤ 5.5V, ENs	Full	2.4	-	-	V
	V_{IH3}	ISL32179E only	2.7V ≤ V_L < 3.0V	Full	2.0	-	-	V
	V_{IH4}		2.3V ≤ V_L < 2.7V	Full	1.6	-	-	V
	V_{IH5}		1.6V ≤ V_L < 2.3V	Full	0.72*V_L	-	-	V
	V_{IH6}		1.5V ≤ V_L < 1.6V	+25	-	0.45*V_L	-	V
Input Low Voltage (Logic Pins, Note 16)	V_{IL1}	All Transmitters and ISL32179E, if $V_L = V_{CC}$		Full	-	-	0.8	V
	V_{IL2}	ISL32179E only	$V_L \ge 2.7V$	Full	-	-	0.6	V
	V_{IL3}		2.3V ≤ V_L < 2.7V	Full	-	-	0.6	V
	V_{IL4}		1.6V ≤ V_L < 2.3V	Full	-	-	0.22*V_L	V
	V_{IL5}		1.5V ≤ V_L < 1.6V	+25	-	0.25*V_L	-	V

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Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V; V_L = V_{CC} (ISL32179E only); Typicals are at V_{CC} = 3.3V or V_{CC} = 5V, T_A = +25°C unless otherwise specified (Notes 8, 12). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Logic Input Current	I_{IN1}	DIX = 0V or V_{CC}		Full	-1	-	1	µA
	I_{IN2}	SP, EN, $\overline{EN}$, ENX, SHDNEN = 0V or V_{CC}		Full	-15	9	15	µA
	I_{IN3}	EN12, EN34 = 0V or V_{CC}		Full	-30	18	30	µA
Output Leakage Current (Y, Z)	I_{OZ}	EN = 0, V_{CC} = 0V to 5.5V, -0.25 ≤ V_O ≤ 6V		Full	-10	-	10	µA
		EN = 0, V_{CC} = 3V to 5.5V, V_O = 0V to V_{CC}		+25	-8	-	8	nA
				(Note 18)	-30	-	30	nA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	EN = 1, V_Y or V_Z = 0V (Note 9)		Full	-	-	±150	mA
		EN = 1, V_Y or V_Z = V_{CC} (Note 9)		Full	-	-	±200	mA
Thermal Shutdown Threshold	T_{SD}			Full	-	160	-	°C
SUPPLY CURRENT								
No-Load Supply Current	I_{CC}	DI = 0V or V_{CC}, EN = 1		Full	-	0.6	0.8	mA
Shutdown Supply Current	I_{SHDN}	DI = 0V or V_{CC}, all outputs disabled (Note 17), SHDNEN = 1 (ISL32179E only)		Full	-	60	90	µA
ESD PERFORMANCE								
RS-422 Pins (Y, Z)		IEC61000-4-2, from bus pins to GND	Air gap	+25	-	±16.5	-	kV
			Contact	+25	-	±9	-	kV
		Human Body Model, from bus pins to GND		+25	-	±15	-	kV
All Pins		HBM, per MIL-STD-883 Method 3015		+25	-	±12	-	kV
		Machine Model		+25	-	700	-	V
DRIVER SWITCHING CHARACTERISTICS (ISL32179E, 460kbps)								
Maximum Data Rate	f_{MAX}	V_{OD} = ±1.5V, C_D = 820pF (see Figure 7)		Full	460	4000	-	kbps
Driver Single-Ended Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	-	90	300	ns
Driver Single-Ended Output Skew	t_{SSK}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	-	55	150	ns
Channel-to-Channel Output Delay Skew	t_{SKCC}	(Figure 5, Note 13)		Full	-	60	200	ns
Part-to-Part Output Delay Skew	t_{SKPP}	(Figure 5, Note 10)		Full	-	-	300	ns
Driver Differential Output Skew	t_{DSK}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	-	2	60	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	60	100	220	ns
Driver Enable to Output High	t_{ZH}	SW = GND (see Figure 6, Note 14)		Full	-	-	200	ns
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (see Figure 6, Note 14)		Full	-	-	200	ns
Driver Disable from Output High	t_{HZ}	SW = GND (see Figure 6)		Full	-	-	100	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (see Figure 6)		Full	-	-	100	ns
Driver Enable from SHDN to High	t_{SDH}	ISL32179E only, SW = GND (see Figure 6, Note 15)		Full	-	-	750	ns
Driver Enable from SHDN to Low	t_{SDL}	ISL32179E only, SW = V_{CC} (see Figure 6, Note 15)		Full	-	-	750	ns
DRIVER SWITCHING CHARACTERISTICS (ISL32272E, ISL32179E, 10Mbps)								
Maximum Data Rate	f_{MAX}	V_{OD} = ±1.5V, C_D = 400pF (see Figure 7)		Full	10	20	-	Mbps
Driver Single-Ended Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	-	13	25	ns
Driver Single-Ended Output Skew	t_{SSK}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	-	2	9	ns
Channel-to-Channel Output Delay Skew	t_{SKCC}	(Figure 5, Note 13)		Full	-	6	12	ns
Part-to-Part Output Delay Skew	t_{SKPP}	(Figure 5, Note 10)		Full	-	-	20	ns
Driver Differential Output Skew	t_{DSK}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	-	2	6	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	7	11	20	ns
Driver Enable to Output High	t_{ZH}	SW = GND (see Figure 6, Note 14)		Full	-	-	20	ns
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (see Figure 6, Note 14)		Full	-	-	20	ns

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Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V; V_L = V_{CC} (ISL32179E only); Typicals are at V_{CC} = 3.3V or V_{CC} = 5V, T_A = +25°C unless otherwise specified (Notes 8, 12). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Driver Disable from Output High	t_{HZ}	SW = GND (see Figure 6)	Full	-	-	20	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (see Figure 6)	Full	-	-	20	ns
Driver Enable from SHDN to High	t_{SDH}	ISL32179E only, SW = GND (see Figure 6, Note 15)	Full	-	-	750	ns
Driver Enable from SHDN to Low	t_{SDL}	ISL32179E only, SW = V_{CC} (see Figure 6, Note 15)	Full	-	-	750	ns
DRIVER SWITCHING CHARACTERISTICS (ISL32172E, ISL32174E, ISL32179E, 32Mbps)							
Maximum Data Rate	f_{MAX}	V_{OD} = ±1.5V, C_D = 100pF (see Figure 7)	Full	32	50	-	Mbps
Driver Single-Ended Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)	Full	3	8	15	ns
Driver Single-Ended Output Skew	t_{SSK}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)	Full	-	1	3.5	ns
Channel-to-Channel Output Delay Skew	t_{SKCC}	(Figure 5, Note 13)	Full	-	3	5.5	ns
Part-to-Part Output Delay Skew	t_{SKPP}	(Figure 5, Note 10)	Full	-	-	8	ns
Driver Differential Output Skew	t_{DSK}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)	Full	-	0.5	2	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)	Full	-	7	12	ns
Driver Enable to Output High	t_{ZH}	SW = GND (see Figure 6, Note 14)	Full	-	-	20	ns
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (see Figure 6, Note 14)	Full	-	-	20	ns
Driver Disable from Output High	t_{HZ}	SW = GND (see Figure 6)	Full	-	-	20	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (see Figure 6)	Full	-	-	20	ns
Driver Enable from SHDN to High	t_{SDH}	ISL32179E only, SW = GND (see Figure 6, Note 15)	Full	-	-	750	ns
Driver Enable from SHDN to Low	t_{SDL}	ISL32179E only, SW = V_{CC} (see Figure 6, Note 15)	Full	-	-	750	ns

NOTES:

8. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
9. Applies to peak current. See "Typical Performance Curves" beginning on page 10 for more information.
10. t_{SKPP} is the magnitude of the difference in propagation delays of the specified terminals of two units tested with identical test conditions (V_{CC}, temperature, etc.).
11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
12. EN = 0 indicates that the output(s) under test are disabled via the appropriate logic pin settings. EN = 1 indicates that the logic pins are set to enable the output(s) under test.
13. Channel-to-channel skew is the magnitude of the worst case delta between any two propagation delays of any two outputs on the same IC at the same test conditions.
14. Keep SHDNEN low to avoid entering shutdown (ISL32179E only).
15. Keep SHDNEN high to enter shutdown when all transmitters are disabled (ISL32179E only).
16. Logic pins are the DIs, the enable variants, and SHDNEN.
17. Only one of the SPX pins low, plus EN1-EN4 low with EN and $\overline{EN}$ high, or EN low and $\overline{EN}$ high with EN1-EN4 high.
18. Temperature range is -20°C to +40°C.

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Test Circuits and Waveforms

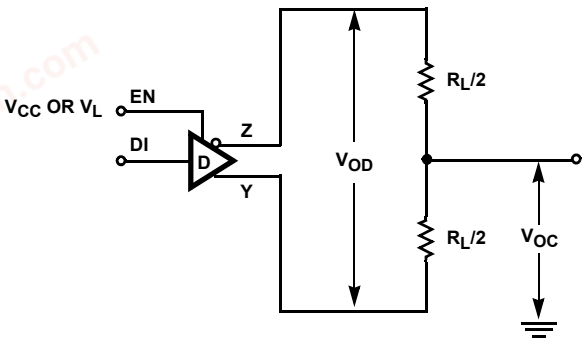


FIGURE 4. DC DRIVER TEST CIRCUITS

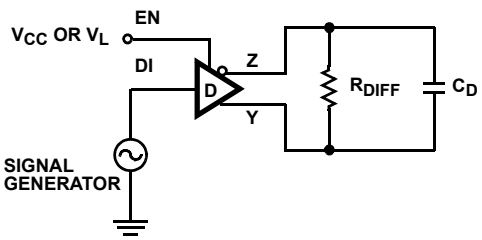


FIGURE 5A. TEST CIRCUIT

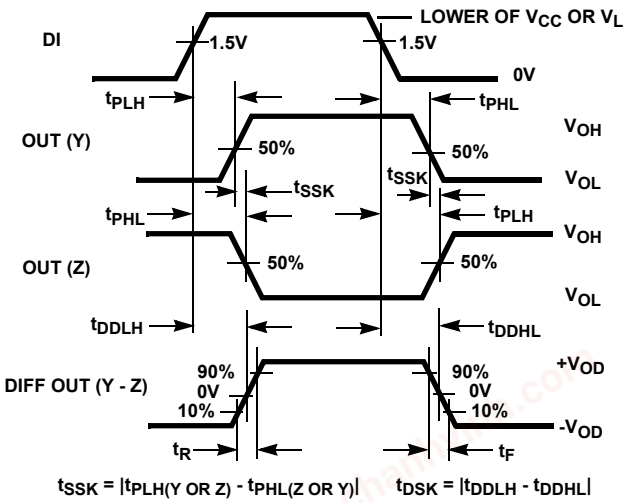
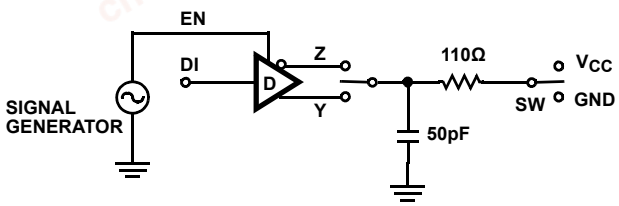


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	DI	SW
t_{HZ}	Y/Z	1/0	GND
t_{LZ}	Y/Z	0/1	V_{CC}
t_{ZH} (Note 14)	Y/Z	1/0	GND
t_{ZL} (Note 14)	Y/Z	0/1	V_{CC}
t_{SDH} (Note 15)	Y/Z	1/0	GND
t_{SDL} (Note 15)	Y/Z	0/1	V_{CC}

FIGURE 6A. TEST CIRCUIT

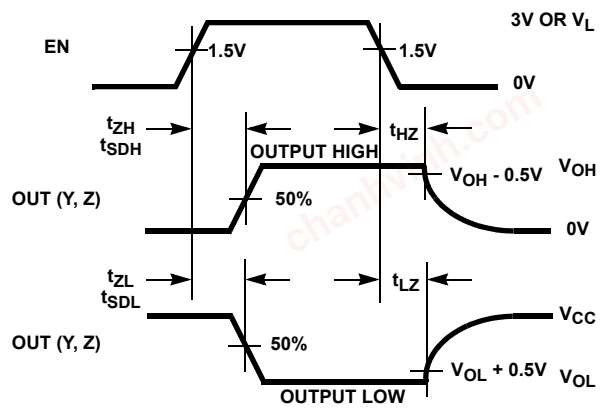


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. DRIVER ENABLE AND DISABLE TIMES

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Test Circuits and Waveforms (Continued)

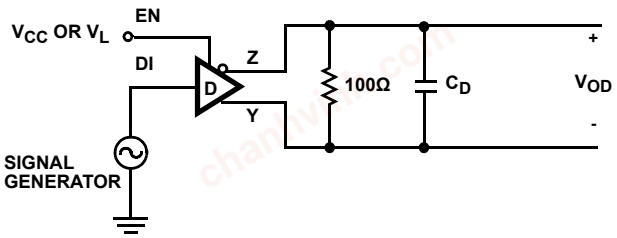


FIGURE 7A. TEST CIRCUIT

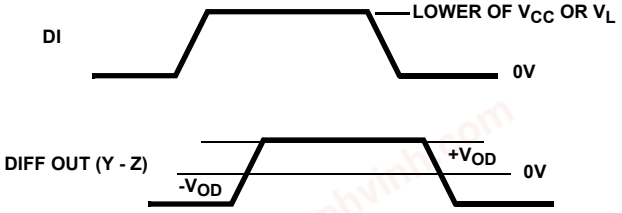


FIGURE 7B. MEASUREMENT POINTS

FIGURE 7. DRIVER DATA RATE

Typical Performance Curves

VCC = VL = 3.3V or 5V, TA = +25°C, unless otherwise specified. V_L notes apply to the ISL32179E only.

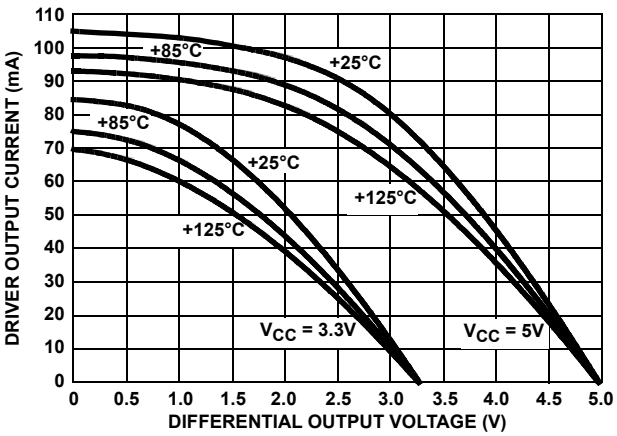


FIGURE 8. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

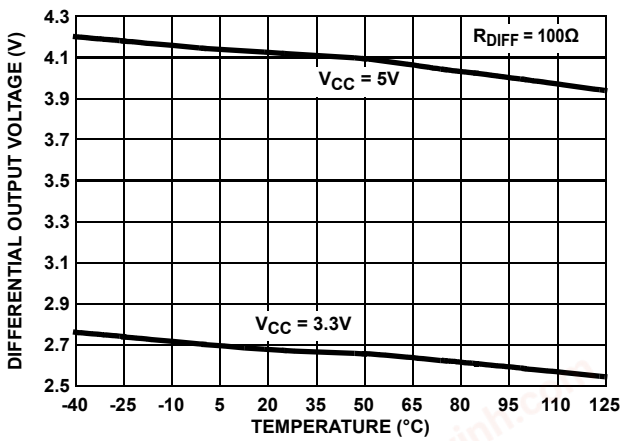


FIGURE 9. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

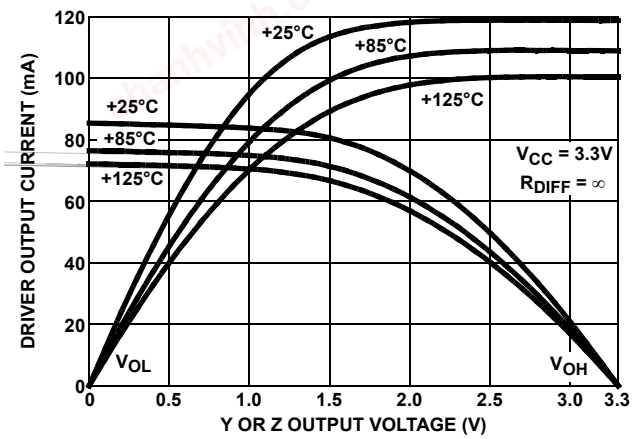


FIGURE 10. DRIVER SINGLE-ENDED (Y OR Z) OUTPUT CURRENT vs OUTPUT VOLTAGE

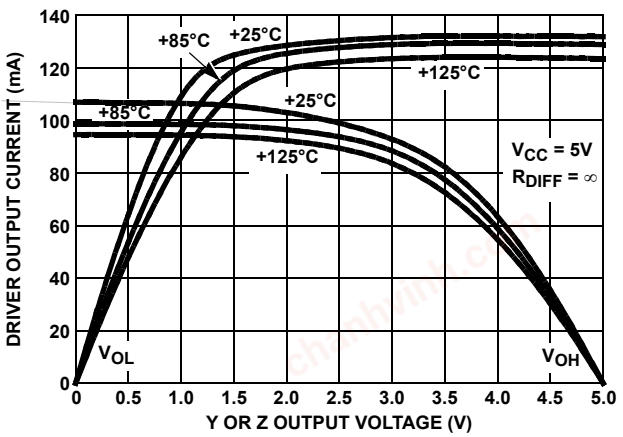


FIGURE 11. DRIVER SINGLE-ENDED (Y OR Z) OUTPUT CURRENT vs OUTPUT VOLTAGE

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Typical Performance Curves

VCC = VL = 3.3V or 5V, TA = +25°C, unless otherwise specified. V_L notes apply to the ISL32179E only. **(Continued)**

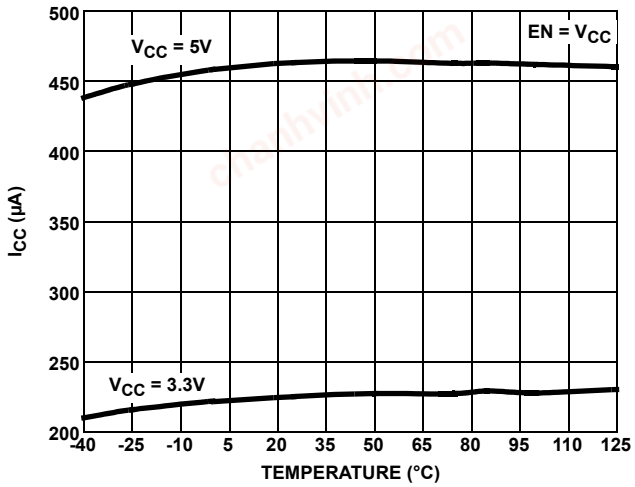


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

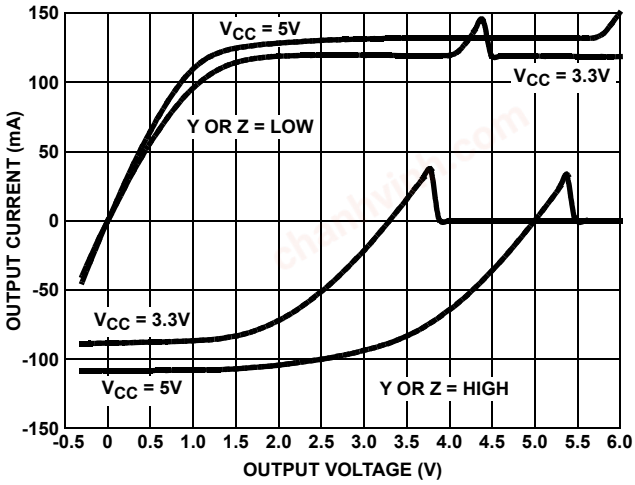


FIGURE 13. DRIVER OUTPUT CURRENT vs SHORT-CIRCUIT VOLTAGE

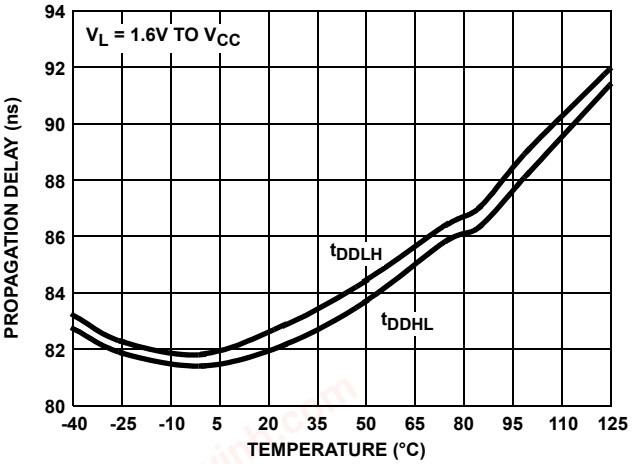


FIGURE 14. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32179E, 460kbps OPTION)

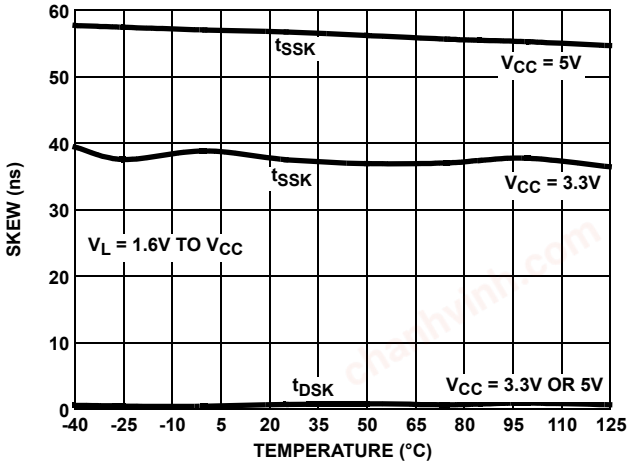


FIGURE 15. DRIVER SKEW vs TEMPERATURE (ISL32179E, 460kbps OPTION)

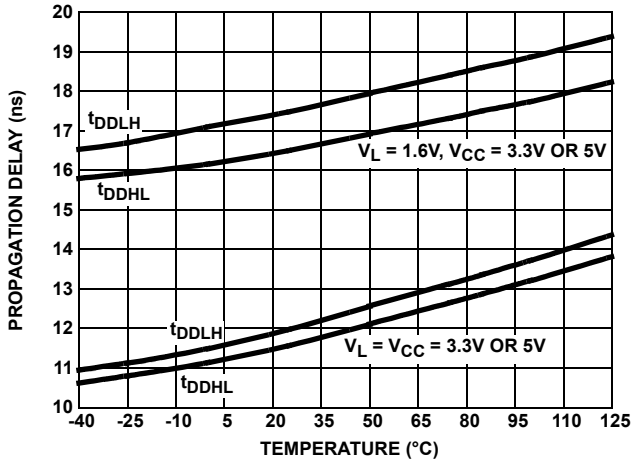


FIGURE 16. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32272E, ISL32179E, 10Mbps OPTION)

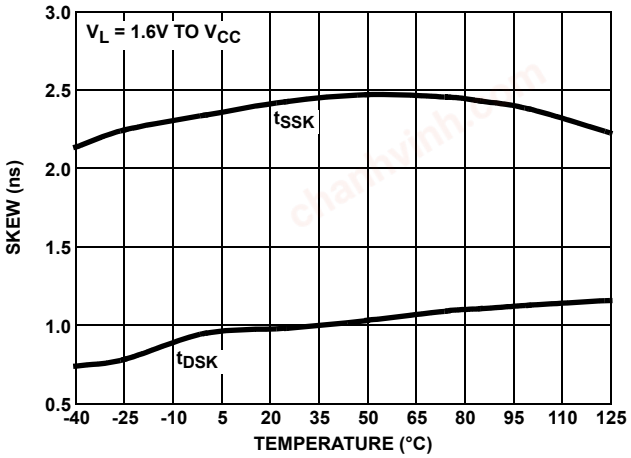


FIGURE 17. DRIVER SKEW vs TEMPERATURE (ISL32272E, ISL32179E, 10Mbps OPTION)

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Typical Performance Curves

VCC = VL = 3.3V or 5V, TA = +25°C, unless otherwise specified. V_L notes apply to the ISL32179E only. **(Continued)**

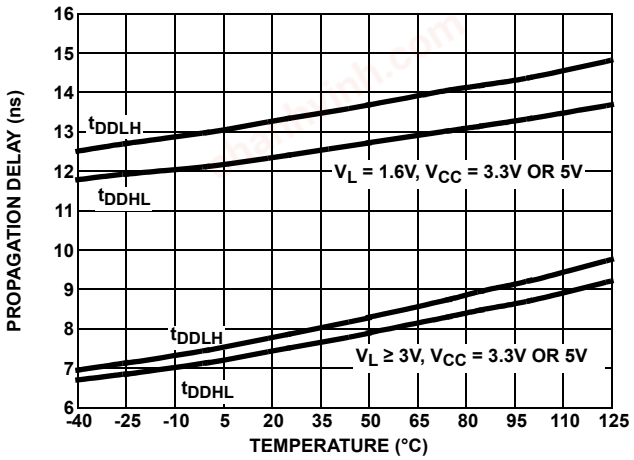


FIGURE 18. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32172E, ISL32174E, ISL32179E, 32Mbps OPTION)

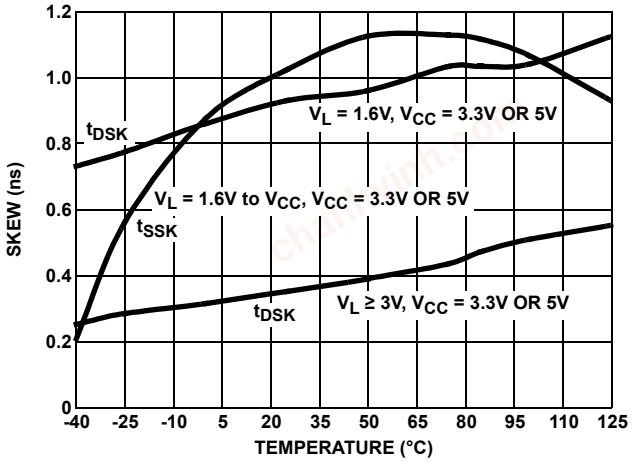


FIGURE 19. DRIVER SKEW vs TEMPERATURE (ISL32172E, ISL32174E, ISL32179E, 32Mbps OPTION)

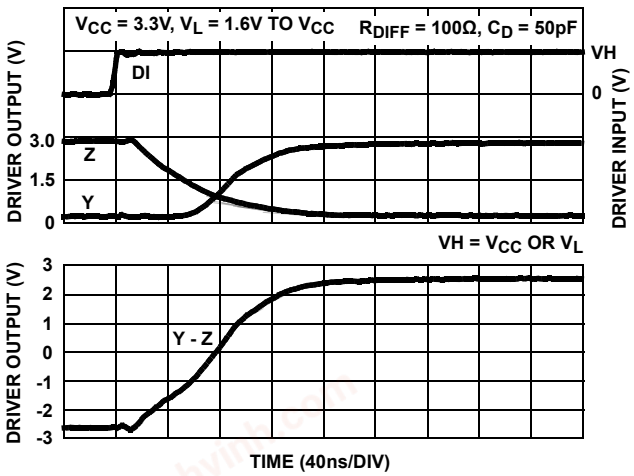


FIGURE 20. DRIVER WAVEFORMS, LOW TO HIGH (ISL32179E)

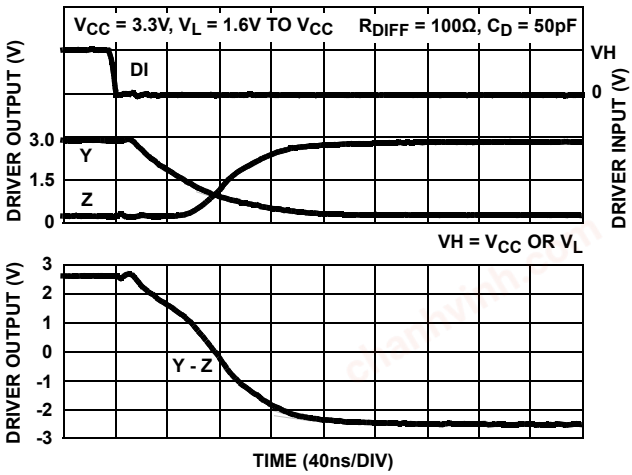


FIGURE 21. DRIVER WAVEFORMS, HIGH TO LOW (ISL32179E)

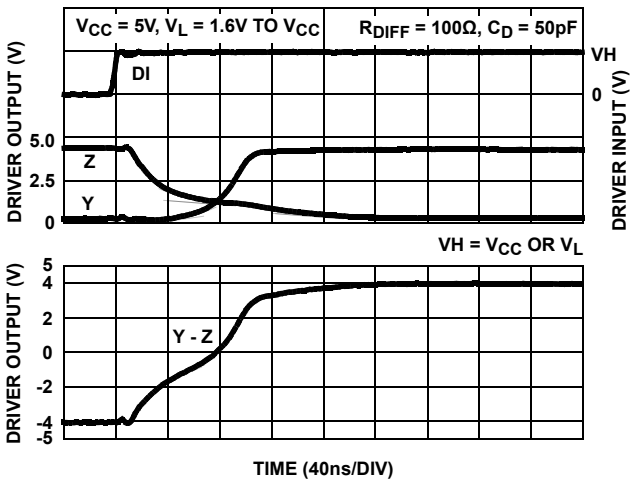


FIGURE 22. DRIVER WAVEFORMS, LOW TO HIGH (ISL32179E)

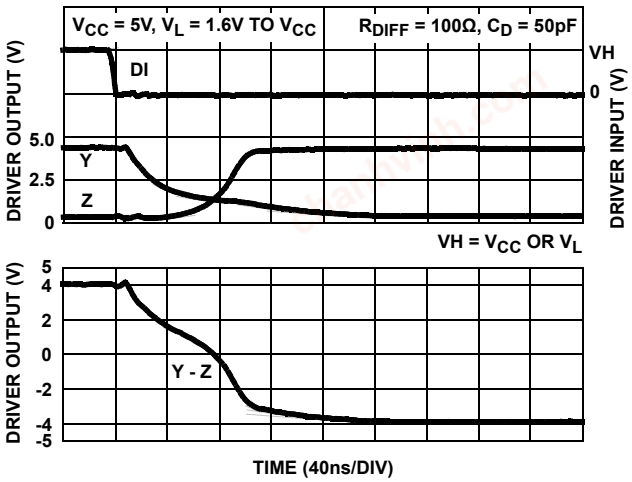


FIGURE 23. DRIVER WAVEFORMS, HIGH TO LOW (ISL32179E)

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Typical Performance Curves

V_{CC} = VL = 3.3V or 5V, TA = +25°C, unless otherwise specified. V_L notes apply to the ISL32179E only. **(Continued)**

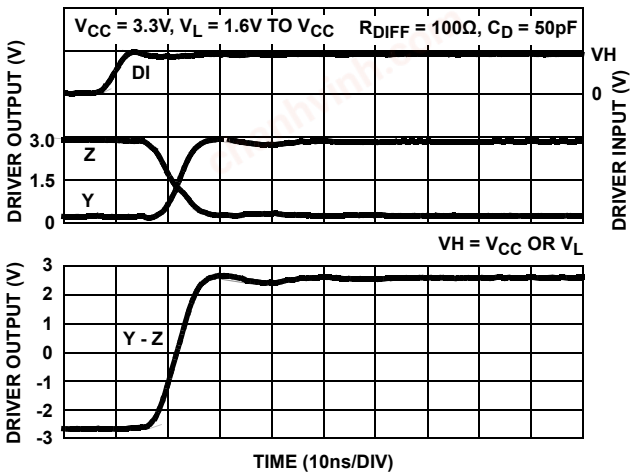


FIGURE 24. DRIVER WAVEFORMS, LOW TO HIGH (ISL32272E, ISL32179E)

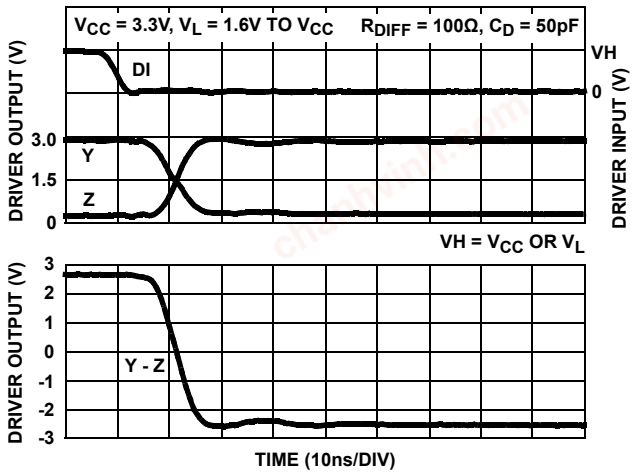


FIGURE 25. DRIVER WAVEFORMS, HIGH TO LOW (ISL32272E, ISL32179E)

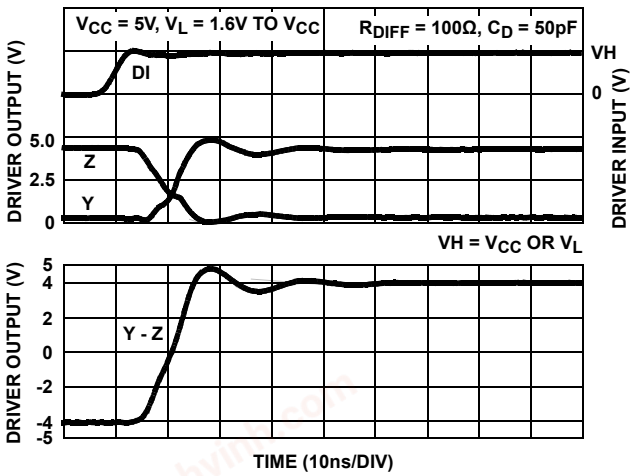


FIGURE 26. DRIVER WAVEFORMS, LOW TO HIGH (ISL32272E, ISL32179E)

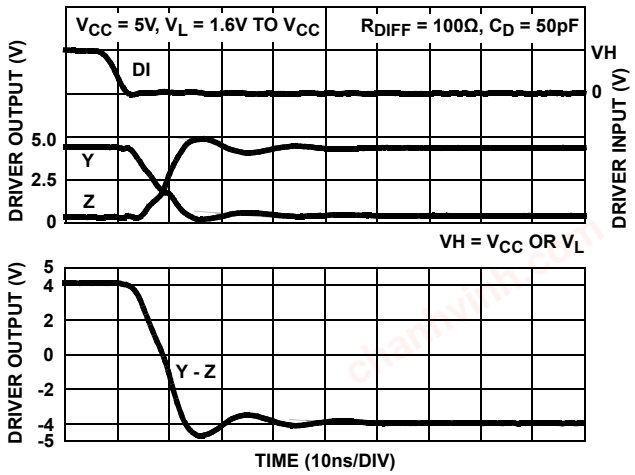


FIGURE 27. DRIVER WAVEFORMS, HIGH TO LOW (ISL32272E, ISL32179E)

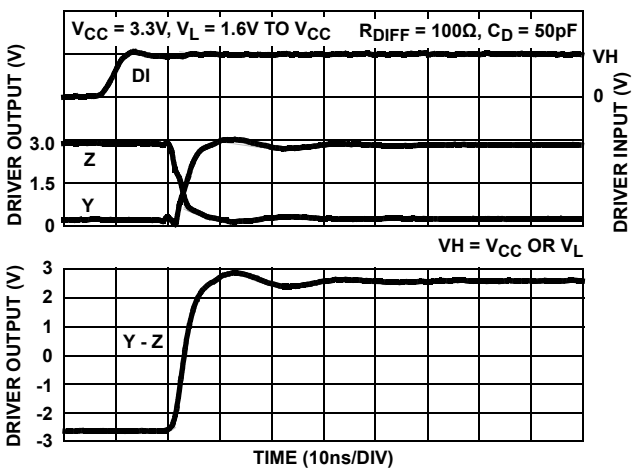


FIGURE 28. DRIVER WAVEFORMS, LOW TO HIGH (ISL32172E, ISL32174E, ISL32179E)

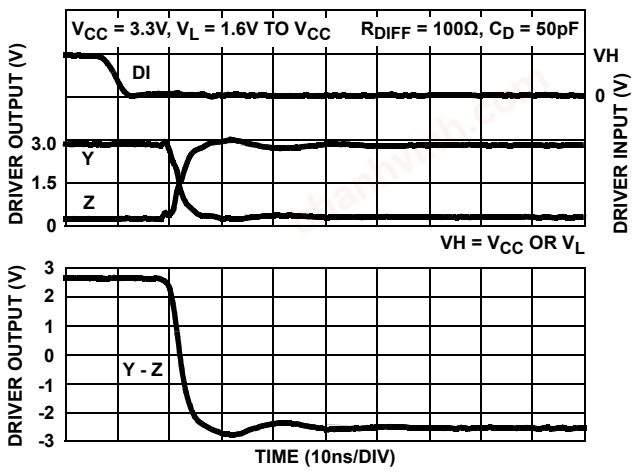


FIGURE 29. DRIVER WAVEFORMS, HIGH TO LOW (ISL32172E, ISL32174E, ISL32179E)

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Typical Performance Curves

V_{CC} = VL = 3.3V or 5V, TA = +25°C, unless otherwise specified. V_L notes apply to the ISL32179E only. **(Continued)**

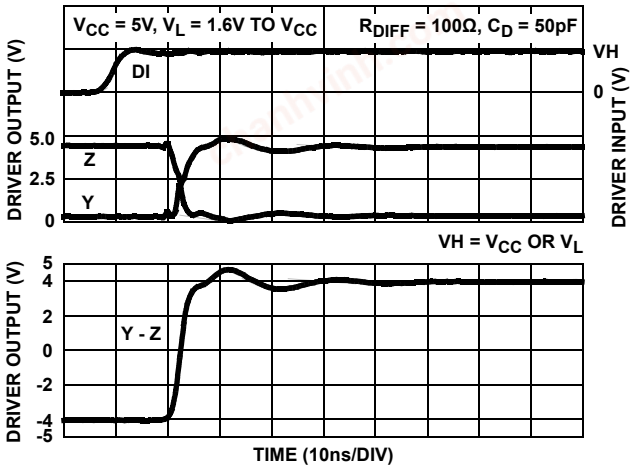


FIGURE 30. DRIVER WAVEFORMS, LOW TO HIGH (ISL32172E, ISL32174E, ISL32179E)

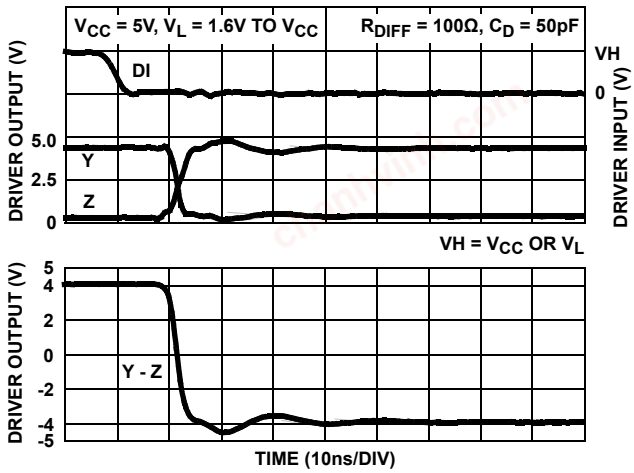


FIGURE 31. DRIVER WAVEFORMS, HIGH TO LOW (ISL32172E, ISL32174E, ISL32179E)

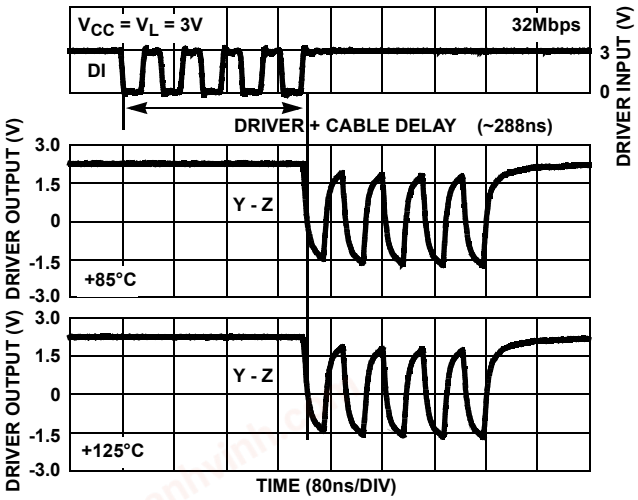


FIGURE 32. WORST CASE (NEGATIVE) FIVE PULSE DRIVER WAVEFORMS DRIVING 200 FEET (62m) OF CAT5 CABLE (SINGLE TERMINATED WITH 121Ω) (ISL32172E, ISL32174E, ISL32179E)

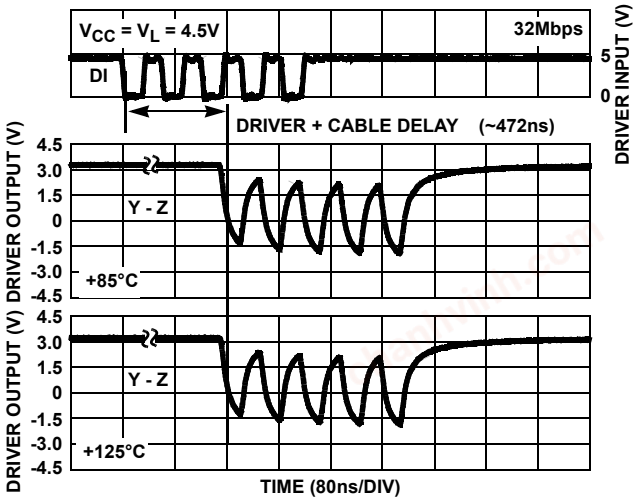


FIGURE 33. WORST CASE (NEGATIVE) FIVE PULSE DRIVER WAVEFORMS DRIVING 328 FEET (100m) OF CAT5 CABLE (SINGLE TERMINATED WITH 121Ω) (ISL32172E, ISL32174E, ISL32179E)

Application Information

RS-422 is a differential (balanced) data transmission standard for use in long haul or noisy environments. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 receivers on each bus (assuming one unit load devices).

Driver Features

The RS-422 drivers are differential output devices that deliver at least 2V across a 100Ω load. The drivers feature low propagation delay skew to maximize bit width and minimize EMI.

The 460kbps driver outputs are slew rate limited to minimize EMI and to reduce reflections in unterminated or improperly terminated networks. The 10Mbps and 32Mbps driver outputs are not limited, so faster output transition times allow the higher data rates.

Driver Enable Functions

All product types allow disabling of the Tx outputs. The ISL32x72E types feature group (all four Tx) enable functions that are active high (EN) or active low ($\overline{EN}$). Drivers enable when EN = 1 or when $\overline{EN}$ = 0, and they disable only when EN = 0 and $\overline{EN}$ = 1. The ISL32174E uses active high paired enable functions (EN12 and EN34) that enable (when high) or disable (when low) the corresponding pairs of Tx. All four of these enable pins have internal pull-up resistors to V_{CC}, but unused enable pins that need to be high (for example, $\overline{EN}$ when using the EN input for enable control, or EN12 and EN34 when using always enabled drivers) should always be connected externally to V_{CC}. If V_{CC} transients might exceed 7V, insert a series resistor between the

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input(s) and V_{CC} to limit the current that flows if the input's ESD protection starts conducting.

The ISL32179E has the most flexible enable scheme. Its six enable pins allow for group, paired, or individual channel enable control. Figure 34 details the ISL32179E's internal enable logic. To use a group enable function, connect all the ENx pins high and set all unused enable pins high. For paired enables, connect EN and $\overline{EN}$ high (for the lowest current in shutdown mode, if SHDNEN is used), tie EN1 and EN2 together, and tie EN3 and EN4 together. For individual channel enables, connect EN and $\overline{EN}$ high and drive the appropriate ENX (active high) for the particular channel. All of the enable pins incorporate pull-up resistors to V_{CC}, but unused enable pins of any type should be externally connected high rather than being left floating. Connecting to V_{CC} is the best choice, but V_L can be used as long as SHDN power is not a primary concern (for each V_L connected input, I_{CC} increases by $((V_{CC} - V_L)/600k\Omega)$. If V_{CC} or V_L transients might exceed 7V, insert a series resistor between the input(s) and the supply to limit the current that flows if the input's ESD protection starts conducting.

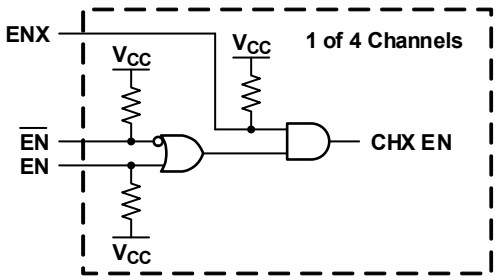


FIGURE 34. ISL32179E ENABLE LOGIC

Wide Supply Range

The ISL 32x7xE devices are designed to operate with a wide range of supply voltages from 3.0V to 5.5V, and they meet the RS-422 specifications for that full supply voltage range.

5.5V TOLERANT LOGIC PINS

The logic input pins (driver inputs, enable pins, and SHDNEN) contain no ESD or parasitic diodes to V_{CC} to V_L, so they withstand input voltages exceeding 5.5V regardless of the V_{CC} and V_L voltages. Input voltages up to 7V are easily tolerated.

Logic Supply (V_L Pin, ISL32179E Only)

Note: If powered from separate supplies, power up V_{CC} before powering up the V_L supply. If unused enable pins are connected to V_L rather than to V_{CC}, a small I_{CC} $((V_{CC} - V_L)/600k\Omega)$ flows due to the internal pull-up resistor connecting to V_{CC}.

The ISL32179E's V_L pin powers the logic inputs (driver inputs, enable pins, and SHDNEN). These pins interface with "logic" devices such as UARTs, ASICs, and microcontrollers, and most of these devices use power supplies significantly lower than 3.3V. Thus, the logic device's low V_{OH} might not exceed the V_{IH} of a 3.3V or 5V powered DI or enable input. Connecting the V_L pin to the power supply of the logic device (as shown in Figure 35) reduces the DI and enable input switching points to values compatible with the logic device's output levels. Configure the logic pin input switching points to the supply voltage of the UART, ASIC, or microcontroller to eliminate the need for a level shifter/translator between the two ICs.

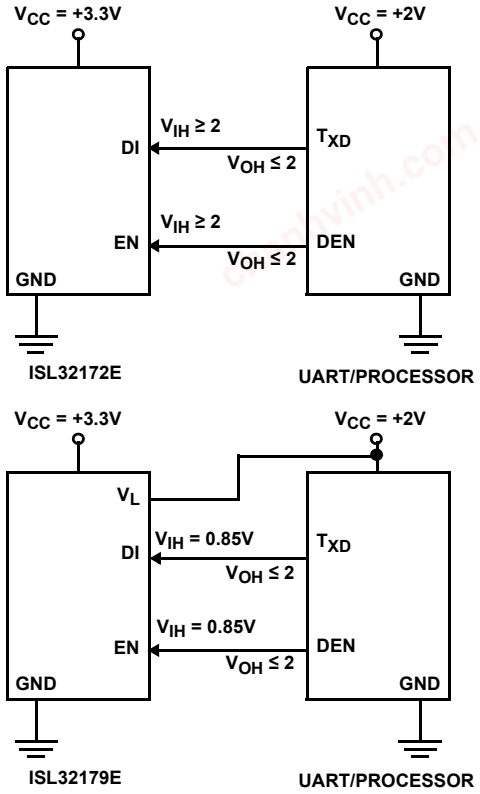


FIGURE 35. USING V_L PIN TO ADJUST LOGIC LEVELS

V_L can be anywhere from V_{CC} down to 1.5V. Table 2 indicates typical V_{IH} and V_{IL} values for various V_L settings so you can determine whether or not a particular V_L voltage meets your needs.

TABLE 2. V_{IH} AND V_{IL} vs V_L FOR V_{CC} = 3.3V OR 5V

V_L (V)	V_{IH} (V)	V_{IL} (V)
1.6	0.7	0.45
2	0.85	0.6
2.3	1.1	0.75
2.7	1.4 (DI), 1.1 (ENs)	0.85
2.7	2	0.8
3.3	2.2	0.8

Hot Plug Function

When a piece of equipment powers up, there is a period of time when the processor or ASIC driving the RS-422 control lines (EN, $\overline{EN}$, ENx) is unable to ensure that the RS-422 Tx outputs remain disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may drive invalid data on the bus. To avoid this scenario, the ISL32172E/32272E/32174E/32179E family incorporates a hot plug function. During power-up, circuitry monitoring V_{CC} ensures that the Tx outputs remain disabled for a period of time,

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regardless of the state of the enable pins. The disabled Tx outputs give the processor/ASIC a chance to stabilize and drive the RS-422 control lines to the proper states.

ESD Protection

All pins on the ISL32172E/32272E/32174E/32179E devices include Class 3 (>12kV) Human Body Model (HBM) ESD protection structures, but the RS-422 pins (driver outputs) incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM, and ±16.5kV to IEC61000-4-2. The RS-422 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Touching the port pins or connecting a cable can cause an ESD event that might destroy unprotected ICs. The new ESD structures protect the device whether or not it is powered up and without degrading the RS-422 common-mode range of -0.3V to +6V. The built-in ESD protection eliminates the need for board level protection structures such as transient suppression diodes and the associated undesirable capacitive load they present.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-422 pins in this case) and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The IEC61000 standard's lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-422 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-422 port.

AIR-GAP DISCHARGE TEST METHOD

For the air-gap discharge test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The RS-422 pins withstand ±16.5kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized and eliminates the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±9kV. The ISL32172E/32272E/32174E/32179E devices survive ±9kV contact discharges on the RS-422 pins.

Data Rate, Cables, and Terminations

RS-422 is intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. Devices opera ting at 32Mbps handle lengths up to 328ft (100m) in 5V systems, and lengths up to 200ft (62m) in 3.3V systems (see Figures 32 and 33). The 460kbps versions can operate at full data rates with lengths of thousands of feet. Note that system jitter requirements may limit a network to shorter distances.

Use twisted pair cable for RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals that are effectively rejected by the differential receivers in RS-422 ICs.

Note: Proper termination is imperative to minimize reflections when using the 10Mbps or 32Mbps devices. Short networks using the 460kbps versions do not need to be terminated, but terminations are recommended unless power dissipation is an overriding concern.

In point-to-point or point-to-multipoint (multiple receivers on bus) networks, terminate the main cable in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multireceiver applications, keep stubs connecting receivers to the main cable as short as possible.

Built-In Driver Overload Protection

The driver output stages incorporate short-circuit current limiting circuitry that ensures that the output current never exceeds the RS-422 specification. A novel design sets the short-circuit current limit depending on the V_{CC} value, so unlike some competing devices, the V_{CC} = 5V short-circuit current is only slightly higher than the corresponding V_{CC} = 3.3V level (see Figure 13).

In the event of a major short-circuit condition, the ISL32172E/32272E/32174E/32179E thermal shutdown feature disables the drivers whenever the die temperature becomes excessive. Thermal shutdown eliminates the power dissipation and allows the die to cool. The drivers automatically reenable after the die temperature drops about 20°. If the fault persists, the thermal shutdown/reenable cycle repeats until the fault is cleared.

High Temperature Operation

With T_A = +125°C and V_{CC} = 5.5V, four 100Ω differentially terminated drivers in the TSSOP package put the IC at the edge of its maximum allowed junction temperature. Using larger termination resistors, a lower maximum supply voltage, or one of the packages with a lower thermal resistance (θ_{JA}) provides more safety margin. When designing for +125°C operation, measure the application's switching current and include it in the thermal calculations.

Low Power Shutdown Mode (ISL32179E Only)

These BiCMOS transmitters all use a fraction of the power required by their bipolar counterparts, but the ISL32179E includes a shutdown feature that reduces the already low quiescent I_{CC} by 90%. The ISL32179E enters shutdown whenever the SHDNEN pin is high and all four drivers are disabled (see "Pin Descriptions" on page 5). Note that the enable times from shutdown are longer than the enable times when the IC is not in shutdown mode.

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Die Characteristics

SUBSTRATE AND QFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

1682

PROCESS:

Si Gate BiCMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

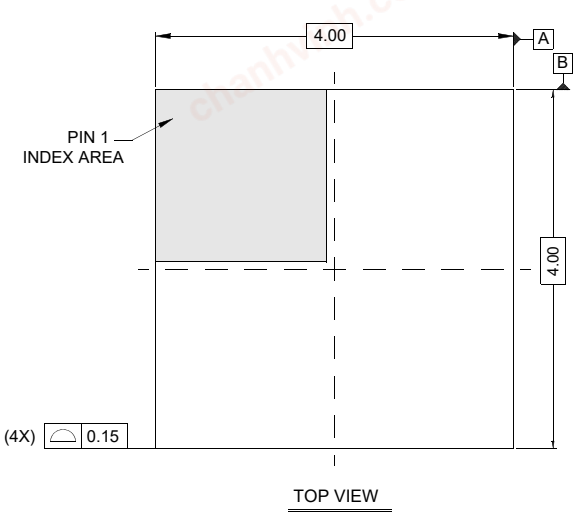
DATE	REVISION	CHANGE
Mar 19, 2020	4.01	Updated the Pin Configurations. Updated the readability of the Test Conditions for the Input High Voltage and Input Low Voltage specifications. Updated Figure 34.
Feb 1, 2019	4.00	Updated typical application diagrams on page 2. Updated disclaimer.
May 1, 2018	3.00	Removed ISL32372E, ISL32274E, and ISL32374E information from datasheet. Changed 1st sentence in 3rd paragraph on front page. Added Related Literature section. Ordering Information table - added tape and reel quantity column and updated Note 1. Changed part number in pin description for EN12, EN34 from ISL32x74E to ISL32774E. Changed Note 4 regarding the use of unused enable pins. Changed part numbers in Figure 2 from ISL32x75E to ISL32173E and from ISL32x74E to ISL32174E. Changed part number in 1st paragraph of Driver Enable Functions from ISL32x74E to ISL32174E. Removed the About Intersil section and updated the disclaimer. Updated POD M16.15 to the latest revision. Changes from previous are as follows: Updated graphics to new standard layout, removing the dimension table
Aug 13, 2015	2.00	Updated Table 1, page 1 and Ordering Information table on page 3 with “(No longer available or supported)” to applicable parts. Updated “About Intersil” section.
Feb 28, 2013	1.00	Added “EP” and description to “Pin Descriptions” on page 5. Added verbiage to clarify that V_{CC} and V_L may power up simultaneously, when powered from the same supply (“Pin Descriptions” table entries “V_{CC}” and “V_L” on page 5; “Notes” near bottom of page 2; “Note” under “Logic Supply” heading on page 15). Added “Revision History” table, and “About Intersil” sections to page 17.
De 16, 2008	0.00	Initial release.

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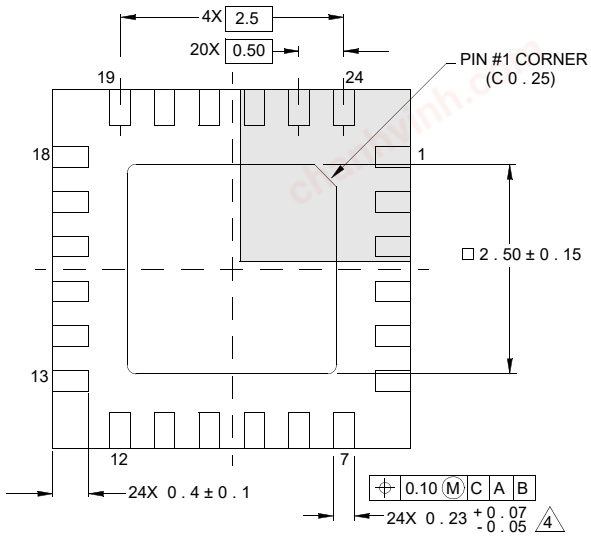
Package Outline Drawings

For the most recent package outline drawing, see L24.4x4C.

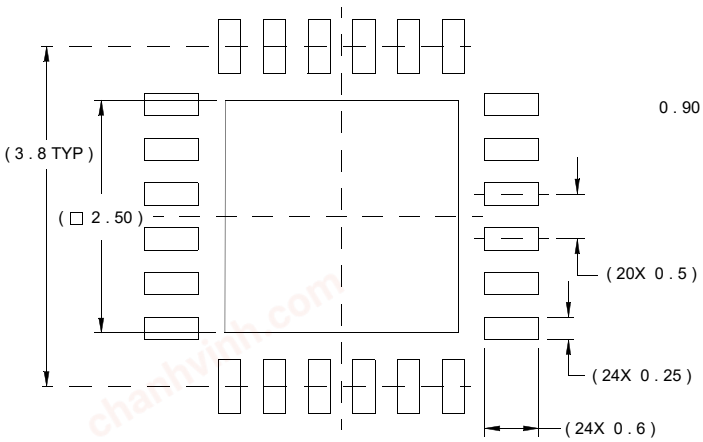
L24.4x4C
24 Lead Quad Flat No-Lead Plastic Package
Rev 2, 10/06



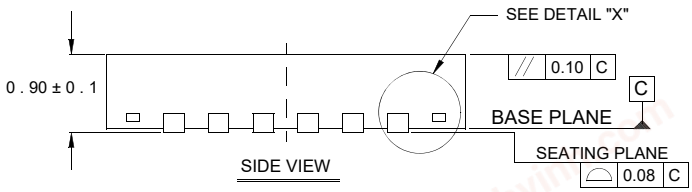
TOP VIEW



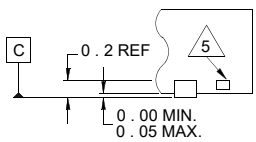
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

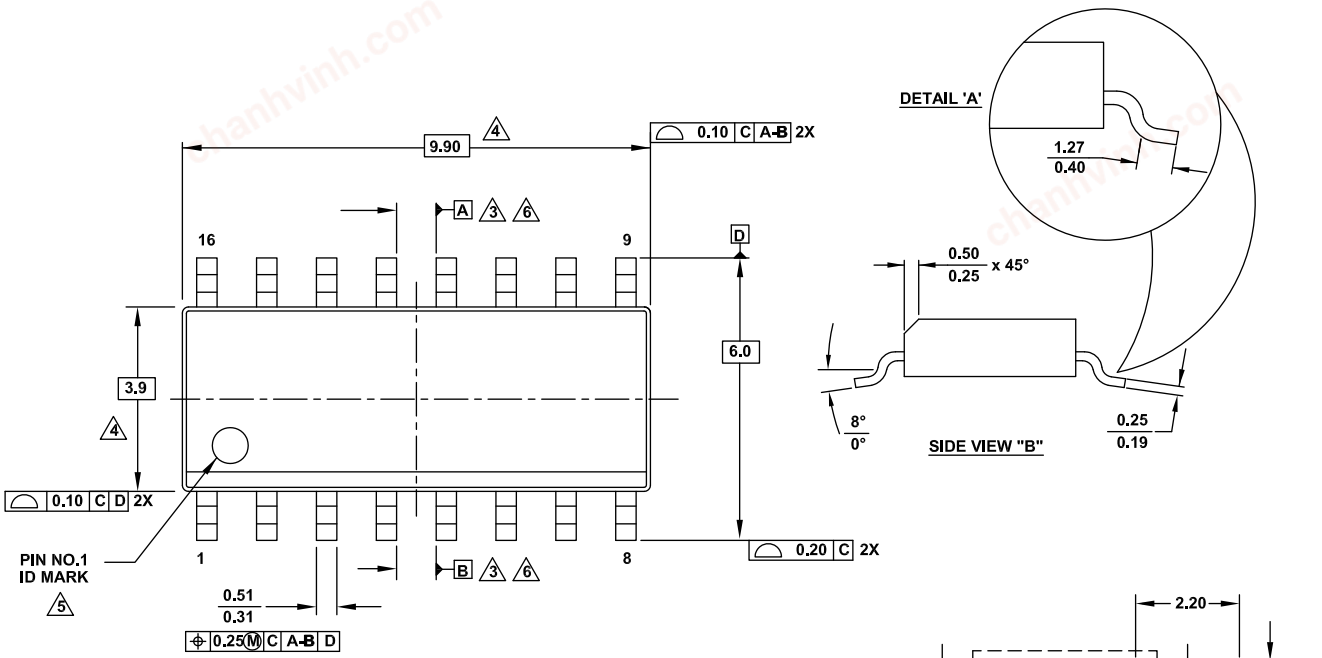
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

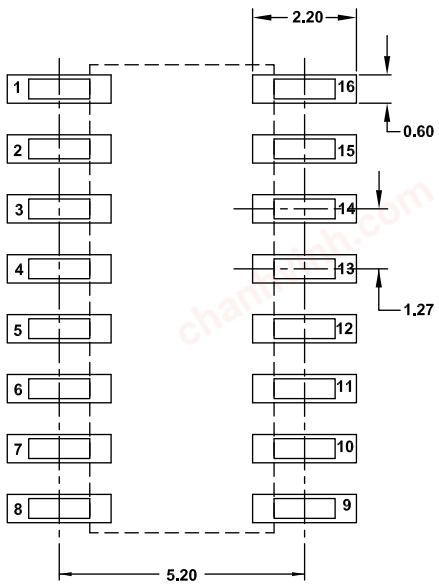
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M16.15 (JEDEC MS-012-AC ISSUE C)

For the most recent package outline drawing, see M16.15.

16 Lead Narrow Body Small Outline Plastic Package
Rev 2, 11/17





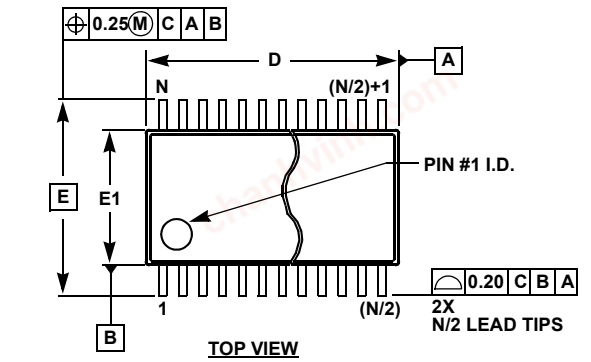
TYPICAL RECOMMENDED LAND PATTERN

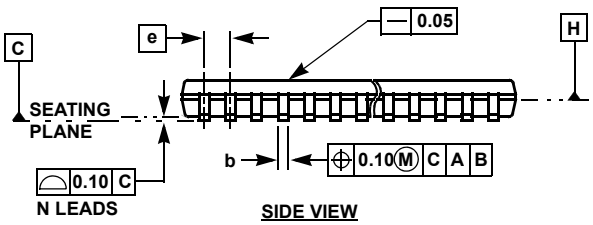
NOTES:

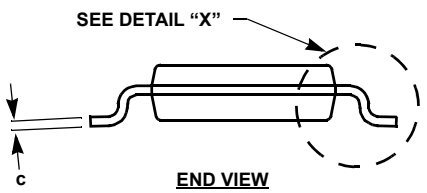
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AC

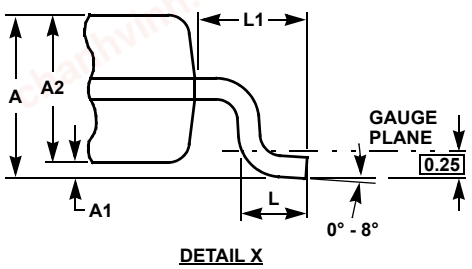
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Thin Shrink Small Outline Package Family (TSSOP)









MDP0044 For the most recent package outline drawing, see MDP0044.

Thin Shrink Small Outline Package Family

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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(Rev.1.0 Mar 2020)

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