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DATASHEET

ISL1208

I²C Real Time Clock/Calendar, Low Power RTC with Battery Backed SRAM

FN8085
Rev 9.01
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The ISL1208 device is a low power real time clock with timing and crystal compensation, clock/calendar, power fail indicator, periodic or polled alarm, intelligent battery backup switching and battery-backed user SRAM.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Applications

- Utility Meters
- HVAC Equipment
- Audio/Video Components
- Set-Top Box/Television
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- POS Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Home Appliances
- Computer Products
- Other Industrial/Medical/Automotive

Features

- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes, and Seconds
  - Day of the Week, Day, Month, and Year
- 15 Selectable Frequency Outputs
- Single Alarm
  - Settable to the Second, Minute, Hour, Day of the Week, Day, or Month
  - Single Event or Pulse Interrupt Mode
- Automatic Backup to Battery or Super Capacitor
- Power Failure Detection
- On-Chip Oscillator Compensation
- 2 Bytes Battery-Backed User SRAM
- I²C Interface
  - 400kHz Data Transfer Rate
- 400nA Battery Supply Current
- Same Pin Out as ST M41Txx and Maxim DS13xx Devices
- Small Package Options
  - 8 Ld MSOP and SOIC Packages
  - 8 Ld TDFN Package
- Pb-Free Available (RoHS Compliant)

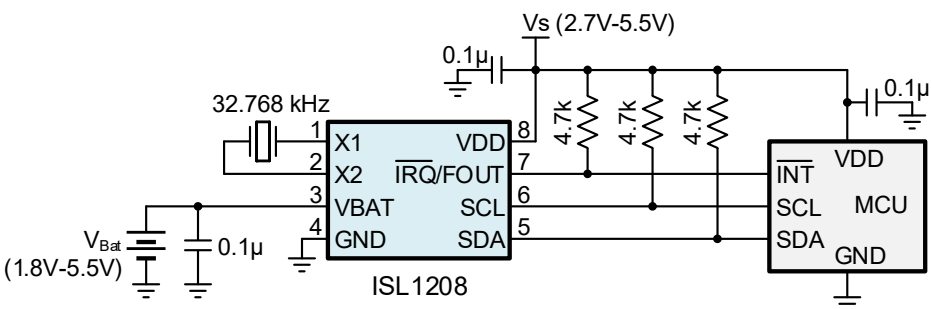


FIGURE 1. TYPICAL APPLICATION

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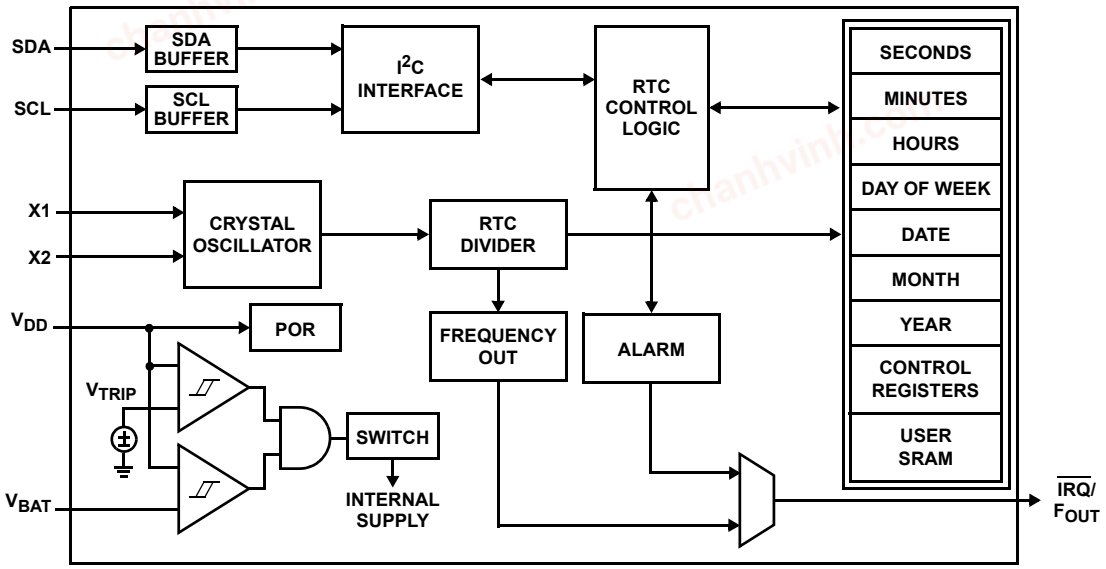


FIGURE 2. Block Diagram

Ordering Information

PART NUMBER	PART MARKING	V_{DD} RANGE (V)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP. RANGE
ISL1208IU8Z	ANW	2.7 to 5.5	8 Ld MSOP	M8.118	Tube	-40 to +85°C
ISL1208IU8Z-TK					Reel, 2.5k	
ISL1208IU8Z-T7A					Reel, 250	
ISL1208IB8Z	1208 ZI		8 Ld SOIC	M8.15E	Tube	
ISL1208IB8Z-TK					Reel, 1k	
ISL1208IB8Z-T7A					Reel, 250	
ISL1208IRT8Z	08TZ		8 Ld TDFN	L8.3x3A	Tube	
ISL1208IRT8Z-TK					Reel, 1k	

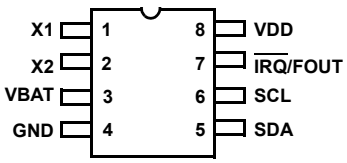
NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL1208 device page. For more information about MSL, see TB363

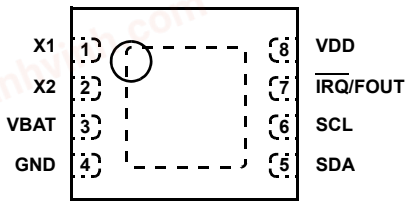
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Pinouts

ISL1208
(8 LD MSOP, SOIC)
TOP VIEW



ISL1208
(8 LD TDFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	X1	The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X1 can also be driven directly from a 32.768kHz source.
2	X2	The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
3	VBAT	This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin should be tied to ground if not used.
4	GND	Ground
5	SDA	Serial Data (SDA) is a bidirectional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs.
6	SCL	The Serial Clock (SCL) input is used to clock all serial data into and out of the device.
7	$\overline{IRQ}$/FOUT	Interrupt Output/Frequency Output is a multi-functional pin that can be used as interrupt or frequency output pin. The function is set via the configuration register.
8	VDD	Power supply

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Absolute Maximum Ratings

Voltage on V_{DD}, V_{BAT}, SCL, SDA, and $\overline{IRQ}$ Pins (Note 8)
(respect to GND) . . . . . -0.5V to 7.0V
Voltage on X1 and X2 Pins
(respect to GND) . . . . . -0.5V to V_{DD} + 0.5 (V_{DD} Mode)
-0.5V to V_{BAT} + 0.5 (V_{BAT} Mode)
Latchup (Note 9) .....Class II, Level B @ +85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Notes 5, 7)	108	55
MSOP Package (Notes 5, 7)	145	55
TDFN Package (Notes 4, 6).	45	3.5

Storage Temperature . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board. See TB379.
6. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the case temperature location is the package top center
8. The V_{DD} and SDA pins should not be subjected to negative voltage while the V_{BAT} pin is biased, otherwise latchup can result. See the Applications section.
9. Jedec Class II pulse conditions and failure criterion used. Level B exceptions are using a negative pulse limited to -0.5V.

DC Operating Characteristics – RTC

Temperature = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN (Note 14)	TYP (Note 13)	MAX (Note 14)	UNITS
V_{DD}	Main Power Supply			2.7		5.5	V
V_{BAT}	Battery Supply Voltage			1.8		5.5	V
I_{DD1}	Supply Current	V_{DD} = 5V	10, 11		2	6	µA
		V_{DD} = 3V			1.2	4	µA
I_{DD2}	Supply Current With I^2C Active	V_{DD} = 5V	10, 11		40	120	µA
I_{DD3}	Supply Current (Low Power Mode)	V_{DD} = 5V, LPMODE = 1	10		1.4	5	µA
I_{BAT}	Battery Supply Current	V_{BAT} = 3V	10		400	950	nA
I_{LI}	Input Leakage Current on SCL				100		nA
I_{LO}	I/O Leakage Current on SDA				100		nA
V_{TRIP}	V_{BAT} Mode Threshold			1.6	2.2	2.6	V
$V_{TRIPHYS}$	V_{TRIP} Hysteresis			10	30	75	mV
V_{BATHYS}	V_{BAT} Hysteresis			15	50	100	mV
$\overline{IRQ}$/F_{OUT}							
V_{OL}	Output Low Voltage	V_{DD} = 5V I_{OL} = 3mA				0.4	V
		V_{DD} = 2.7V I_{OL} = 1mA				0.4	V

Power-Down Timing

Temperature = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN (Note 14)	TYP (Note 13)	MAX (Note 14)	UNITS
$V_{DD\ SR-}$	V_{DD} Negative Slewrate		12			10	V/ms

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Serial Interface Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NOTES	MIN (Note 14)	TYP (Note 13)	MAX (Note 14)	UNITS
SERIAL INTERFACE SPECS							
V_{IL}	SDA and SCL Input Buffer LOW Voltage			-0.3		0.3 x V_{DD}	V
V_{IH}	SDA and SCL Input Buffer HIGH Voltage			0.7 x V_{DD}		V_{DD} + 0.3	V
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.05 x V_{DD}			V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA			0		0.4	V
C_{PIN}	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V	15, 16			10	pF
f_{SCL}	SCL Frequency					400	kHz
t_{IN}	Pulse width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.				50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.				900	ns
t_{BUF}	Time the Bus Must Be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.		1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing.		1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing.		600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}.		600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}.		600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}		100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.		20		900	ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}.		600			ns
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}.		600			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window.		0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}	15, 16	20 + 0.1 x Cb		300	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}	15, 16	20 + 0.1 x Cb		300	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	15, 16	10		400	pF

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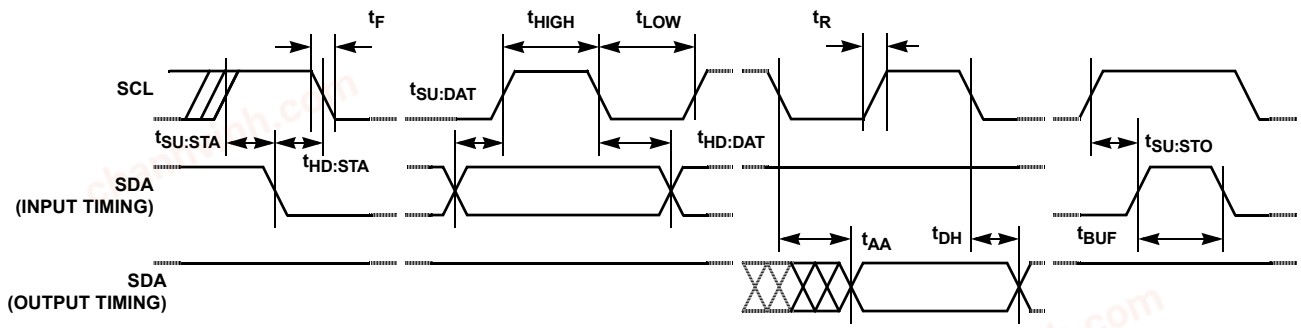
Serial Interface Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	NOTES	MIN (Note 14)	TYP (Note 13)	MAX (Note 14)	UNITS
Rpu	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ to~2.5kΩ. For Cb = 40pF, max is about 15kΩ to ~20kΩ	15, 16	1			kΩ

NOTES:

10. $\overline{IRQ}$ and F_{OUT} Inactive.
11. LPMODE = 0 (default).
12. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
13. Typical values are for T = +25°C and 3.3V supply voltage.
14. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
15. Parameter is not 100% tested.
16. These are I^2C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.

SDA vs SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

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Typical Performance Curves Temperature is +25°C unless otherwise specified

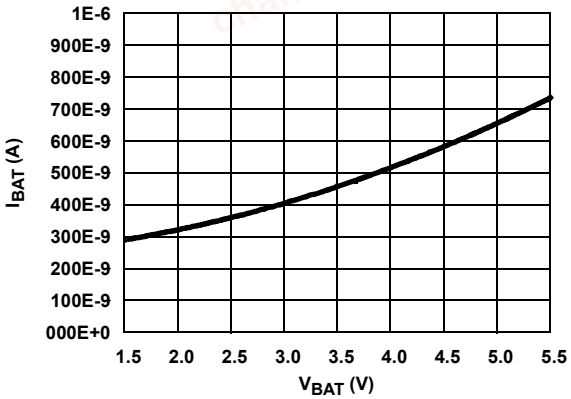


FIGURE 3. I_{BAT} vs V_{BAT}

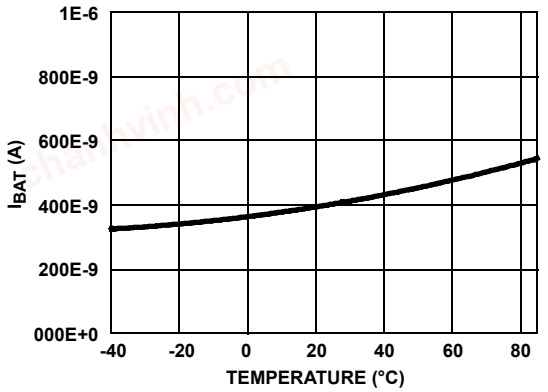


FIGURE 4. I_{BAT} vs TEMPERATURE AT V_{BAT} = 3V

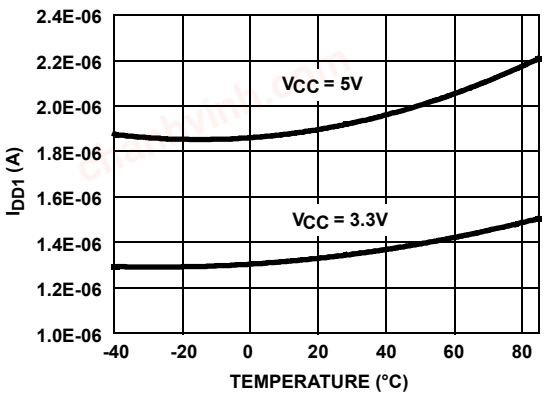


FIGURE 5. I_{DD1} vs TEMPERATURE

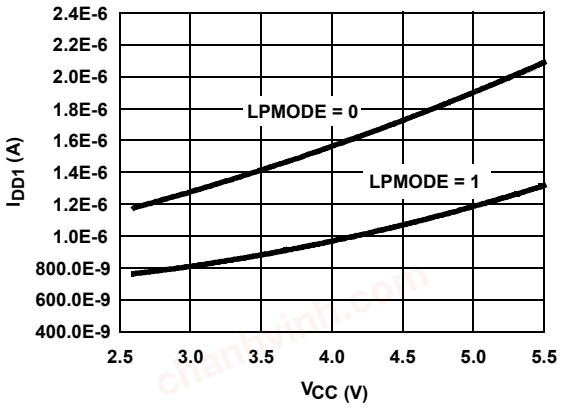


FIGURE 6. I_{DD1} vs V_{CC} WITH LPMODE ON AND OFF

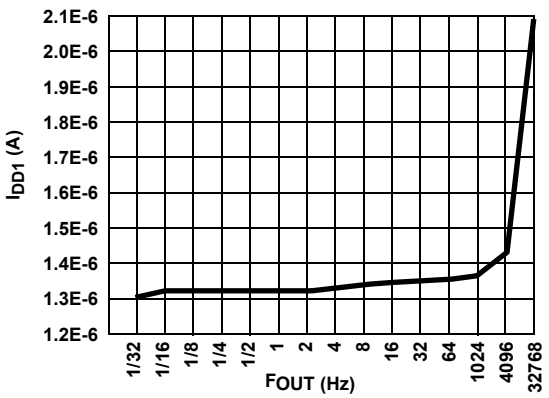


FIGURE 7. I_{DD1} vs F_{OUT} AT V_{DD} = 3.3V

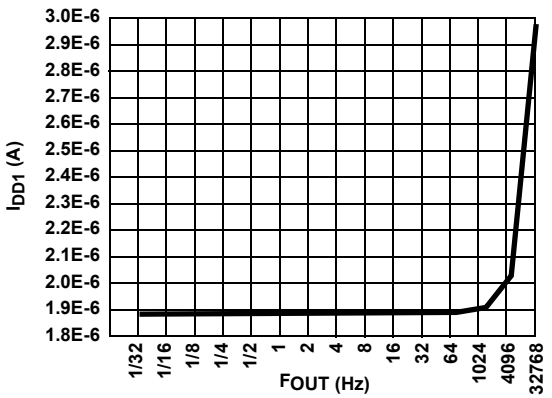


FIGURE 8. I_{DD1} vs F_{OUT} AT V_{DD} = 5V

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EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 5V

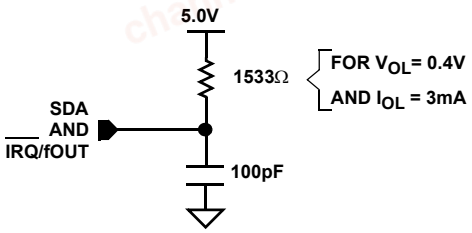


FIGURE 9. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 5.0V

General Description

The ISL1208 device is a low power real time clock with timing and crystal compensation, clock/calendar, power fail indicator, periodic or polled alarm, intelligent battery backup switching, and battery-backed user SRAM.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

The ISL1208's powerful alarm can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the IRQ pin. There is a repeat mode for the alarm allowing a periodic interrupt every minute, every hour, every day, etc.

The device also offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or Super Capacitor with automatic switchover from V_{DD} to V_{BAT}. The entire ISL1208 device is fully operational from 2.0V to 5.5V and the clock/calendar portion of the device remains fully operational down to 1.8V (Standby Mode).

Pin Description

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the ISL1208 to supply a timebase for the real time clock. Internal compensation circuitry provides high accuracy over the operating temperature range from -40°C to +85°C. This oscillator compensation network can be used to calibrate the crystal timing accuracy over temperature either during manufacturing or with an external temperature sensor and microcontroller for active compensation. The device can also be driven directly from a 32.768kHz source at pin X1.

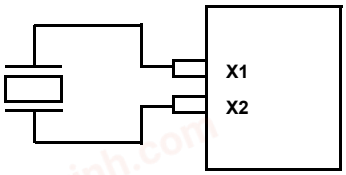


FIGURE 10. RECOMMENDED CRYSTAL CONNECTION

V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin can be connected to a battery, a Super Cap or tied to ground if not used.

$\overline{IRQ}$/fOUT (Interrupt Output/Frequency Output)

This dual function pin can be used as an interrupt or frequency output pin. The $\overline{IRQ}/F_{OUT}$ mode is selected via the frequency out control bits of the control/status register.

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active low output.
- **Frequency Output Mode.** The pin outputs a clock signal which is related to the crystal frequency. The frequency output is user selectable and enabled via the I^2C bus. It is an open drain active low output.

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the V_{BAT} pin is activated to minimize power consumption.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds. It is disabled when the backup power supply on the VBAT pin is activated.

V_{DD}, GND

Chip power supply and ground pins. The device will operate with a power supply from 2.0V to 5.5VDC. A 0.1µF capacitor is recommended on the VDD pin to ground.

Functional Description

Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power the ISL1208 for up

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to 10 years. Another option is to use a Super Cap for applications where V_{DD} is interrupted for up to a month. See the “Application Section” on page 18 for more information.

Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

Condition 1:

$V_{DD} < V_{BAT} - V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} < V_{TRIP}$
where $V_{TRIP} \approx 2.2V$

Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The ISL1208 device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

Condition 1:

$V_{DD} > V_{BAT} + V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} > V_{TRIP} + V_{TRIPHYS}$
where $V_{TRIPHYS} \approx 30mV$

These power control situations are illustrated in Figures 11 and 12.

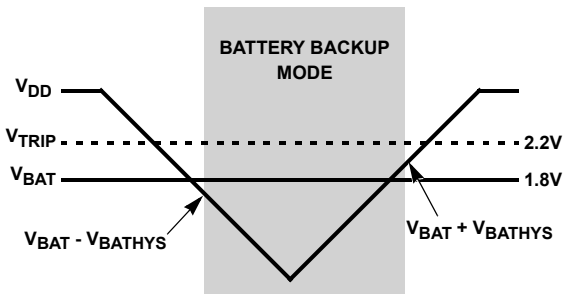


FIGURE 11. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$

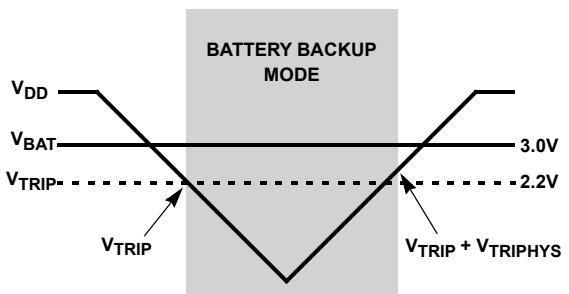


FIGURE 12. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$

The I^2C bus is deactivated in battery backup mode to provide lower power. Aside from this, all RTC functions are operational during battery backup mode. Except for SCL and SDA, all the inputs and outputs of the ISL1208 are active during battery backup mode unless disabled via the control register. The User SRAM is operational in battery backup mode down to 2V.

Power Failure Detection

The ISL1208 provides a Real Time Clock Failure Bit (RTCF) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both V_{DD} and V_{BAT}).

Low Power Mode

The normal power switching of the ISL1208 is designed to switch into battery backup mode only if the V_{DD} power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode. Another mode, called Low Power Mode, is available to allow direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below V_{TRIP}. Since the additional monitoring of V_{DD} vs V_{TRIP} is no longer needed, that circuitry is shut down and less power is used while operating from V_{DD}. Power savings are typically 600nA at V_{DD} = 5V. Low Power Mode is activated via the LPMODE bit in the control and status registers.

Low Power Mode is useful in systems where V_{DD} is normally higher than V_{BAT} at all times. The device will switch from V_{DD} to V_{BAT} when V_{DD} drops below V_{BAT}, with about 50mV of hysteresis to prevent any switchback of V_{DD} after switchover. In a system with a V_{DD} = 5V and backup lithium battery of V_{BAT} = 3V, Low Power Mode can be used. However, it is not recommended to use Low Power Mode in a system with V_{DD} = 3.3V ±10%, $V_{BAT} \geq 3.0V$, and when there is a finite I-R voltage drop in the V_{DD} line.

InterSeal™ Battery Saver

The ISL1208 has the InterSeal™ Battery Saver which prevents initial battery current drain before it is first used. For example, battery-backed RTCs are commonly packaged on a board with a battery connected. In order to preserve battery life, the ISL1208 will not draw any power from the battery source until after the device is first powered up from the V_{DD} source. Thereafter, the device will switchover to battery backup mode whenever V_{DD} power is lost.

Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24-hour or AM/PM format. When the ISL1208 powers up after the loss of both V_{DD} and V_{BAT}, the clock will not begin incrementing until at least one byte is written to the clock register.

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for

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the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal's nominal frequency. For example, a ~20ppm frequency deviation translates into an accuracy of ~1 minute per month. These parameters are available from the crystal manufacturer. The ISL1208 provides on-chip crystal compensation networks to adjust load capacitance to tune oscillator frequency from -94ppm to +140ppm. For more detailed information. See "Application Section" on page 18.

Single Event and Interrupt

The alarm mode is enabled via the ALME bit. Choosing single event or interrupt alarm mode is selected via the IM bit. Note that when the frequency output function is enabled, the alarm function is disabled.

The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs in single event mode, an $\overline{IRQ}$ pin will be pulled low and the alarm status bit (ALM) will be set to "1".

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence, once the alarm is set, the device will continue to alarm for each occurring match of the alarm and present time. Thus, it will alarm as often as every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{IRQ}$ pin will be pulled low for 250ms and the alarm status bit (ALM) will be set to "1".

NOTE: The ALM bit can be reset by the user or cleared automatically using the auto reset mode (see ARST bit).

The alarm function can be enabled/disabled during battery backup mode using the FOBATB bit. For more information on the alarm, See "Alarm Registers" on page 14.

Frequency Output Mode

The ISL1208 has the option to provide a frequency output signal using the $\overline{IRQ}$/FOUT pin. The frequency output mode is set by using the FO bits to select 15 possible output frequency values from 0kHz to 32kHz. The frequency output can be enabled/disabled during battery backup mode using the FOBATB bit.

General Purpose User SRAM

The ISL1208 provides 2 bytes of user SRAM. The SRAM will continue to operate in battery backup mode. However, it should be noted that the I^2C bus is disabled in battery backup mode.

I^2C Serial Interface

The ISL1208 has an I^2C serial bus interface that provides access to the control and status registers and the user SRAM. The I^2C serial interface is compatible with other industry I^2C serial bus protocols using a bidirectional data signal (SDA) and a clock signal (SCL).

Oscillator Compensation

The ISL1208 provides the option of timing correction due to temperature variation of the crystal oscillator for either manufacturing calibration or active calibration. The total possible compensation is typically -94ppm to +140ppm. Two compensation mechanisms that are available are as follows:

1. An analog trimming (ATR) register that can be used to adjust individual on-chip digital capacitors for oscillator capacitance trimming. The individual digital capacitor is selectable from a range of 9pF to 40.5pF (based upon 32.758kHz). This translates to a calculated compensation of approximately -34ppm to +80ppm. (See ATR description on page 18).
2. A digital trimming register (DTR) that can be used to adjust the timing counter by ±60ppm. (See DTR description on page 18).

Also provided is the ability to adjust the crystal capacitance when the ISL1208 switches from V_{DD} to battery backup mode. See "Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})" on page 9.

Register Descriptions

The battery-backed registers are accessible following a slave byte of "1101111x" and reads or writes to addresses [00h:13h]. The defined addresses and default values are described in Table 1. Address 09h is not used. Reads or writes to 09h will not affect operation of the device but should be avoided.

REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 4 sections. These are:

1. Real Time Clock (7 bytes): Address 00h to 06h.
2. Control and Status (5 bytes): Address 07h to 0Bh.
3. Alarm (6 bytes): Address 0Ch to 11h.
4. User SRAM (2 bytes): Address 12h to 13h.

There are no addresses above 13h.

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Write capability is allowable into the RTC registers (00h to 06h) only when the WRTC bit (bit 4 of address 07h) is set to “1”. **A multi-byte read or write operation is limited to one section per operation.** Access to another section requires a new operation. A read or write can begin at any address within the section.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

It is not necessary to set the WRTC bit prior to writing into the control and status, alarm, and user SRAM registers.

TABLE 1. REGISTER MEMORY MAP

ADDR.	SECTION	REG NAME	BIT								RANGE	DEFAULT
			7	6	5	4	3	2	1	0		
00h	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0 to 59	00h
02h		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	00h
04h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	00h
05h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
06h		DW	0	0	0	0	0	DW2	DW1	DW0	0 to 6	00h
07h	Control and Status	SR	ARST	XTOSCB	Reserved	WRTC	Reserved	ALM	BAT	RTCF	N/A	01h
08h		INT	IM	ALME	LPMODE	FOBATB	FO3	FO2	FO1	FO0	N/A	00h
09h		Reserved									N/A	00h
0Ah		ATR	BMATR1	BMATR0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0	N/A	00h
0Bh		DTR	Reserved					DTR2	DTR1	DTR0	N/A	00h
0Ch	Alarm	SCA	ESCA	ASC22	ASC21	ASC20	ASC13	ASC12	ASC11	ASC10	00 to 59	00h
0Dh		MNA	EMNA	AMN22	AMN21	AMN20	AMN13	AMN12	AMN11	AMN10	00 to 59	00h
0Eh		HRA	EHRA	0	AHR21	AHR20	AHR13	AHR12	AHR11	AHR10	0 to 23	00h
0Fh		DTA	EDTA	0	ADT21	ADT20	ADT13	ADT12	ADT11	ADT10	1 to 31	00h
10h		MOA	EMOA	0	0	AMO20	AMO13	AMO12	AMO11	AMO10	1 to 12	00h
11h		DWA	EDWA	0	0	0	0	ADW12	ADW11	ADW10	0 to 6	00h
12h	User	USR1	USR17	USR16	USR15	USR14	USR13	USR12	USR11	USR10	N/A	00h
13h		USR2	USR27	USR26	USR25	USR24	USR23	USR22	USR21	USR20	N/A	00h

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Real Time Clock Registers

Addresses [00h to 06h]

RTC REGISTERS (SC, MN, HR, DT, MO, YR, DW)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) can either be a 12-hour or 24-hour mode, DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99, and DW (Day of the Week) is 0 to 6.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as “0”.

24 HOUR TIME

If the MIL bit of the HR register is “1”, the RTC uses a 24-hour format. If the MIL bit is “0”, the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a “1” representing PM. The clock defaults to 12-hour format time with HR21 = “0”.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The ISL1208 does not correct for the leap year in the year 2100.

Control and Status Registers

Addresses [07h to 0Bh]

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register, Analog Trimming and Digital Trimming Registers.

Status Register (SR)

The Status Register is located in the memory map at address 07h. This is a volatile register that provides either control or status of RTC failure, battery mode, alarm trigger, write protection of clock counter, crystal oscillator enable and auto reset of status bits.

TABLE 2. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
07h	ARST	XTOSCB	reserved	WRTC	reserved	ALM	BAT	RTCF
Default	0	0	0	0	0	0	0	0

REAL TIME CLOCK FAIL BIT (RTCF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL1208 internally) when the device powers up after having lost all power to the device (both V_{DD} and V_{BAT} go to 0V). The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. On power-up after a total power failure, all registers are set to their default states and the clock will not increment until at least one byte is written to the clock register. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

BATTERY BIT (BAT)

This bit is set to a “1” when the device enters battery backup mode. This bit can be reset either manually by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

ALARM BIT (ALM)

These bits announce if the alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

NOTE: An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is “0”. Upon initialization or power-up, the WRTC must be set to “1” to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

CRYSTAL OSCILLATOR ENABLE BIT (XTOSCB)

This bit enables/disables the internal crystal oscillator. When the XTOSCB is set to “1”, the oscillator is disabled, and the X1 pin allows for an external 32kHz signal to drive the RTC. The XTOSCB bit is set to “0” on power-up.

AUTO RESET ENABLE BIT (ARST)

This bit enables/disables the automatic reset of the BAT and ALM status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the respective status register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the BAT and ALM bits.

Interrupt Control Register (INT)

TABLE 3. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
08h	IM	ALME	LPMODE	FOBATB	FO3	FO2	FO1	FO0
Default	0	0	0	0	0	0	0	0

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FREQUENCY OUT CONTROL BITS (FO <3:0>)

These bits enable/disable the frequency output function and select the output frequency at the $\overline{IRQ}$/fOUT pin. See Table 4 for frequency selection. When the frequency mode is enabled, it will override the alarm mode at the $\overline{IRQ}$/fOUT pin.

TABLE 4. FREQUENCY SELECTION OF fOUT PIN

FREQUENCY, f_{OUT}	UNITS	FO3	FO2	FO1	FO0
0	Hz	0	0	0	0
32768	Hz	0	0	0	1
4096	Hz	0	0	1	0
1024	Hz	0	0	1	1
64	Hz	0	1	0	0
32	Hz	0	1	0	1
16	Hz	0	1	1	0
8	Hz	0	1	1	1
4	Hz	1	0	0	0
2	Hz	1	0	0	1
1	Hz	1	0	1	0
1/2	Hz	1	0	1	1
1/4	Hz	1	1	0	0
1/8	Hz	1	1	0	1
1/16	Hz	1	1	1	0
1/32	Hz	1	1	1	1

FREQUENCY OUTPUT AND INTERRUPT BIT (FOBATB)

This bit enables/disables the fOUT/$\overline{IRQ}$ pin during battery backup mode (i.e. V_{BAT} power source active). When the FOBATB is set to “1” the fOUT/$\overline{IRQ}$ pin is disabled during battery backup mode. This means that both the frequency output and alarm output functions are disabled. When the FOBATB is cleared to “0”, the fOUT/$\overline{IRQ}$ pin is enabled during battery backup mode.

LOW POWER MODE BIT (LPMODE)

This bit enables/disables low power mode. With LPMODE = “0”, the device will be in normal mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$ and $V_{DD} < V_{TRIP}$. With LPMODE = “1”, the device will be in low power mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$. There is a supply current saving of about 600nA when using LPMODE = “1” with V_{DD} = 5V. (See Typical Performance Curves on page 7: I_{DD} vs V_{CC} with LPMODE ON and OFF.) Avoid setting the device into low power mode with $V_{DD} < V_{BAT}$, the I2C communications will stop permanently. The V_{BAT} input must be lowered below V_{DD} to resume communications.

ALARM ENABLE BIT (ALME)

This bit enables/disables the alarm function. When the ALME bit is set to “1”, the alarm function is enabled. When the ALME is cleared to “0”, the alarm function is disabled. The alarm function can operate in either a single event alarm or a periodic interrupt alarm (see IM bit).

NOTE: When the frequency output mode is enabled, the alarm function is disabled.

INTERRUPT/ALARM MODE BIT (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to “1”, the alarm will operate in the interrupt mode, where an active low pulse width of 250ms will appear at the $\overline{IRQ}$/fOUT pin when the RTC is triggered by the alarm as defined by the alarm registers (0Ch to 11h). When the IM bit is cleared to “0”, the alarm will operate in standard mode, where the $\overline{IRQ}$/fOUT pin will be tied low until the ALM status bit is cleared to “0”.

IM BIT	INTERRUPT/ALARM FREQUENCY
0	Single Time Event Set By Alarm
1	Repetitive/Recurring Time Event Set By Alarm

Analog Trimming Register

ANALOG TRIMMING REGISTER (ATR<5:0>)

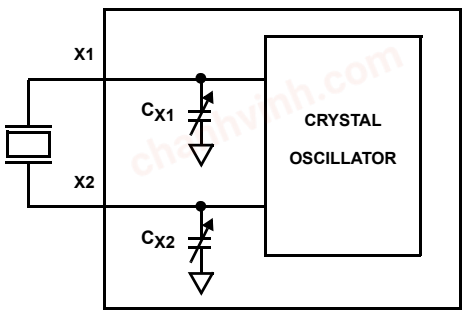


FIGURE 13. DIAGRAM OF ATR

Six analog trimming bits, **ATR0** to **ATR5**, are provided in order to adjust the on-chip load capacitance value for frequency compensation of the RTC. Each bit has a different weight for capacitance adjustment. For example, using a Citizen CFS-206 crystal with different ATR bit combinations provides an estimated ppm adjustment range from -34ppm to +80ppm to the nominal frequency compensation. The combination of analog and digital trimming can give up to -94ppm to +140ppm of total adjustment.

The effective on-chip series load capacitance, C_{LOAD}, ranges from 4.5pF to 20.25pF with a mid-scale value of 12.5pF (default). C_{LOAD} is changed via two digitally controlled capacitors, C_{X1} and C_{X2}, connected from the X1 and X2 pins to ground (see Figure 11). The value of C_{X1} and C_{X2} are given in Equation 1:

$$C_X = (16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9)pF \quad \text{(EQ. 1)}$$

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The effective series load capacitance is the combination of C_{X1} and C_{X2} in Equation 2.:

$$C_{LOAD} = \frac{1}{\left(\frac{1}{C_{X1}} + \frac{1}{C_{X2}}\right)} \quad \text{(EQ. 2)}$$

$$C_{LOAD} = \left(\frac{16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9}{2}\right) pF$$

For example, C_{LOAD} (ATR = 00000) = 12.5pF, C_{LOAD} (ATR = 100000) = 4.5pF, and C_{LOAD} (ATR = 011111) = 20.25pF. The entire range for the series combination of load capacitance goes from 4.5pF to 20.25pF in 0.25pF steps. Note that these are typical values.

BATTERY MODE ATR SELECTION (BMATR <1:0>)

Since the accuracy of the crystal oscillator is dependent on the V_{DD}/V_{BAT} operation, the ISL1208 provides the capability to adjust the capacitance between V_{DD} and V_{BAT} when the device switches between power sources.

BMATR1	BMATR0	DELTA CAPACITANCE (C_{BAT} TO C_{VDD})
0	0	0pF
0	1	-0.5pF (≈ +2ppm)
1	0	+0.5pF (≈ -2ppm)
1	1	+1pF (≈ -4ppm)

DIGITAL TRIMMING REGISTER (DTR <2:0>)

The digital trimming bits DTR0, DTR1, and DTR2 adjust the average number of counts per second and average the ppm error to achieve better accuracy.

- DTR2 is a sign bit. DTR2 = “0” means frequency compensation is >0. DTR2 = “1” means frequency compensation is <0.
- DTR1 and DTR0 are both scale bits. DTR1 gives 40ppm adjustment and DTR0 gives 20ppm adjustment.

A range from -60ppm to +60ppm can be represented by using these three bits (see Table 5).

TABLE 5. DIGITAL TRIMMING REGISTERS

DTR REGISTER			ESTIMATED FREQUENCY PPM
DTR2	DTR1	DTR0	
0	0	0	0 (default)
0	0	1	+20
0	1	0	+40
0	1	1	+60
1	0	0	0
1	0	1	-20
1	1	0	-40
1	1	1	-60

Alarm Registers

Addresses [0Ch to 11h]

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

- **Single Event Mode** is enabled by setting the ALME bit to “1”, the IM bit to “0”, and disabling the frequency output. This mode permits a one-time match between the alarm registers and the RTC registers. Once this match occurs, the ALM bit is set to “1” and the $\overline{IRQ}$ output will be pulled low and will remain low until the ALM bit is reset. This can be done manually or by using the auto-reset feature.
- **Interrupt Mode** is enabled by setting the ALME bit to “1”, the IM bit to “1”, and disabling the frequency output. The $\overline{IRQ}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading.

To clear an alarm, the ALM bit in the status register must be set to “0” with a write. Note that if the ARST bit is set to 1 (address 07h, bit 7), the ALM bit will automatically be cleared when the status register is read.

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Below are examples of both Single Event and periodic Interrupt Mode alarms.

Example 1 – Alarm set with single interrupt (IM="0")

A single alarm will occur on January 1 at 11:30am.

A. Set Alarm registers as follows:

ALARM REGISTER	BIT								HEX	DESCRIPTION
	7	6	5	4	3	2	1	0		
SCA	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Also the ALME bit must be set as follows:

CONTROL REGISTER	BIT								HEX	DESCRIPTION
	7	6	5	4	3	2	1	0		
INT	0	1	x	x	0	0	0	0	x0h	Enable Alarm

xx indicate other control bits

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30am on January 1 (after seconds changes from 59 to 00) by setting the ALM bit in the status register to "1" and also bringing the $\overline{IRQ}$ output low.

Example 2 – Pulsed interrupt once per minute (IM="1")

Interrupts at one minute intervals when the seconds register is at 30 seconds.

A. Set Alarm registers as follows:

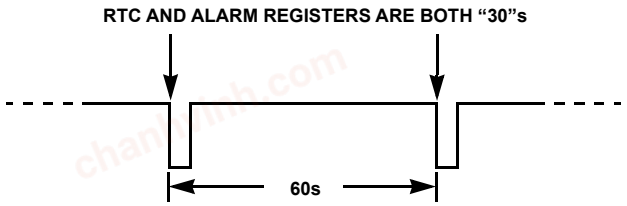
ALARM REGISTER	BIT								HEX	DESCRIPTION
	7	6	5	4	3	2	1	0		
SCA	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA	0	0	0	0	0	0	0	0	00h	Date disabled
MOA	0	0	0	0	0	0	0	0	00h	Month disabled
DWA	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Set the Interrupt register as follows:

CONTROL REGISTER	BIT								HEX	DESCRIPTION
	7	6	5	4	3	2	1	0		
INT	1	1	x	x	0	0	0	0	x0h	Enable Alarm and Int Mode

xx indicate other control bits

Once the registers are set, the following waveform will be seen at IRQ-:



Note that the status register ALM bit will be set each time the alarm is triggered, but does not need to be read or cleared.

User Registers

Addresses [12h to 13h]

These registers are 2 bytes of battery-backed user memory storage.

I^2C Serial Interface

The ISL1208 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL1208 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 14). On power-up of the ISL1208, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL1208 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 14). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 14). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 15).

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The ISL1208 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL1208 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

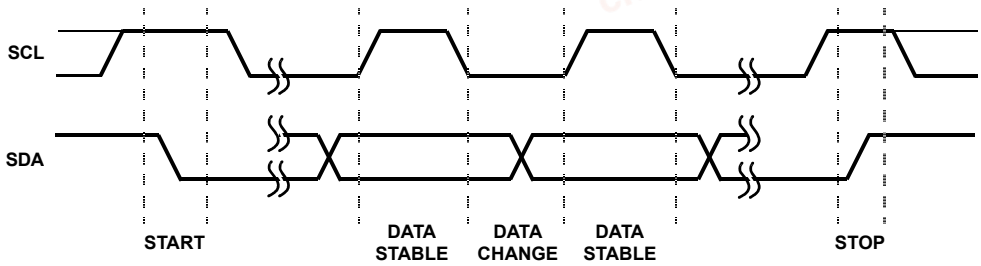


FIGURE 14. VALID DATA CHANGES, START, AND STOP CONDITIONS

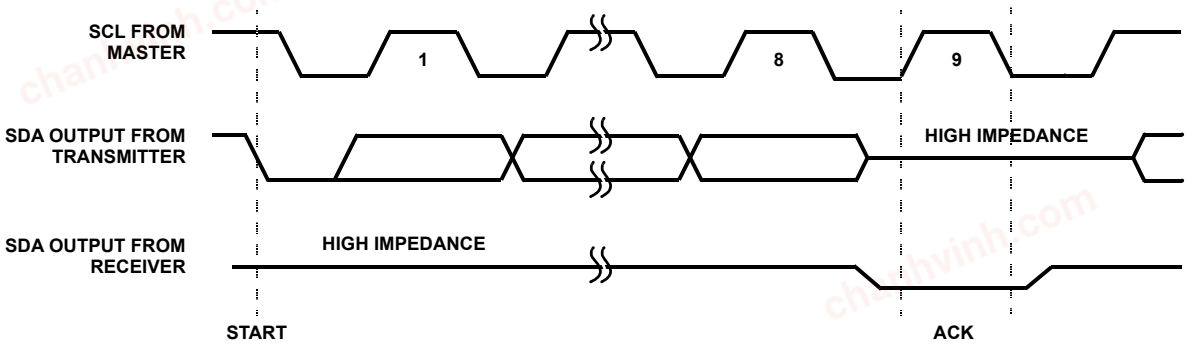


FIGURE 15. ACKNOWLEDGE RESPONSE FROM RECEIVER

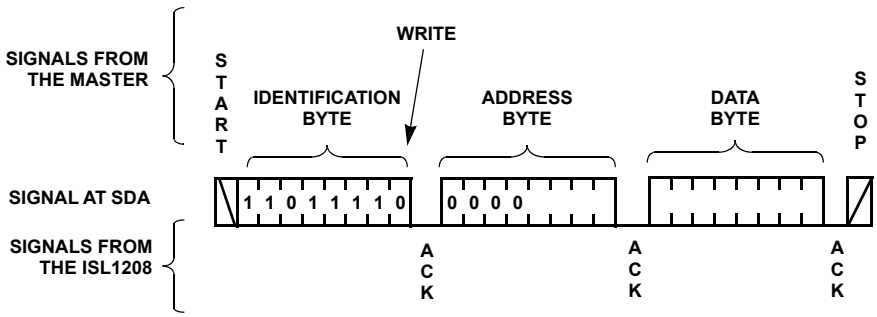


FIGURE 16. BYTE WRITE SEQUENCE

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Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifier. These bits are “1101111”. Slave bits “1101” access the register. Slave bits “111” specify the device select bits.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a “1”, then a read operation is selected. A “0” selects a write operation (Refer to Figure 17).

After loading the entire Slave Address Byte from the SDA bus, the ISL1208 compares the device identifier and device select bits with “1101111”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up the internal address counter is set to address 0h, so a current address read of the CCR array starts at address 0h. When required, as part of a random read, the master must supply the 1 Word Address Bytes as shown in Figure 18.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Clock/Control Registers, the slave byte must be “1101111x” in both places.

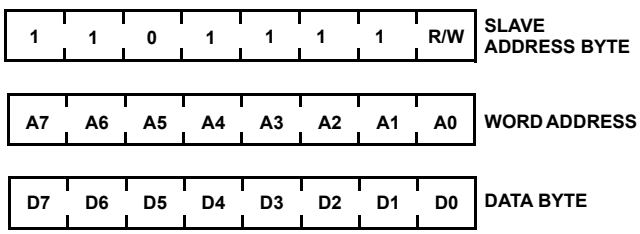


FIGURE 17. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL1208 responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (See Figure 18). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL1208 responds with an ACK. Then the ISL1208 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (See Figure 18).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 13h the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

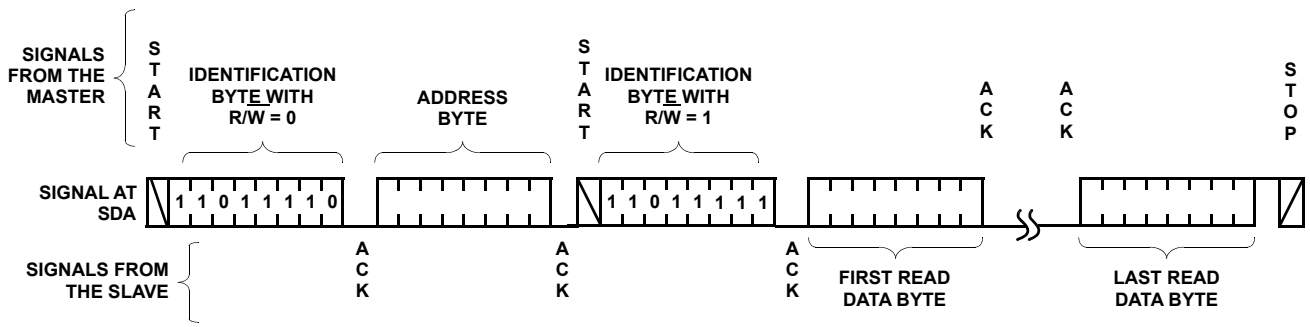


FIGURE 18. READ SEQUENCE

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Application Section

Oscillator Crystal Requirements

The ISL1208 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 6 lists some recommended surface mount crystals. Other surface mount crystals can be used, if their specifications are very similar to the devices listed.

The crystal should have the following parameters:

- a maximum drive power of $D_{L(max)}$ = 1µW
- a required parallel load capacitance of C_L = 12.5pF
- an equivalent series resistance of ESR ≤ 50kΩ.

The temperature range specification of the crystal should match the application (especially through hole and tuning fork types). The crystals in Table 6 are rated for -40°C to +85°C.

TABLE 6. SUGGESTED SURFACE MOUNT CRYSTALS

MANUFACTURER	PART NUMBER
ECS	ECS-.327-12.5-17X-TR
Epson	FC-135R 32.7680KA-E3
Abracon	ABS25-32.768KHZ-4-T
Fox	FSRLF327
Pletronics	SM13S-32.768K
Diodes Inc.(Note 17)	G43270019
Epson (Note 17)	MC-306 32.7680K-A0: PURE SN
Epson (Note 17)	MC-30AY32.7680K-A3:PURE SN

NOTE:

17. ESR_{max} = 35kΩ

Crystal Oscillator Frequency Adjustment

The ISL1208 device contains circuitry for adjusting the frequency of the crystal oscillator. This circuitry can be used to trim oscillator initial accuracy as well as adjust the frequency to compensate for temperature changes.

The Analog Trimming Register (ATR) is used to adjust the load capacitance seen by the crystal. There are six bits of ATR control, with linear capacitance increments available for adjustment. Since the ATR adjustment is essentially “pulling” the frequency of the oscillator, the resulting frequency changes will not be linear with incremental capacitance changes. The equations which govern pulling show that lower capacitor values of ATR adjustment will provide larger increments. Also, the higher values of ATR adjustment will produce smaller incremental frequency changes. These values typically vary from 6ppm to 10 ppm/bit at the low end to <1ppm/bit at the highest capacitance settings. The range afforded by the ATR adjustment with a typical surface mount crystal is typically -34ppm to +80ppm around the ATR=0 default setting because of this property. The user should note this when using the ATR for calibration. The temperature drift of the capacitance used in the ATR control is extremely low, so this feature can be used for temperature compensation with good accuracy.

In addition to the analog compensation afforded by the adjustable load capacitance, a digital compensation feature is available for the ISL1208. There are 3 bits known as the Digital Trimming Register (DTR). The range provided is ±60ppm in increments of 20ppm. DTR operates by adding or skipping pulses in the clock counter. It is very useful for coarse adjustments of frequency drift over temperature or extending the adjustment range available with the ATR register.

Initial accuracy is best adjusted by enabling the frequency output (using the INT register, address 08h), and monitoring the ~IRQ/fOUT pin with a calibrated frequency counter. The frequency used is unimportant, although 1Hz is the easiest to monitor. The gating time should be set long enough to ensure accuracy to at least 1ppm. The ATR should be set to the center position, or 100000Bh, to begin with. Once the initial measurement is made, then the ATR register can be changed to adjust the frequency. Note that increasing the ATR register for increased capacitance will lower the frequency, and vice-versa. If the initial measurement shows the frequency is far off, it will be necessary to use the DTR register to do a coarse adjustment. Note that most all crystals will have tight enough initial accuracy at room temperature so that a small ATR register adjustment should be all that is needed.

Temperature Compensation

The ATR and DTR controls can be combined to provide crystal drift temperature compensation. The typical 32.768kHz crystal has a drift characteristic that is similar to that shown in Figure 19. There is a turnover temperature (T_0) where the drift is very near zero. The shape is parabolic as it varies with the square of the difference between the actual temperature and the turnover temperature.

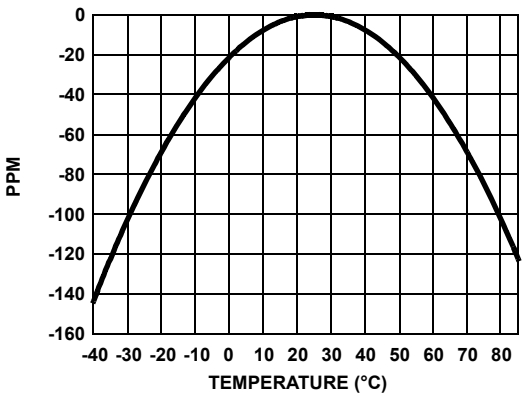


FIGURE 19. RTC CRYSTAL TEMPERATURE DRIFT

If full industrial temperature compensation is desired in an ISL1208 circuit, then both the DTR and ATR registers will need to be utilized (total correction range = -94ppm to +140ppm).

A system to implement temperature compensation would consist of the ISL1208, a temperature sensor, and a

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microcontroller. These devices may already be in the system so the function will just be a matter of implementing software and performing some calculations. Fairly accurate temperature compensation can be implemented just by using the crystal manufacturer's specifications for the turnover temperature T_0 and the drift coefficient (β). The formula for calculating the oscillator adjustment necessary is Equation 3:

$$\text{Adjustment(ppm)} = (T - T_0)^2 * \beta \quad \text{(EQ. 3)}$$

Once the temperature curve for a crystal is established, then the designer should decide at what discrete temperatures the compensation will change. Since drift is higher at extreme temperatures, the compensation may not be needed until the temperature is greater than +20°C from T_0.

A sample curve of the ATR setting vs Frequency Adjustment for the ISL1208 and a typical RTC crystal is given in Figure 20. This curve may vary with different crystals, so it is good practice to evaluate a given crystal in an ISL1208 circuit before establishing the adjustment values.

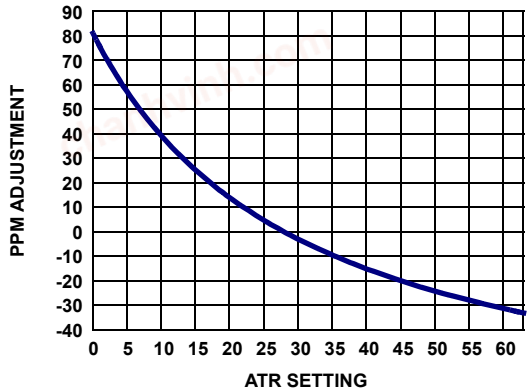


FIGURE 20. ATR SETTING vs OSCILLATOR FREQUENCY ADJUSTMENT

This curve is then used to figure what ATR and DTR settings are used for compensation. The results would be placed in a lookup table for the microcontroller to access.

Note that the ATR register affects the F_{OUT} frequency directly. Also, the DTR setting will affect the F_{OUT} frequency for all but the 32.768Khz setting, due to the clock correction in the divider chain.

Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies such as 32.768kHz are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 21 shows a suggested layout for the ISL1208 device using a surface mount crystal. Two main precautions should be followed:

1. Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.
2. Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

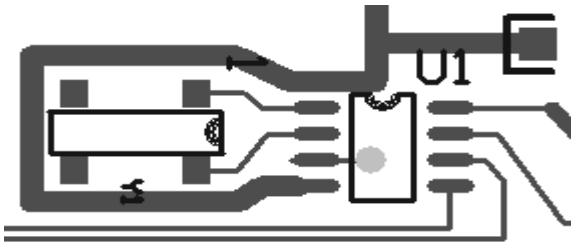


FIGURE 21. SUGGESTED LAYOUT FOR ISL1208 AND CRYSTAL

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the $\overline{IRQ}$/FOUT pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{BAT} and V_{CC} pins can be treated as a ground, and should be routed around the crystal.

Battery Backup Considerations

The ISL1208 device provides a V_{BAT} pin which is used for a battery backup input. The battery voltage can vary from 1.8V up to 5.5V, independent of the V_{DD} supply voltage. An internal switch automatically connects the VBAT supply to the to the internal power node when V_{DD} power goes away, and switches back to V_{DD} when power returns.

Since this battery switch draws power from the battery, it is very low power and not very fast. If the V_{DD} drops too quickly to 0V, there is not enough time for the switch to connect the V_{BAT} source to the internal power node, and the SRAM contents can be lost or corrupted. It is a good idea to keep power-down ramps longer than 50us to insure data retention.

Battery drain can be minimized by using the LPMODE option. Since normally the V_{BAT} and V_{DD} need to be monitored in order to switch at the lower voltage, two comparator function are needed during battery backup. LPMODE shuts off one of the comparators and just compares V_{DD} to V_{BAT} to activate switchover. This saves about 500nA of VBAT current at 3.0V. Do not use LPMODE when $V_{BAT} \geq V_{DD}$ - 0.2V, to avoid permanently placing the device in battery backup mode.

Another consideration is systems with either ground bounce or power supply transients that cause the V_{DD} pin to drop below ground for more than a few nanoseconds. This type of power glitch can override the V_{BAT} backup and reset or corrupt the SRAM. If these transient glitches are present in a system with the ISL1208, or the device is experiencing unexplained loss of

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data when returning from V_{BAT} mode, a protection circuit should be added. Figure 22 shows a circuit which effectively isolates the V_{DD} input from negative glitches. The Schottky diode is needed to for low voltage drop and effective protection from the negative transient. Note that this circuit will also help if the V_{DD} fall time is less than 50us as CIN holds up the V_{DD} pin during the transient.

There is also a shunt shown between the battery and the V_{BAT} pin. This is for quick disconnect if there is a situation where a transient has latched the device and it will not communicate on the I2C bus. If ground bounce is a problem, then a second Schottky diode should be added between the battery and the V_{BAT} pin.

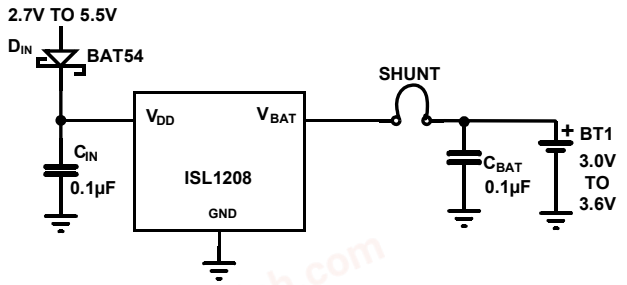


FIGURE 22. POWER GLITCH PROTECTION CIRCUIT

Super Capacitor Backup

A Super Capacitor can be used as an alternative to a battery in cases where shorter backup times are required. Since the battery backup supply current required by the ISL1208 is extremely low, it is possible to get months of backup operation using a Super Capacitor. Typical capacitor values are a few µF to 1F or more depending on the application.

If backup is only needed for a few minutes, then a small inexpensive electrolytic capacitor can be used. For extended periods, a low leakage, high capacity Super Capacitor is the best choice. These devices are available from such vendors as Panasonic and Murata. The main specifications include working voltage and leakage current. If the application is for charging the capacitor from a +5V ±5% supply with a signal diode, then the voltage on the capacitor can vary from ~4.5V to slightly over 5.0V. A capacitor with a rated WV of 5.0V may have a reduced lifetime if the supply voltage is slightly high. The leakage current should be as small as possible. For example, a Super Capacitor should be specified with leakage of well below 1µA. A standard electrolytic capacitor with DC leakage current in the microamps will have a severely shortened backup time.

Below are some examples with equations to assist with calculating backup times and required capacitance for the ISL1208 device. The backup supply current plays a major part in these equations, and a typical value was chosen for example purposes. For a robust design, a margin of 30% should be included to cover supply current and capacitance tolerances over the results of the calculations. Even more margin should be included if periods of very warm temperature operation are expected.

Example 1. Calculating Backup Time Given Voltages and Capacitor Value

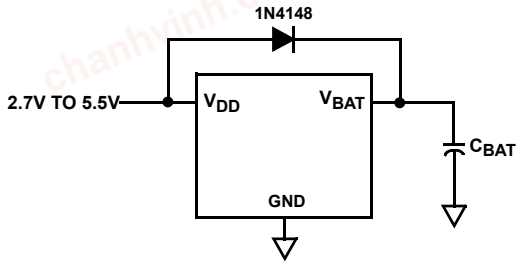


FIGURE 23. SUPERCAPACITOR CHARGING CIRCUIT

In Figure 23, use C_{BAT} = 0.47F and V_{CC} = 5.0V. With V_{CC} = 5.0V, the voltage at V_{BAT} will approach 4.7V as the diode turns off completely. The ISL1208 is specified to operate down to V_{BAT} = 1.8V. The capacitance charge/discharge equation (Equation 4) is used to estimate the total backup time:

$$I = C_{BAT} * dV/dT \quad \text{(EQ. 4)}$$

Rearranging gives:

$$dT = C_{BAT} * dV/I_{TOT} \text{ to solve for backup time.} \quad \text{(EQ. 5)}$$

C_{BAT} is the backup capacitance and dV is the change in voltage from fully charged to loss of operation. Note that I_{TOT} is the total of the supply current of the ISL1208 (I_{BAT}) plus the leakage current of the capacitor and the diode, I_{LKG}. In these calculations, I_{LKG} is assumed to be extremely small and will be ignored. If an application requires extended operation at temperatures over +50°C, these leakages will increase and hence reduce backup time.

Note that I_{BAT} changes with V_{BAT} almost linearly (see Typical Performance Curves on page 7). This allows us to make an approximation of I_{BAT}, using a value midway between the two endpoints. The typical linear equation for I_{BAT} vs V_{BAT} is in Equation 6:

$$I_{BAT} = 1.031E\text{-}7*(V_{BAT}) + 1.036E\text{-}7 \text{ Amps} \quad \text{(EQ. 6)}$$

Using this equation to solve for the average current given 2 voltage points gives Equation 7:

$$I_{BATAVG} = 5.155E\text{-}8*(V_{BAT2} + V_{BAT1}) + 1.036E\text{-}7 \text{ Amps} \quad \text{(EQ. 7)}$$

Combining with Equation 5 gives the equation for backup time in Equation 8:

$$T_{BACKUP} = C_{BAT} * (V_{BAT2} - V_{BAT1}) / (I_{BATAVG} + I_{LKG}) \text{ seconds} \quad \text{(EQ. 8)}$$

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where:

C_{BAT} = 0.47F

V_{BAT2} = 4.7V

V_{BAT1} = 1.8V

I_{LKG} = 0 (assumed minimal)

Solving Equation 7 for this example, I_{BATAVG} = 4.387E-7 A

T_{BACKUP} = 0.47 * (2.9) / 4.38E-7 = 3.107E6 sec

Since there are 86,400 seconds in a day, this corresponds to 35.96 days. If the 30% tolerance is included for capacitor and supply current tolerances, then worst case backup time would be:

C_{BAT} = 0.70 * 35.96 = 25.2 days

Example 2. Calculating a Capacitor Value for a Given Backup Time

Referring to Figure 23 again, the capacitor value needs to be calculated to give 2 months (60 days) of backup time, given V_{CC} = 5.0V. As in Example 1, the V_{BAT} voltage will vary from 4.7V down to 1.8V. We will need to rearrange Equation 5 to solve for capacitance in Equation 9:

$$C_{BAT} = dT*I/dV \quad \text{(EQ. 9)}$$

Using the terms described above, this equation becomes Equation 10:

$$C_{BAT} = T_{BACKUP} * (I_{BATAVG} + I_{LKG})/(V_{BAT2} - V_{BAT1}) \quad \text{(EQ. 10)}$$

where:

T_{BACKUP} = 60 days * 86,400 sec/day = 5.18 E6 seconds

I_{BATAVG} = 4.387 E-7 A (same as Example 1)

I_{LKG} = 0 (assumed)

V_{BAT2} = 4.7V

V_{BAT1} = 1.8VSolving gives

C_{BAT} = 5.18 E6 * (4.387 E-7)/(2.9) = 0.784F

If the 30% tolerance is included for tolerances, then worst case capacitor value would be:

$$C_{BAT} = 1.3 \times 0.784 = 1.02F \quad \text{(EQ. 11)}$$

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

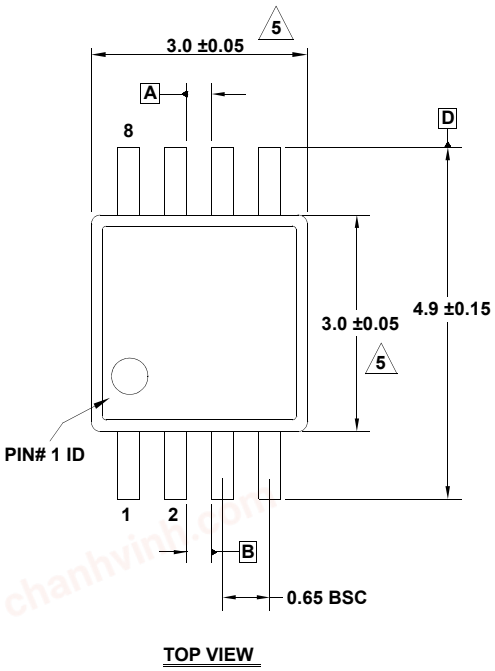
DATE	REVISION	CHANGE
Jul 15, 2022	9.01	Added Figure 1.
Jul 21, 2021	9.00	Updated external links throughout. **Updated Ordering Information table removing retired parts and formatting table and notes.** **Updated Oscillator Crystal Requirements section.** **Updated Thermal Information as follows:** **-Changed SOIC Theta JA from 95 to 108 and Theta JC from N/A to 55** **-Changed MSOP Theta JA from 128 to 145 and Theta JC from N/A to 55** **-Changed TDFN Theta JA from 53.7 to 45 and Theta JC from 2.8 to 3.5** **-Updated Notes.** **Updated POD M8.118 to the latest revision, changes are as follows:** **-Updated to new format by adding land pattern and moving dimensions from table onto drawing** **-Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36"** **-Corrected typo in the side view 1 updating package thickness tolerance from ±010 to ±0.10.** **Updated POD L8.3x3A to the latest revision, changes are as follows:** **-Updated to new standards by adding land pattern and moving dimensions from table onto drawing.** **-Updated Tiebar Note** **Changed POD MDP0027 to POD** M8.15E. **Added Revision History.**

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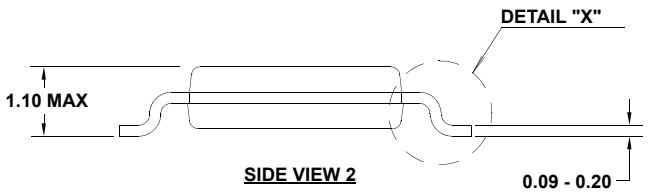
Package Outline Drawings

For the most recent package outline drawing, see M8.118.

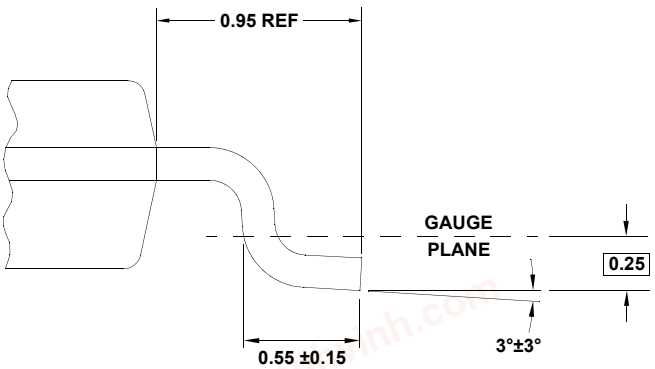
M8.118
8 Lead Mini Small Outline Plastic Package
Rev 5, 5/2021



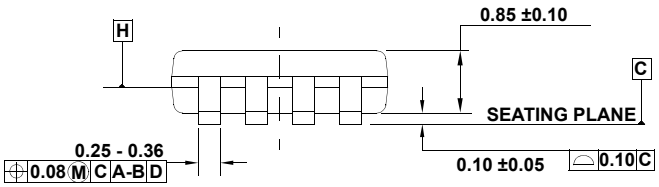
TOP VIEW



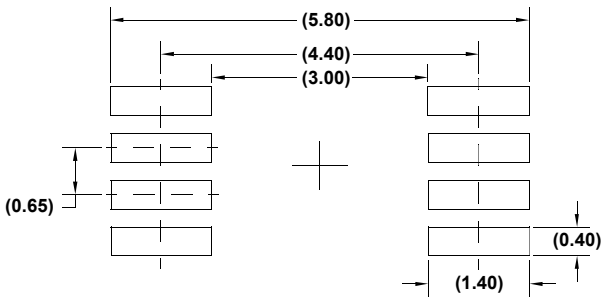
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

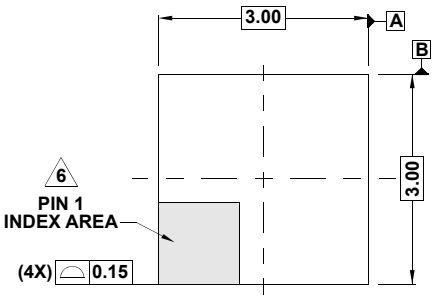
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

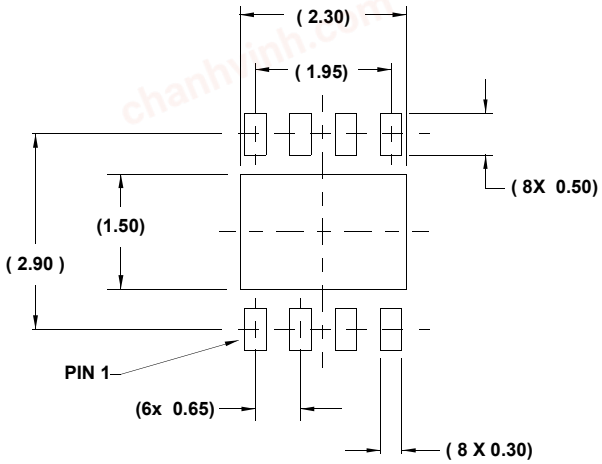
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For the most recent package outline drawing, see L8.3x3A.

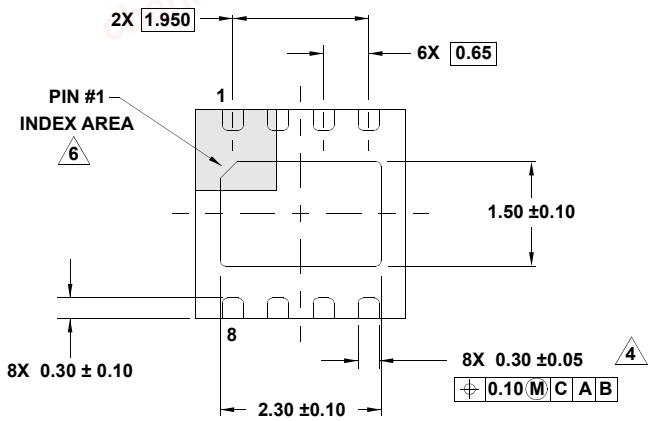
L8.3x3A
8 Lead Thin Dual Flat No-Lead Plastic Package
Rev 5, 5/15



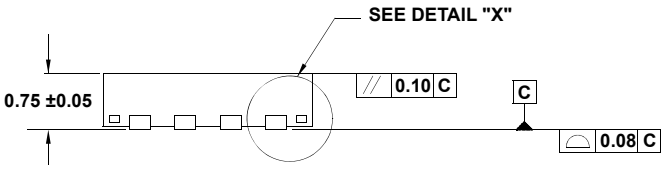
TOP VIEW



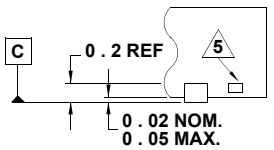
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

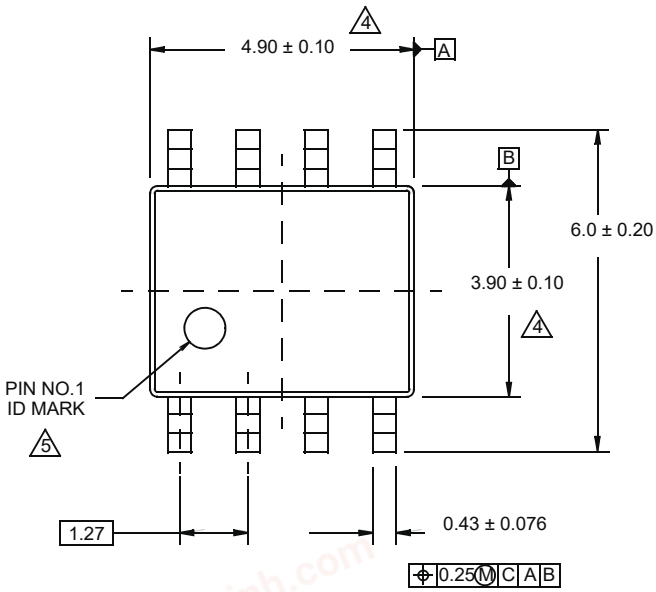
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

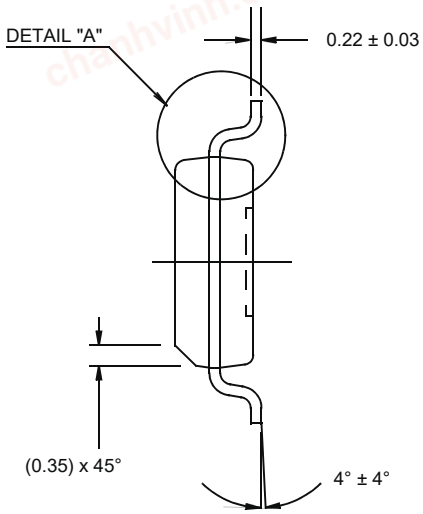
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For the most recent package outline drawing, see M8.15E.

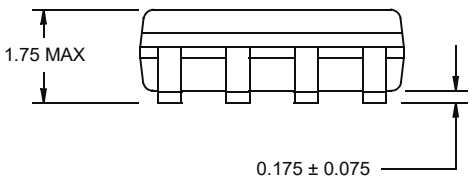
M8.15E
8 Lead Narrow Body Small Outline Plastic Package
Rev 0, 08/09



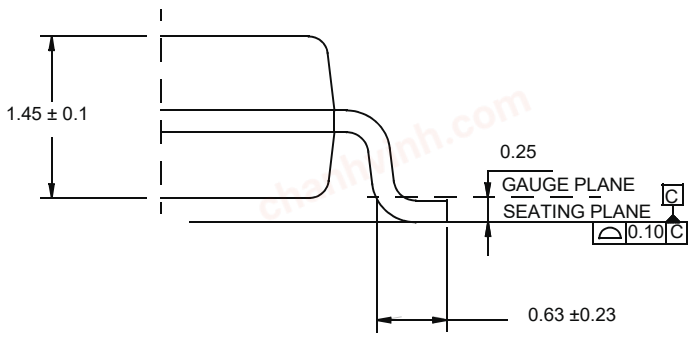
TOP VIEW



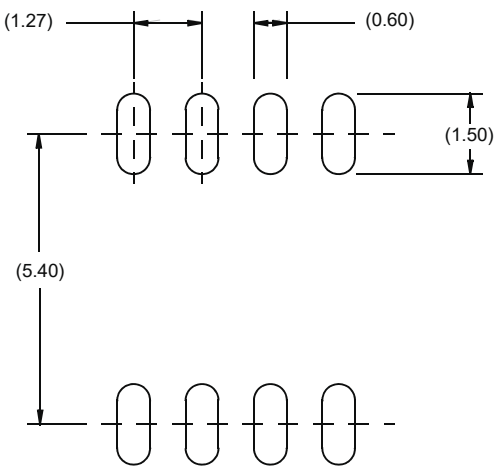
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

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