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ISL12057

Low Cost and Low Power I^{2}C RTC Real Time Clock/Calendar with Alarm Function and Dual IRQ Pins

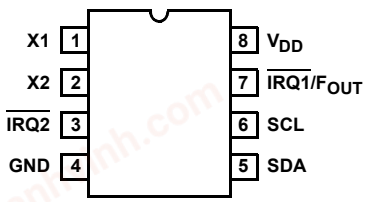
FN6755
Rev 2.00
Sep 25, 2015

The ISL12057 device is a low-power, real-time clock that is pin compatible and functionally equivalent to Maxim DS1337 with clock/calendar and alarm function.

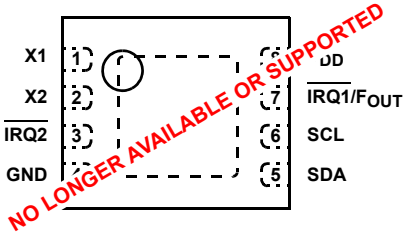
The oscillator uses an external, low-cost 32.768kHz crystal with 6pF load capacitance. The real-time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year, and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Pinouts

ISL12057
(8 LD SOIC, MSOP)
TOP VIEW



ISL12057
(8 LD UTDFN)
TOP VIEW



Features

- **Pin Compatible to Maxim DS1337**
- **Functionally Equivalent to Maxim DS1337**
- **Real-Time Clock/Calendar**
  - Tracks Time in Hours, Minutes, and Seconds
  - Day of the Week, Date, Month, and Year
- **Dual Interrupts for Frequency Output and Alarm interrupts**
- **Four Selectable Frequency Outputs**
- **Two Alarms**
  - Settable to the Second, Minute, Hour, Day of the Week, and Date
- **I^{2}C Interface**
  - 400kHz Data Transfer Rate
- **Small Package Options**
  - 8 Ld 2mmx2mm UTDFN
  - 8 Ld MSOP
  - 8 Ld SOIC
  - Pb-Free (RoHS Compliant)

Applications

- **Utility Meters**
- **HVAC Equipment**
- **Audio/Video Components**
- **Set-Top Box/Television**
- **Modems**
- **Network Routers, Hubs, Switches, Bridges**
- **Cellular Infrastructure Equipment**
- **Fixed Broadband Wireless Equipment**
- **Pagers/PDA**
- **Point Of Sale Equipment**
- **Test Meters/Fixtures**
- **Office Automation (Copiers, Fax)**
- **Home Appliances**
- **Computer Products**
- **Other Industrial/Medical/Automotive**

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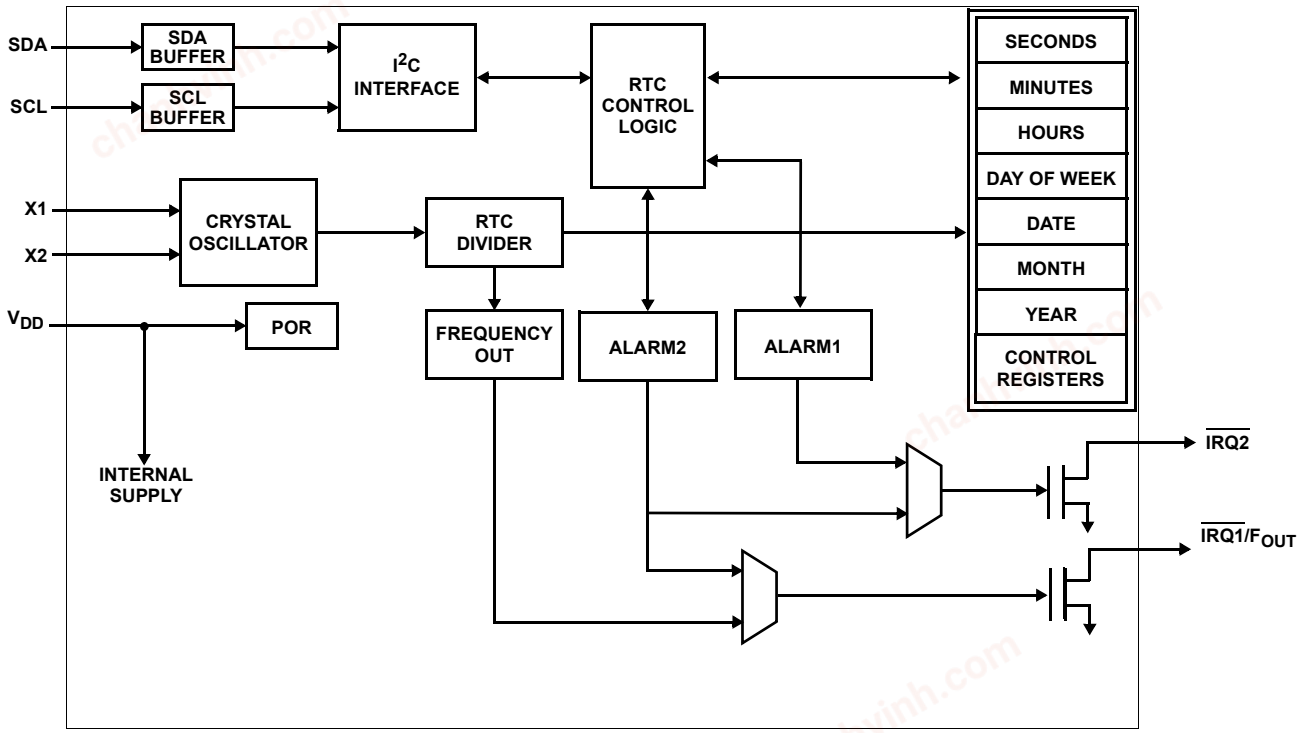
Ordering Information

PART NUMBER	PART MARKING	V_{DD} RANGE (V)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL12057IBZ (Notes 1, 2)	12057 IBZ	1.4 to 3.6	-40 to +85	8 Ld SOIC	M8.15
ISL12057IUZ (Notes 1, 2)	12057	1.4 to 3.6	-40 to +85	8 Ld MSOP	M8.118
ISL12057IRUZ-T (Notes 3, 4) **(No longer available or supported)**	057	1.4 to 3.6	-40 to +85	8 Ld UTDFN (Tape and Reel)	L8.2x2
ISL12057EVALZ	Evaluation Board				

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. Please refer to TB347 for details on reel specifications.

Block Diagram



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Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	X1	The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. The required crystal load capacitance is 6pF. This pin can also be driven by an external 32.768kHz oscillator with X2 pin floating.
2	X2	The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. The required crystal load capacitance is 6pF.
3	$\overline{IRQ2}$	Interrupt Output 2 is a multi-functional pin that can be used as an alarm interrupt. This pin is open drain and requires an external pull-up resistor. This pin is at high impedance at power-up.
4	GND	Ground
5	SDA	Serial Data (SDA) is a bidirectional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs.
6	SCL	The Serial Clock (SCL) input is used to clock all serial data into and out of the device.
7	$\overline{IRQ1}/F_{OUT}$	Interrupt Output 1/Frequency Output is a multi-functional pin that can be used as an alarm interrupt or frequency output pin. The function is set via the configuration register. This pin is open drain and requires an external pull-up resistor. It has a default output of 32.768kHz at power-up.
8	V_{DD}	Power supply

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Absolute Maximum Ratings

Voltage on V_{DD} (Respect to GND) . . . . . -0.2V to 4V
Voltage on $\overline{IRQ1}/F_{OUT}$, $\overline{IRQ2}$, SCL and SDA (Respect to GND). . . . . -0.2V to 6V
Voltage on X1 and X2 Pins (Respect to GND). . . . . -0.2V to 4V
ESD Rating ((Per MIL-STD-883 Method 3014)
Human Body Model . . . . . >4kV
Machine Model. . . . . >350V

Thermal Information

Thermal Resistance (Typical) (Note 5)	θ_{JA} (°C/W)
8 Lead SOIC	120
8 Lead MSOP	169
8 Lead UTDFN	160

Storage Temperature . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

DC Operating Characteristics – RTC

Temperature = -40°C to +85°C, unless otherwise stated. Crystal load capacitance = 6pF.
Boldface limits apply over the operating temperature range, -40°C to +85°C.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 8)	TYP (Note 7)	MAX (Note 8)	UNITS	NOTES
V_{DD}	Full Operation Power Supply		**1.8**		**3.6**	V	
V_{DDT}	Timekeeping Power Supply		**1.4**		**1.8**	V	
I_{DD1}	Standby Supply Current	V_{DD} = 3.6V		600	950	nA	6, 11
		V_{DD} = 3.3V		500		nA	
I_{DD2}	Timekeeping Current	V_{DD} = 1.8V		400	650	nA	6, 11
		V_{DD} = 1.6V		350		nA	
I_{DD3}	Supply Current With I^2C Active at Clock Speed of 400kHz	V_{DD} = 3.6V		15	**40**	µA	6
I_{LI}	Input Leakage Current on SCL		**-100**		**100**	nA	
I_{LO}	I/O Leakage Current on SDA		**-100**		**100**	nA	
$\overline{IRQ1}/F_{OUT}$ and $\overline{IRQ2}$							
V_{OL}	Output Low Voltage	V_{DD} = 1.8V, I_{OL} = 3mA			**0.4**	V	

Serial Interface Specifications

Over the recommended operating conditions unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP (Note 7)	MAX (Note 8)	UNITS	NOTES
SERIAL INTERFACE SPECS							
V_{IL}	SDA and SCL Input Buffer LOW Voltage		**-0.3**		**0.3 x V_{DD}**	V	
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		**0.7 x V_{DD}**		**5.5**	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.04 x V_{DD}		V	
V_{PULLUP}	Maximum Pull-up voltage on SDA during I^2C communication				**V_{DD} + 2**	V	10
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{DD} > 1.8V, V_{PULLUP} = 5.0V	**0**		**0.4**	V	
Cpin	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			**10**	pF	9
f_{SCL}	SCL Frequency				**400**	kHz	
t_{IN}	Pulse width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			**50**	ns	

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Serial Interface Specifications Over the recommended operating conditions unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

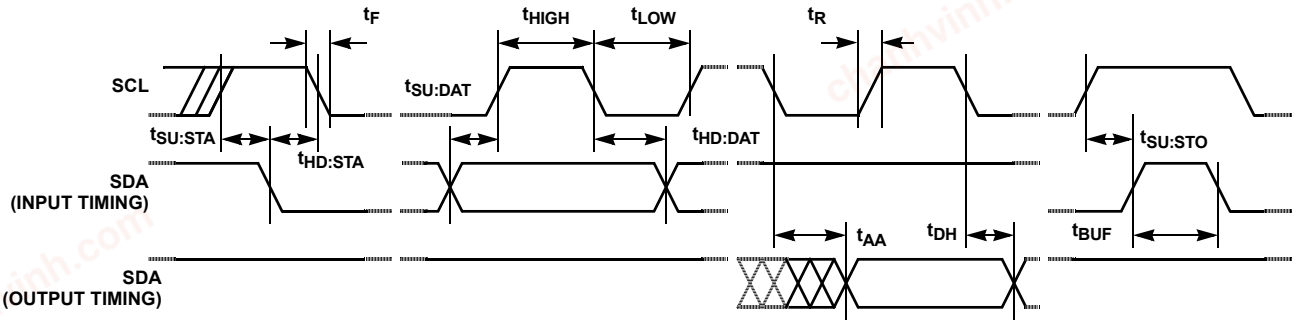
SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP (Note 7)	MAX (Note 8)	UNITS	NOTES
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.			**900**	ns	10
t_{BUF}	Time the Bus Must Be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition	**1300**			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing	**1300**			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing	**600**			ns	
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}	**600**			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}	**600**			ns	
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}	**100**			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window	**0**		**900**	ns	
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}	**600**			ns	
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}	**600**			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window	**0**			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}	**20 + 0.1 x Cb**		**300**	ns	9
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}	**20 + 0.1 x Cb**		**300**	ns	9, 10
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	**10**		**400**	pF	9
Rpu	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ to~2.5kΩ. For Cb = 40pF, max is about 15kΩ to ~20kΩ	**1**			kΩ	9

NOTES:

6. $\overline{IRQ1}/F_{OUT}$ inactive.
7. Typical values are for T = +25°C and 3.3V supply voltage.
8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
9. These are I^2C specific parameters and are not production tested; however, they are used to set conditions for testing devices to validate specification.
10. Parts will work with SDA pull-up voltage above the V_{PULLUP} limit but the t_{AA} and t_F in the I^2C parameters are not guaranteed.
11. Specified at +25°C.

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SDA vs SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 5V

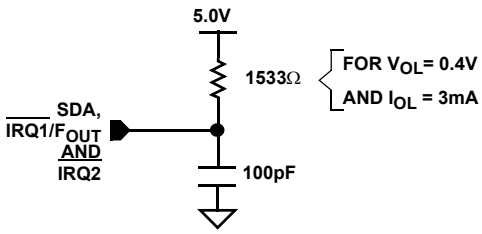


FIGURE 1. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 5.0V

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Typical Performance Curves

Temperature is +25°C unless otherwise specified

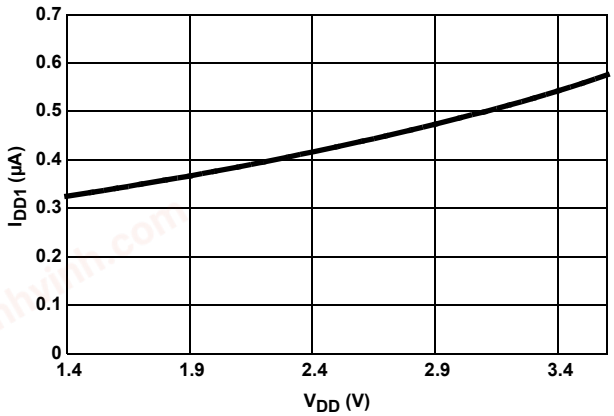


FIGURE 2. I_{DD1} vs V_{DD}

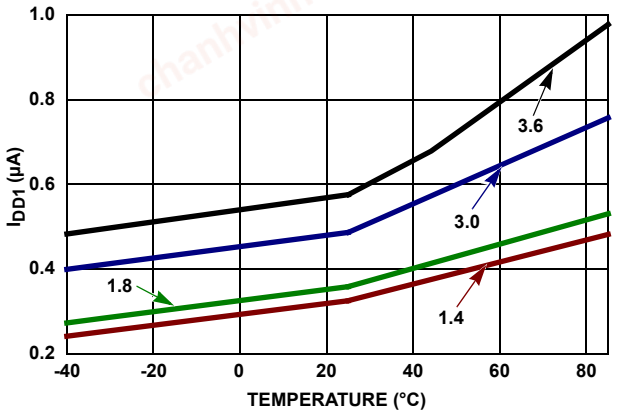


FIGURE 3. I_{DD1} vs TEMPERATURE

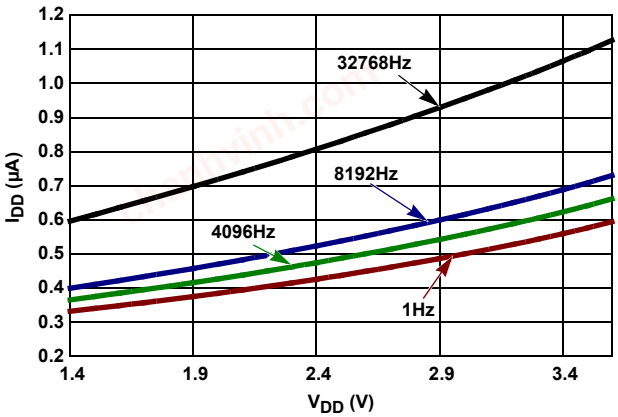


FIGURE 4. I_{DD} vs V_{DD} vs F_{OUT}

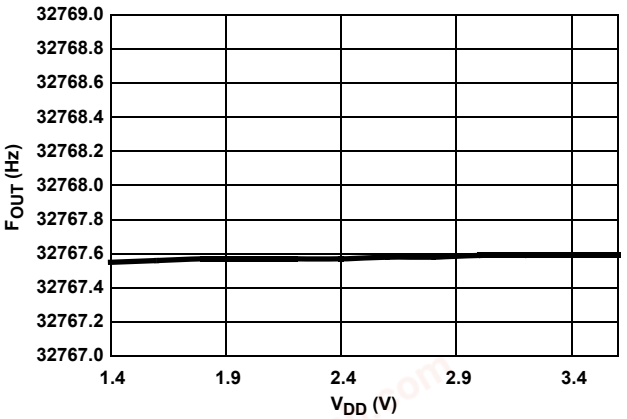


FIGURE 5. F_{OUT} VS V_{DD} WITH A TYPICAL 32.768kHZ CRYSTAL

General Description

The ISL12057 device is a low-power, real-time clock with clock/calendar, power-fail indicator, and alarm function.

The oscillator uses an external, low-cost 32.768kHz crystal with 6pF load capacitance. The real-time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year, and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

The ISL12057 has two flexible alarms, and each can be set to any clock/calendar value for a match; for example, every minute, every Tuesday, or at 5:23 a.m. on the first day of every month. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the $\overline{IRQ1}/F_{OUT}$ or $\overline{IRQ2}$ pin. There is a repeat mode for the alarm, which allows a periodic interrupt every second or every minute.

Pin Description

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal with 6pF load capacitance is used with the ISL12057 to supply a timebase for the real-time clock. See Figure 6.

The device can also be driven directly from a 32.768kHz square wave source with peak-to-peak voltage from 0V to VDD at X1 pin with X2 pin floating.

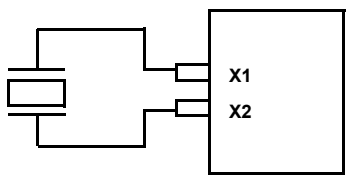


FIGURE 6. RECOMMENDED CRYSTAL CONNECTION

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$\overline{IRQ1}/F_{OUT}$ (Interrupt Output 1/Frequency Output)

This dual-function pin can be used as an alarm interrupt or a frequency output pin. The $\overline{IRQ1}/F_{OUT}$ mode is selected via the control register (address 0Eh). The $\overline{IRQ1}/F_{OUT}$ is an open drain output.

This pin has a default output of 32.768kHz at power-up.

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action.
- **Frequency Output Mode.** The pin outputs a clock signal that is related to the crystal frequency. The frequency output is user selectable and is enabled via the I^2C bus.

$\overline{IRQ2}$ (Interrupt Output 2)

The $\overline{IRQ2}$ pin is used as an Alarm1 interrupt and/or an Alarm2 interrupt. The $\overline{IRQ2}$ mode is selected via the control register (address 0Eh). The $\overline{IRQ2}$ is an open drain output.

This pin is high impedance at power-up.

The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action.

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). The SCL pin can accept a logic high voltage up to 5.5V.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor, and it can accept a pull-up voltage up to 5.5V. The output circuitry controls the fall time of the output signal with the use of a slope-controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds.

NOTE: Parts will work with SDA pull-up voltage above the V_{PULLUP} limit, but the t_{AA} and t_F in the I^2C parameters are not guaranteed.

V_{DD}, GND

These are chip power supply and ground pins. The device will have full operation with a power supply from 1.8V to 3.6VDC, and a timekeeping function with a power supply from 1.4V to 1.8V.

A 0.1µF decoupling capacitor is recommended on the V_{DD} pin to ground.

Functional Description

Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The RTC corrects for months having fewer than 31 days and has a bit that controls 24-hour or AM/PM format. The clock begins incrementing after power-up with valid oscillator condition.

ACCURACY OF THE REAL TIME CLOCK

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, RTC performance also depends upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal's nominal frequency. For example, a ~20ppm frequency deviation translates into an accuracy of ~1 minute per month. These parameters are available from the crystal manufacturer.

I^2C Serial Interface

The ISL12057 has an I^2C serial bus interface that provides access to the real-time clock registers, the control and status registers, and the alarm registers. The I^2C serial interface is compatible with other industry I^2C serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

Register Descriptions

The registers are accessible following a slave byte of "1101000x" and they read or write to addresses [00h:0Fh]. The defined addresses and default values are described in Table 1.

REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address. The address will wrap around from 0Fh to 00h.

The registers are divided into three sections:

1. Real Time Clock (7 bytes): Address 00h to 06h
2. Alarm (7 bytes): Address 07h to 0Dh
3. Control and Status (2 bytes): Address 0Eh to 0Fh

There are no addresses above 0Fh.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read or write instruction, the address remains at the previous address plus one, so the user can execute a current address read and continue reading the next register.

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TABLE 1. REGISTER MEMORY MAP

ADDR	SECTION	REG NAME	BIT								REG	
			7	6	5	4	3	2	1	0	RANGE	DEFAULT
00H	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0-59	00h
01H		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0-59	00h
02H		HR	0	$\overline{MIL}$	$\overline{AM}$/PM	HR20	HR13	HR12	HR11	HR10	1-12 +AM/PM	00h
					HR21						0-23	
03H		DW	0	0	0	0	0	DW12	DW11	DW10	1-7	01h
04H		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1-31	01h
05H		MO	CENTURY	0	0	MO20	MO13	MO12	MO11	MO10	0-12 +Century	01h
06h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0-99	00h
07h	Alarm1	A1SC	A1M1	A1SC22	A1SC21	A1SC20	A1SC13	A1SC12	A1SC11	A1SC10	0-59	00h
08h		A1MN	A1M2	A1MN22	A1MN21	A1MN20	A1MN13	A1MN12	A1MN11	A1MN10	0-59	00h
09h		A1HR	A1M3	A1$\overline{MIL}$	A1$\overline{AM}$/PM	A1HR20	A1HR13	A1HR12	A1HR11	A1HR10	1-12 +AM/PM	00h
					A1HR21						0-23	
0Ah		A1DW/$\overline{DT}$	A1M4	A1DW/$\overline{DT}$	0	0	0	A1DW12	A1DW11	A1DW10	1-7	00h
					A1DT21	A1DT20	A1DT13	A1DT12	A1DT11	A1DT10	1-31	00h
0Bh	Alarm2	A2MN	A2M2	A2MN22	A2MN21	A2MN20	A2MN13	A2MN12	A2MN11	A2MN10	0-59	00h
0Ch		A2HR	A2M3	A2$\overline{MIL}$	A2$\overline{AM}$/PM	A2HR20	A2HR13	A2HR12	A2HR11	A2HR10	1-12 +AM/PM	00h
					A2HR21						0-23	
0Dh		A2DW/$\overline{DT}$	A2M4	A2DW/$\overline{DT}$	0	0	0	A2DW12	A2DW11	A2DW10	1-7	00h
					A2DT21	A2DT20	A2DT13	A2DT12	A2DT11	A2DT10	1-31	00h
0Eh	Control	INT	$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE	N/A	18h
0Fh	Status	SR	OSF	0	0	0	0	0	A2F	A1F	N/A	80h

Real-Time Clock Registers

Addresses [00h to 06h]

RTC REGISTERS (SC, MN, HR, DW, DT, MO, YR)

These registers depict BCD representations of the time. As such, SC (Seconds, address 00h) and MN (Minutes, address 01h) range from 0 to 59, HR (Hour, address 02h) can either be a 12-hour or 24-hour mode, DW (Day of the Week, address 03h) is 1 to 7, DT (Date, address 04h) is 1 to 31, MO (Month, address 05h) is 1 to 12, and YR (Year, address 06h) is 0 to 99.

The DW register provides a Day of the Week status and uses three bits (DW2 to DW0) to represent the seven days of the week. The counter advances in the cycle, 1-2-3-4-5-6-7-1-2-…

The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer.

24-HOUR TIME

If the $\overline{MIL}$ bit of the HR register is “0”, the RTC uses a 24-hour format, and bit 5 of the HR register is the second 10-hour bit (20–23 hours). If the MIL bit is “1”, the RTC uses a 12-hour format and bit 5 of the HR register is the $\overline{AM}$/PM bit, with logic high being PM. The clock defaults to 24-hour format time.

CENTURY INDICATOR

The century bit (bit 7 of the MO register) is toggled when the years register overflows from 99 to 00 to indicate the change of century.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, and the year 2100 is not. The ISL12057 does not correct for the leap year in the year 2100.

Addresses [0Eh to 0Fh]

The Control and Status Registers consist of the Status Register, Interrupt, and Alarm Register.

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Interrupt Control Register (INT) [Address 0Eh]

TABLE 2. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
0Eh	$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE
Default	0	0	0	1	1	0	0	0

OSCILLATOR ENABLE BIT ($\overline{EOSC}$)

The $\overline{EOSC}$ bit enables the crystal oscillator function when it is set to “0”. When the $\overline{EOSC}$ bit is set to “1”, the crystal oscillator function is disabled, and the device enters power-saving mode. The $\overline{EOSC}$ bit is set to “0” at power-up.

FREQUENCY OUT CONTROL BITS (RS2, RS1)

These bits select the output frequency at the $\overline{IRQ1}/F_{OUT}$ pin. INTCN must be set to “0” for frequency output at the $\overline{IRQ1}/F_{OUT}$ pin. See Table 3 for Frequency Selection of the F_{OUT} pin.

TABLE 3. FREQUENCY SELECTION OF F_{OUT} PIN

FREQUENCY F_{OUT} (Hz)	RS2	RS1	COMMENT
32768	1	1	Free-running crystal clock
8192	1	0	Free-running crystal clock
4096	0	1	Free-running crystal clock
1	0	0	Sync at RTC write

INTERRUPT CONTROL BIT (INTCN) AND ALARM INTERRUPT ENABLE BITS (A2IE, A1IE)

The INTCN bit controls the relationship between the alarm interrupts and the $\overline{IRQ1}/F_{OUT}$ and $\overline{IRQ2}$ pins. The A2IE and A1IE bits enable the alarm interrupts, A2F and A1F, to assert the $\overline{IRQ1}/F_{OUT}$ and $\overline{IRQ2}$ pins. See Table 4 for Alarm Interrupt Selection with INTCN, A2IE and A1IE bits.

TABLE 4. ALARM INTERRUPT SELECTION WITH INTCN, A2IE AND A1IE BITS

INTCN	A2IE	A1IE	$\overline{IRQ1}/F_{OUT}$	$\overline{IRQ2}$
0	0	0	F_{OUT}	HIGH
0	0	1	F_{OUT}	A1F
0	1	0	F_{OUT}	A2F
0	1	1	F_{OUT}	A1F or A2F
1	0	0	HIGH	HIGH
1	0	1	HIGH	A1F
1	1	0	A2F	HIGH
1	1	1	A2F	A1F

Status Register (SR) [Address 0Fh]

The Status Register is located in the memory map at address 0Fh. This is a volatile register that provides status of oscillator failure and alarm interrupts.

TABLE 5. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
0Fh	OSF	0	0	0	0	0	A2F	A1F
Default	1	0	0	0	0	0	0	0

ALARM1 INTERRUPT BIT (A1F)

These bits announce if the Alarm1 matches the real-time clock. If there is a match, the respective bit is set to “1”. This bit is manually reset to “0” by the user. A write to this bit in the SR can only set it to “0”, not to “1”.

ALARM2 INTERRUPT BIT (A2F)

These bits announce if the Alarm2 matches the real-time clock. If there is a match, the respective bit is set to “1”. This bit is manually reset to “0” by the user. A write to this bit in the SR can only set it to “0”, not to “1”.

OSCILLATOR FAILURE BIT (OSF)

This bit is set to a “1” when there is no oscillation on the X1 pin. The bit is set by hardware (ISL12057 internally) and can only be disabled by having an oscillation on X1 and manually resetting to “0” to reset it.

Alarm1 Registers

Addresses [Address 07h to 0Ah]

The Alarm1 register bytes are set up identically to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “0”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. When all the enable bits are set to “1”, Alarm1 triggers once per second. Note that there is no alarm byte for month and year.

The Alarm1 function works as a comparison between the Alarm1 registers and the RTC registers. As the RTC advances, Alarm1 is triggered when a match occurs between the Alarm1 registers and the RTC registers. Any one Alarm1 register, multiple registers, or all registers can be enabled for a match.

To clear Alarm1, the A1F status bit must be set to “0” with a write.

TABLE 6. ALARM1 INTERRUPT WITH ENABLE BITS SELECTION

$A1DW/\overline{DT}$	A1M1	A1M2	A1M3	A1M4	ALARM1 INTERRUPT
X	1	1	1	1	Every Second
X	0	1	1	1	Match Second
X	1	0	1	1	Match Minute

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TABLE 6. ALARM1 INTERRUPT WITH ENABLE BITS SELECTION (Continued)

A1DW/$\overline{DT}$	A1M1	A1M2	A1M3	A1M4	ALARM1 INTERRUPT
X (see Note)	1	1	0	1	Match Hour
0	1	1	1	0	Match Date
1	1	1	1	0	Match Day
0	0	0	1	1	Match Second and Minute
0	0	1	0	1	Match Second and Hour
0	0	0	0	0	Match Second, Minute and Hour
. .	. .	. .	. .	. .	. .
0	1	0	0	0	Match Minute Hour and Date
0	0	0	0	0	Match Second, Minute Hour and Date
. .	. .	. .	. .	. .	. .
1	1	0	0	0	Match Minute, Hour, and Day
1	0	0	0	0	Match Second, Minute, Hour, and Day

NOTE: “X” is “Don’t care”; it can be set to 0 or 1.

Following is example of an Alarm1 Interrupt: a single alarm will occur on Monday at 11:30 a.m. (Monday is when DW = 2). Set the Alarm1 registers as follows:

ALARM1 REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
A1SC	1	0	0	0	0	0	0	0	80h	Seconds disabled
A1MN	0	0	1	1	0	0	0	0	30h	Minutes set to 30, enabled
A1HR	0	1	0	1	0	0	0	1	51h	Hours set to 11am, enabled
A1DW/$\overline{DT}$	0	1	0	0	0	0	1	0	42h	Day set to 1, enabled

After these registers are set, an alarm is generated when the RTC advances to exactly 11:30 a.m. on January 1 (after seconds changes from 59 to 00) by setting the A1F bit in the status register to “1”.

Alarm2 Registers

Addresses [Address 12h to 14h]

The Alarm2 register bytes are set up identically to the RTC register bytes except that the MSB of each byte functions as an enable bit (enable = “0”). These enable bits specify which alarm registers (minutes, hour, and date/day) are used to make the comparison. When all the enable bits are set to “1”, Alarm2 will trigger once per minute. Note that there are no alarm bytes for seconds, month, and year.

The Alarm2 function works as a comparison between the Alarm2 registers and the RTC registers. As the RTC advances, Alarm2 is triggered when a match occurs between the Alarm2 registers and the RTC registers. Any one Alarm2 register, multiple registers, or all registers can be enabled for a match.

To clear Alarm2, the A2F status bit must be set to “0” with a write.

TABLE 7. ALARM2 INTERRUPT WITH ENABLE BITS SELECTION

A2DW/$\overline{DT}$	A2M2	A2M3	A2M4	ALARM2 INTERRUPT
X (see Note)	1	1	1	Every Minute (Second=00)
X	0	1	1	Match Minute
X	1	0	1	Match Hour
0	1	1	0	Match Date
1	1	1	0	Match Day
X	0	0	1	Match Minute and Hour
0	1	0	0	Match Hour and Date
0	0	1	0	Match Minute and Date
0	0	0	0	Match Minute, Hour, and Date
1	0	1	0	Match Minute and Day
1	1	0	0	Match Hour and Day
1	0	0	0	Match Minute, Hour, and Day

NOTE: “X” is “Don’t care”; it can be set to 0 or 1.

Following is example of Alarm2 Interrupt: a single alarm will occur on the first day of every month at 20:00 military time. Set the Alarm2 registers as follows:

ALARM2 REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
A2MN	1	0	0	0	0	0	0	0	80h	Minutes disabled
A2HR	0	0	1	0	0	0	0	0	20h	Hours set to 20, enabled
A2DW/$\overline{DT}$	0	0	0	0	0	0	0	1	01h	Date set to 1st, enabled

After these registers are set, an alarm is generated when the RTC advances to exactly 20:00 on Monday (after minutes changes from 59 to 00) by setting the A2F bit in the status register to “1”.

I^2C Serial Interface

The ISL12057 supports a bi-directional, bus-oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The

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device controlling the transfer is the master, and the device being controlled is the slave. The master device always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12057 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 7). On power-up of the ISL12057, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12057 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 7). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 7). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting 8 bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge reception of the 8 bits of data (see Figure 8).

The ISL12057 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL12057 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

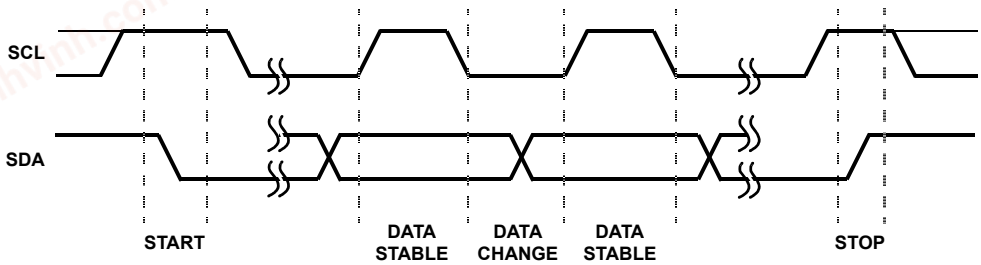


FIGURE 7. VALID DATA CHANGES, START, AND STOP CONDITIONS

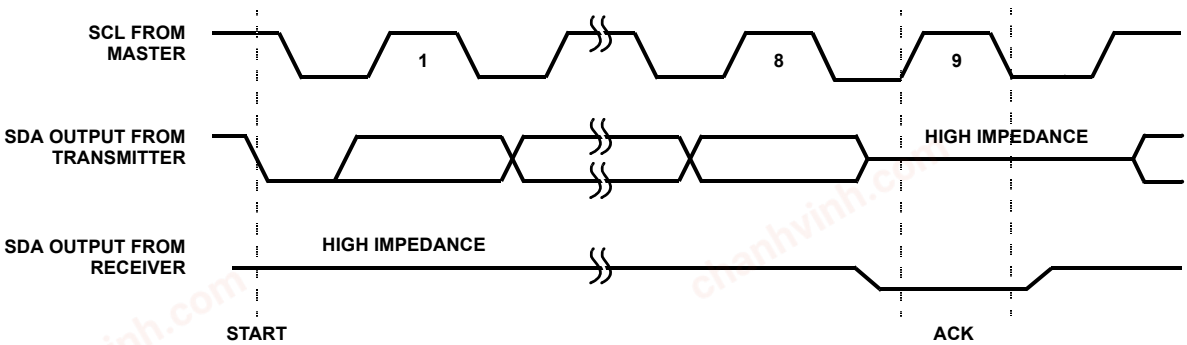


FIGURE 8. ACKNOWLEDGE RESPONSE FROM RECEIVER

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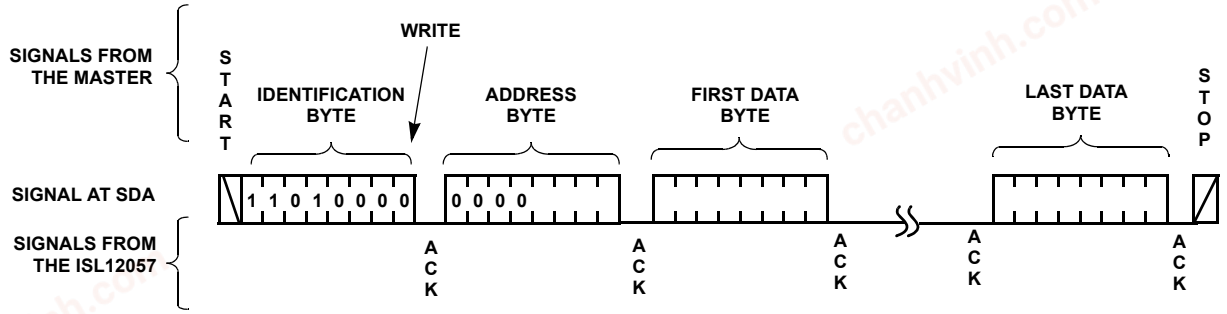


FIGURE 9. SEQUENTIAL BYTE WRITE SEQUENCE

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The seven MSBs are the device identifier. These bits are “1101000”. Slave bits “1101” access the register. Slave bits “000” specify the device select bits.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a “1”, then a read operation is selected. A “0” selects a write operation (see Figure 10).

After loading the entire Slave Address Byte from the SDA bus, the ISL12057 compares the device identifier and device select bits with “1101000”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one-byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 0h, so a current address read of the RTC array starts at address 0h. When required, as part of a random read, the master must supply the 1 Word Address Bytes as shown in Figure 11.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Clock/Control Registers, the slave byte must be “1101000x” in both places.

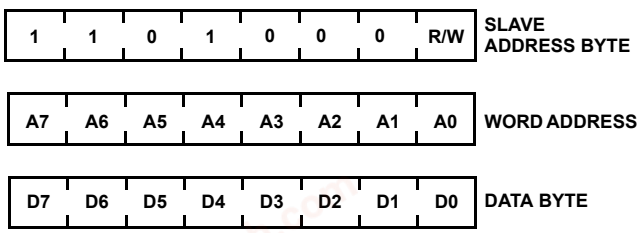


FIGURE 10. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12057 responds with an ACK. At this point, the I^2C interface enters a standby state.

Read Operation

A Read operation consists of a 3- byte instruction followed by one or more Data Bytes (see Figure 11). The master device initiates the operation by issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL12057 responds with an ACK. Then, the ISL12057 transmits Data Bytes, as long as the master device responds with an ACK during the SCL cycle following the eighth bit of each byte. The master device terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 11).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer’s initial value is determined by the Address Byte in the Read operation instruction. It increments by one during transmission of each Data Byte. After reaching the memory location 13h, the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

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Application Section

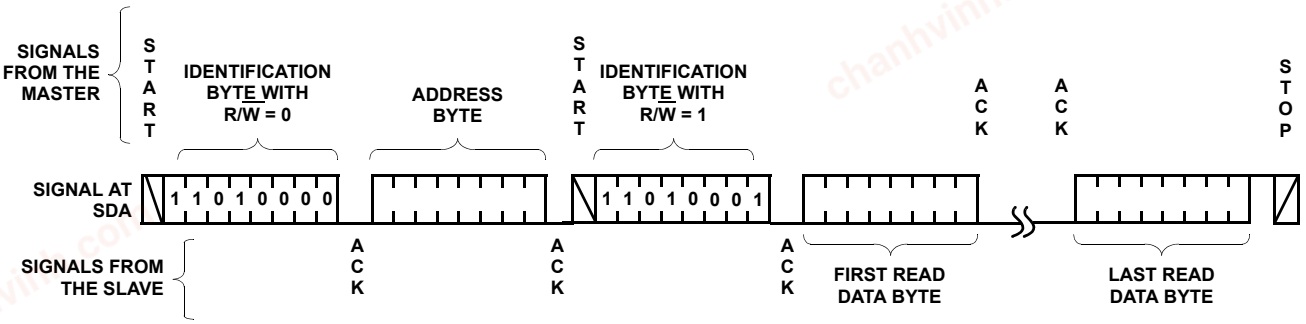


FIGURE 11. READ SEQUENCE

Oscillator Crystal Requirements

The ISL12057 uses a standard 32.768kHz crystal. Either through-hole or surface-mount crystals can be used. Table 8 lists some recommended surface-mount crystals and the parameters of each. This list is not exhaustive, and other surface-mount devices can be used with the ISL12057 if their specifications are very similar to the devices listed. The crystal required parallel load capacitance is 6pF, and equivalent series resistance needs to be less than 50k. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through-hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

TABLE 8. SUGGESTED SURFACE MOUNT CRYSTALS

MANUFACTURER	PART NUMBER
Citizen	CM200S
MicroCrystal	MS3V
ECS	ECX-306

Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies (such as 32.768kHz) are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high-speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and ensure accurate clocking.

Figure 12 shows a suggested layout for the ISL12057 device using a surface-mount crystal. Two main precautions should be followed:

1. Do not run the serial bus lines or any high-speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.
2. Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

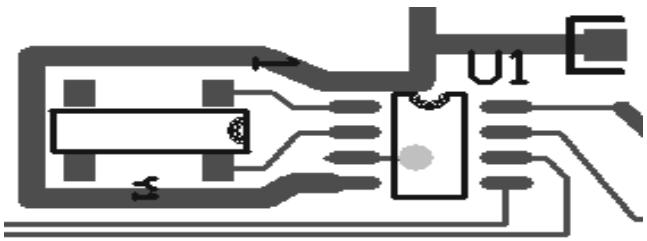


FIGURE 12. SUGGESTED LAYOUT FOR ISL12057 AND CRYSTAL

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the $\overline{IRQ1}/F_{OUT}$ pin is used as a clock, it should be routed away from the RTC device as well. The trace for the V_{CC} pins can be treated as a ground, and it should be routed around the crystal.

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 25, 2015	FN6755.2	Updated Ordering Information Table on page 2. Added Revision History and About Intersil sections. Updated POD M8.118 from rev 3 to rev 4. Changes since rev 4: Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36" Updated POD M8.15 from rev 2 to rev 4. Changes since rev 2: Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Changed Note 1 "1982" to "1994"

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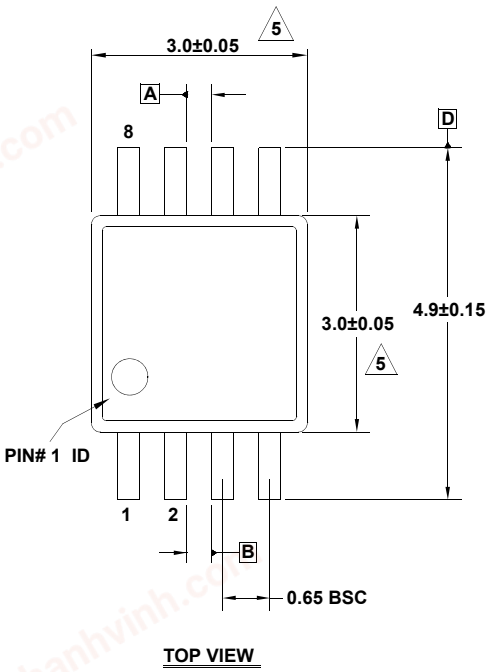
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Package Outline Drawing

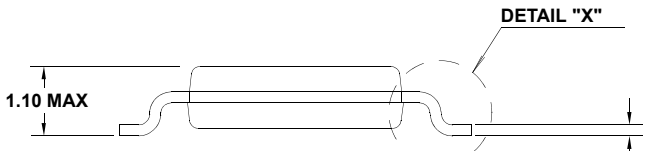
M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

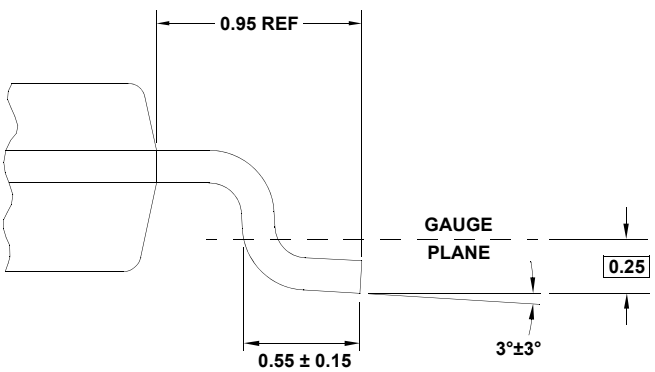
Rev 4, 7/11



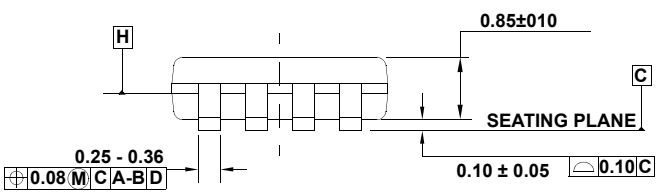
TOP VIEW



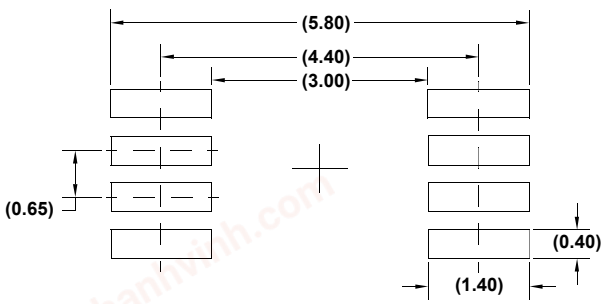
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

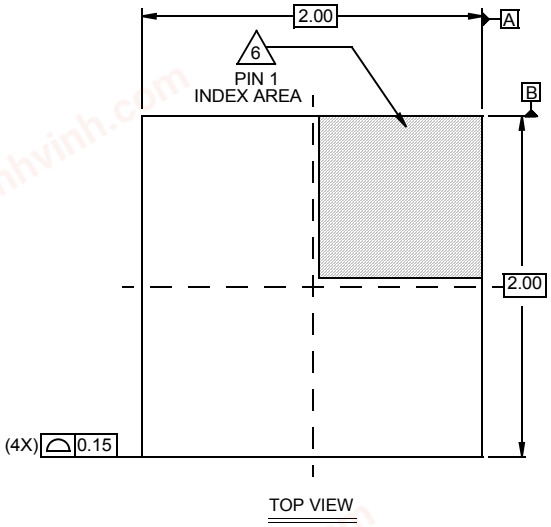
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Package Outline Drawing

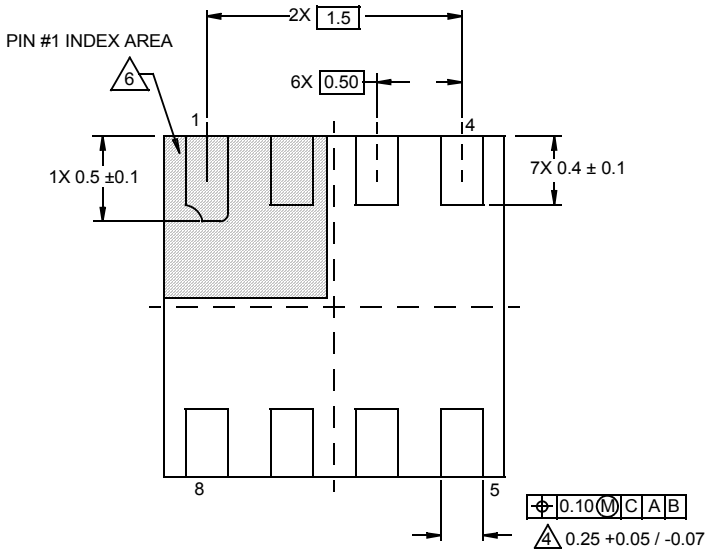
L8.2x2

8 Lead Ultra Thin Dual Flat No-Lead COL Plastic Package (UTDFN COL)

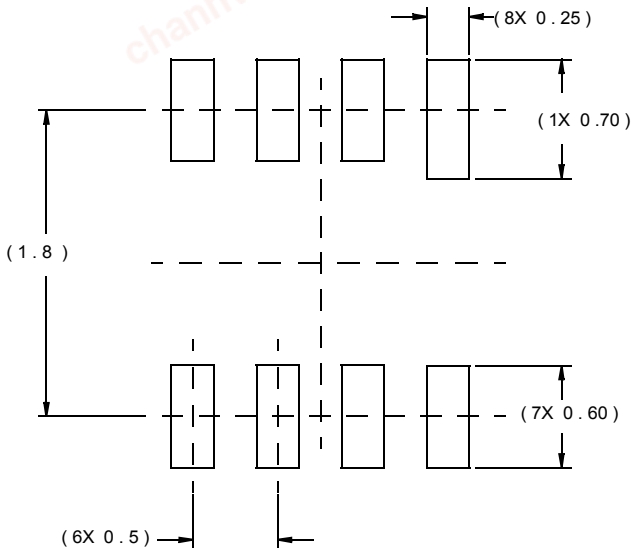
Rev 3, 11/07



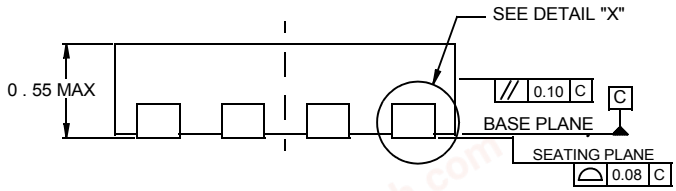
TOP VIEW



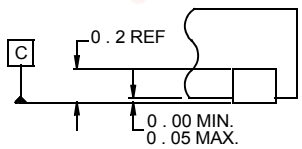
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

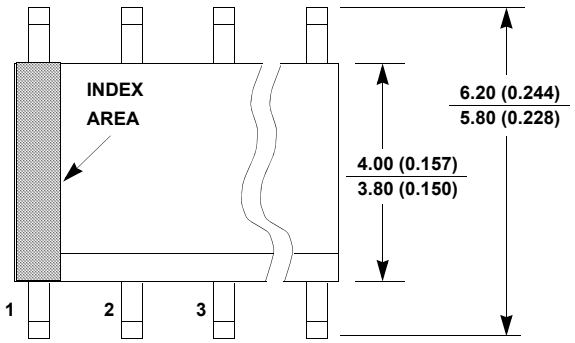
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Package Outline Drawing

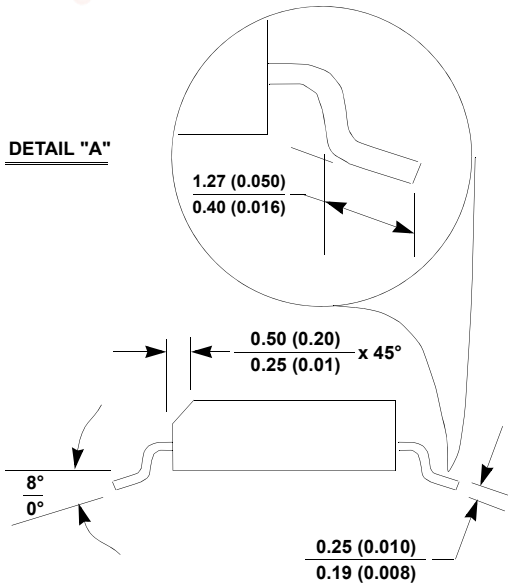
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

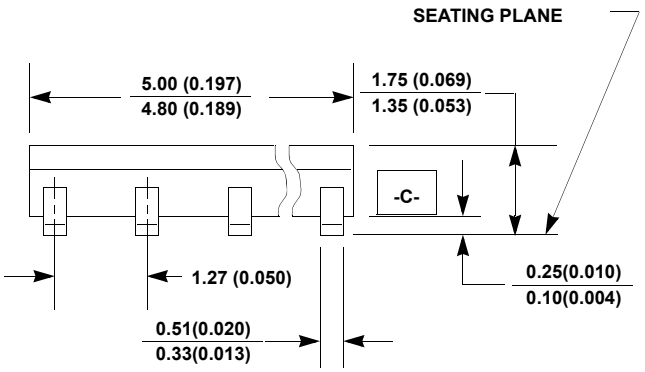
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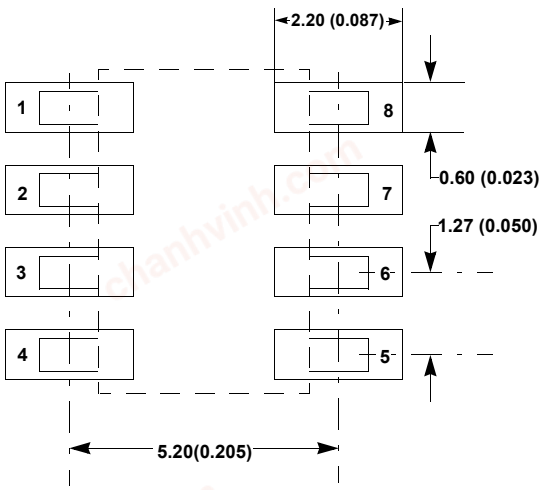
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.