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Datasheet

ICL3221E, ICL3222E, ICL3223E, ICL3232E, ICL3241E, ICL3243E

±15kV ESD Protected, +3V to +5.5V, 1µA, 250kbps, RS-232 Transmitters/Receivers

The ICL3221E, ICL3222E, ICL3223E, ICL3232E, ICL3241E, and ICL3243E are 3.0V to 5.5V powered RS-232 transmitters/receivers that meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Additionally, they provide ±15kV ESD protection (IEC61000-4-2 Air Gap and Human Body Model) on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications are notebook and laptop computers in which the low operational power consumption and even lower standby power consumption is critical. Efficient on-chip charge pumps, coupled with manual and automatic power-down functions (except for the ICL3232E), reduce the standby supply current to a 1µA trickle. Small footprint packaging and the use of small, low value capacitors ensure board space savings. Data rates greater than 250kbps are ensured at worst case load conditions. This family is fully compatible with 3.3V-only systems, mixed 3.3V and 5.0V systems, and 5.0V-only systems.

The ICL324XE are 3-driver, 5-receiver devices that provide a complete serial port suitable for laptop or notebook computers. Both devices also include noninverting always-active receivers for “wake-up” capability.

The ICL3221E, ICL3223E, and ICL3243E feature an automatic power-down function that powers down the on-chip power supply and driver circuits. Power-down occurs when an attached peripheral device is shut off or the RS-232 cable is removed, which conserves system power automatically without changes to the hardware or operating system. These devices power up again when a valid RS-232 voltage is applied to any receiver input.

Table 1 on page 2 summarizes the features of the devices represented by this datasheet, and Application Note AN9863 summarizes the features of each device in the ICL32xxE 3V family.

Related Literature

For a full list of documents, visit our website:

- ICL3221E, ICL3222E, ICL3223E, ICL3232E, ICL3241E, and ICL3243E device pages

Features

- ESD protection for RS-232 I/O pins to ±15kV (IEC61000)
- Drop-in replacements for the MAX3221E, MAX3222E, MAX3223E, MAX3232E, MAX3241E, MAX3243E, and SP3243E
- The ICL3221E is a low-power, pin-compatible upgrade for the 5V MAX221E
- The ICL3222E is a low-power, pin-compatible upgrade for the 5V MAX242E and SP312E
- The ICL3232E is a low-power upgrade for the HIN232E, ICL232, and pin-compatible competitor devices
- RS-232 compatible with V_{CC} = 2.7V
- Meets EIA/TIA-232 and V.28/V.24 specifications at 3V
- Latch-up free
- On-chip voltage converters require only four external 0.1µF capacitors at V_{CC} = 3.3V
- Manual and automatic power-down features
- Ensured mouse driveability (ICL324xE only)
- Receiver hysteresis for improved noise immunity
- Ensured minimum data rate: 250kbps
- Wide power supply range: single +3V to +5.5V
- Low supply current in power-down state: 1µA
- Pb-free (RoHS compliant)

Applications

- Any system requiring RS-232 communication ports
  - Battery powered, hand-held, and portable equipment
  - Laptop computers and notebooks
  - Modems, printers, and other peripherals
  - Digital cameras
  - Cellular/mobile phones

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Table 1. Summary of Features

Part Number	Number of Tx	Number of Rx	Number of Monitor Receivers (R_{outb})	Data Rate (kbps)	Receiver Enable Function?	Ready Output?	Manual Power-Down?	Automatic Power-Down Function?
ICL3221E	1	1	0	250	Yes	No	Yes	Yes
ICL3222E	2	2	0	250	Yes	No	Yes	No
ICL3223E	2	2	0	250	Yes	No	Yes	Yes
ICL3232E	2	2	0	250	No	No	No	No
ICL3241E	3	5	2	250	Yes	No	Yes	No
ICL3243E	3	5	1	250	No	No	Yes	Yes

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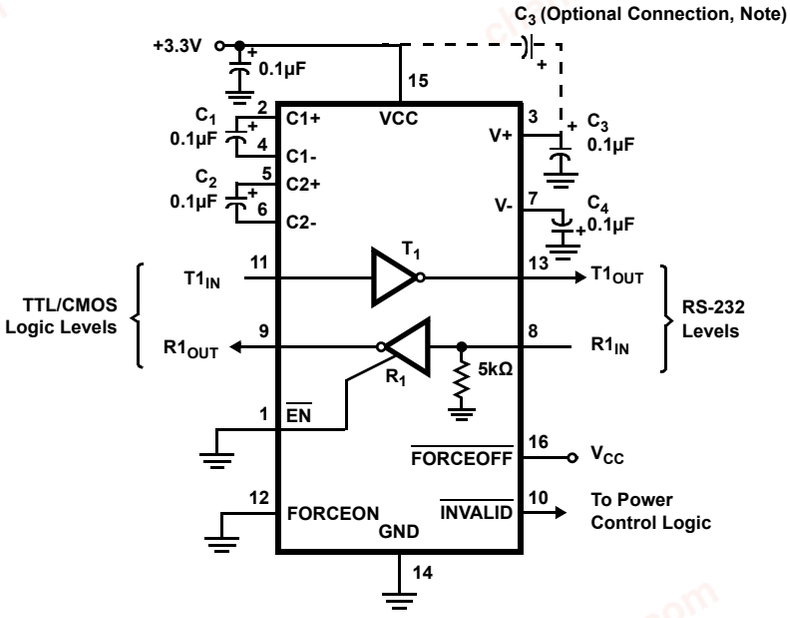
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1. Overview

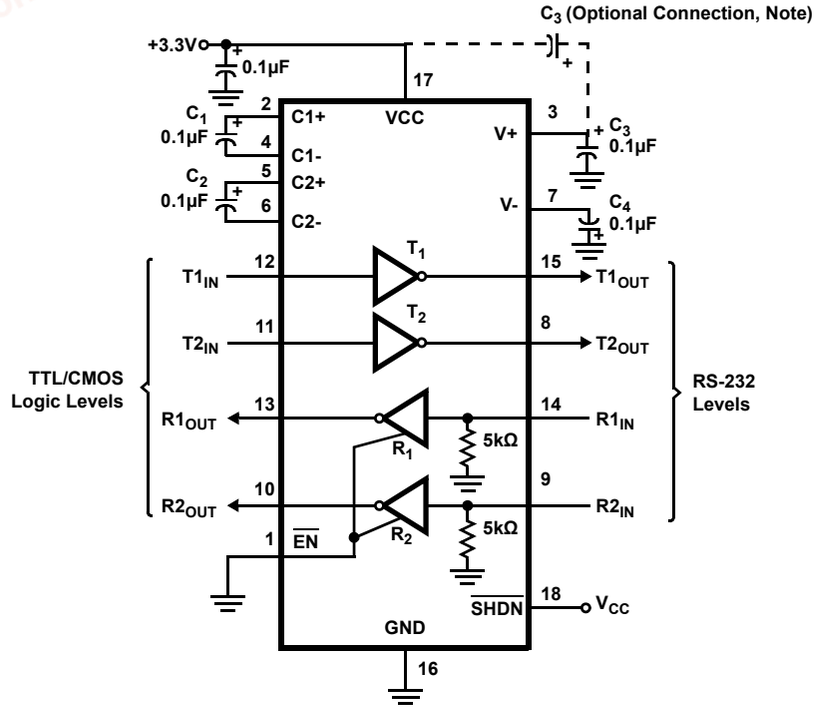
1.1 Typical Operating Circuits

ICL3221E



Note: The negative terminal of C3 can be connected to either VCC or GND

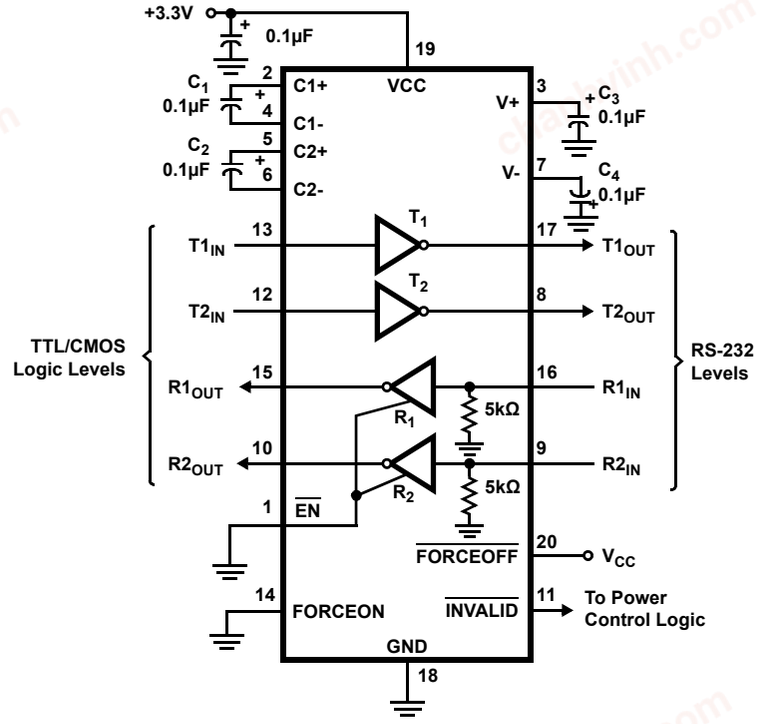
ICL3222E



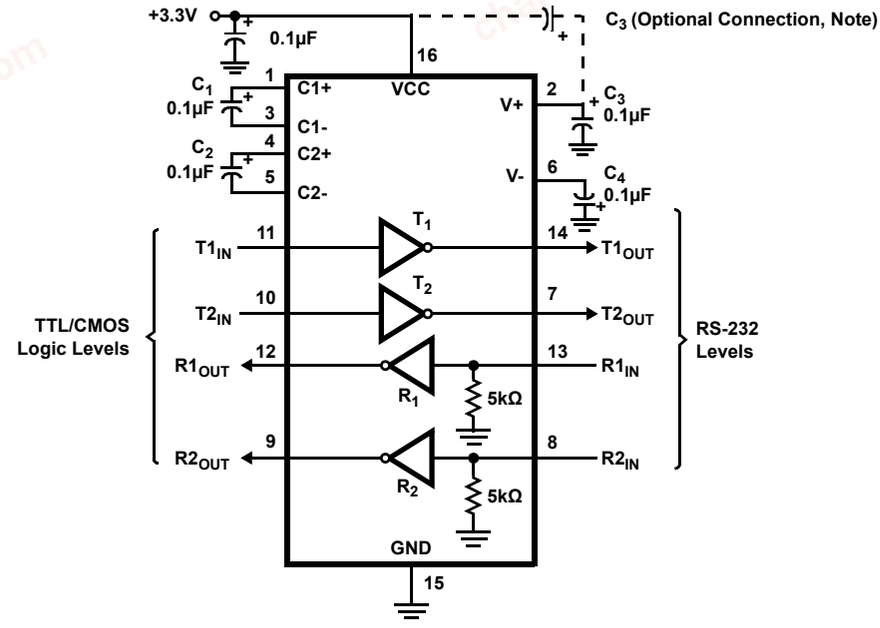
Note: The negative terminal of C3 can be connected to either VCC or GND

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ICL3223E



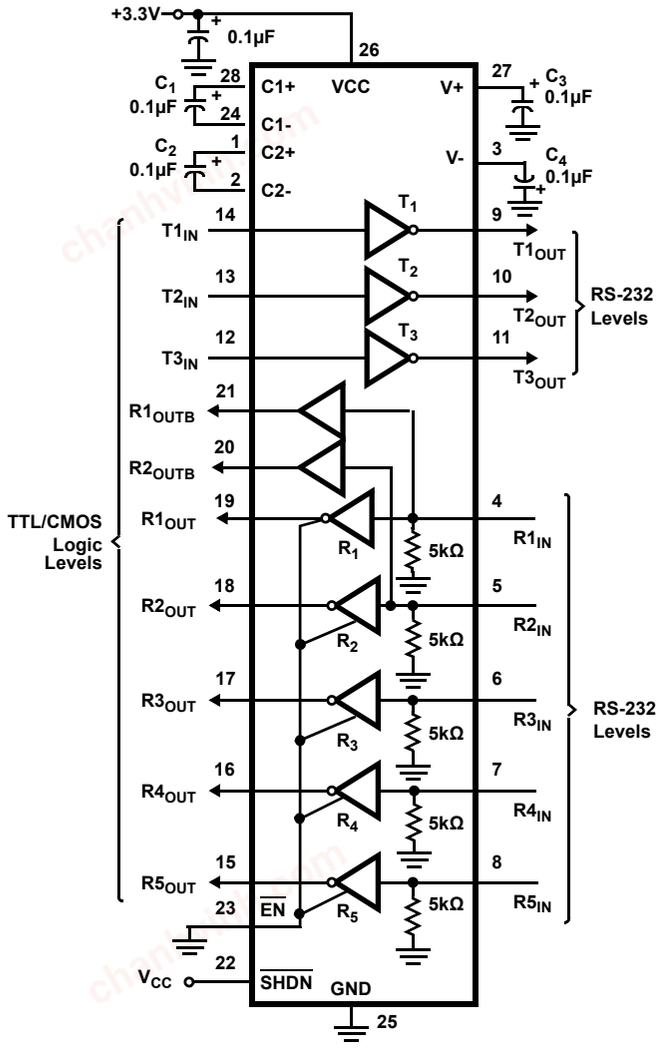
ICL3232E



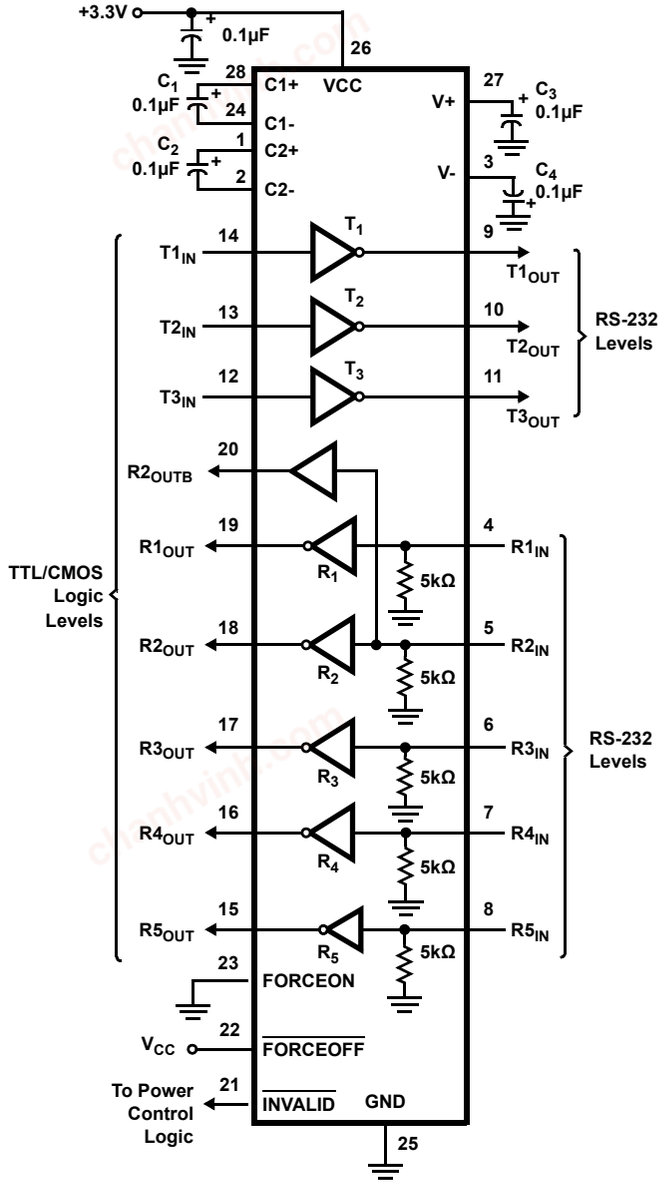
Note: The negative terminal of C3 can be connected to either VCC or GND

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ICL3241E



ICL3243E



1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ICL3221ECAZ	ICL32 21ECAZ	0 to +70	-	16 Ld SSOP	M16.209
ICL3221ECAZ-T	ICL32 21ECAZ	0 to +70	1k	16 Ld SSOP	M16.209
ICL3221ECAZ-T7A	ICL32 21ECAZ	0 to +70	250	16 Ld SSOP	M16.209
ICL3221ECVZ	3221 ECVZ	0 to +70	-	16 Ld TSSOP	M16.173
ICL3221ECVZ-T	3221 ECVZ	0 to +70	2.5k	16 Ld TSSOP	M16.173
ICL3221EIAZ	ICL32 21EIAZ	-40 to +85	-	16 Ld SSOP	M16.209
ICL3221EIAZ-T	ICL32 21EIAZ	-40 to +85	1k	16 Ld SSOP	M16.209
ICL3221EIAZ-T7A	ICL32 21EIAZ	-40 to +85	250	16 Ld SSOP	M16.209
ICL3221EIVZ	3221 EIVZ	-40 to +85	-	16 Ld TSSOP	M16.173
ICL3221EIVZ-T	3221 EIVZ	-40 to +85	2.5k	16 Ld TSSOP	M16.173
ICL3221EIVZ-T7A	3221 EIVZ	-40 to +85	250	16 Ld TSSOP	M16.173
ICL3222ECAZ	ICL32 22ECAZ	0 to +70	-	20 Ld SSOP	M20.209

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Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ICL3222ECAZ-T	ICL32 22ECAZ	0 to +70	1k	20 Ld SSOP	M20.209
ICL3222ECVZ	ICL32 22ECVZ	0 to +70	-	20 Ld TSSOP	M20.173
ICL3222ECVZ-T	ICL32 22ECVZ	0 to +70	2.5k	20 Ld TSSOP	M20.173
ICL3222EIAZ	ICL32 22EIAZ	-40 to +85	-	20 Ld SSOP	M20.209
ICL3222EIAZ-T	ICL32 22EIAZ	-40 to +85	1k	20 Ld SSOP	M20.209
ICL3222EIBZ	3222EIBZ	-40 to +85	-	18 Ld SOIC	M18.3
ICL3222EIBZ-T	3222EIBZ	-40 to +85	1k	18 Ld SOIC	M18.3
ICL3222EIVZ	ICL32 22EIVZ	-40 to +85	-	20 Ld TSSOP	M20.173
ICL3222EIVZ-T	ICL32 22EIVZ	-40 to +85	2.5k	20 Ld TSSOP	M20.173
ICL3223ECAZ	ICL32 23ECAZ	0 to +70	-	20 Ld SSOP	M20.209
ICL3223ECAZ-T	ICL32 23ECAZ	0 to +70	1k	20 Ld SSOP	M20.209
ICL3223ECVZ **(No longer available, recommended replacement: ICL3223EIVZ)**	ICL32 23ECVZ	0 to +70	-	20 Ld TSSOP	M20.173
ICL3223ECVZ-T **(No longer available, recommended replacement: ICL3223EIVZ-T)**	ICL32 23ECVZ	0 to +70	2.5k	20 Ld TSSOP	M20.173
ICL3223EIAZ	ICL32 23EIAZ	-40 to +85	-	20 Ld SSOP	M20.209
ICL3223EIAZ-T	ICL32 23EIAZ	-40 to +85	1k	20 Ld SSOP	M20.209
ICL3223EIVZ	ICL32 23EIVZ	-40 to +85	-	20 Ld TSSOP	M20.173
ICL3223EIVZ-T	ICL32 23EIVZ	-40 to +85	2.5k	20 Ld TSSOP	M20.173
ICL3232ECAZ	3232 ECAZ	0 to +70	-	16 Ld SSOP	M16.209
ICL3232ECAZ-T	3232 ECAZ	0 to +70	1k	16 Ld SSOP	M16.209
ICL3232ECAZ-T7A	3232 ECAZ	0 to +70	250	16 Ld SSOP	M16.209
ICL3232ECBZ	3232ECBZ	0 to +70	-	16 Ld SOIC	M16.3
ICL3232ECBZ-T	3232ECBZ	0 to +70	1k	16 Ld SOIC	M16.3
ICL3232ECBNZ	3232ECBNZ	0 to +70	-	16 Ld SOIC	M16.15
ICL3232ECBNZ-T	3232ECBNZ	0 to +70	2.5k	16 Ld SOIC	M16.15
ICL3232ECBNZ-T7A	3232ECBNZ	0 to +70	250	16 Ld SOIC	M16.15
ICL3232ECV-16Z	3232E CV-16Z	0 to +70	-	16 Ld TSSOP	M16.173
ICL3232ECV-16Z-T	3232E CV-16Z	0 to +70	2.5k	16 Ld TSSOP	M16.173
ICL3232ECV-16Z-T7A	3232E CV-16Z	0 to +70	250	16 Ld TSSOP	M16.173
ICL3232ECV-20Z **(No longer available, recommended replacement: ICL3232EIV-16Z)**	ICL3232 ECV-20Z	0 to +70	-	20 Ld TSSOP	M20.173
ICL3232ECV-20Z-T **(No longer available, recommended replacement: ICL3232EIV-16Z-T)**	ICL3232 ECV-20Z	0 to +70	2.5k	20 Ld TSSOP	M20.173
ICL3232EFV-16Z **(No longer available, recommended replacement: ICL3232EIV-16Z)**	3232E FV-16Z	-40 to +125	-	16 Ld TSSOP	M16.173
ICL3232EFV-16Z-T **(No longer available, recommended replacement: ICL3232EIV-16Z-T)**	3232E FV-16Z	-40 to +125	2.5k	16 Ld TSSOP	M16.173
ICL3232EIAZ	3232 EIAZ	-40 to +85	-	16 Ld SSOP	M16.209
ICL3232EIAZ-T	3232 EIAZ	-40 to +85	1k	16 Ld SSOP	M16.209
ICL3232EIBZ	3232EIBZ	-40 to +85	-	16 Ld SOIC	M16.3

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Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ICL3232EIBZ-T	3232EIBZ	-40 to +85	1k	16 Ld SOIC	M16.3
ICL3232EIBNZ	3232EIBNZ	-40 to +85	-	16 Ld SOIC	M16.15
ICL3232EIBNZ-T	3232EIBNZ	-40 to +85	2.5k	16 Ld SOIC	M16.15
ICL3232EIV-16Z	3232E IV-16Z	-40 to +85	-	16 Ld TSSOP	M16.173
ICL3232EIV-16Z-T	3232E IV-16Z	-40 to +85	2.5k	16 Ld TSSOP	M16.173
ICL3232EIV-16Z-T7A	3232E IV-16Z	-40 to +85	250	16 Ld TSSOP	M16.173
ICL3232EIV-20Z	ICL3232 EIV-20Z	-40 to +85	-	20 Ld TSSOP	M20.173
ICL3232EIV-20Z-T	ICL3232 EIV-20Z	-40 to +85	2.5k	20 Ld TSSOP	M20.173
ICL3241ECAZ	ICL3241 ECAZ	0 to +70	-	28 Ld SSOP	M28.209
ICL3241ECAZ-T	ICL3241 ECAZ	0 to +70	1k	28 Ld SSOP	M28.209
ICL3241ECVZ	ICL3241 ECVZ	0 to +70	-	28 Ld TSSOP	M28.173
ICL3241ECVZ-T	ICL3241 ECVZ	0 to +70	2.5k	28 Ld TSSOP	M28.173
ICL3241EIAZ	ICL3241 EIAZ	-40 to +85	-	28 Ld SSOP	M28.209
ICL3241EIAZ-T	ICL3241 EIAZ	-40 to +85	1k	28 Ld SSOP	M28.209
ICL3241EIVZ	ICL3241 EIVZ	-40 to +85	-	28 Ld TSSOP	M28.173
ICL3241EIVZ-T	ICL3241 EIVZ	-40 to +85	2.5k	28 Ld TSSOP	M28.173
ICL3243ECAZ	ICL32 43ECAZ	0 to +70	-	28 Ld SSOP	M28.209
ICL3243ECAZ-T	ICL32 43ECAZ	0 to +70	1k	28 Ld SSOP	M28.209
ICL3243ECBZ	ICL3243ECBZ	0 to +70	-	28 Ld SOIC	M28.3
ICL3243ECBZ-T	ICL3243ECBZ	0 to +70	1k	28 Ld SOIC	M28.3
ICL3243ECVZ	ICL3243 ECVZ	0 to +70	-	28 Ld TSSOP	M28.173
ICL3243ECVZ-T	ICL3243 ECVZ	0 to +70	2.5k	28 Ld TSSOP	M28.173
ICL3243EIAZ	ICL32 43EIAZ	-40 to +85	-	28 Ld SSOP	M28.209
ICL3243EIAZ-T	ICL32 43EIAZ	-40 to +85	1k	28 Ld SSOP	M28.209
ICL3243EIVZ	ICL3243 EIVZ	-40 to +85	-	28 Ld TSSOP	M28.173
ICL3243EIVZ-T	ICL3243 EIVZ	-40 to +85	2.5k	28 Ld TSSOP	M28.173
ICL3243EIVZ-T7A	ICL3243 EIVZ	-40 to +85	250	28 Ld TSSOP	M28.173

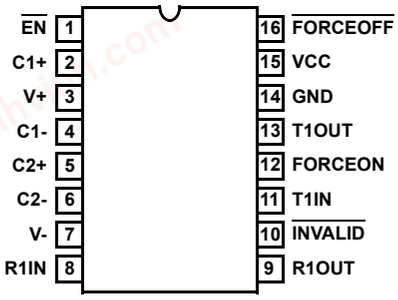
Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ICL3221E, ICL3222E, ICL3223E, ICL3232E, ICL3241E, ICL3243E device pages. For more information about MSL, see TB363.

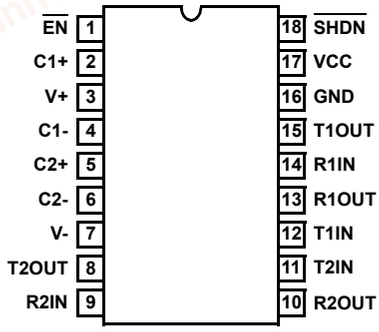
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1.3 Pin Configurations

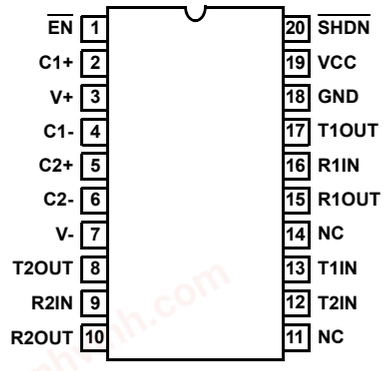
ICL3221E
(16 LD SSOP, TSSOP)
Top View



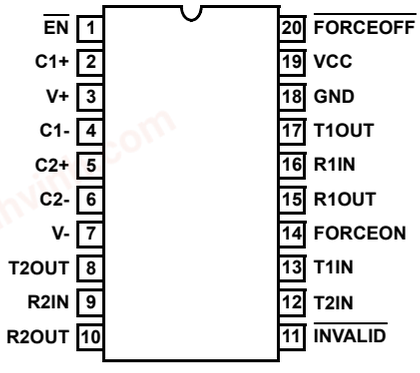
ICL3222E
(18 LD SOIC)
Top View



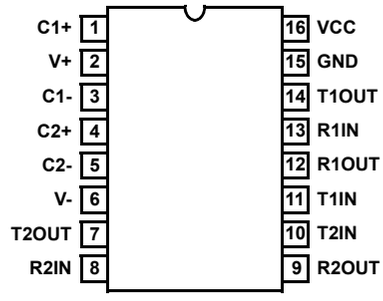
ICL3222E
(20 LD SSOP, TSSOP)
Top View



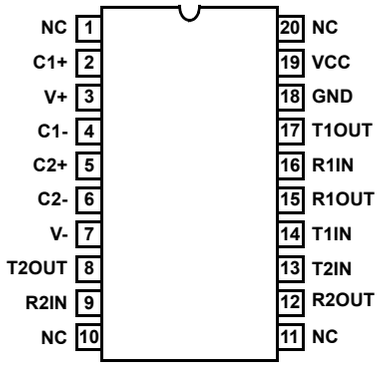
ICL3223E
(20 LD SSOP, TSSOP)
Top View



ICL3232E
(16 LD SOIC, SSOP, TSSOP-16)
Top View

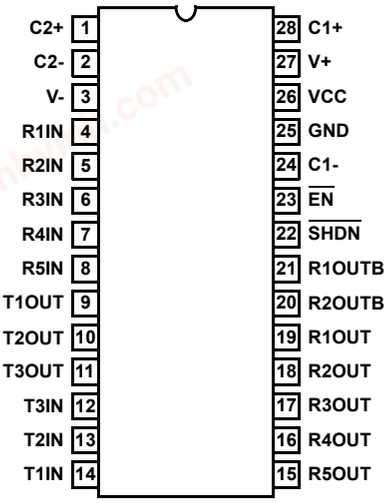


ICL3232E
(20 LD TSSOP-20)
Top View

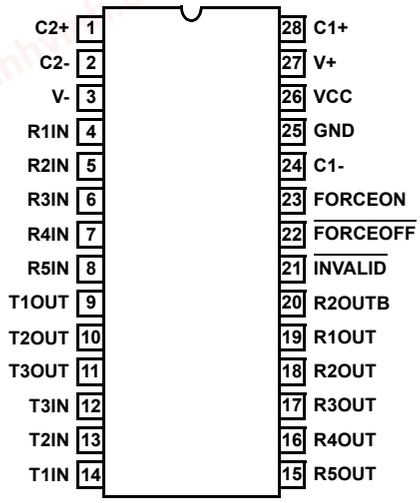


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ICL3241E
(28 ld SOIC, SSOP, TSSOP)
Top View



ICL3243E
(28 ld SOIC, SSOP, TSSOP)
Top VIew



1.4 Pin Descriptions

Pin	Function
VCC	System power supply input (3.0V to 5.5V)
V+	Internally generated positive transmitter supply (+5.5V)
V-	Internally generated negative transmitter supply (-5.5V)
GND	Ground connection
C1+	External capacitor (voltage doubler) is connected to this lead
C1-	External capacitor (voltage doubler) is connected to this lead
C2+	External capacitor (voltage inverter) is connected to this lead
C2-	External capacitor (voltage inverter) is connected to this lead
TIN	TTL/CMOS compatible transmitter inputs
TOUT	±15kV ESD protected, RS-232 level (nominally ±5.5V) transmitter outputs
RIN	±15kV ESD protected, RS-232 compatible receiver inputs
ROUT	TTL/CMOS level receiver outputs
ROUTB	TTL/CMOS level, noninverting, always enabled receiver outputs
INVALID	Active low output that indicates no valid RS-232 levels are present on any receiver input
EN	Active low receiver enable control; does not disable R_{OUTB} outputs
SHDN	Active low input to shut down transmitters and on-board power supply to place device in low-power mode
FORCEOFF	Active low to shut down transmitters and on-chip power supply, which overrides any automatic circuitry and FORCEON (see Table 5 on page 18)
FORCEON	Active high input to override automatic power-down circuitry, which keeps transmitters active ($\overline{\text{FORCEOFF}}$ must be high)

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2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{CC} to GND	-0.3	6	V
V+ to GND	-0.3	7	V
V- to GND	+0.3	-7	V
V+ to V-		14	V
Input Voltages			
T_{IN}, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$, $\overline{SHDN}$	-0.3	6	V
R_{IN}		±28	V
Output Voltages			
T_{OUT}		±13.2	V
R_{OUT}, $\overline{INVALID}$	-0.3	V_{CC} + 0.3	V
Short-Circuit Duration			
T_{OUT}	Continuous		
ESD Rating	See "Electrical Specifications" on page 12		

2.2 Thermal Information

Thermal Resistance (Typical) Note 4	θ_{JA} (°C/W)
16 Ld Wide SOIC Package	100
16 Ld Narrow SOIC Package	115
18 Ld SOIC Package	75
28 Ld SOIC Package	75
16 Ld SSOP Package	135
20 Ld SSOP Package	122
16 Ld TSSOP Package	145
20 Ld TSSOP Package	140
28 Ld SSOP and TSSOP Packages	100

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Note:

4. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379 for details.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

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2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range			
ICL32xxECX	0°	+70	°C
ICL32xxEFX	-40°	+125	°C
ICL32xxEIX	-40	+85	°C
Supply Voltage (V_{CC})	3.3	5	V
Rx Input Voltage	-15	+15	V

2.4 Electrical Specifications

Test conditions: V_{CC} = 3.0V to 5.5V, C_1 - C_4 = 0.1µF; unless otherwise specified. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range.**

Parameter	Test Conditions		Temp (°C)	Min (Note 6)	Typ	Max (Note 6)	Unit
DC Characteristics							
Supply Current, Automatic Power-Down	All R_{IN} Open, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC} (ICL3221E, ICL3223E, ICL3243E Only)		25	-	1.0	10	µA
Supply Current, Power-Down	$\overline{FORCEOFF}$ = $\overline{SHDN}$ = GND (Except ICL3232E)		25	-	1.0	10	µA
Supply Current, Automatic Power-Down Disabled	All Outputs Unloaded, FORCEON = $\overline{FORCEOFF}$ = $\overline{SHDN}$ = V_{CC}	V_{CC} = 3.0V, ICL3241, ICL3243	25	-	0.3	1.0	mA
		V_{CC} = 3.0V, ICL3223	25	-	0.7	3.0	mA
		V_{CC} = 3.15V, ICL3221, ICL3222, ICL3223, ICL3232	25	-	0.3	1.0	mA
Logic and Transmitter Inputs, Receiver Outputs							
Input Logic Threshold Low	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$		Full	-	-	**0.8**	V
Input Logic Threshold High	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$	V_{CC} = 3.3V	Full	**2.0**	-	-	V
		V_{CC} = 5.0V	Full	**2.4**	-	-	V
Input Leakage Current	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$	All but ICL3232EF	Full	-	±0.01	**±1.0**	µA
		ICL3232EF	Full	-	±0.01	**±10**	µA
Output Leakage Current (Except ICL3232E)	$\overline{FORCEOFF}$ = GND or $\overline{EN}$ = V_{CC}		Full	-	±0.05	**±10**	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	**0.4**	V
Output Voltage High	I_{OUT} = -1.0mA	All but ICL3232EF	Full	**V_{CC} - 0.6**	V_{CC} - 0.1	-	V
		ICL3232EF	Full	**V_{CC} - 0.9**	V_{CC} - 0.1	-	V
Automatic Powerdown (ICL3221E, ICL3223E, ICL3243E only, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC})							
Receiver Input Thresholds to Enable Transmitters	ICL32xxE Powers Up (see Figure 6 on page 14)		Full	**-2.7**	-	**2.7**	V
Receiver Input Thresholds to Disable Transmitters	ICL32xxE Powers Down (see Figure 6 on page 14)		Full	**-0.3**	-	**0.3**	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	**0.4**	V
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1.0mA		Full	**V_{CC} - 0.6**	-	-	V
Receiver Threshold to Transmitters Enabled Delay (t_{WU})			25	-	100	-	µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High Delay (t_{INVH})			25	-	1	-	µs

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Test conditions: V_{CC} = 3.0V to 5.5V, C_1 - C_4 = 0.1µF; unless otherwise specified. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range. (Continued)**

Parameter	Test Conditions		Temp (°C)	Min (Note 6)	Typ	Max (Note 6)	Unit
Receiver Positive or Negative Threshold to $\overline{\text{INVALID}}$ Low Delay (t_{INVL})			25	-	30	-	µs
Receiver Inputs							
Input Voltage Range			25	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		25	0.6	1.2	-	V
	V_{CC} = 5.0V		25	0.8	1.5	-	V
Input Threshold High	V_{CC} = 3.3V		25	-	1.5	2.4	V
	V_{CC} = 5.0V		25	-	1.8	2.4	V
Input Hysteresis			25	-	0.5	-	V
Input Resistance			25	3	5	7	kΩ
Transmitter Outputs							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	**±5.0**	±5.4	**-**	V
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	**300**	10M	**-**	Ω
Output Short-Circuit Current			Full	**-**	±35	**±60**	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 5.5V, Automatic Power-Down or $\overline{\text{FORCEOFF}}$ = $\overline{\text{SHDN}}$ = GND		Full	**-**	-	**±25**	µA
Mouse Driveability (ICL324XE Only)							
Transmitter Output Voltage (see Figure 15 on page 22)	$T1_{IN}$ = $T2_{IN}$ = GND, $T3_{IN}$ = V_{CC}, $T3_{OUT}$ Loaded with 3kΩ to GND, $T1_{OUT}$ and $T2_{OUT}$ Loaded with 2.5mA Each		Full	**±5**	-	-	V
Timing Characteristics							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, One Transmitter Switching		Full	**250**	500	-	kbps
Receiver Propagation Delay	Receiver Input to Receiver Output, C_L = 150pF	t_{PHL}	25	-	0.15	-	µs
		t_{PLH}	25	-	0.15	-	µs
Receiver Output Enable Time	Normal Operation (Except ICL3232E)		25	-	200	-	ns
Receiver Output Disable Time	Normal Operation (Except ICL3232E)		25	-	200	-	ns
Transmitter Skew	t_{PHL} to t_{PLH} (Note 5)		25	-	100	-	ns
Receiver Skew	t_{PHL} to t_{PLH}		25	-	50	-	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, Measured from 3V to -3V or -3V to 3V	C_L = 150pF to 2500pF	25	4	-	30	V/µs
		C_L = 150pF to 1000pF	25	6	-	30	V/µs
ESD Performance							
RS-232 Pins (TOUT, RIN)	Human Body Model		25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge		25	-	±8	-	kV
	IEC61000-4-2 Air Gap Discharge		25	-	±15	-	kV
All Other Pins	Human Body Model		25	-	±2	-	kV

Notes:

5. Transmitter skew is measured at the transmitter zero crossing points.
6. Parameters with Min and/or Max limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

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3. Typical Performance Curves

V_{CC} = 3.3V, T_A = +25°C.

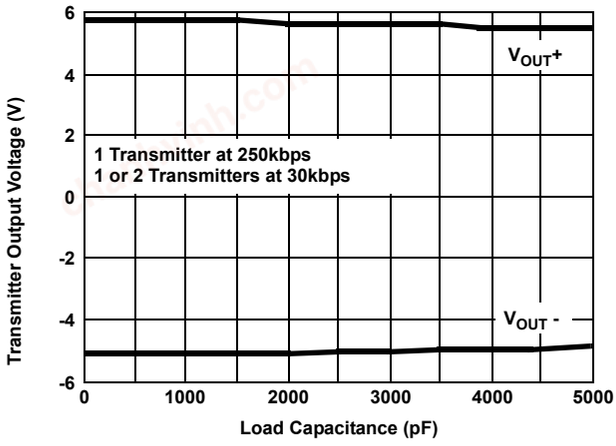


Figure 1. Transmitter Output Voltage vs Load Capacitance

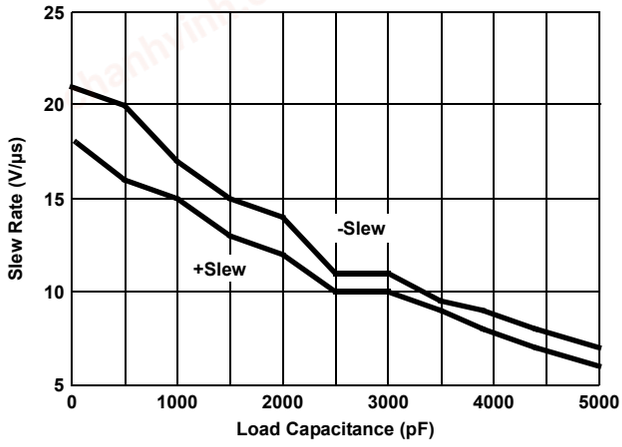


Figure 2. Slew Rate vs Load Capacitance

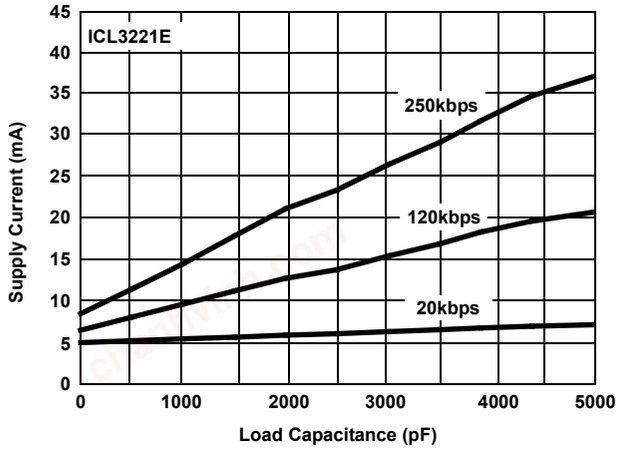


Figure 3. Supply Current vs Load Capacitance When Transmitting Data

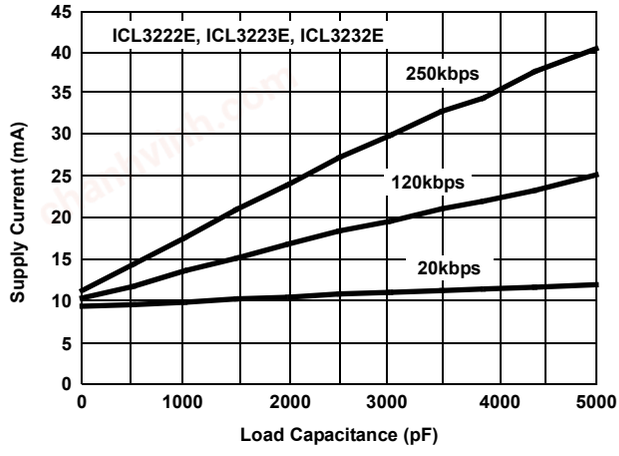


Figure 4. Supply Current vs Load Capacitance When Transmitting Data

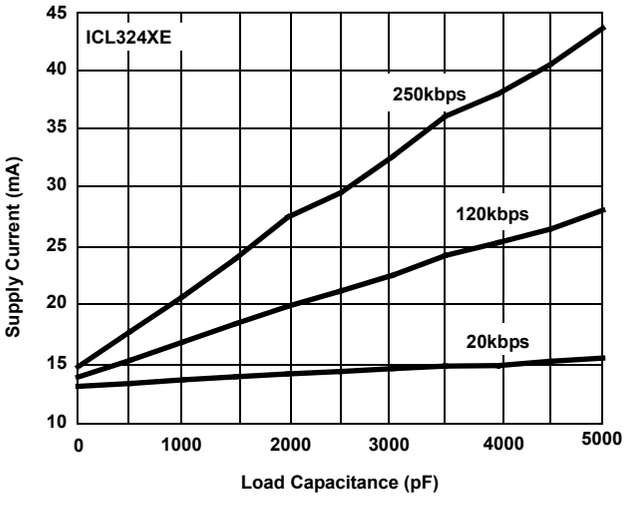


Figure 5. Supply Current vs Load Capacitance When Transmitting Data

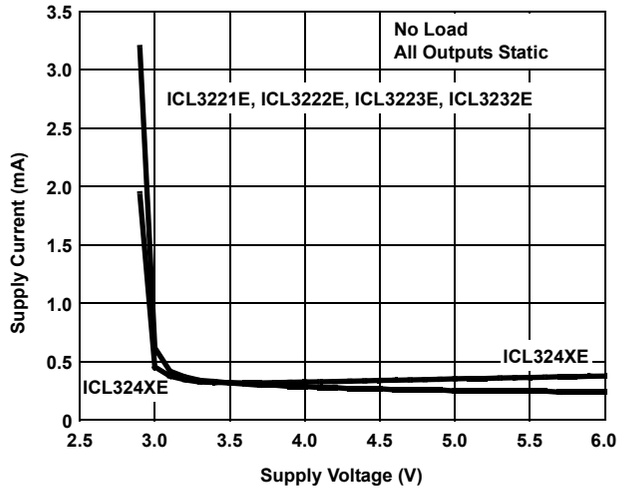


Figure 6. Supply Current vs Supply Voltage

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4. Application Information

The ICL32xxE interface ICs operate from a single +3V to +5.5V supply, ensure a 250kbps minimum data rate, require only four small external 0.1µF capacitors, feature low power consumption, and meet all EIA RS-232C and V.28 specifications.

4.1 Charge-Pump

The ICL32xxE family uses regulated on-chip dual charge-pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. The charge-pumps allow the devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small external 0.1µF capacitors for the voltage doubler and inverter functions at V_{CC} = 3.3V. See "Capacitor Selection" on page 21 and Table 6 on page 21 for capacitor recommendations for other operating conditions. The charge-pumps operate discontinuously (they turn off as soon as the V+ and V- supplies are pumped up to the nominal values) and provide significant power savings.

4.1.1 Charge-Pump Abs Max Ratings

These 3V to 5V RS-232 transceivers have been fully characterized for 3.0V to 3.6V operation, and at critical points for 4.5V to 5.5V operation. Furthermore, load conditions were favorable using static logic states only.

The specified maximum values for V+ and V- are +7V and -7V, respectively. These limits apply for V_{CC} values set to 3.0V and 3.6V (see Table 2). For V_{CC} values set to 4.5V and 5.5V, the maximum values for V+ and V- can approach +9V and -7V, respectively (Table 3). The breakdown characteristics for V+ and V- were measured with ±13V.

Table 2. V+ and V- Values for V_{CC} = 3.0V to 3.6V

C_1 (µF)	C_2, C_3, C_4 (µF)	Load	T1IN (Logic State)	V+ (V)		V- (V)	
				V_{CC} = 3.0V	V_{CC} = 3.6V	V_{CC} = 3.0V	V_{CC} = 3.6V
0.1	0.1	Open	H	5.80	6.56	-5.60	-5.88
			L	5.80	6.56	-5.60	-5.88
			2.4kbps	5.80	6.56	-5.60	-5.88
		3kΩ // 1000pF	H	5.88	6.60	-5.56	-5.92
			L	5.76	6.36	-5.56	-5.76
			2.4kbps	6.00	6.64	-5.64	-5.96
0.047	0.33	Open	H	5.68	6.00	-5.60	-5.60
			L	5.68	6.00	-5.60	-5.60
			2.4kbps	5.68	6.00	-5.60	-5.60
		3kΩ // 1000pF	H	5.76	6.08	-5.64	-5.64
			L	5.68	6.04	-5.60	-5.60
			2.4kbps	5.84	6.16	-5.64	-5.72
1	1	Open	H	5.88	6.24	-5.60	-5.60
			L	5.88	6.28	-5.60	-5.64
			2.4kbps	5.80	6.20	-5.60	-5.60
		3kΩ // 1000pF	H	5.88	6.44	-5.64	-5.72
			L	5.88	6.04	-5.64	-5.64
			2.4kbps	5.92	6.40	-5.64	-5.64

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Table 3. V+ and V- Values for V_{CC} = 4.5V to 5.5V

C_1 (µF)	C_2, C_3, C_4 (µF)	Load	T1IN (Logic State)	V+ (V)		V- (V)	
				V_{CC} = 4.5V	V_{CC} = 5.5V	V_{CC} = 4.5V	V_{CC} = 5.5V
0.1	0.1	Open	H	7.44	8.48	-6.16	-6.40
			L	7.44	8.48	-6.16	-6.44
			2.4kbps	7.44	8.48	-6.17	-6.44
		3kΩ // 1000pF	H	7.76	8.88	-6.36	-6.72
			L	7.08	8.00	-5.76	-5.76
			2.4kbps	7.76	8.84	-6.40	-6.64
0.047	0.33	Open	H	6.44	6.88	-5.80	-5.88
			L	6.48	6.88	-5.84	-5.88
			2.4kbps	6.44	6.88	-5.80	-5.88
		3kΩ // 1000pF	H	6.64	7.28	-5.92	-6.04
			L	6.24	6.60	-5.52	-5.52
			2.4kbps	6.72	7.16	-5.92	-5.96
1	1	Open	H	6.84	7.60	-5.76	-5.76
			L	6.88	7.60	-5.76	-5.76
			2.4kbps	6.92	7.56	-5.72	-5.76
		3kΩ // 1000pF	H	7.28	8.16	-5.80	-5.92
			L	6.44	6.84	-5.64	-6.84
			2.4kbps	7.08	7.76	-5.80	-5.80

The resulting new maximum voltages at V+ and V- are listed in Table 4.

Table 4. New Measured Withstanding Voltages

V+, V- to Ground	±13V
V+ to V-	20V

4.2 Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. The transmitters are coupled with the on-chip ±5.5V supplies and deliver true RS-232 levels across a wide range of single supply system voltages.

Except for the ICL3232E, all transmitter outputs disable and assume a high impedance state when the device enters the power-down mode (see Table 5 on page 18). The outputs can be driven to ±12V when disabled.

All devices operate at a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 900kbps.

The transmitter inputs float if left unconnected and can increase I_{CC}. Connect unused inputs to GND for the best performance.

4.3 Receivers

All the ICL32xxE devices except for the ICL3232E contain standard inverting receivers that three-state from the EN or FORCEOFF control lines. The two ICL324XE devices include noninverting (monitor) receivers (denoted by the ROUTB label) that are always active, regardless of the state of any control lines. All the receivers convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 7) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

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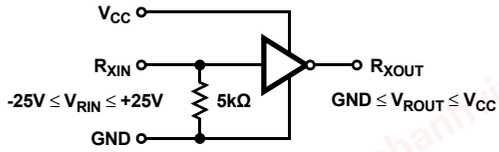


Figure 7. Inverting Receiver Connections

The ICL3221E, ICL3222E, ICL3223E, and ICL3241E inverting receivers disable only when $\overline{EN}$ is driven high. The ICL3243E receiver disables during forced (manual) power-down, but not during automatic power-down (see Table 5 on page 18).

The ICL3241E and ICL3243E monitor receivers remain active even during manual power-down and forced receiver disable, which makes them extremely useful for Ring Indicator monitoring. Standard receivers driving powered down peripherals must be disabled to prevent current flow through the peripheral's protection diodes (see Figures 8 and 9). When disabled, the receivers cannot be used for wake up functions, but the corresponding monitor receiver can be dedicated to this task, as shown in Figure 9.

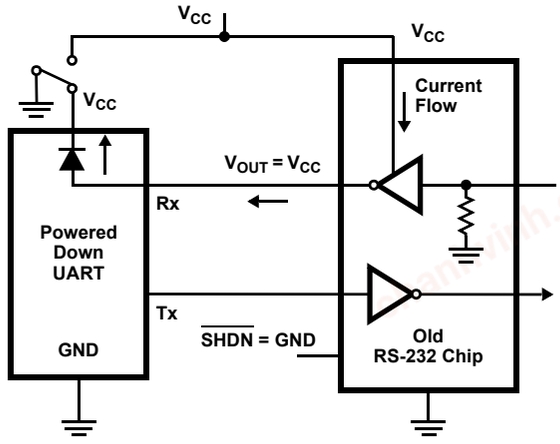


Figure 8. Power Drain Through Powered Down Peripheral

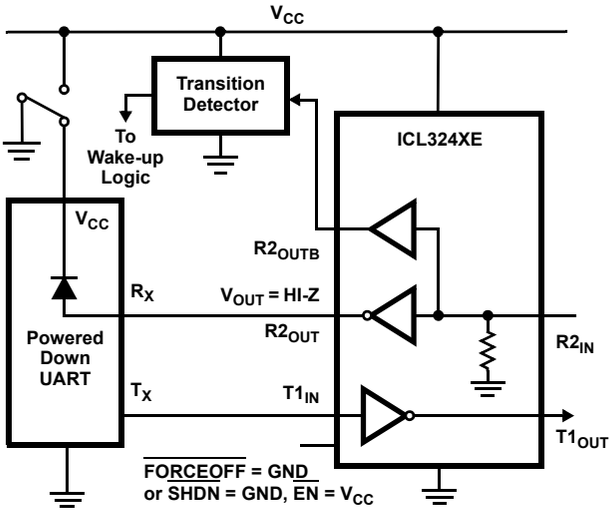


Figure 9. Disabled Receivers Prevent Power Drain

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4.4 Low Power Operation

These 3V devices require a nominal supply current of 0.3mA, even at V_{CC} = 5.5V, during normal operation (not in power-down mode). This current is considerably less than the 5mA to 11mA current required by comparable 5V RS-232 devices and allows you to reduce system power simply by switching to this family.

4.5 Power-Down Functionality (Except ICL3232E)

The already low current requirement drops significantly when the device enters power-down mode. In power-down, the supply current drops to 1µA because the on-chip charge pump turns off (V+ collapses to V_{CC} and V- collapses to GND), and the transmitter outputs three-state. Inverting receiver outputs may disable in power-down; see Table 5 for details. This micro-power mode makes these devices ideal for battery powered and portable applications.

4.5.1 Software Controlled (Manual) Power-Down

Most devices in the ICL32xxE family provide pins that allow you to force the IC into the low power standby state.

On the ICL3222E and ICL3241E, the power-down control is a simple shutdown ($\overline{SHDN}$) pin. Driving this pin high enables normal operation, and driving it low forces the IC into its power-down state. Connect $\overline{SHDN}$ to V_{CC} if the power-down function is not needed. Note that all the receiver outputs remain enabled during shutdown (see Table 5). For the lowest power consumption during power-down, the receivers should also be disabled by driving the $\overline{EN}$ input high (see "Receiver ENABLE Control (ICL3221E, ICL3222E, ICL3223E, and ICL3241E Only)" on page 21 and Figures 8 and 9).

The ICL3221E, ICL3223E, and ICL3243E use a two pin approach in which the FORCEON and $\overline{FORCEOFF}$ inputs determine the IC's mode. For always enabled operation, FORCEON and $\overline{FORCEOFF}$ are both strapped high. Under logic or software control, only the $\overline{FORCEOFF}$ input needs to be driven to switch between active and power-down modes. The FORCEON state is not critical because $\overline{FORCEOFF}$ overrides FORCEON. However, if strictly manual control over power-down is needed, you must strap FORCEON high to disable the automatic power-down circuitry. The ICL3243E inverting (standard) receiver outputs also disable when the device is in manual power-down, which eliminates the possible current path through a shutdown peripheral's input protection diode (see Figures 8 and 9).

Table 5. Power-Down and Enable Logic Truth Table

RS-232 Signal Present at Receiver Input?	$\overline{FORCEOFF}$ or $\overline{SHDN}$ Input	FORCEON Input	$\overline{EN}$ Input	Transmitter Outputs	Receiver Outputs	R_{OUTB} Outputs (Note 7)	$\overline{INVALID}$ Output	Mode of Operation
ICL3222E, ICL3241E								
N/A	L	N/A	L	High-Z	Active	Active	N/A	Manual Power-Down
N/A	L	N/A	H	High-Z	High-Z	Active	N/A	Manual Power-Down with Receiver Disabled
N/A	H	N/A	L	Active	Active	Active	N/A	Normal Operation
N/A	H	N/A	H	Active	High-Z	Active	N/A	Normal Operation with Receiver Disabled
ICL3221E, ICL3223E								
No	H	H	L	Active	Active	N/A	L	Normal Operation (Auto Power-Down Disabled)
No	H	H	H	Active	High-Z	N/A	L	
Yes	H	L	L	Active	Active	N/A	H	Normal Operation (Auto Power-Down Enabled)
Yes	H	L	H	Active	High-Z	N/A	H	
No	H	L	L	High-Z	Active	N/A	L	Power-Down Due to Auto Power-Down Logic
No	H	L	H	High-Z	High-Z	N/A	L	
Yes	L	X	L	High-Z	Active	N/A	H	Manual Power-Down

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Table 5. Power-Down and Enable Logic Truth Table (Continued)

RS-232 Signal Present at Receiver Input?	$\overline{\text{FORCEOFF}}$ or $\overline{\text{SHDN}}$ Input	FORCEON Input	$\overline{\text{EN}}$ Input	Transmitter Outputs	Receiver Outputs	R_{OUTB} Outputs (Note 7)	$\overline{\text{INVALID}}$ Output	Mode of Operation
Yes	L	X	H	High-Z	High-Z	N/A	H	Manual Power-Down with Receiver Disabled
No	L	X	L	High-Z	Active	N/A	L	Manual Power-Down
No	L	X	H	High-Z	High-Z	N/A	L	Manual Power-Down with Receiver Disabled
ICL3243E								
No	H	H	N/A	Active	Active	Active	L	Normal Operation (Auto Power-Down Disabled)
Yes	H	L	N/A	Active	Active	Active	H	Normal Operation (Auto Power-Down Enabled)
No	H	L	N/A	High-Z	Active	Active	L	Power-Down Due to Auto Power-Down Logic
Yes	L	X	N/A	High-Z	High-Z	Active	H	Manual Power-Down
No	L	X	N/A	High-Z	High-Z	Active	L	Manual Power-Down

Note:
7. Applies only to the ICL3241E and ICL3243E.

4.5.2 $\overline{\text{INVALID}}$ Output

The $\overline{\text{INVALID}}$ output always indicates whether a valid RS-232 signal is present at any of the receiver inputs (see Table 5) and provides an easy way to determine when the interface block should power down. If an interface cable is disconnected and all the receiver inputs are floating (but pulled to GND by the internal receiver pull down resistors), the $\overline{\text{INVALID}}$ logic detects the invalid levels and drives the output low. The power management logic then uses this indicator to power down the interface block. Reconnecting the cable restores valid levels at the receiver inputs, $\overline{\text{INVALID}}$ switches high, and the power management logic wakes up the interface block. $\overline{\text{INVALID}}$ can also indicate the DTR or RING INDICATOR signal as long as the other receiver inputs are floating or driven to GND (as in the case of a powered down driver). Connecting $\overline{\text{FORCEOFF}}$ and FORCEON together disables the automatic power-down feature and enables them to function as a manual $\overline{\text{SHUTDOWN}}$ input (see Figure 10).

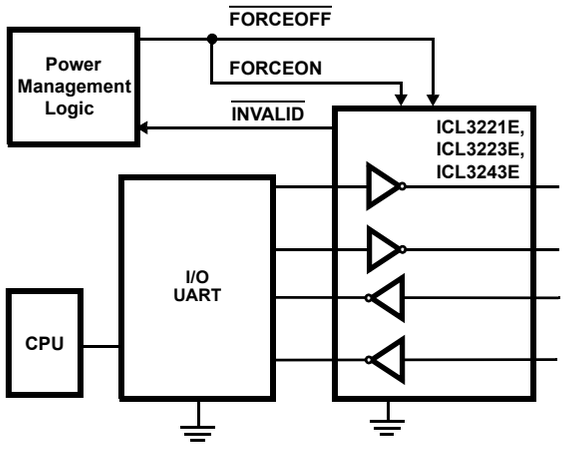


Figure 10. Connections For Manual Power-Down When no Valid Receiver Signals are Present

With any of the control schemes, the time required to exit power-down and resume transmission is 100µs. A mouse or other application may need more time to wake up from shutdown. If automatic power-down is used, the RS-232 device reenters power-down if valid receiver levels are not reestablished within 30µs of the ICL32xxE

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powering up. Figure 11 shows a circuit that prevents the ICL32xxE from initiating automatic power-down for 100ms after powering up. The delay gives the slow-to-wake peripheral circuit time to reestablish valid RS-232 output levels.

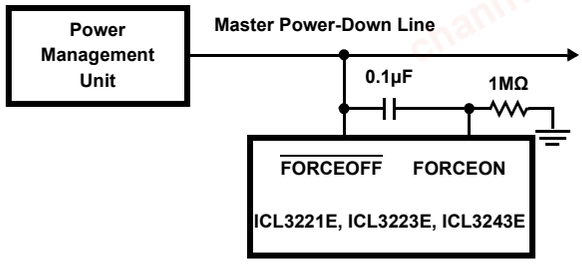


Figure 11. Circuit to Prevent Auto Power-Down For 100ms After Forced Power-Up

4.5.3 Automatic Power-Down (ICL3221E, ICL3223E, and ICL3243E Only)

Even greater power savings are available by using the ICL3221E, ICL3223E, or ICL3243E's automatic power-down function. When no valid RS-232 voltages are sensed on any receiver input for 30µs (see Figure 12), the charge-pump and transmitters power down and reduce the supply current to 1µA. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. The ICL32xxE powers back up whenever it detects a valid RS-232 voltage level on any receiver input. The automatic power-down feature provides additional system power savings without changes to the existing operating system.

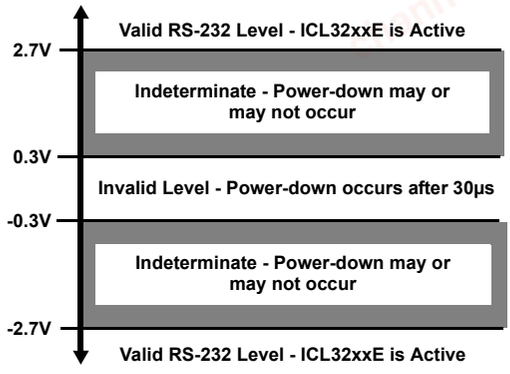


Figure 12. Definition of Valid RS-232 Receiver Levels

Automatic power-down operates when the FORCEON input is low and the $\overline{\text{FORCEOFF}}$ input is high. Tying FORCEON high disables automatic power-down, but manual power-down is always available with the overriding $\overline{\text{FORCEOFF}}$ input. Table 5 on page 18 summarizes the automatic power-down functionality.

Devices with the automatic power-down feature include an $\overline{\text{INVALID}}$ output signal that switches low to indicate that invalid levels have persisted on all of the receiver inputs for more than 30µs (see Figure 13). $\overline{\text{INVALID}}$ switches high 1µs after detecting a valid RS-232 level on a receiver input. $\overline{\text{INVALID}}$ operates in all modes (forced or automatic power-down, or forced on), so it is also useful for systems employing manual power-down circuitry. When automatic power-down is used, $\overline{\text{INVALID}}$ = 0 indicates that the ICL32xxE is in power-down mode.

The time to recover from automatic power-down mode is typically 100µs.

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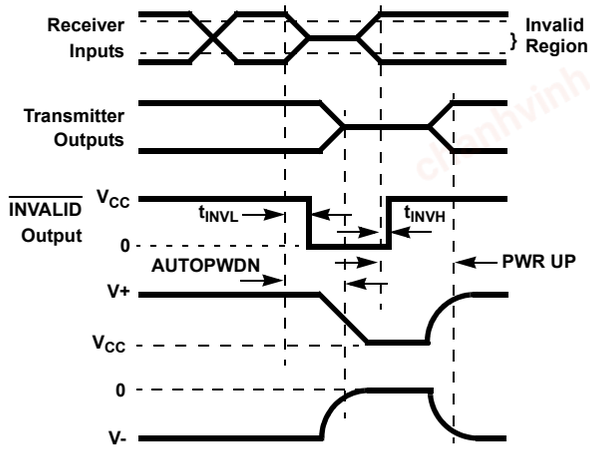


Figure 13. Automatic Power-Down and $\overline{\text{INVALID}}$ Timing Diagrams

4.6 Receiver ENABLE Control (ICL3221E, ICL3222E, ICL3223E, and ICL3241E Only)

The ICL3221E, ICL3222E, ICL3223E, and ICL3241E also feature an $\overline{\text{EN}}$ input to control the receiver outputs. Driving $\overline{\text{EN}}$ high disables all the inverting (standard) receiver outputs and places them in a high impedance state. The high impedance state is useful for eliminating supply current, due to a receiver output forward biasing the protection diode when driving the input of a powered down (V_{CC} = GND) peripheral (see Figure 8 on page 17). The enable input has no effect on transmitter or monitor (R_{OUTB}) outputs.

4.7 Capacitor Selection

The charge-pumps require 0.1µF capacitors for 3.3V operation. For other supply voltages, see Table 6 for capacitor values. Do not use values smaller than those listed in Table 6. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C_2, C_3, and C_4 can be increased without increasing C_1's value; however, do not increase C_1 without also increasing C_2, C_3, and C_4 to maintain the proper ratios (C_1 to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's Equivalent Series Resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

Table 6. Required Capacitor ValueS

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

4.8 Power Supply Decoupling

In most circumstances, a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

4.9 Operation Down to 2.7V

The ICL32xxE transmitter outputs meet RS-562 levels (±3.7V) at full data rate, with V_{CC} as low as 2.7V. RS-562 levels typically ensure interoperability with RS-232 devices.

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4.10 Transmitter Outputs when Exiting Power-Down

Figure 14 shows the response of two transmitter outputs when exiting power-down mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, or undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceeds approximately 3V.

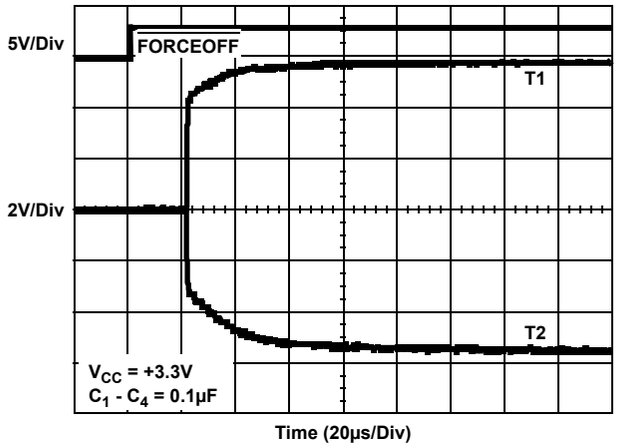


Figure 14. TRansmitter Outputs When Exiting Power-Down

4.11 Mouse Driveability

The ICL3241E and ICL3243E are specifically designed to power a serial mouse while operating from low voltage supplies. Figure 15 shows the transmitter output voltages under increasing load current. The on-chip switching regulator ensures the transmitters supply at least ±5V during worst case conditions (15mA for paralleled V+ transmitters, 7.3mA for a single V- transmitter). The Automatic Power-Down feature does not work with a mouse, so $\overline{\text{FORCEOFF}}$ and FORCEON should be connected to V_{CC}.

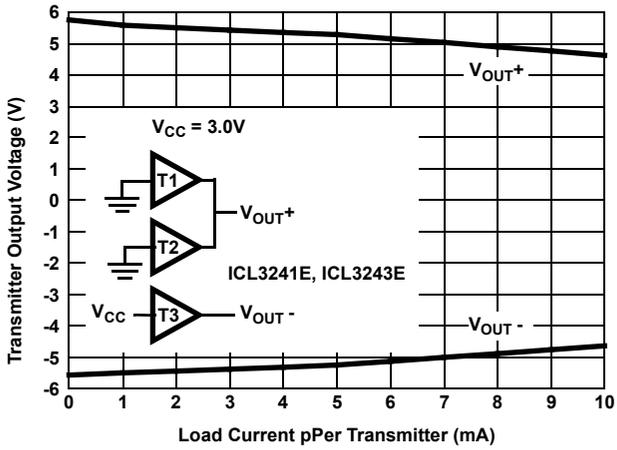


Figure 15. Transmitter Output Voltage vs Load Current (Per Transmitter, Double Current Axis for Total V_{OUT+} Current)

4.12 High Data Rates

The ICL32xxE devices maintain the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 16 shows a transmitter loopback test circuit and Figure 17 shows the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF at 120kbps. Figure 18 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

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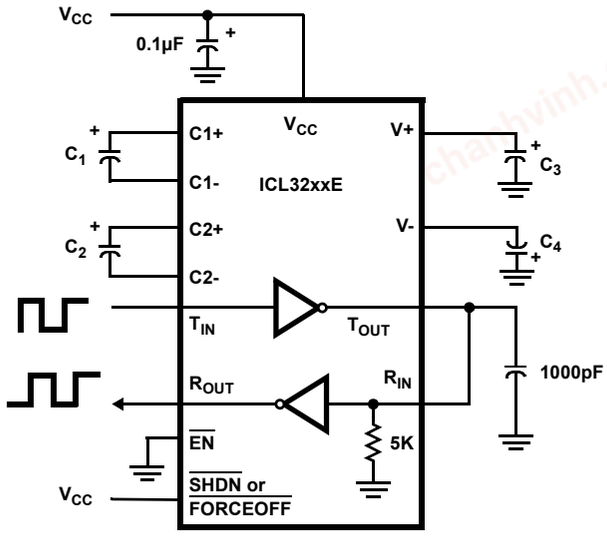


Figure 16. Transmitter Loopback Test Circuit

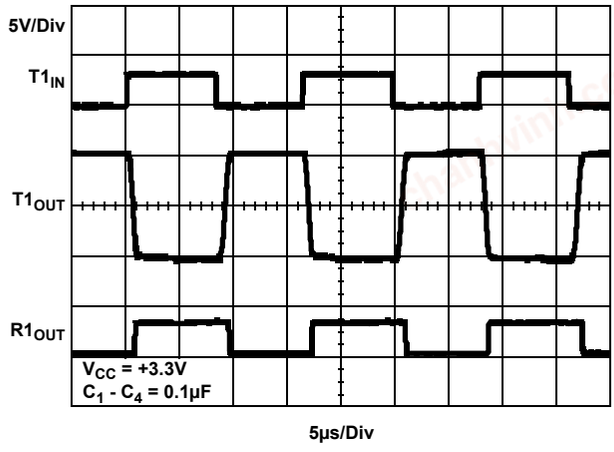


Figure 17. Loopback Test at 120kbps

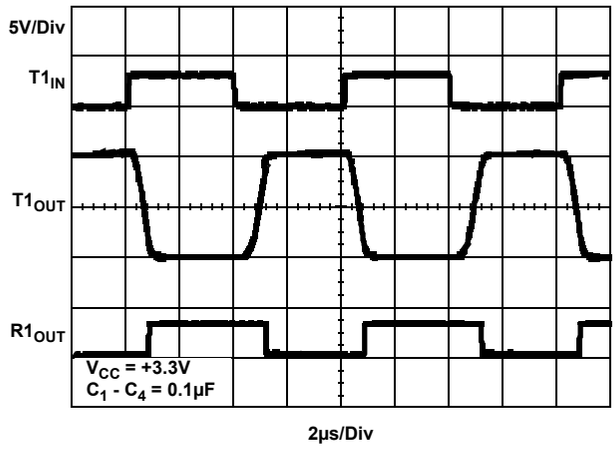


Figure 18. Loopback Test at 250kbps

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4.13 Interconnection with 3V and 5V Logic

The ICL32Exx devices directly interface with 5V CMOS and TTL logic families. The AC, HC, and CD4000 outputs can drive ICL32Exx inputs with the ICL32Exx at 3.3V and the logic supply at 5V, but ICL32Exx outputs do not reach the minimum V_{IH} for these logic families. See Table 7.

Table 7. Logic Family Compatibility with Various Supply Voltages

System Power Supply Voltage (V)	V_{CC} Supply Voltage (V)	Compatibility
3.3	3.3	Compatible with all CMOS families
5	5	Compatible with all TTL and CMOS logic families
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ICL32XX outputs are incompatible with AC, HC, and CD4000 CMOS inputs

4.14 Pin-Compatible Replacements for 5V Devices

The ICL3221E, ICL3222E, and ICL3232E are pin-compatible with existing 5V RS-232 transceivers. See “Features” on page 1 for more information.

The pin compatibility coupled with the low I_{CC} and wide operating supply range make the ICL32xxE potential lower power, higher performance drop-in replacements for existing 5V applications. The ICL32xxE works in most 5V applications as long as the ±5V RS-232 output swings are acceptable and transmitter input pull-up resistors are not required.

When replacing a device in an existing 5V application, you can terminate C_3 to V_{CC} as shown in the “Typical Operating Circuits” on page 4. If possible, terminate C_3 to GND for slightly better performance.

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5. ±15kV ESD Protection

All pins on the ICL32Exx devices include ESD protection structures, but the ICL32xxE family incorporates advanced structures that allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Touching the port pins or connecting a cable, can cause an ESD event that might destroy unprotected ICs. The ESD structures protect the device whether or not it is powered up, protect without allowing any latch-up mechanism to activate, and do not interfere with RS-232 signals as large as ±25V.

5.1 Human Body Model (HBM) Testing

This test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor and makes the test less severe than the IEC61000 test, which uses a 330Ω limiting resistor. The HBM method determines an IC's ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

5.2 IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

5.3 Air-Gap Discharge Test Method

For the air-gap discharge test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on factors such as approach speed, humidity, and temperature, so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

5.4 Contact Discharge Test Method

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized and eliminates the variables associated with the air-gap discharge. The test is more repeatable and predictable, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

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6. Die Characteristics

Table 8. Die and Assembly Related Information

Substrate and QFN Thermal Pad Potential (Powered Up)	GND
Transistor Count	
ICL3221E	286
ICL3222E	338
ICL3223E	357
ICL3232E	296
ICL324xE	464
Process	Si Gate CMOS

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7. Revision History

Rev.	Date	Description
FN4910.24	5/30/19	Applied new formatting. Updated the Ordering Information table: Removed: ICL3222ECP ICL3241ECBZ ICL3241ECBZ-T ICL3241EIBZ ICL3241EIBZ-T Added: ICL3221ECVZ ICL3221ECVZ-T ICL3232ECV-16Z-T7A ICL3232EIV-16Z-T7A Added Charge-Pump Abs Max Ratings section on pages 14 and 15. Removed package outline drawing E18.3. Updated disclaimer.
FN4910.23	9/24/18	-Updated on-chip voltage converter V_{CC} conditions from 2.7V to 3.3V on page 1 -Added product information page links to Related Literature section on page 1 -Updated Ordering Information table on page 8: -Added Tape and Reel (Units) column -Removed the following retired parts: -ICL3221ECA, ICL3221ECA-T -ICL3221ECAZA, ICL3221ECAZA-T -ICL3221ECV, ICL3221ECV-T -ICL3221EIA, ICL3221EIA-T -ICL3221ECA, ICL3221ECA-T -ICL3222ECV, ICL3222ECV-T -ICL3222EIAZ, ICL3222EIAZ-T -ICL3222EIB, ICL3222EIB-T -ICL3223ECA, ICL3223ECA-T -ICL3223ECV, ICL3223ECV-T -ICL3223EIAZ, ICL3223EIAZ-T -Added retirement notifications and replacement recommendations for the following parts: -ICL3232ECV-20Z -ICL3232ECV-20Z-T -ICL3232EFV-16Z -ICL3232EFV-16Z -Updated R_{IN} from ±25V to ±28V in the Absolute Maximum Ratings on page 12 -Updated Package Outline Drawing M16.15 from Rev. 1 to Rev. 2 on page 25 -Updated graphics to new standard layout and removed the dimensions table -Removed About Intersil section -Added Renesas disclaimer
FN4910.22	12/9/15	-Updated Ordering Information table starting on page 8 -Updated “Products” section to “About Intersil” -POD E18.3 updated from rev 2 to rev 3. Changes since rev 2: 1) Removed the dimension chart and replaced with new standard format values for each dimension letter. 2) Updated D dimension (in side view; length of package) from 0.845(min) : 0.880(max) to 0.880(33.27)(min) : 0.920(34.65)(max) 3) Change JEDEC reference from MS-001-BC issue D to MS-001-AC issue D -POD M16.173 updated from rev 1 to rev 2. Changes since rev 1: Converted to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. -POD M20.173 updated from rev 1 to rev 2. Changes since rev 1: Converted to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. -POD M28.173 udpated from rev 0 to rev 1. Changes since rev 1: Converted to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. -POD M28.3 updated from rev 0 to rev 1. Changes since rev 1: Added land pattern

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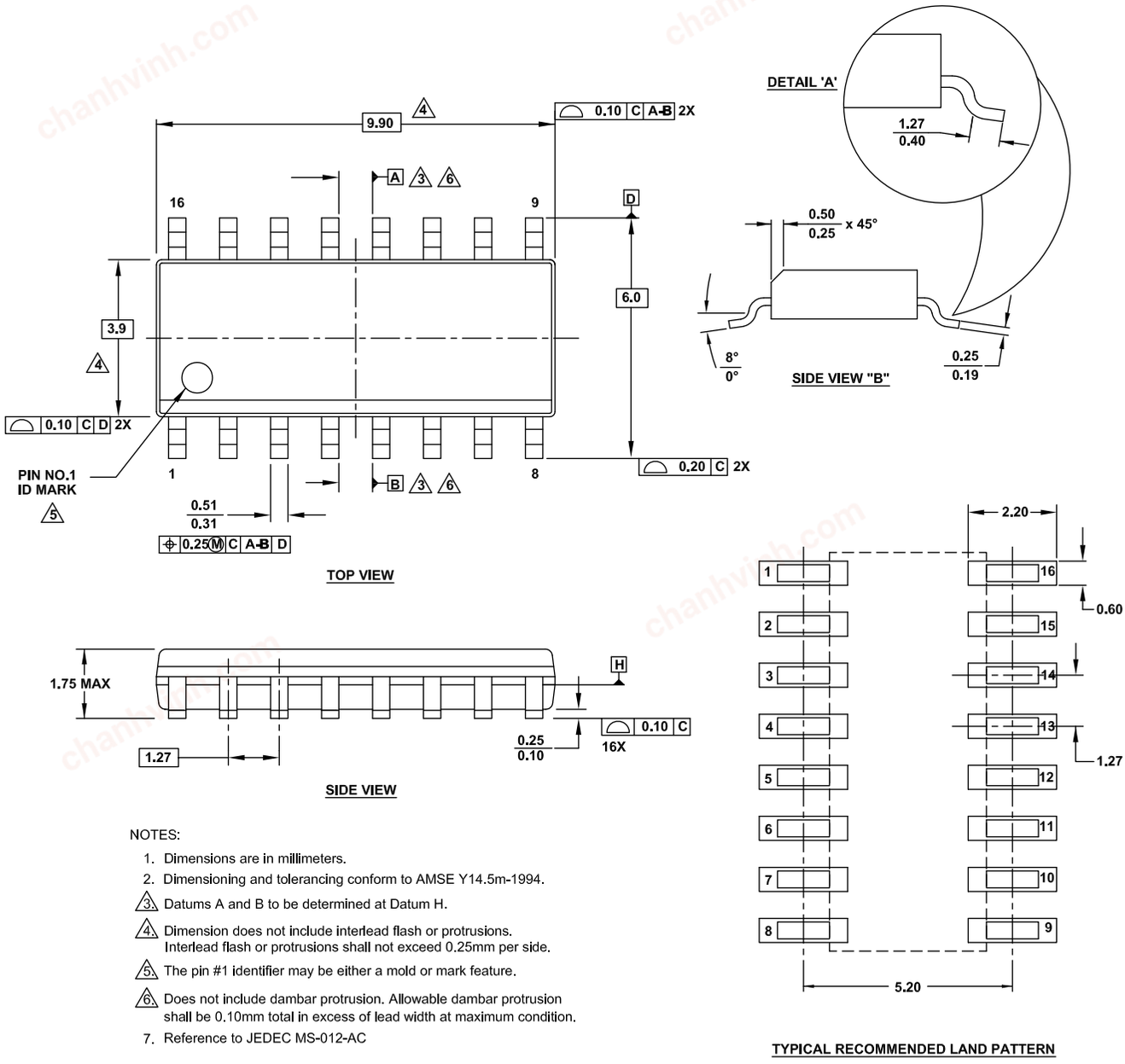
Rev.	Date	Description
FN4910.21	2/22/10	Revision history begins with this revision. -Converted to new Intersil template. -Added new temp grade (F = extended industrial) to ICL3232. Updated ordering info table, Operating Conditions, and added 125°C specs for input lkg currents, and rcvr output high voltage. -Pages 8-10: Removed all withdrawn devices from Ordering Information table. -Pages 12-14: Added "Boldface limits apply over the operating temperature range." to common conditions of Electrical Specs table. Replaced Note 6 "Parts are 100% tested at +25°C. Full temp limits are guaranteed by bench and tester characterization." with "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested."

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8. Package Outline Drawings

For the most recent package outline drawing, see M16.15.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 Lead Narrow Body Small Outline Plastic Package
Rev 2, 11/17



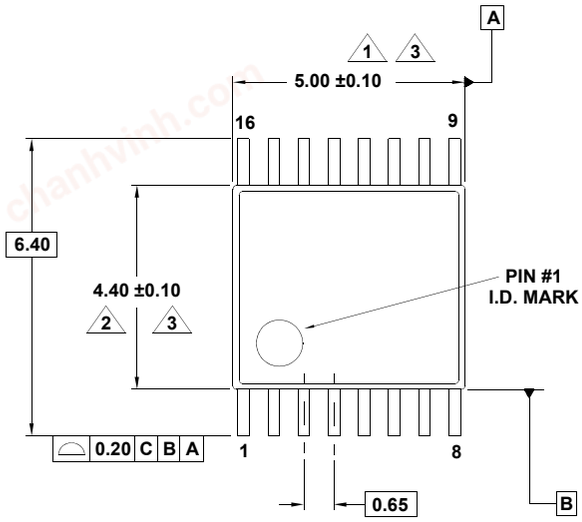
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AC

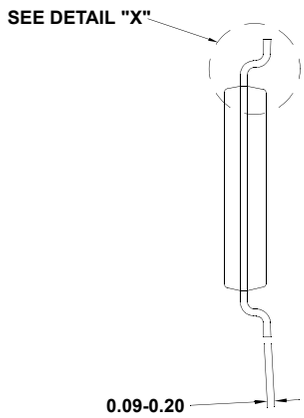
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M16.173
16 Lead Thin Shrink Small Outline Package (TSSOP)
Rev 2, 5/10

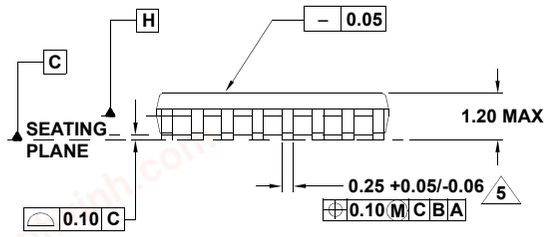
For the most recent package outline drawing, see M16.173.



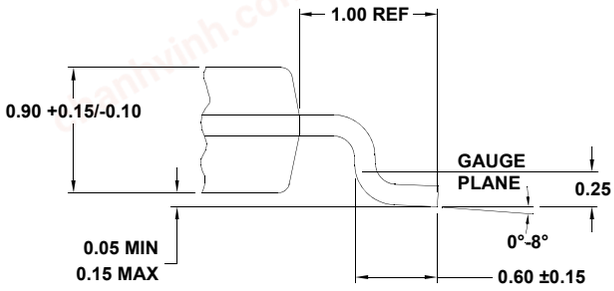
TOP VIEW



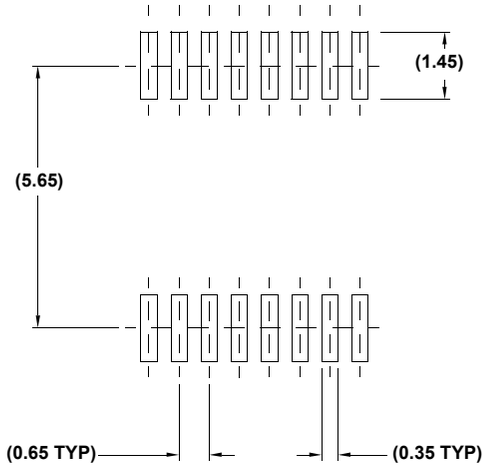
END VIEW



SIDE VIEW



DETAIL "X"



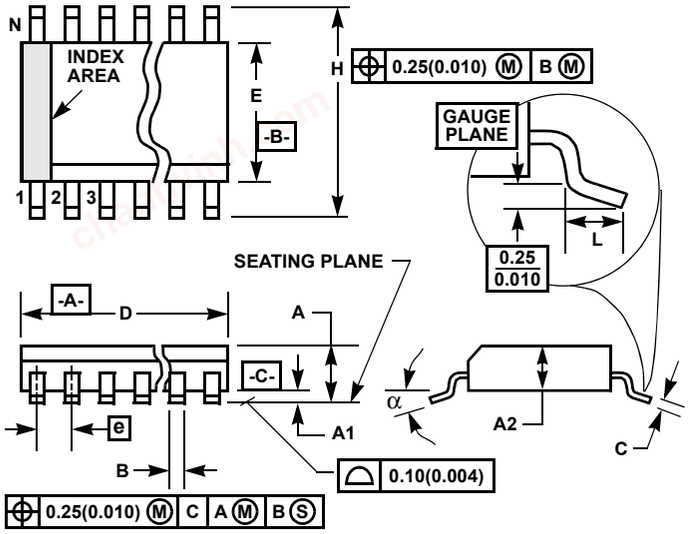
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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For the most recent package outline drawing, see M16.209.



Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.209 (JEDEC MO-150-AC ISSUE B)

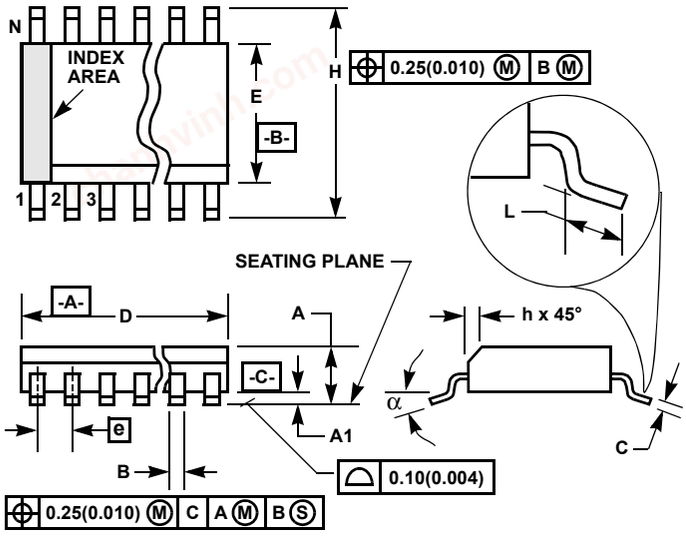
16 Lead Shrink Small Outline Plastic Package (SSOP)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.233	0.255	5.90	6.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 3 6/05

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For the most recent package outline drawing, see M16.3.



M16.3 (JEDEC MS-013-AA ISSUE C)

16 Lead Wide Body Small Outline Plastic Package (SOIC)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

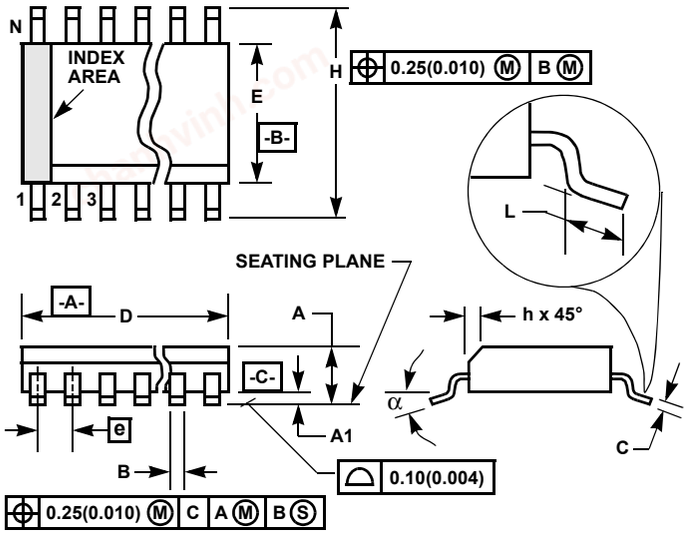
Rev. 1 6/05

Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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For the most recent package outline drawing, see M18.3.



M18.3 (JEDEC MS-013-AB ISSUE C)

18 Lead Wide Body Small Outline Plastic Package (SOIC)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4469	0.4625	11.35	11.75	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	18		18		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

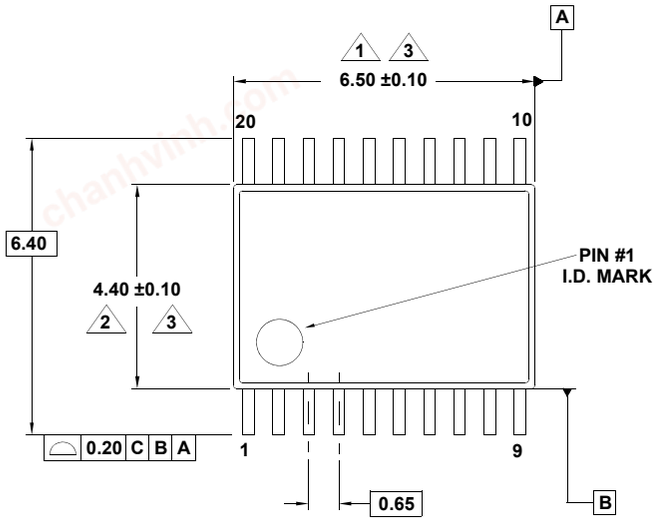
Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

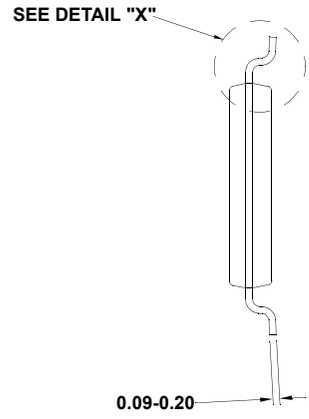
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M20.173
20 Lead Thin Shrink Small Outline Package (TSSOP)
Rev 2, 5/10

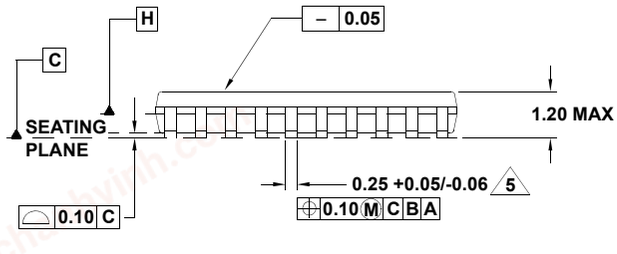
For the most recent package outline drawing, see M20.173.



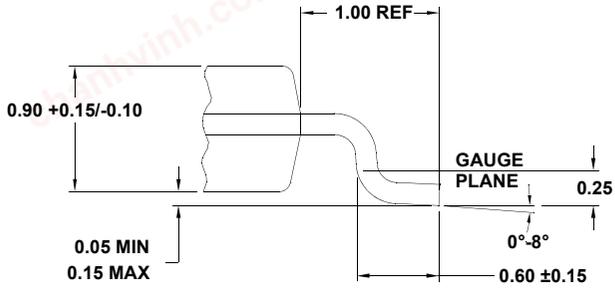
TOP VIEW



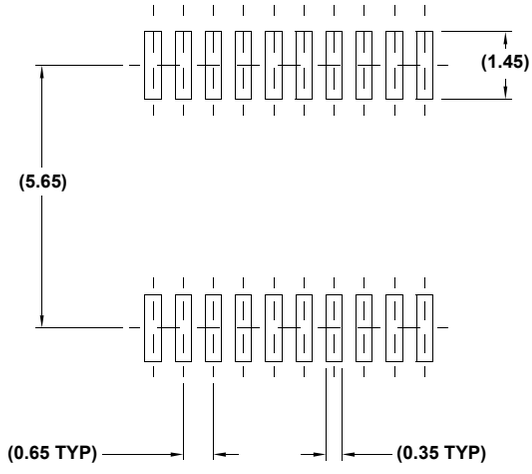
END VIEW



SIDE VIEW



DETAIL "X"



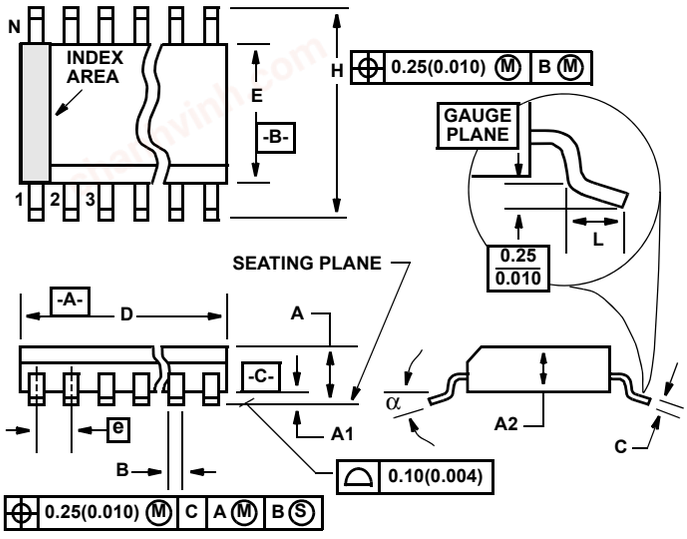
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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For the most recent package outline drawing, see M20.209.



M20.209 (JEDEC MO-150-AE ISSUE B)

20 Lead Shrink Small Outline Plastic Package (SSOP)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.068	0.078	1.73	1.99	
A1	0.002	0.008’	0.05	0.21	
A2	0.066	0.070’	1.68	1.78	
B	0.010’	0.015	0.25	0.38	9
C	0.004	0.008	0.09	0.20’	
D	0.278	0.289	7.07	7.33	3
E	0.205	0.212	5.20’	5.38	4
e	0.026 BSC		0.65 BSC		
H	0.301	0.311	7.65	7.90’	
L	0.025	0.037	0.63	0.95	6
N	20		20		7
α	0 deg.	8 deg.	0 deg.	8 deg.	

Rev. 3 11/02

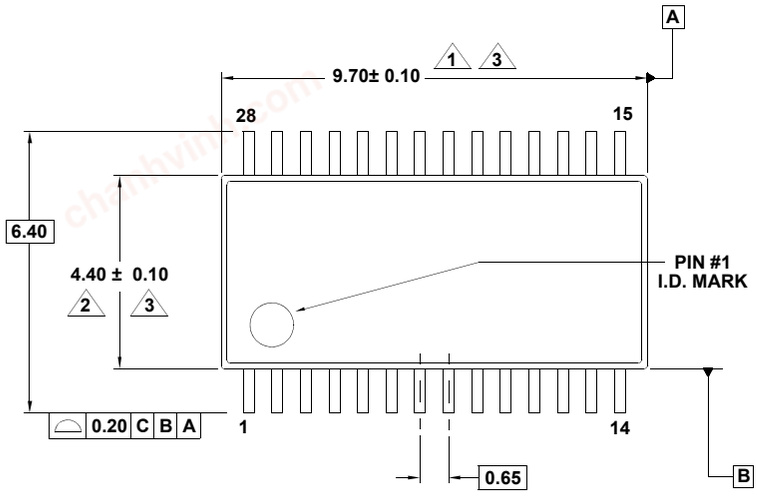
Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

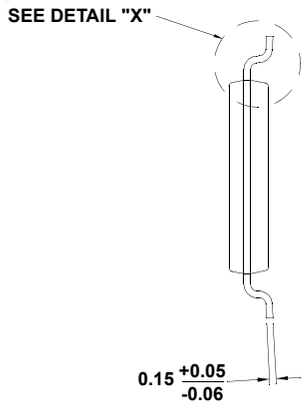
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M28.173
28 Lead Thin Shrink Small Outline Package (TSSOP)
Rev 1, 5/10

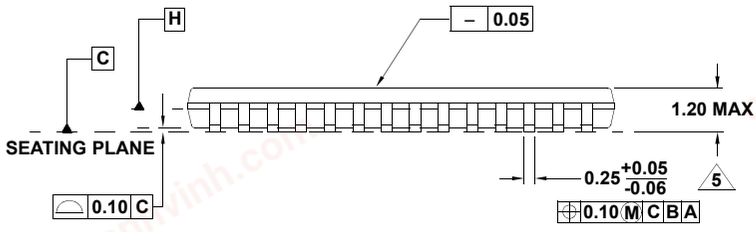
For the most recent package outline drawing, see M28.173.



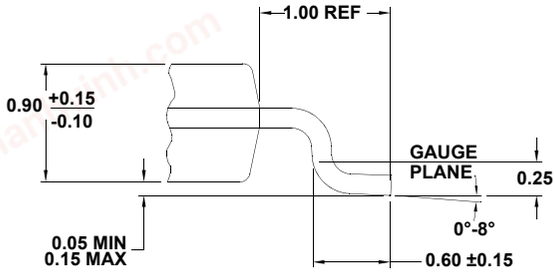
TOP VIEW



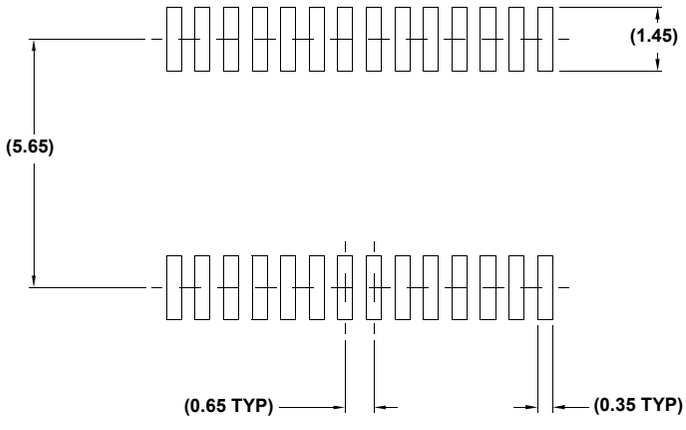
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

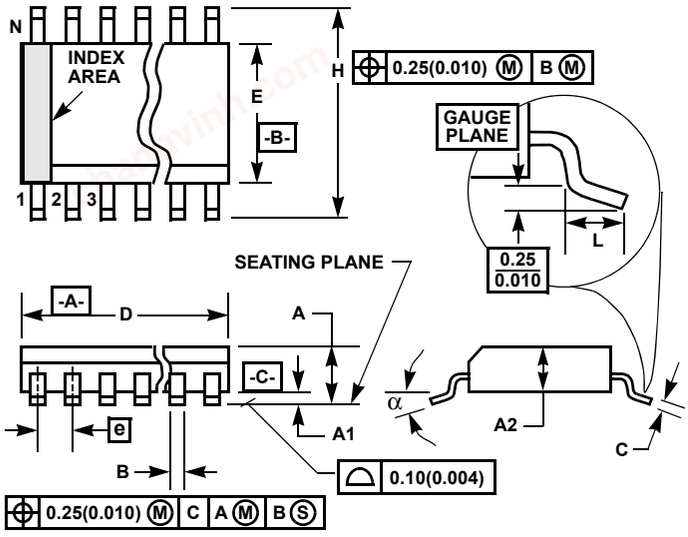
1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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For the most recent package outline drawing, see M28.209.

M28.209 (JEDEC MO-150-AH ISSUE B)

28 Lead Shrink Small Outline Plastic Package (SSOP)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 2 6/05

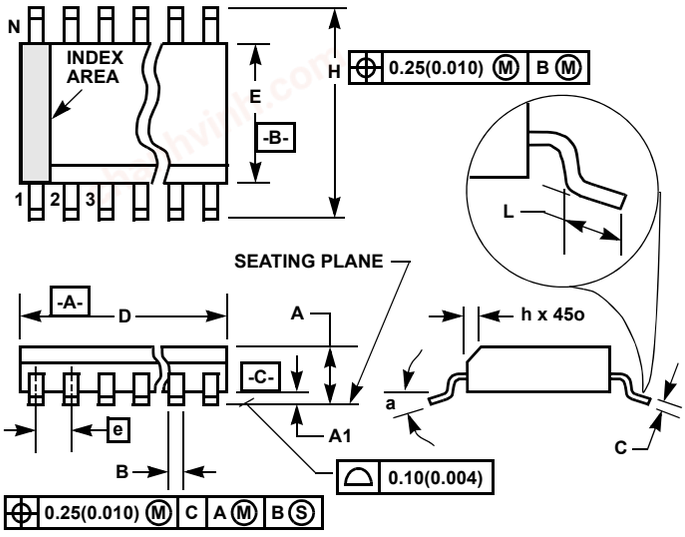
Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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For the most recent package outline drawing, see M28.3.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 Lead Wide Body Small Outline Plastic Package (SOIC)



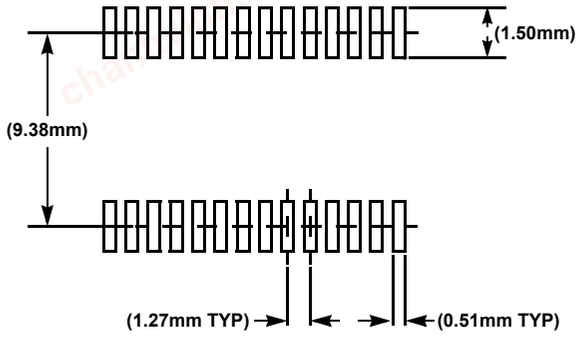
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0º	8º	0º	8º	-

Rev. 1, 1/13

Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

TYPICAL RECOMMENDED LAND PATTERN



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(Rev.4.0-1 November 2017)

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