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RENESAS

DATASHEET

HI-201HS

High Speed, Quad SPST, CMOS Analog Switch

FN3123
Rev.4.00
September 2004

The HI-201HS is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. The integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

Fabricated using silicon-gate technology and the Intersil Dielectric Isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS can be found in Application Note AN543.)

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI1-0201HS-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0201HS-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0201HS-5	0 to 75	16 Ld CERDIP	F16.3
HI3-0201HS-5	0 to 75	16 Ld PDIP	E16.3
HI3-0201HS-5Z (See Note)	0 to 75	16 Ld PDIP (Pb-free)	E16.3
HI9P0201HS-5	0 to 75	16 Ld SOIC	M16.3
HI9P0201HS-5Z (See Note)	0 to 75	16 Ld SOIC (Pb-free)	M16.3
HI9P0201HS-9	-40 to 85	16 Ld SOIC	M16.3
HI9P0201HS-9Z (See Note)	-40 to 85	16 Ld SOIC (Pb-free)	M16.3

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Features

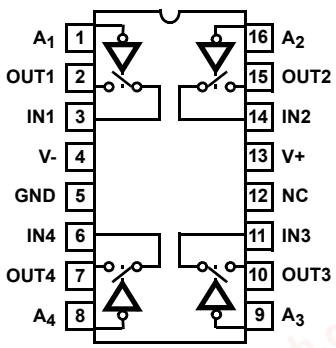
- Pb-free Available as an Option
- Fast Switching Times
  - t_{ON} 30ns
  - t_{OFF} 40ns
- Low “ON” Resistance 30Ω
- Pin Compatible with Standard HI-201
- Wide Analog Voltage Range (±15V Supplies) . . . . . ±15V
- Low Charge Injection (±15V Supplies) 10pC
- TTL Compatible
- Symmetrical Switching Analog Current Range 80mA

Applications

- High Speed Multiplexing
- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks
- Integrator Reset Circuits

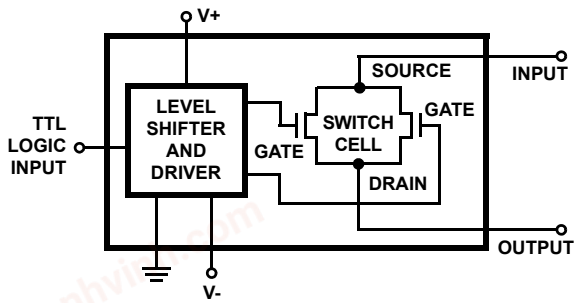
Pinout (Switches Shown For Logic “1” Input)

HI-201HS (CERDIP, PDIP, SOIC)
TOP VIEW



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Functional Diagram

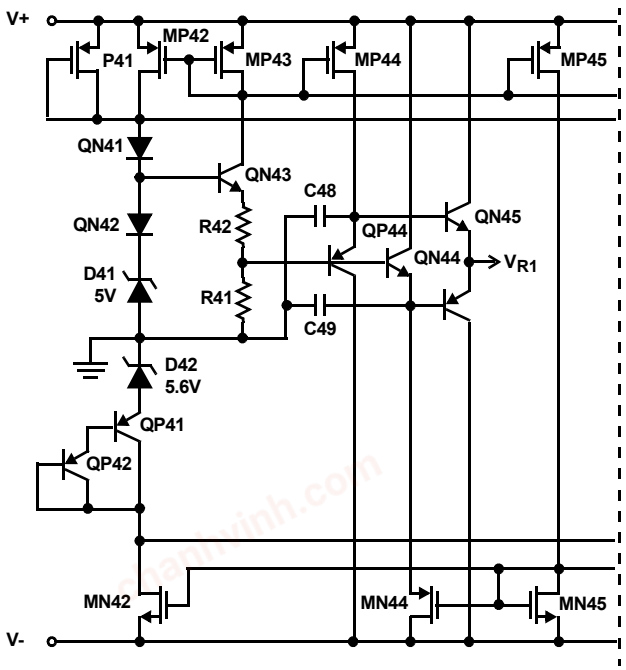


TRUTH TABLE

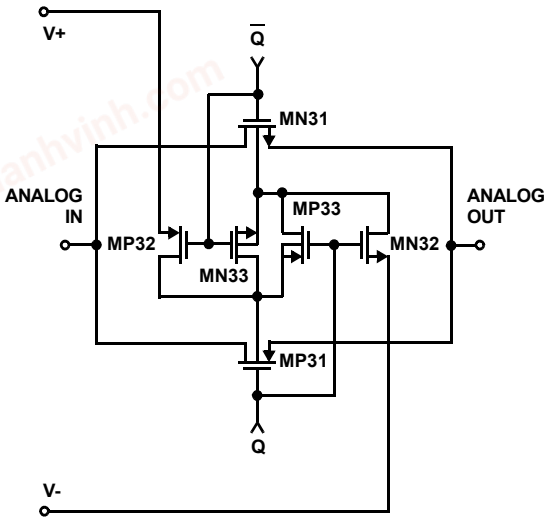
LOGIC	SWITCH
0	ON
1	OFF

Schematic Diagrams

TTL/CMOS REFERENCE CIRCUIT



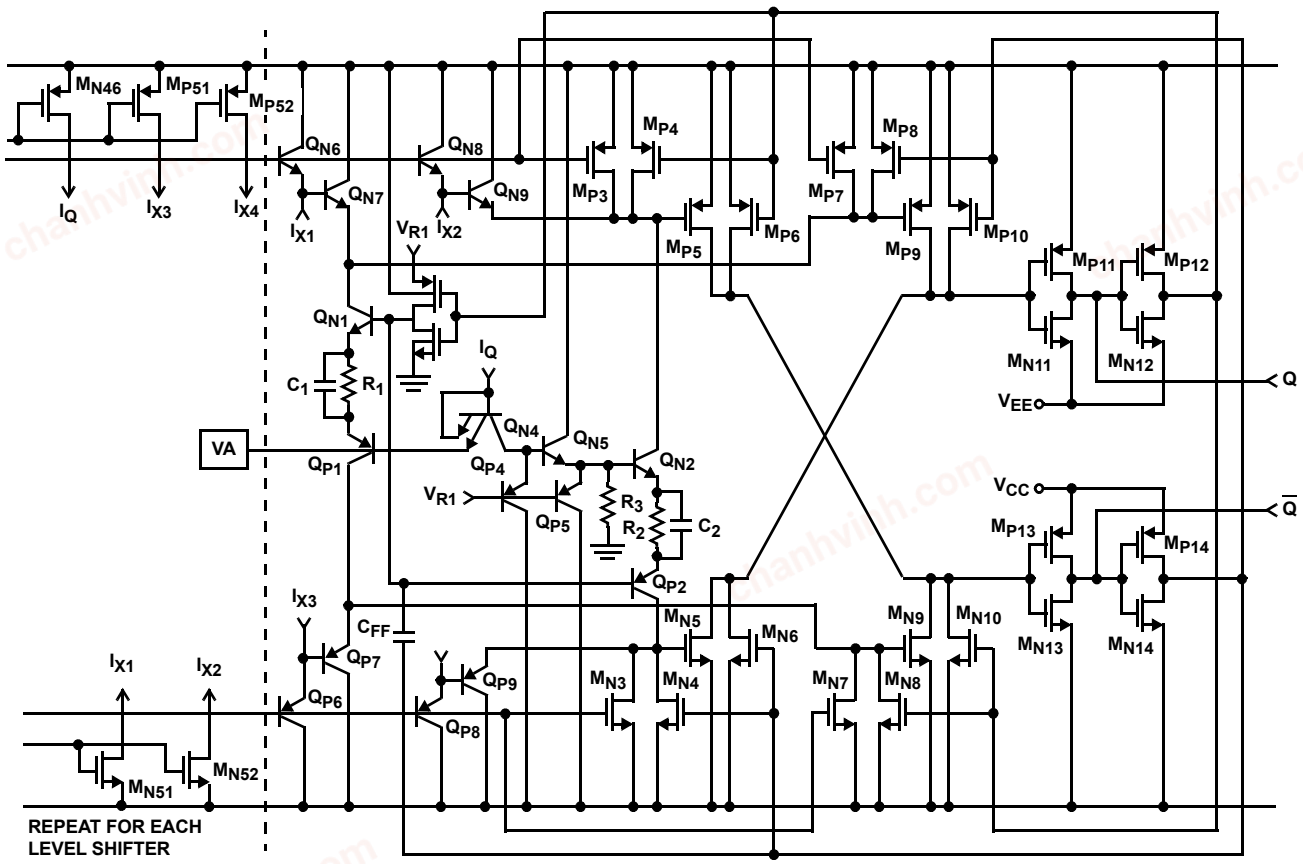
SWITCH CELL



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Schematic Diagrams (Continued)

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



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Absolute Maximum Ratings

Supply Voltage (V+ to V-) 36V
Digital Input Voltage . . . . . (V+) +4V to (V-) -4V
Analog Input Voltage (One Switch) . . . . . (V+) +2.0V to (V-) -2.0V
Peak Current, S or D (Pulse 1ms, 10% Duty Cycle Max) 50mA
Continuous Current Any Terminal (Except S or D) 25mA

Operating Conditions

Temperature Ranges
HI-201HS-2 . . . . . -55^oC to 125^oC
HI-201HS-4 . . . . . -25^oC to 85^oC
HI-201HS-5 . . . . . 0^oC to 75^oC
HI-201HS-9 . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	80	20
PDIP Package	90	N/A
SOIC Package	100	N/A

Maximum Junction Temperature
Ceramic Package . . . . . 175^oC
Plastic Package . . . . . 150^oC
Maximum Storage Temperature . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	-2			-4, -5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS									
Switch ON Time, t_{ON}	(Note 3)	25	-	30	50	-	30	50	ns
Switch OFF Time, t_{OFF1}	(Note 3)	25	-	40	50	-	40	50	ns
Switch OFF Time, t_{OFF2}	(Note 3)	25	-	150	-	-	150	-	ns
Output Settling Time	To 0.1%	25	-	180	-	-	180	-	ns
Charge Injection, Q	(Note 6)	25	-	10	-	-	10	-	pC
OFF Isolation	(Note 4)	25	-	72	-	-	72	-	dB
Crosstalk	(Note 5)	25	-	86	-	-	86	-	dB
Input Switch Capacitance, $C_{S(OFF)}$		25	-	10	-	-	10	-	pF
Output Switch Capacitance $C_{D(OFF)}$		25	-	10	-	-	10	-	pF
Output Switch Capacitance $C_{D(ON)}$		25	-	30	-	-	30	-	pF
Digital Input Capacitance, C_A		25	-	18	-	-	18	-	pF
Drain-To-Source Capacitance, $C_{DS(OFF)}$		25	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH}		25	2.0	-	-	2.0	-	-	V
		Full	2.4	-	-	2.4	-	-	V
Input Leakage Current (Low), I_{AL}		25	-	200	-	-	200	-	µA
		Full	-	-	500	-	-	500	µA
Input Leakage Current (High), I_{AH}	V_{AH} = 4.0V	25	-	20	-	-	20	-	µA
		Full	-	-	40	-	-	40	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
ON Resistance, r_{ON}	(Note 2)	25	-	30	50	-	30	50	Ω
		Full	-	-	75	-	-	75	Ω

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Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	-2			-4, -5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
r_{ON} Match		25	-	3	-	-	3	-	%
OFF Input Leakage Current, $I_{S(OFF)}$		25	-	0.3	10	-	0.3	10	nA
		Full	-	-	100	-	-	50	nA
OFF Output Leakage Current, $I_{D(OFF)}$		25	-	0.3	10	-	0.3	10	nA
		Full	-	-	100	-	-	50	nA
ON Leakage Current, $I_{D(ON)}$		25	-	0.1	10	-	0.1	10	nA
		Full	-	-	100	-	-	50	nA
POWER SUPPLY CHARACTERISTICS (Note 7)									
Power Dissipation, P_D		25	-	120	-	-	120	-	mW
		Full	-	-	240	-	-	240	mW
Current, I+ (Pin 13)		25	-	4.5	-	-	4.5	-	mA
		Full	-	-	10.0	-	-	10.0	mA
Current, I- (Pin 4)		25	-	3.5	-	-	3.5	-	mA
		Full	-	-	6	-	-	6	mA

NOTES:

2. $V_{OUT} = \pm 10V$, $I_{OUT} = 1mA$.
3. $R_L = 1k\Omega$, $C_L = 35pF$, $V_{IN} = +10V$, $V_A = +3V$. (See Figure 1).
4. $V_A = 3V$, $R_L = 1k\Omega$, $C_L = 10pF$, $V_{IN} = 3V_{RMS}$, f = 100kHz.
5. $V_A = 3V$, $R_L = 1k\Omega$, $V_{IN} = 3V_{RMS}$, f = 100kHz.
6. $C_L = 1nF$, $V_{IN} = 0V$, $Q = C_L \times \Delta V_O$.
7. $V_A = 3V$ or $V_A = 0$ for all switches.

Test Circuits and Waveforms

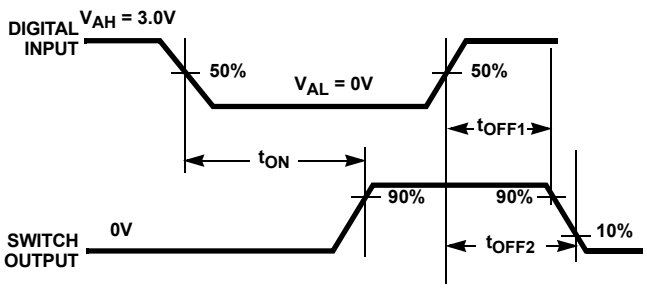
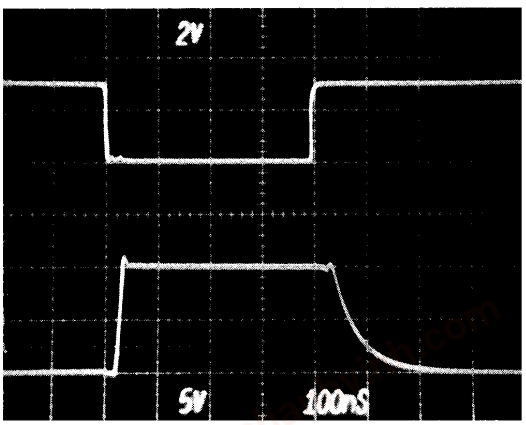


FIGURE 1A. MEASUREMENT POINTS



TOP: Logic Input (2V/Div.) BOTTOM: Output (5V/Div.)
HORIZONTAL: 100ns/Div.

FIGURE 1B. WAVEFORMS

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Test Circuits and Waveforms (Continued)

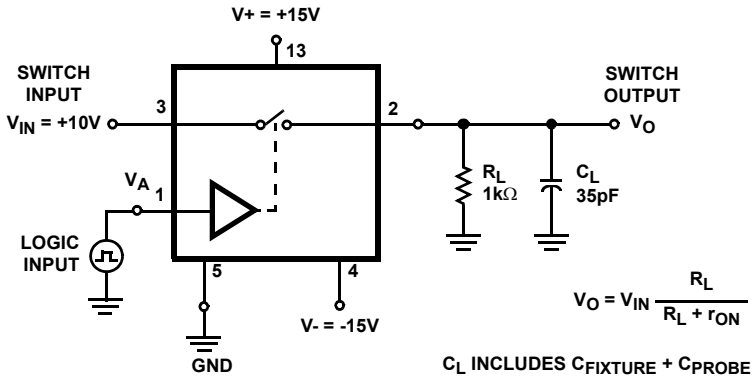


FIGURE 1C. TEST CIRCUIT

FIGURE 1. SWITCH t_{ON} AND t_{OFF}

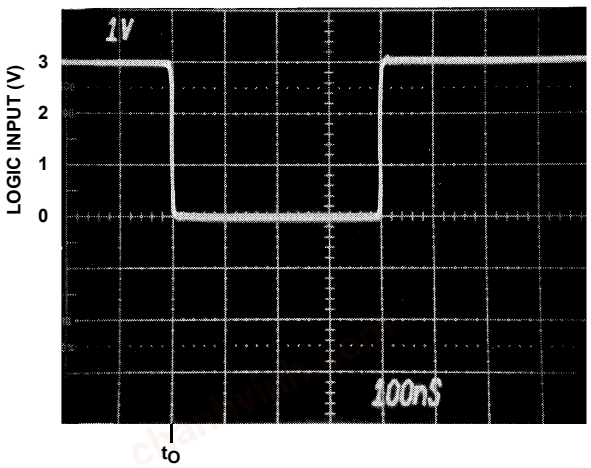


FIGURE 2A. LOGIC INPUT WAVEFORM

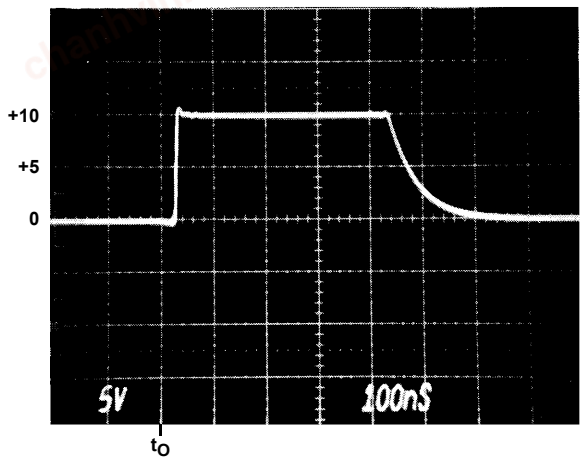


FIGURE 2B. V_{IN} = +10V

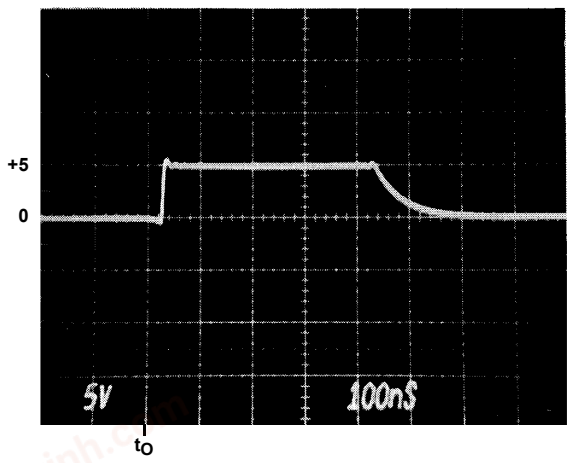


FIGURE 2C. V_{IN} = +5V

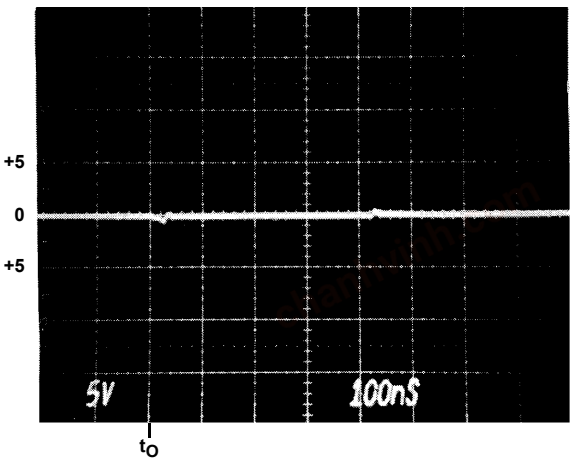


FIGURE 2D. V_{IN} = 0V

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Test Circuits and Waveforms (Continued)

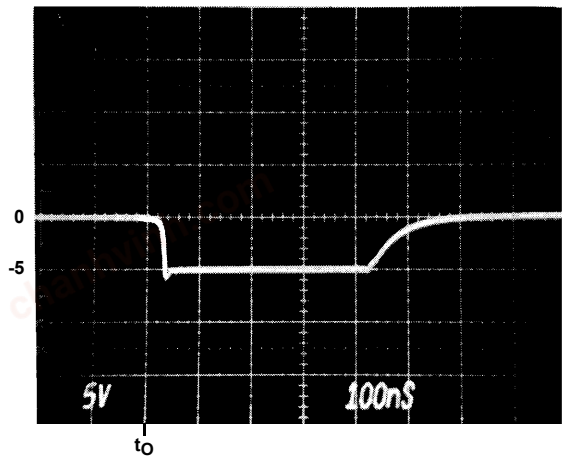


FIGURE 2E. V_{IN} = -5V

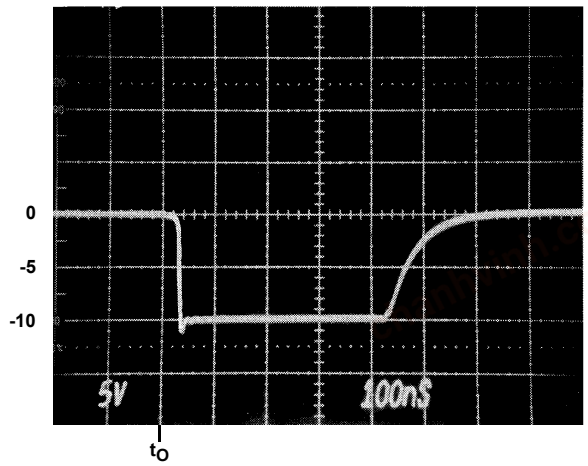


FIGURE 2F. V_{IN} = -10V

FIGURE 2. SWITCHING WAVEFORMS FOR VARIOUS ANALOG INPUT VOLTAGES

Application Information

Logic Compatibility

The HI-201HS is TTL compatible. Its logic inputs (pins 1, 8, 9, and 16) are designed to react to digital inputs which exceed a fixed, internally generated TTL switching threshold. The HI-201HS can also be driven with CMOS logic (0V-15V), although the switch performance with CMOS logic will be inferior to that with TTL logic (0V-5V).

The logic input design of the HI-201HS is largely responsible for its fast switching speed. It is a design which features a unique input stage consisting of complementary vertical PNP and NPN bipolar transistors. This design differs from that of the standard HI-201 product where the logic inputs are MOS transistors.

Although the new logic design enhances the switching speed performance, it also increases the logic input leakage currents. Therefore, the HI-201HS will exhibit larger digital input leakage currents in comparison to the standard HI-201 product.

Charge Injection

Charge injection is the charge transferred, through the internal gate-to-channel capacitances, from the digital logic input to the analog output. To optimize charge injection performance for the HI-201HS, it is advisable to provide a TTL logic input with fast rise and fall times.

If the power supplies are reduced from ±15V, charge injection will become increasingly dependent upon the digital input frequency. Increased logic input frequency will result in larger output error due to charge injection.

Power Supply Considerations

The electrical characteristics specified in this data sheet are guaranteed for power supplies V_S = ±15V. Power supply voltages less than ±15V will result in reduced switch performance. The following information is intended as a design aid only.

POWER SUPPLY VOLTAGES	SWITCH PERFORMANCE
$\pm 12 \le V_S \le \pm 15V$	Minimal Variation
$V_S < \pm 12V$	Parametric variation becomes increasingly large (increased ON resistance, longer switching times).
$V_S < \pm 10V$	Not Recommended.
$V_S > \pm 16V$	Not Recommended.

Single Supply

The switch operation of the HI-201HS is dependent upon an internally generated switching threshold voltage optimized for ±15V power supplies. The HI-201HS does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels (±15V). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

For further information see Application Notes AN520, AN521, AN531, AN532, AN543 and AN557.

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Typical Performance Curves

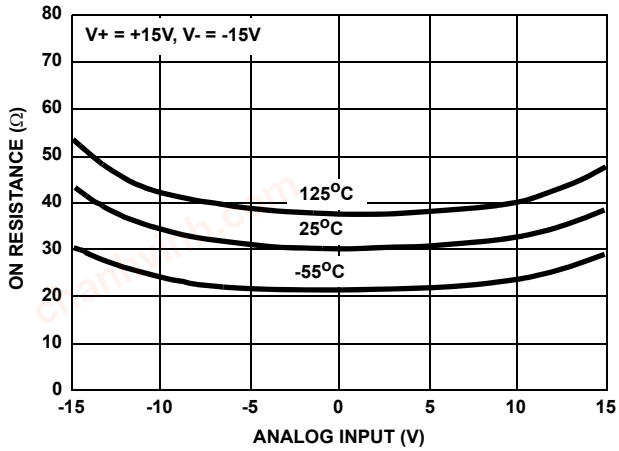


FIGURE 3. ON RESISTANCE vs ANALOG SIGNAL LEVEL

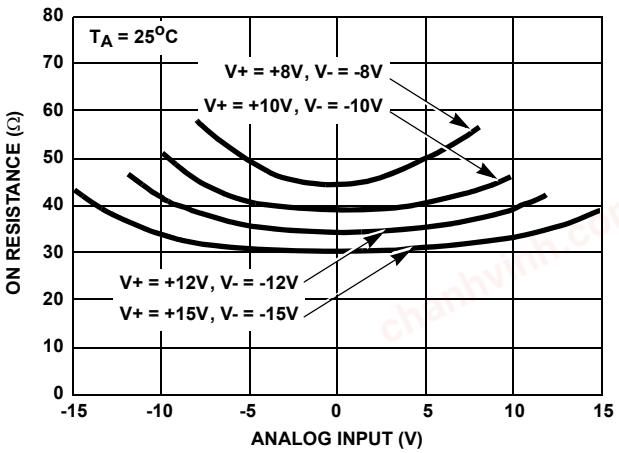


FIGURE 4. ON RESISTANCE vs ANALOG SIGNAL LEVEL

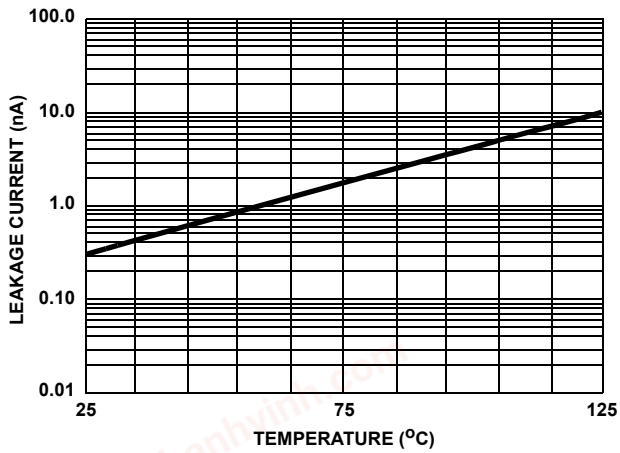


FIGURE 5. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE †

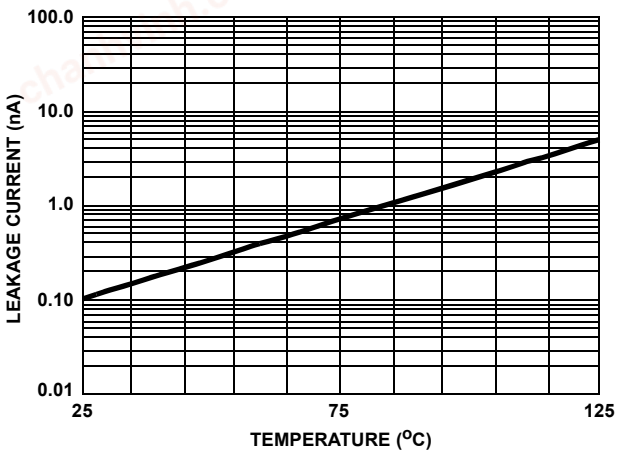


FIGURE 6. $I_{D(ON)}$ vs TEMPERATURE †

† Theoretically, leakage current will continue to decrease below 25°C. But due to environmental conditions, leakage measurements below this temperature are not representative of actual switch performance.

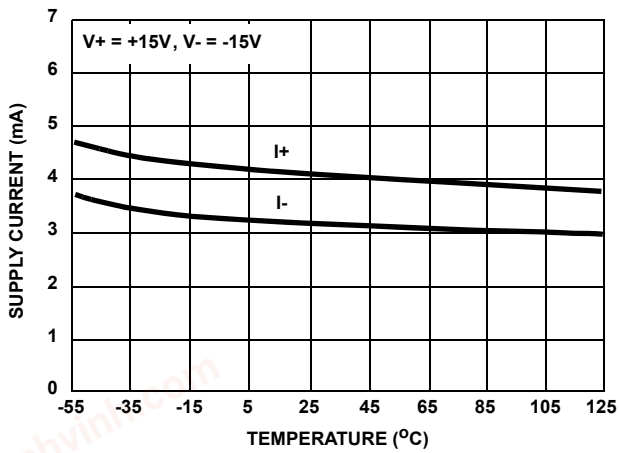


FIGURE 7. SUPPLY CURRENT vs TEMPERATURE

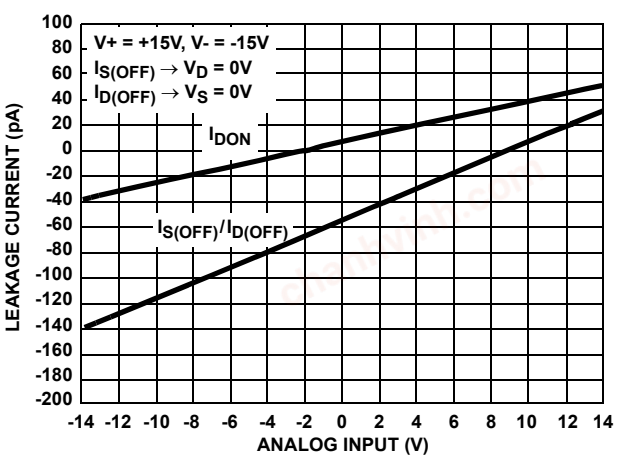


FIGURE 8. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

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Typical Performance Curves (Continued)

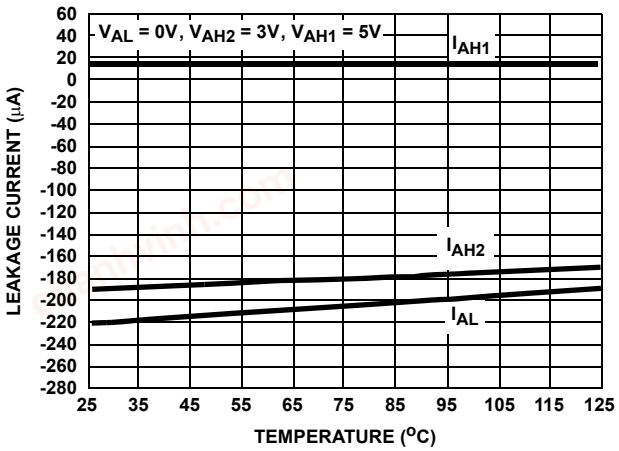


FIGURE 9. DIGITAL INPUT LEAKAGE CURRENT vs TEMPERATURE †

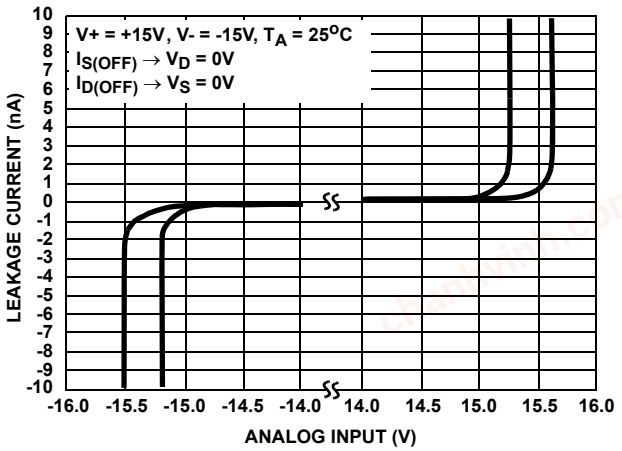


FIGURE 10. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

† Theoretically, leakage current will continue to decrease below 25°C. But due to environmental conditions, leakage measurements below this temperature are not representative of actual switch performance.

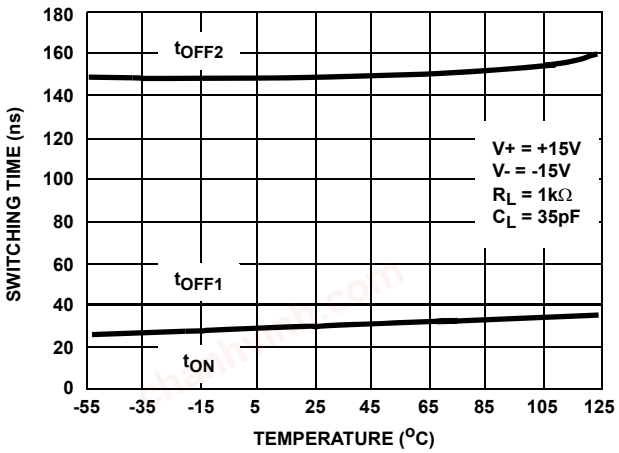


FIGURE 11. SWITCHING TIME vs TEMPERATURE

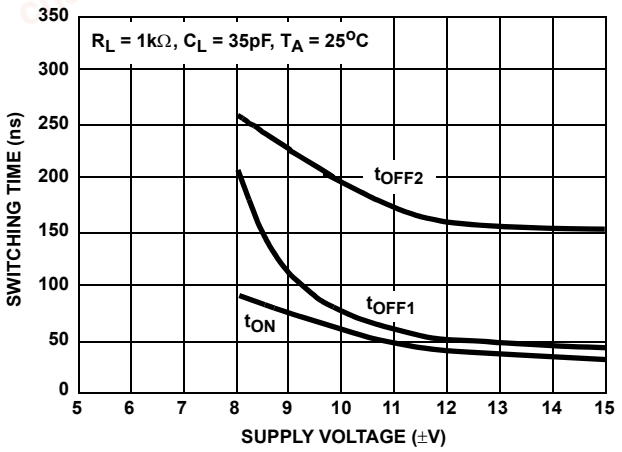


FIGURE 12. SWITCHING TIME vs SUPPLY VOLTAGE

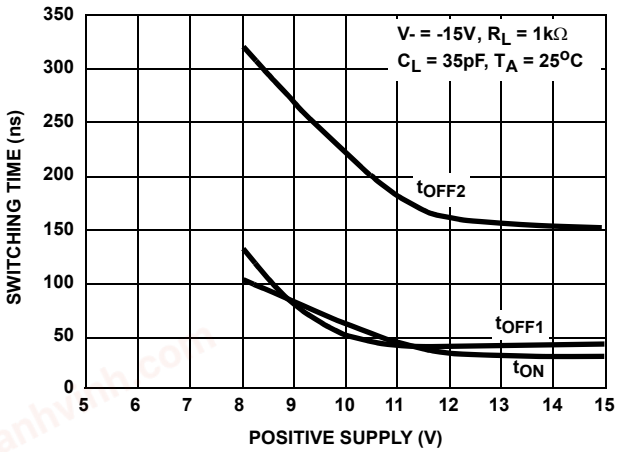


FIGURE 13. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

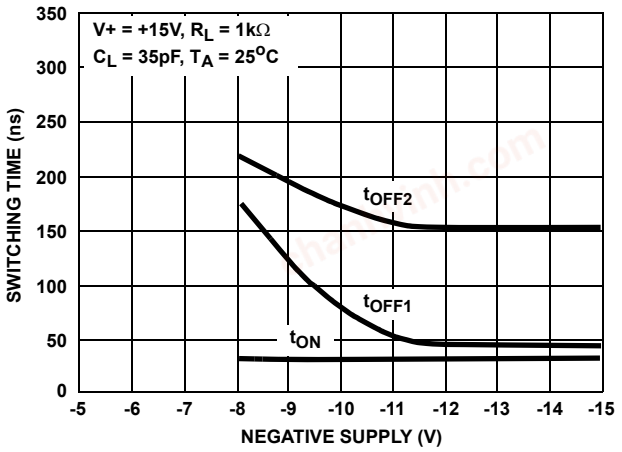


FIGURE 14. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

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Typical Performance Curves (Continued)

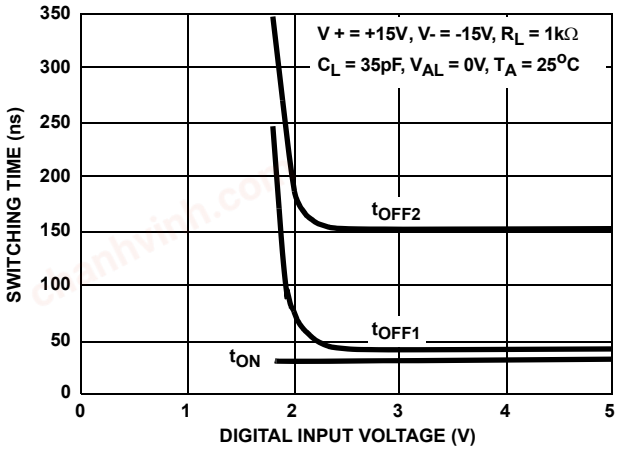


FIGURE 15. SWITCHING TIME vs INPUT LOGIC VOLTAGE

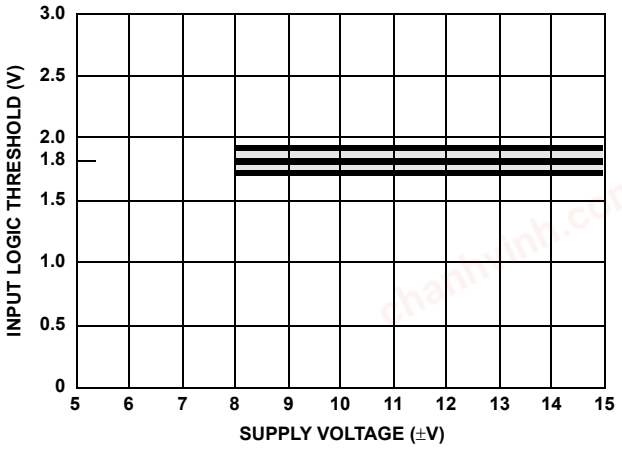


FIGURE 16. INPUT SWITCHING THRESHOLD vs SUPPLY VOLTAGE

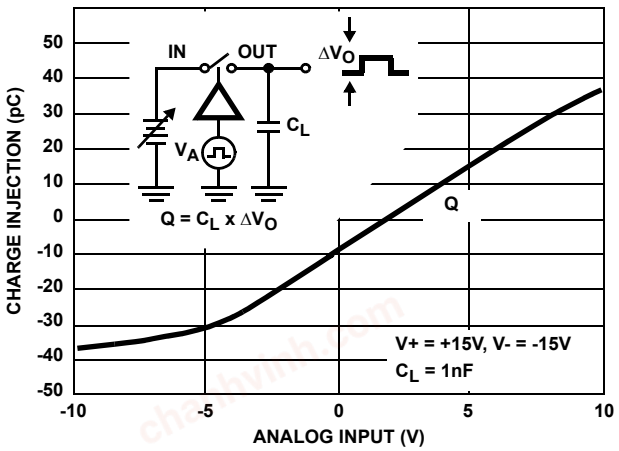


FIGURE 17. CHARGE INJECTION vs ANALOG VOLTAGE

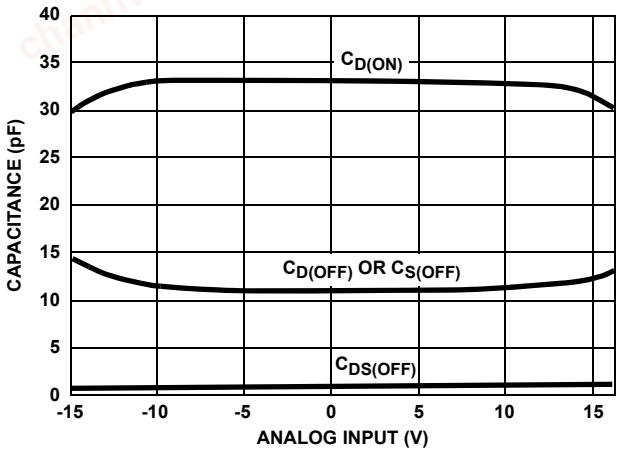


FIGURE 18. CAPACITANCE vs ANALOG VOLTAGE

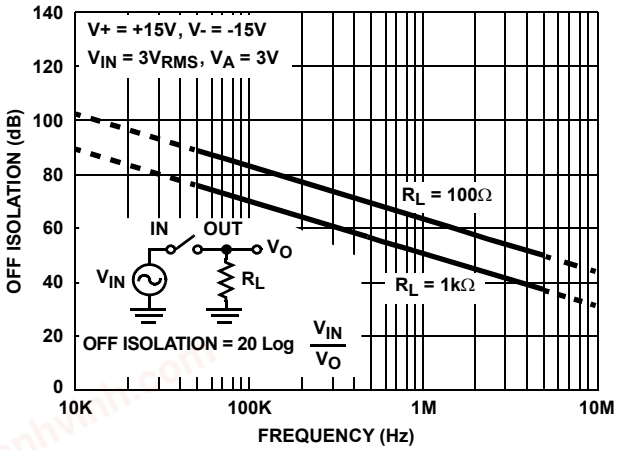


FIGURE 19. OFF ISOLATION vs FREQUENCY

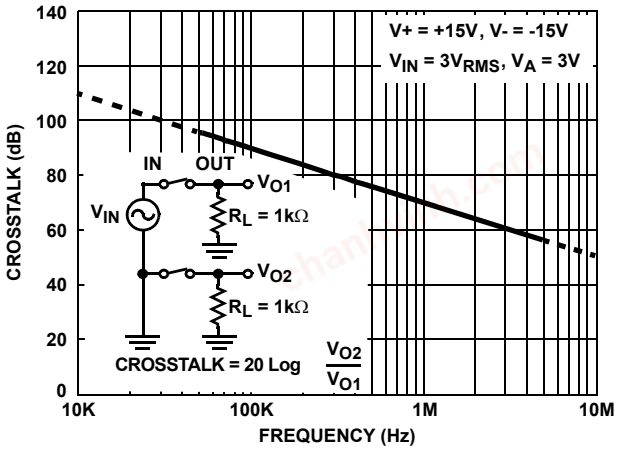


FIGURE 20. CROSSTALK vs FREQUENCY

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Die Characteristics

DIE DIMENSIONS

2440µm x 2860µm x 485µm

METALLIZATION

Type: CuAl
Thickness: 16kÅ ±2kÅ

PASSIVATION

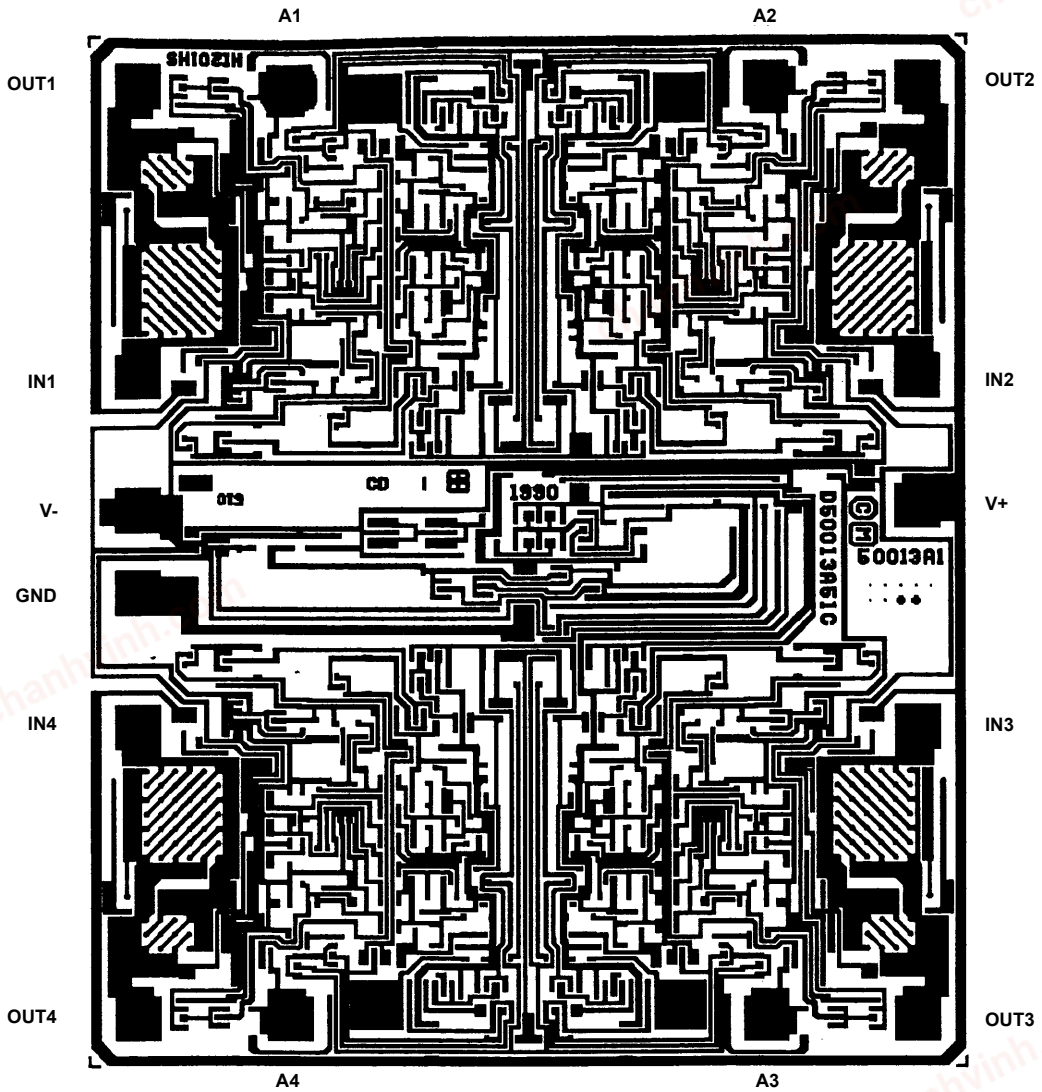
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY

9.5×10^4 A/cm^2

Metallization Mask Layout

HI-201HS



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