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RENESAS

DATASHEET

DG444, DG445

Monolithic, Quad SPST, CMOS Analog Switches

FN3586
Rev 10.00
Jun 4, 2007

The DG444 and DG445 monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole single throw (SPST) analog switches and TTL and CMOS compatible digital inputs.

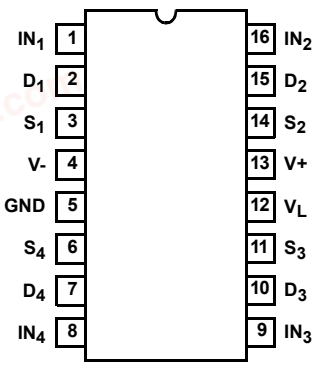
These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} <250ns) compared to the DG211 and DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG444 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling ±20V signals when operating with ±20V power supplies.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG444 and DG445 are identical, differing only in the polarity of the selection logic.

Pinout

DG444, DG445
(16 LD SOIC, TSSOP)
TOP VIEW



Features

- ON Resistance (Max) 85Ω
- Low Power Consumption (P_D) . . . . . <35µW
- Fast Switching Action
  - t_{ON} (Max) 250ns
  - t_{OFF} (Max, DG444) 140ns
- Low Charge Injection
- Upgrade from DG211, DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Ordering Information

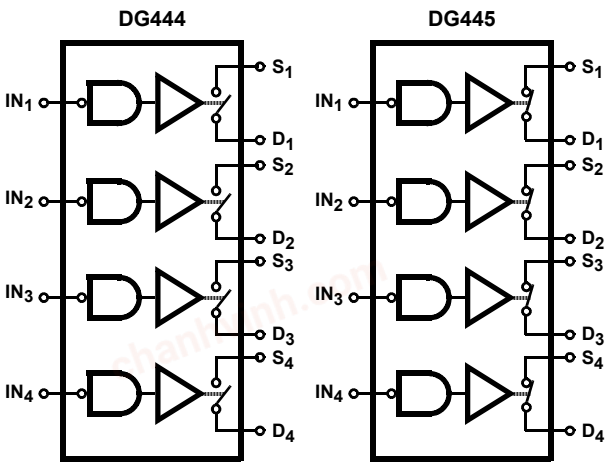
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
DG444DY*	DG444DY	-40 to +85	16 Ld SOIC	M16.15
DG444DYZ* (Note)	DG444DYZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
DG444DVZ* (Note)	DG444DVZ	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173
DG445DY*	DG445DY	-40 to +85	16 Ld SOIC	M16.15
DG445DYZ* (Note)	DG445DYZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
DG445DVZ* (Note)	DG445DVZ	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173

*Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

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Functional Diagrams



SWITCHES SHOWN FOR LOGIC "1" INPUT

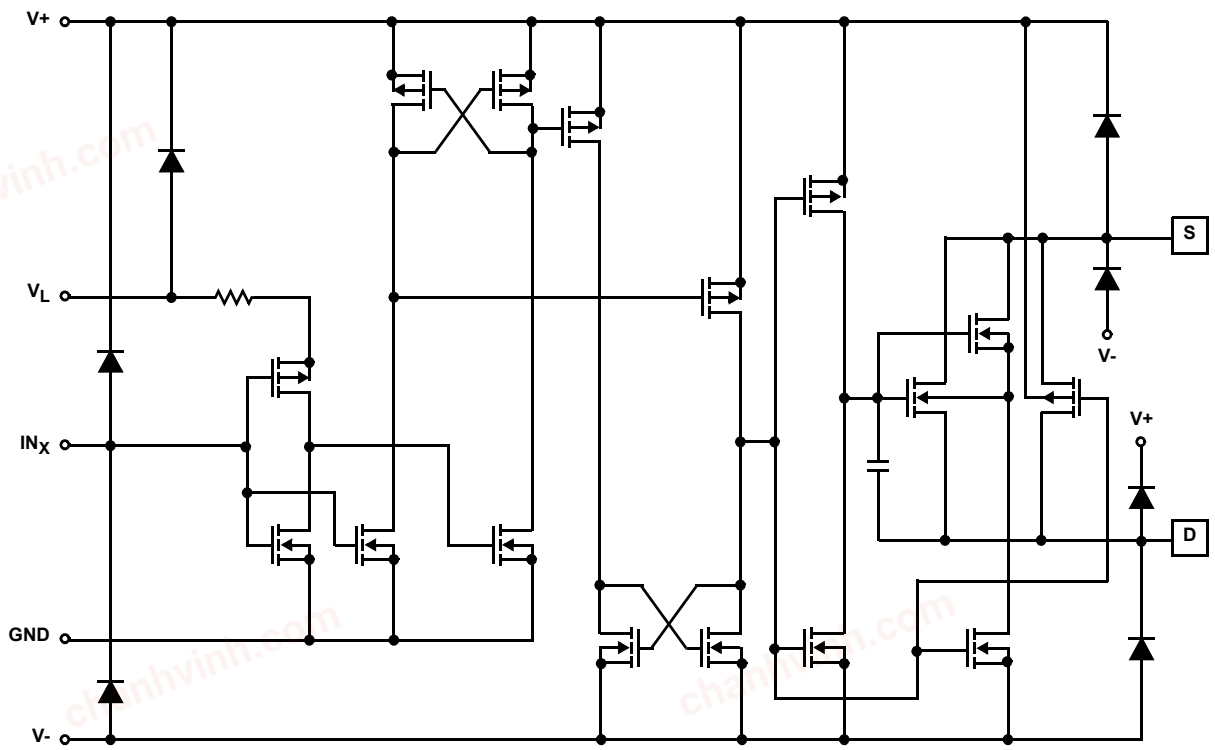
TRUTH TABLE

LOGIC	V_{IN}	DG444	DG445
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	V_L	Logic Reference Voltage
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

Schematic Diagram (One Channel)



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Absolute Maximum Ratings

V+ to V- 44V
GND to V-. 25V
V_L. . . . . (GND - 0.3V) to (V+) + 0.3V
Digital Inputs, V_S, V_D (Note 1). . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) . . 100mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	115
TSSOP Package	150

Maximum Junction Temperature (Plastic Packages). . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Voltage Range . . . . . ±20V (Max)
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time . . . . . ≤20ns

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V (Figure 1)	+25	-	120	250	ns
Turn-OFF Time, t_{OFF}						
DG444		+25	-	110	140	ns
DG445		+25	-	160	210	ns
Charge Injection, Q (Figure 2)	C_L = 1nF, V_G = 0V, R_G = 0Ω	+25	-	-1	-	pC
OFF Isolation (Figure 4)	R_L = 50Ω, C_L = 5pF, f = 1MHz	+25	-	60	-	dB
Crosstalk (Channel-to-Channel) (Figure 3)		+25	-	-100	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz, V_{ANALOG} = 0 (Figure 5)	+25	-	4	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$		+25	-	4	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$		+25	-	16	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = ∓10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	+25	-	50	85	Ω
		Full	-	-	100	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	+25	-0.5	0.01	0.5	nA
		+85	-5	-	5	nA

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Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
Drain OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	+25	-0.5	0.01	0.5	nA
		+85	-5	-	5	nA
Channel ON Leakage Current, $I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_S = V_D, = ±15.5V	+25	-0.5	0.08	0.5	nA
		+85	-10	-	10	nA
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	+25	-	0.001	1	µA
		+85	-	-	5	µA
Negative Supply Current, I-		+25	-1	-0.0001	-	µA
		+85	-5	-	-	µA
Logic Supply Current, I_L		+25	-	0.001	1	µA
		+85	-	-	5	µA
Ground Current, I_{GND}		+25	-1	-0.001	-	µA
		+85	-5	-	-	µA

Electrical Specifications

(Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = 8V (Figure 1)	+25	-	300	450	ns
Turn-OFF Time, t_{OFF}		+25	-	60	200	ns
Charge Injection, Q (Figure 2)	C_L = 1nF, V_G = 6V, R_G = 0Ω	+25	-	2	-	pC
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = -10mA, V_D = 3V, 8V V+ = 10.8V, V_L = 5.25V	+25	-	100	160	Ω
		Full	-	-	200	Ω
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13.2V, V_{IN} = 0V or 5V, V_L = 5.25V	+25	-	0.001	1	µA
		Full	-	-	5	µA
Negative Supply Current, I-		+25	-1	-0.0001	-	µA
		Full	-5	-	-	µA
Logic Supply Current, I_L		+25	-	0.001	1	µA
		Full	-	-	5	µA
Ground Current, I_{GND}		+25	-1	-0.001	-	µA
		Full	-5	-	-	µA

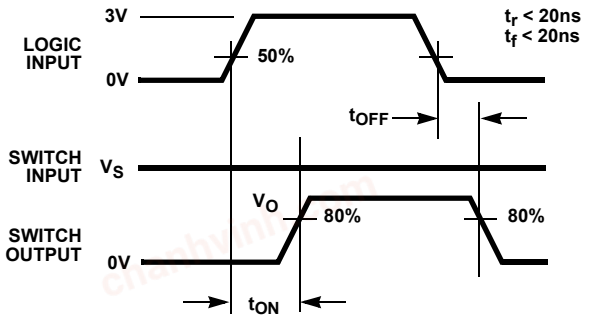
NOTES:

3. V_{IN} = input voltage to perform proper function.
4. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
5. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

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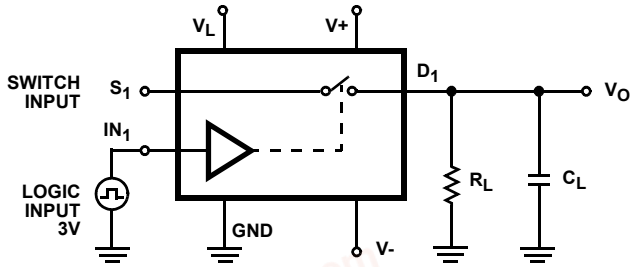
Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications. C_L includes fixture and stray capacitance.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

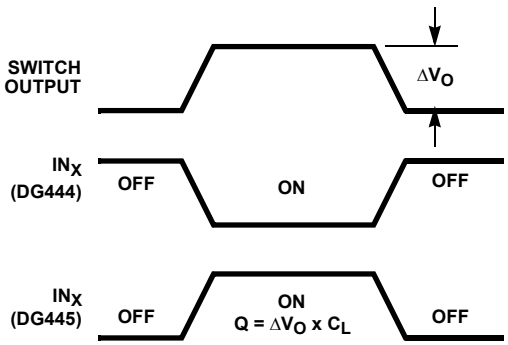


FIGURE 2A. MEASUREMENT POINTS

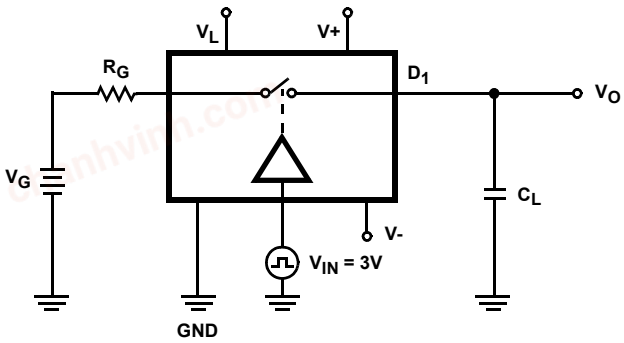


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

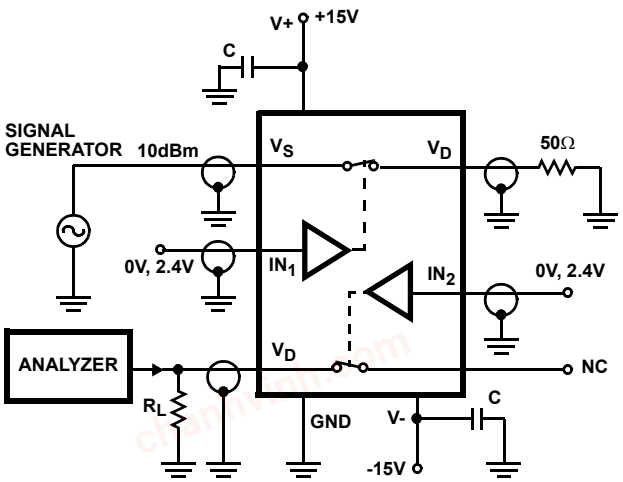


FIGURE 3. CROSSTALK TEST CIRCUIT

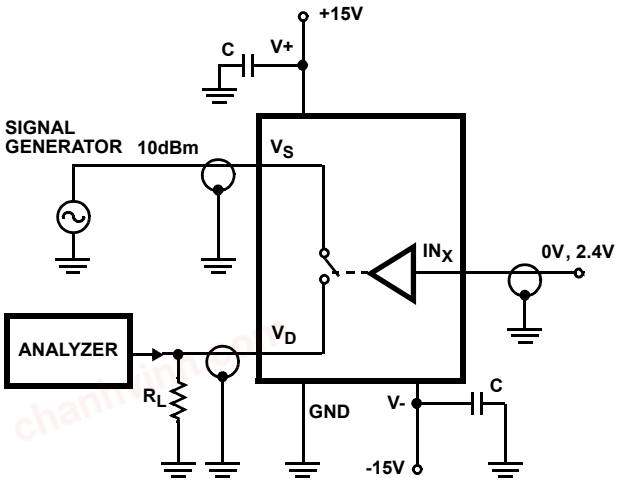


FIGURE 4. OFF ISOLATION TEST CIRCUIT

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Test Circuits and Waveforms (Continued)

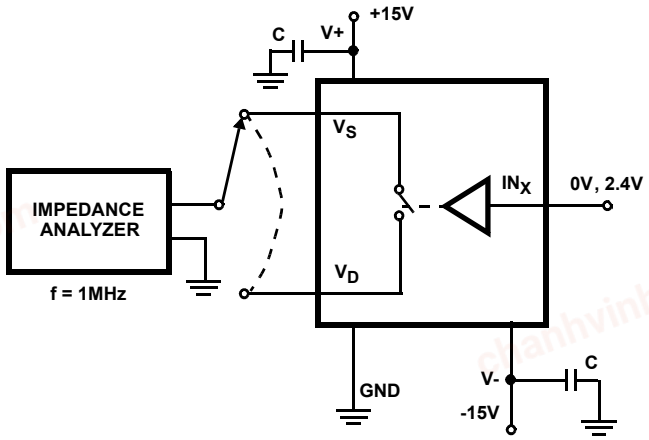
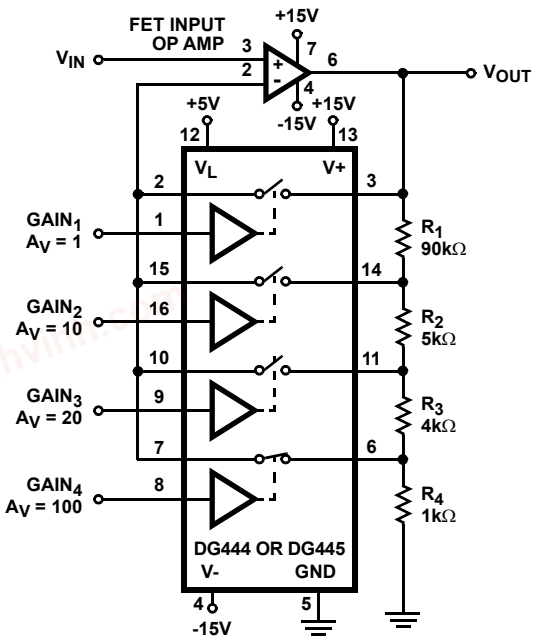


FIGURE 5. SOURCE/DRAIN CAPACITANCES TEST CIRCUIT

Application Information



GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE, OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OF CIRCUIT

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

WITH SW_4 CLOSED

FIGURE 6. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

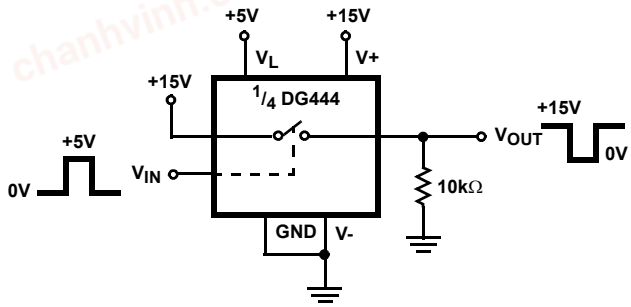


FIGURE 7. LEVEL SHIFTER

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Typical Performance Curves

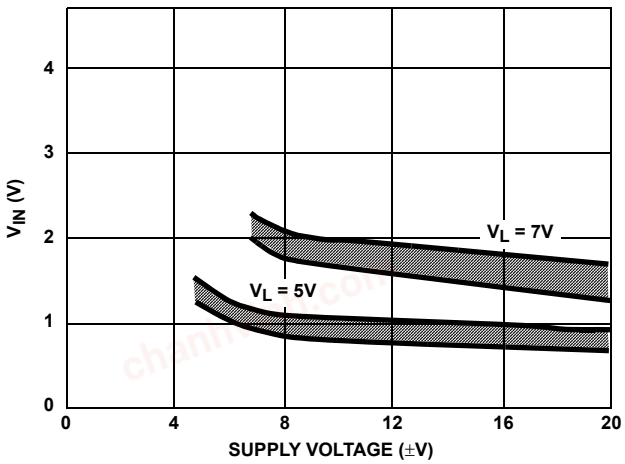


FIGURE 8. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

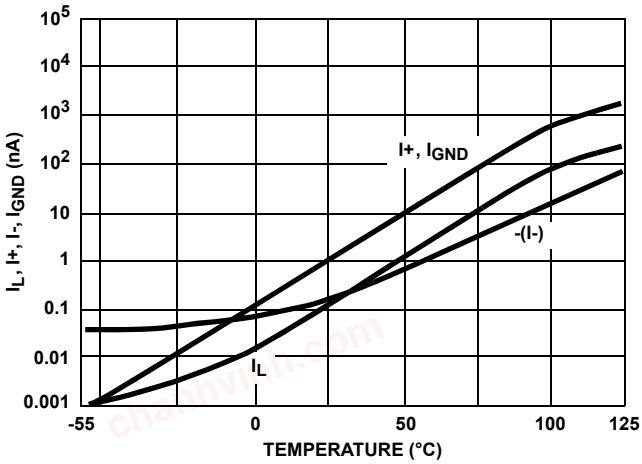


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE

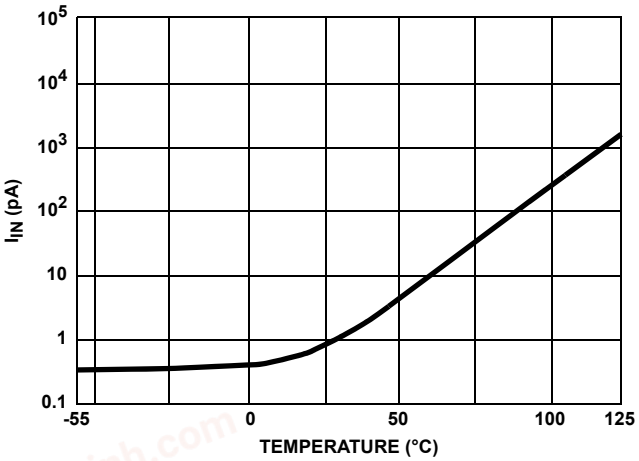


FIGURE 10. INPUT CURRENT vs TEMPERATURE

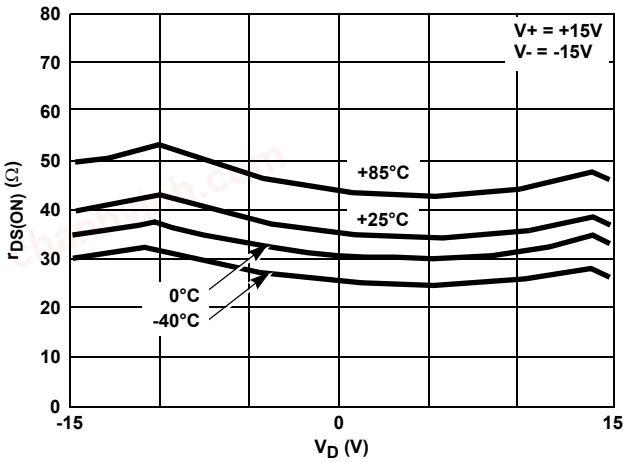


FIGURE 11. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

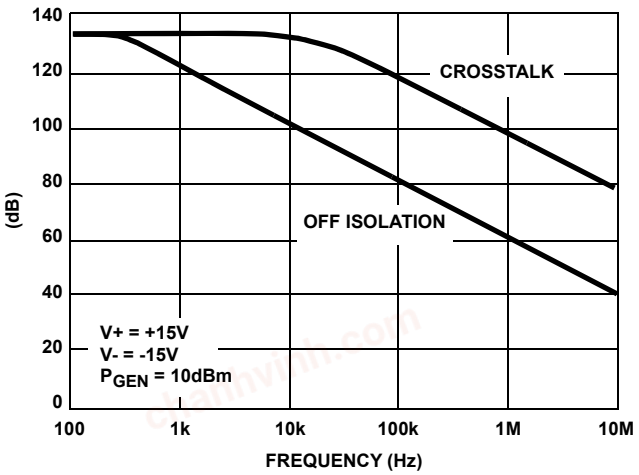


FIGURE 12. CROSSTALK REJECTION AND OFF ISOLATION vs FREQUENCY

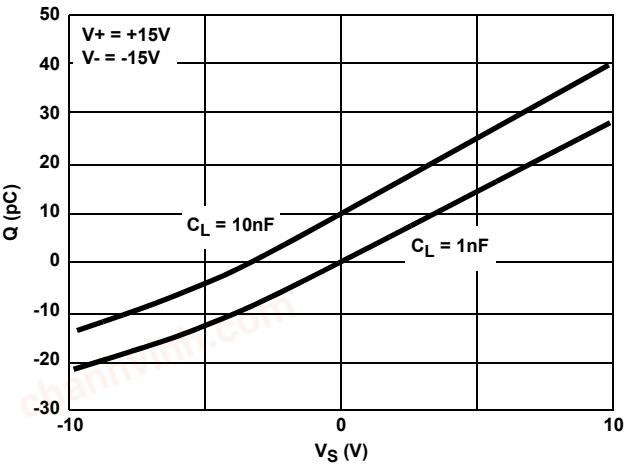


FIGURE 13. CHARGE INJECTION vs SOURCE VOLTAGE

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Typical Performance Curves (Continued)

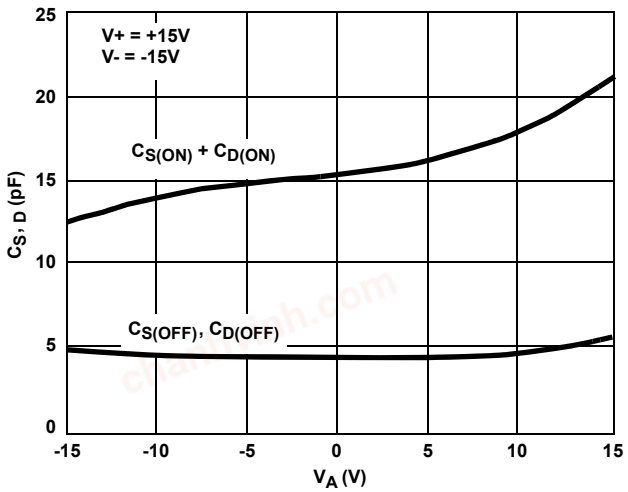


FIGURE 14. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

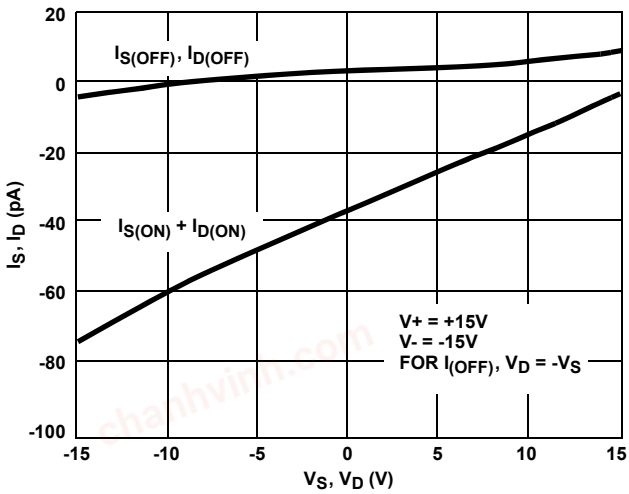


FIGURE 15. LEAKAGE CURRENTS vs ANALOG VOLTAGE

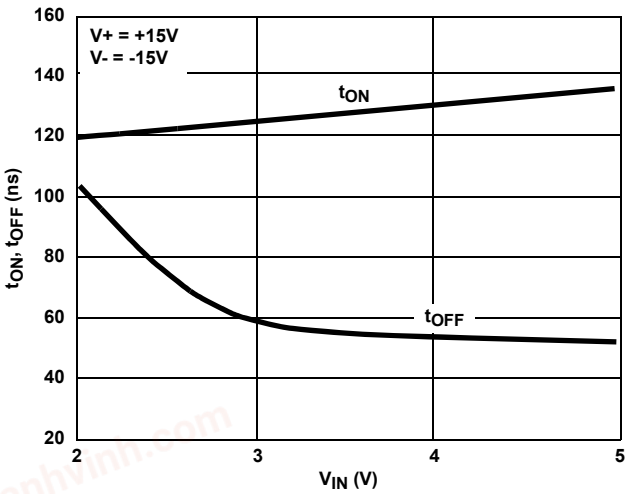


FIGURE 16. SWITCHING TIME vs INPUT VOLTAGE (DG444)

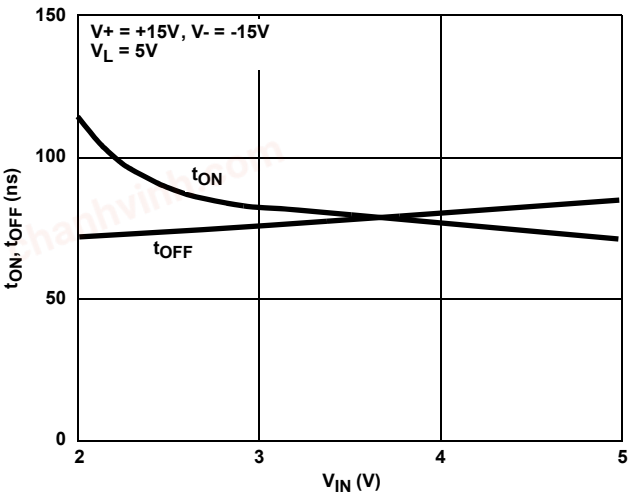


FIGURE 17. SWITCHING TIME vs INPUT VOLTAGE (DG445)

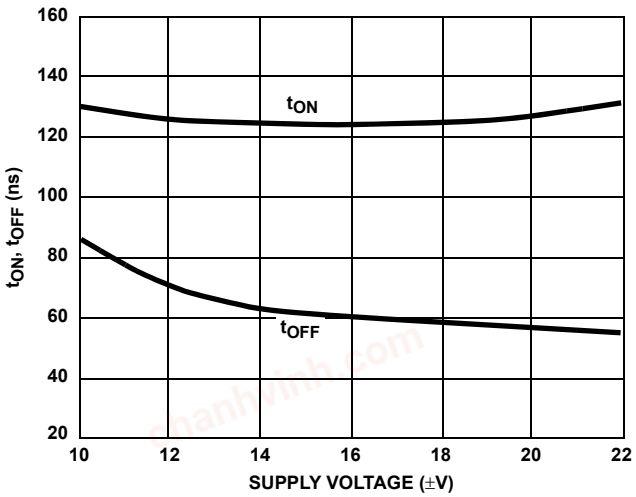


FIGURE 18. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG444)

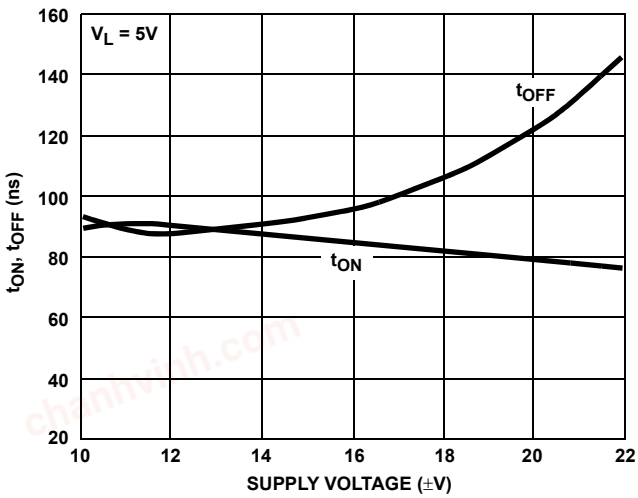


FIGURE 19. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG445)

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Typical Performance Curves (Continued)

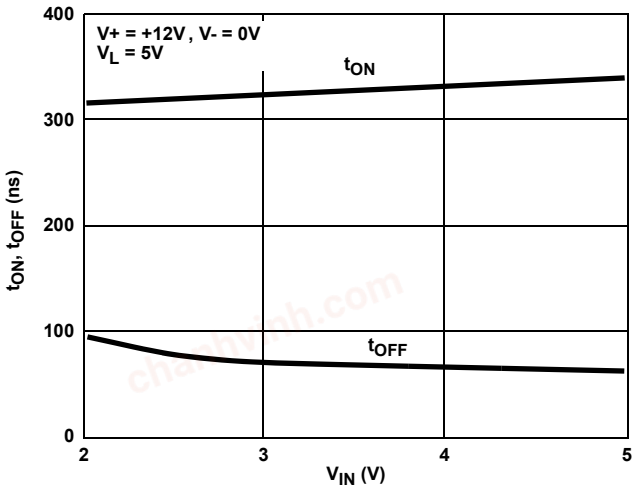


FIGURE 20. SWITCHING TIME vs INPUT VOLTAGE (DG444) (SINGLE 12V SUPPLY)

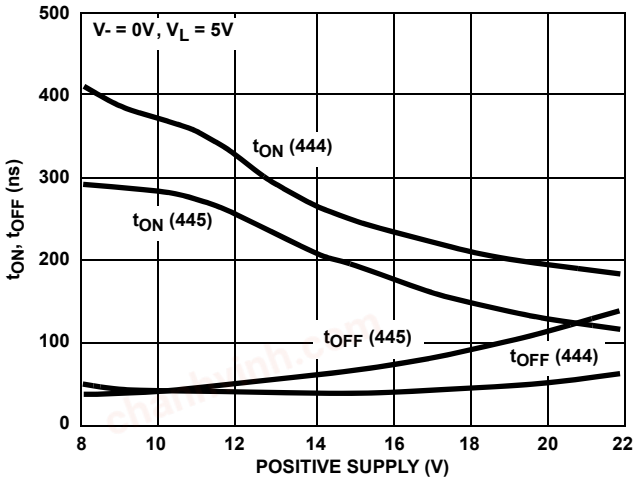


FIGURE 21. SWITCHING TIMES vs SINGLE SUPPLY VOLTAGE

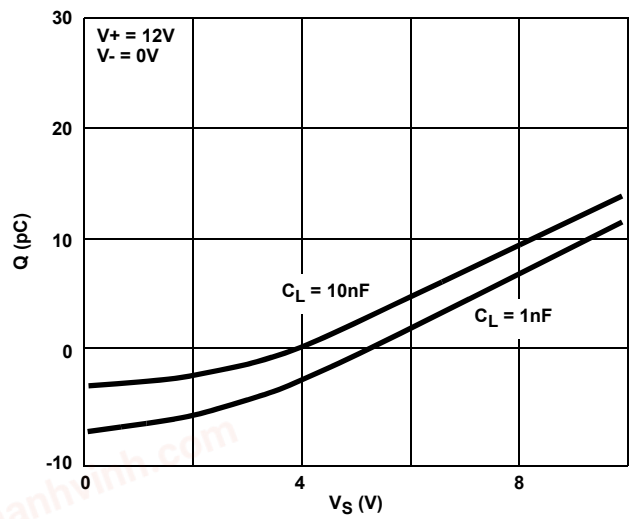


FIGURE 22. CHARGE INJECTION vs SOURCE VOLTAGE (SINGLE 12V SUPPLY)

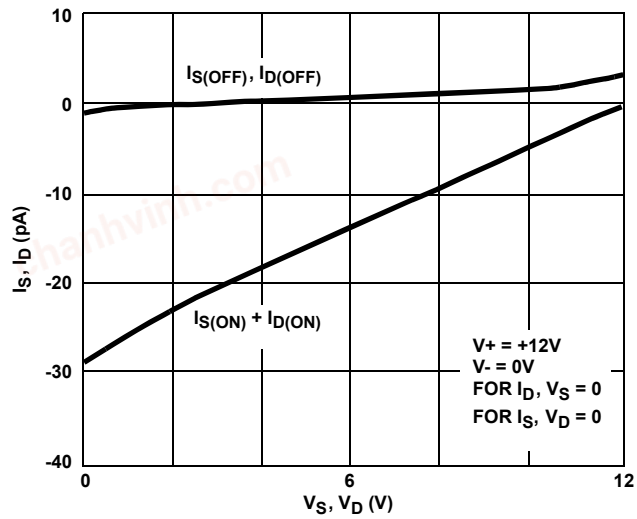


FIGURE 23. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

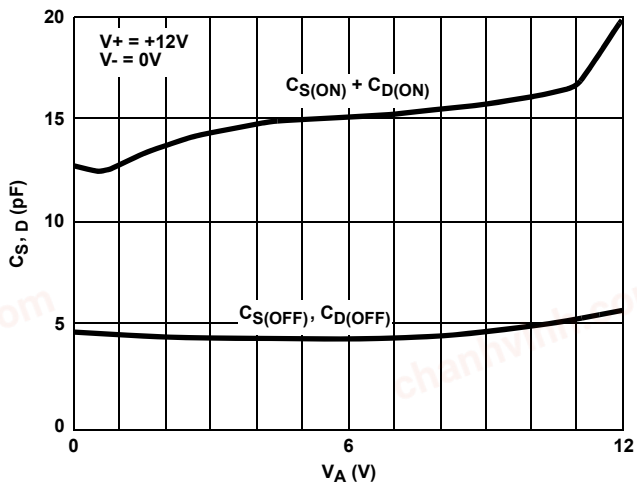


FIGURE 24. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

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Die Characteristics

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

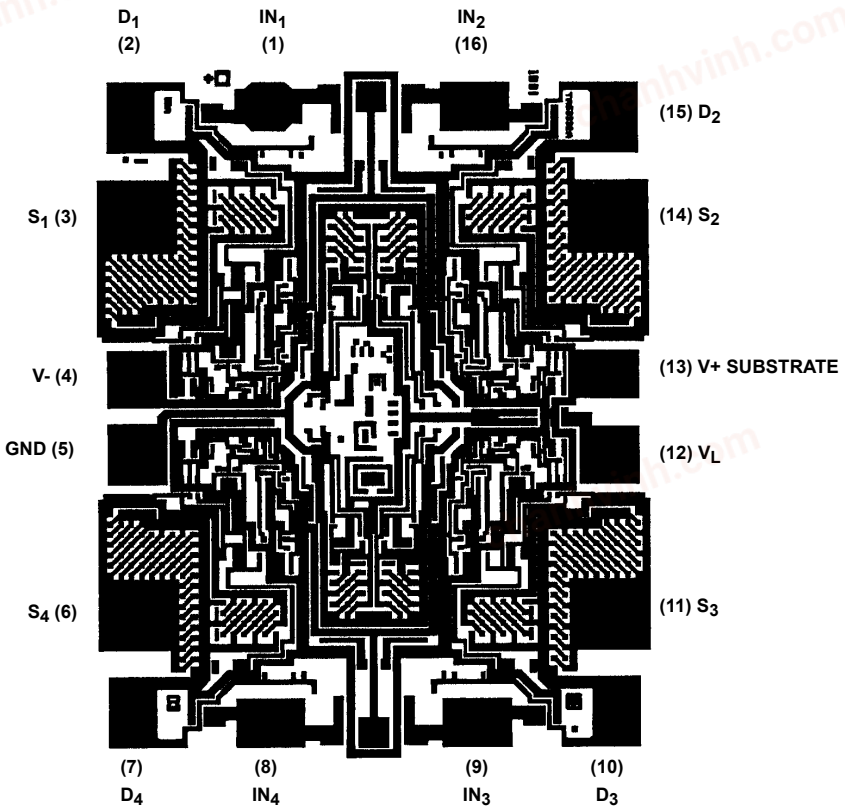
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

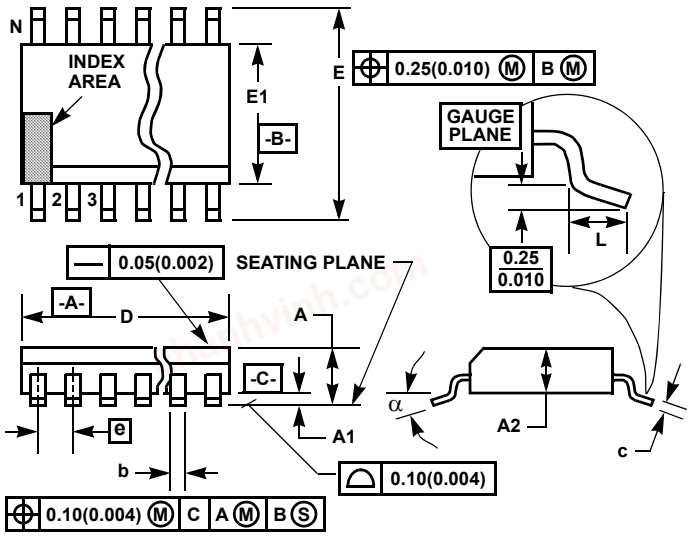
Metallization Mask Layout

DG444, DG445



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Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M16.173

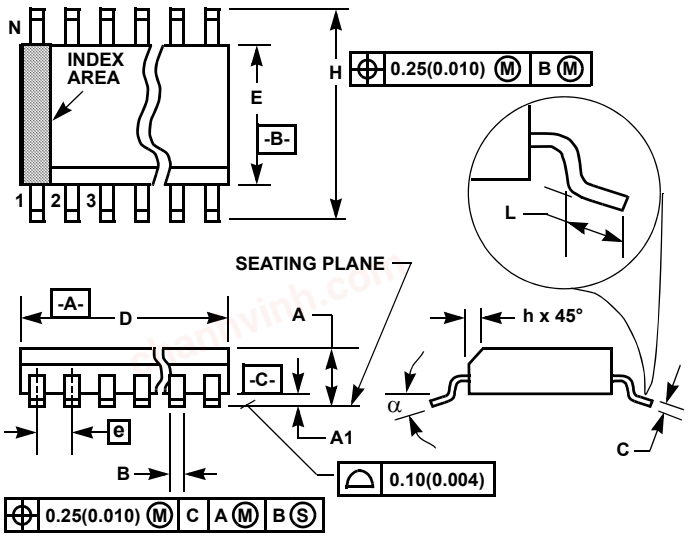
16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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