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RENESAS

DATASHEET

DG411, DG412, DG413

Monolithic Quad SPST, CMOS Analog Switches

FN3282
Rev 13.00
June 20, 2007

The DG411 series monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole throw (SPST) analog switches, and TTL and CMOS compatible digital inputs.

These switches feature lower analog ON-resistance (<35Ω) and faster switch time (t_{ON}<175ns) compared to the DG211 or DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG411 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 40V_{P-P} signals. Power supplies may be single-ended from +5V to 44V, or split from ±5V to ±20V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON-resistance variation with analog signals is quite low over a ±15V analog input range. The switches in the DG411 and DG412 are identical, differing only in the polarity of the selection logic. Two of the switches in the DG413 (#2 and #3) use the logic of the DG211 and DG411 (i.e., a logic “0” turns the switch ON) and the other two switches use DG212 and DG412 positive logic. This permits independent control of turn-on and turn-off times for SPDT configurations, permitting “break-before-make” or “make-before-break” operation with a minimum of external logic.

Features

- ON-Resistance (Max) 35Ω
- Low Power Consumption (P_D) . . . . . <35µW
- Fast Switching Action
  - t_{ON} (Max) 175ns
  - t_{OFF} (Max) 145ns
- Low Charge Injection
- Upgrade from DG211, DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

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Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
DG411DJ	DG411DJ	-40 to +85	16 Ld PDIP	E16.3
DG411DJZ (Note)	DG411DJZ	-40 to +85	16 Ld PDIP** (Pb-free)	E16.3
DG411DY*	DG411DY	-40 to +85	16 Ld SOIC (150 mil)	M16.15
DG411DYZ* (Note)	DG411DYZ	-40 to +85	16 Ld SOIC (150 mil) (Pb-free)	M16.15
DG411DVZ* (Note)	DG411 DVZ	-40 to +85	16 Ld TSSOP (4.4mm) (Pb-free)	M16.173
DG412DJ	DG412DJ	-40 to +85	16 Ld PDIP	E16.3
DG412DJZ (Note)	DG412DJZ	-40 to +85	16 Ld PDIP** (Pb-free)	E16.3
DG412DY*	DG412DY	-40 to +85	16 Ld SOIC (150 mil)	M16.15
DG412DYZ* (Note)	DG412DYZ	-40 to +85	16 Ld SOIC (150 mil) (Pb-free)	M16.15
DG412DVZ* (Note)	DG412 DVZ	-40 to +85	16 Ld TSSOP (4.4mm) (Pb-free)	M16.173
DG413DJ	DG413DJ	-40 to +85	16 Ld PDIP	E16.3
DG413DJZ (Note)	DG413DJZ	-40 to +85	16 Ld PDIP** (Pb-free)	E16.3
DG413DY*	DG413DY	-40 to +85	16 Ld SOIC (150 mil)	M16.15
DG413DYZ* (Note)	DG413DYZ	-40 to +85	16 Ld SOIC (150 mil) (Pb-free)	M16.15
DG413DVZ* (Note)	DG413 DVZ	-40 to +85	16 Ld TSSOP (4.4mm) (Pb-free)	M16.173

*Add “-T” suffix for tape and reel.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

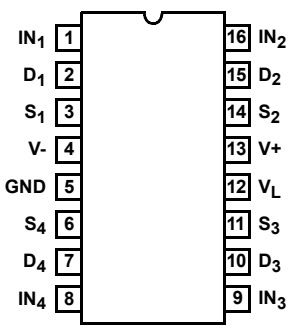
TRUTH TABLE

LOGIC	DG411 SWITCH	DG412 SWITCH	DG413 SWITCH 1, 4	DG413 SWITCH 2, 3
0	On	Off	Off	On
1	Off	On	On	Off

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V.

Pinout

DG411, DG412, DG413
(16 LD PDIP, SOIC, TSSOP)
TOP VIEW



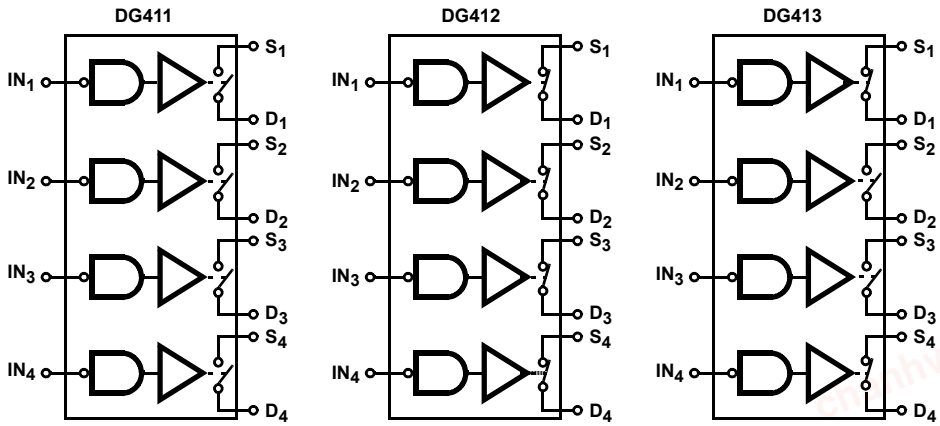
Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1.
2	D_1	Drain (Output) Terminal for Switch 1.
3	S_1	Source (Input) Terminal for Switch 1.
4	V-	Negative Power Supply Terminal.
5	GND	Ground Terminal (Logic Common).
6	S_4	Source (Input) Terminal for Switch 4.
7	D_4	Drain (Output) Terminal for Switch 4.
8	IN_4	Logic Control for Switch 4.
9	IN_3	Logic Control for Switch 3.
10	D_3	Drain (Output) Terminal for Switch 3.
11	S_3	Source (Input) Terminal for Switch 3.
12	V_L	Logic Reference Voltage.
13	V+	Positive Power Supply Terminal (Substrate).
14	S_2	Source (Input) Terminal for Switch 2.
15	D_2	Drain (Output) Terminal for Switch 2.
16	IN_2	Logic Control for Switch 2.

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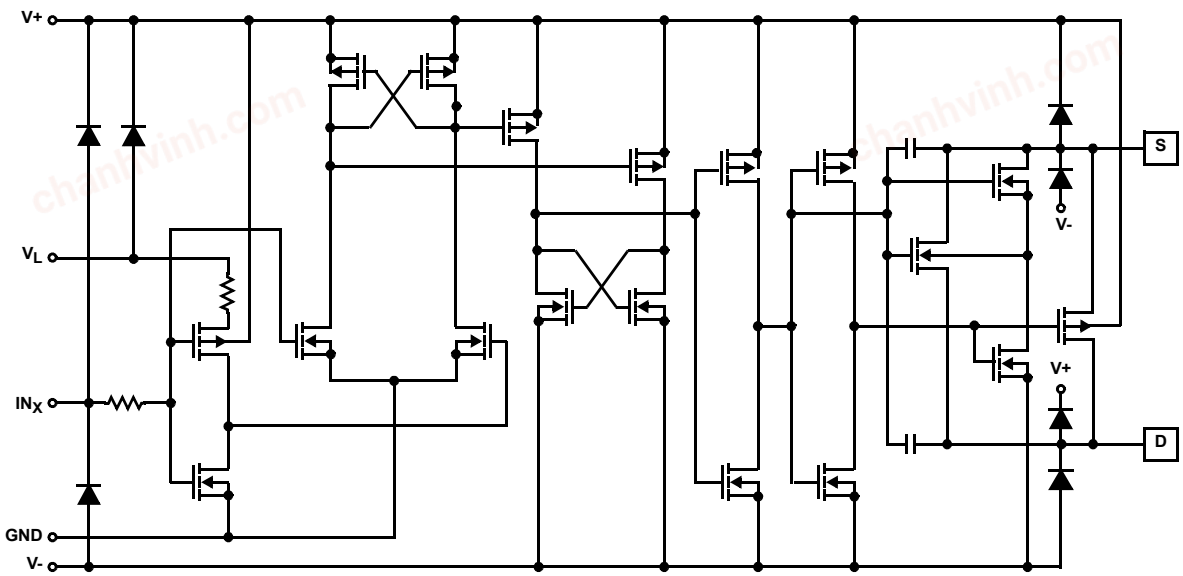
Functional Diagrams

Four SPST Switches per Package Switches Shown for Logic “1” Input



Schematic Diagram

(1 Channel)



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Absolute Maximum Ratings

V+ to V- 44V
GND to V- 25V
V_L . . . . . (GND -0.3V) to (V+) +0.3V
Digital Inputs, V_S, V_D (Note 1). . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) . . 100mA

Operating Conditions

Voltage Range . . . . . ±20V (Max)
Temperature Range . . . . . -40°C to +85°C
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time . . . . . ≤20ns

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package*	90
SOIC Package	110
TSSOP Package	150

Maximum Junction Temperature (Plastic Packages) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
(SOIC and TSSOP - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 4)	TYP (Note 5)	MAX (Note 4)	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF, V_S = ±10V (Figure 1)	25	-	110	175	ns
		85	-	-	220	ns
Turn-OFF Time, t_{OFF}		25	-	100	145	ns
		85	-	-	160	ns
Break-Before-Make Time Delay	DG413 Only, R_L = 300Ω, C_L = 35pF (Figure 2)	25	-	25	-	ns
Charge Injection, Q (Figure 3)	C_L = 10nF, V_G = 0V, R_G = 0Ω	25	-	5	-	pC
OFF Isolation (Figure 5)	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	68	-	dB
Crosstalk (Channel-to-Channel), (Figure 4)		25	-	-85	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz (Figure 6)	25	-	9	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$		25	-	9	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$		25	-	35	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	0.005	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.005	0.5	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}	I_S = ∓10mA	Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = ∓10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	25	-	25	35	Ω
		Full	-	-	45	Ω

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Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 4)	TYP (Note 5)	MAX (Note 4)	UNITS
Source OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	25	-0.25	±0.1	0.25	nA
		Full	-5	-	+5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		25	-0.25	±0.1	0.25	nA
		Full	-5	-	+5	nA
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_S = V_D = ±15.5V	25	-0.4	±0.1	0.4	nA
		Full	-10	-	+10	nA
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	25	-	0.0001	1	µA
		85	-	-	5	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		85	-5	-	-	µA
Logic Supply Current, I_L		25	-	0.0001	1	µA
		85	-	-	5	µA
Ground Current, I_{GND}		25	-1	-0.0001	-	µA
		85	-5	-	-	µA

Electrical Specifications

(Single Supply) Test Conditions: V+ = +12V, V- = 0V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 4)	TYP (Note 5)	MAX (Note 4)	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF, V_S = 8V, (Figure 1)	25	-	175	250	ns
		85	-	-	315	ns
Turn-OFF Time, t_{OFF}		25	-	95	125	ns
		85	-	-	140	ns
Break-Before-Make Time Delay	DG413 Only, R_L = 300Ω, C_L = 35pF, V_S = 8V	25	-	25	-	ns
Charge Injection, Q	C_L = 10nF, V_G = 6.0V, R_G = 0Ω	25	-	25	-	pC
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	I_S = -10mA, V_D = 3V, 8V V+ = 10.8V	25	-	40	80	Ω
		Full	-	-	100	Ω

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Electrical Specifications (Single Supply) Test Conditions: V+ = +12V, V- = 0V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified. **(Continued)**

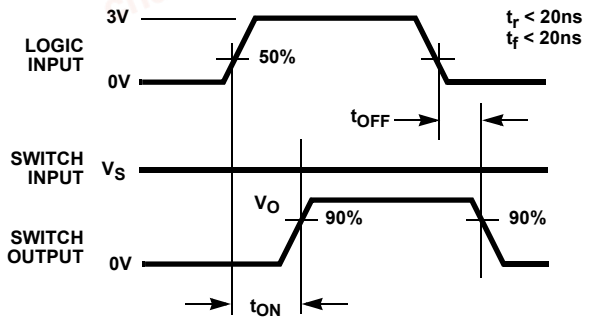
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 4)	TYP (Note 5)	MAX (Note 4)	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13.2V, V- = 0V V_{IN} = 0V or 5V	25	-	0.0001	1	µA
		85	-	-	5	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		85	-5	-	-	µA
Logic Supply Current, I_L		25	-	0.0001	1	µA
		85	-	-	5	µA
Ground Current, I_{GND}		25	-1	-0.0001	-	µA
		85	-5	-	-	µA

NOTES:

3. V_{IN} = input voltage to perform proper function.
4. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
5. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

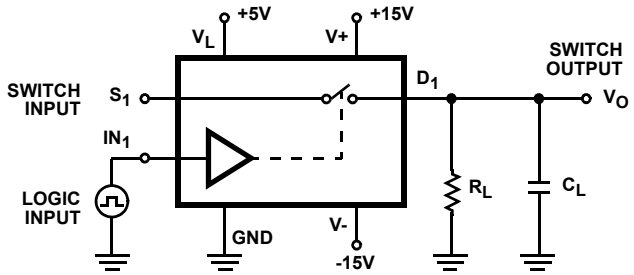
Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENTS POINTS



Repeat test for all IN and S.
For load conditions, see Specifications. C_L includes fixture and stray capacitance.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

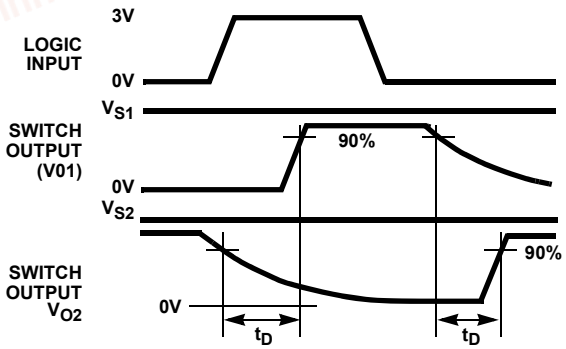
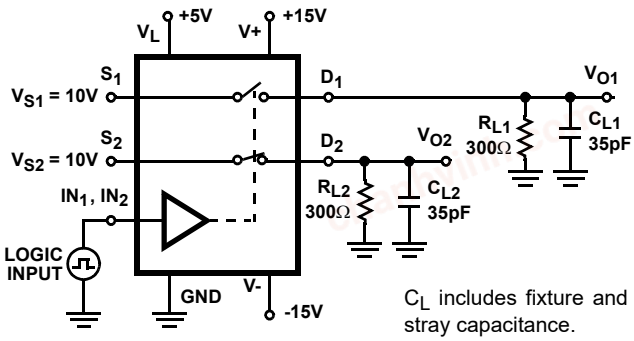


FIGURE 2A. MEASUREMENT POINTS



C_L includes fixture and stray capacitance.

FIGURE 2B. TEST CIRCUITS

FIGURE 2. BREAK-BEFORE-MAKE TIME

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Test Circuits and Waveforms (Continued)

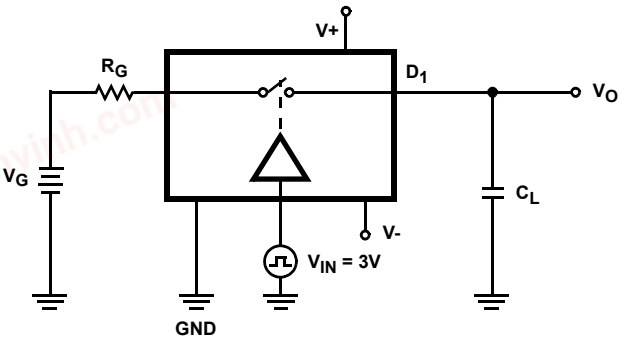
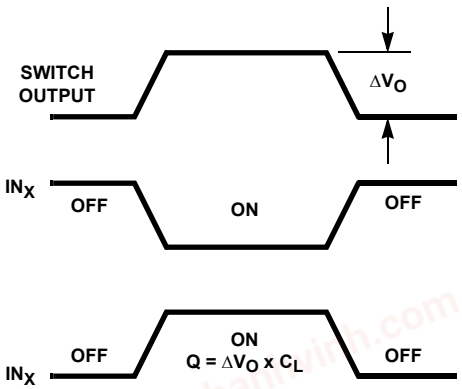


FIGURE 3A. TEST CIRCUIT



NOTE: IN_X dependent on switch configuration, input polarity determined by sense of switch.

FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. CHARGE INJECTION

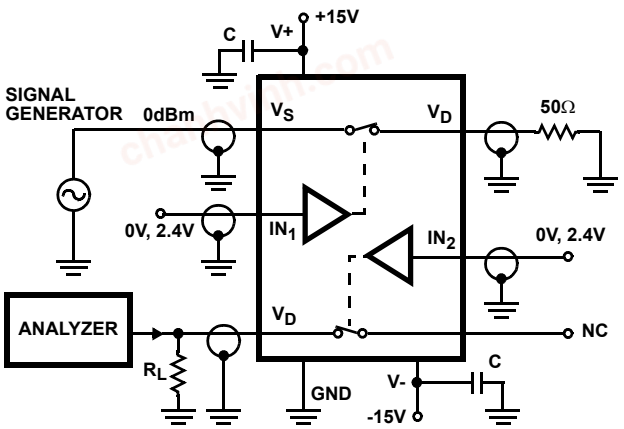


FIGURE 4. CROSSTALK TEST CIRCUIT

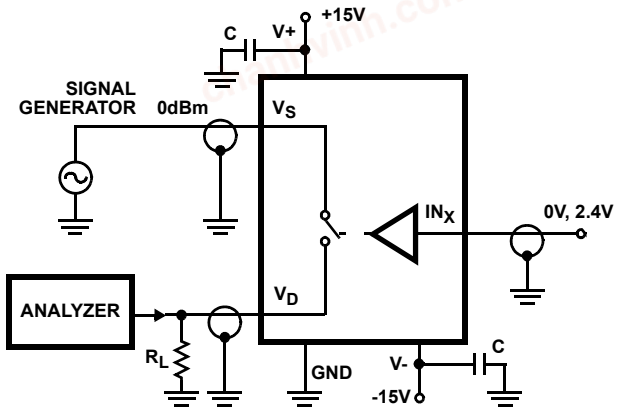


FIGURE 5. OFF ISOLATION TEST CIRCUIT

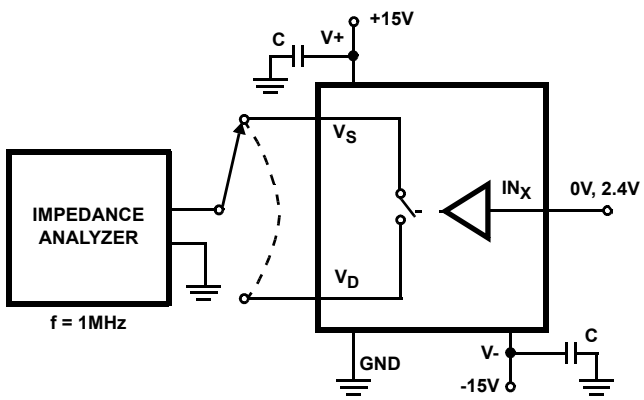


FIGURE 6. SOURCE/DRAIN CAPACITANCES TEST CIRCUIT

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Application Information

Single Supply Operation

The DG411, DG412, DG413 can be operated with unipolar supplies from 5V to 44V. These devices are characterized and tested for single supply operation at 12V to facilitate the majority of applications. To function properly, 12V is tied to Pins 13 and 0V is tied to Pin 4.

Pin 12 still requires 5V for TTL compatible switching.

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 7, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

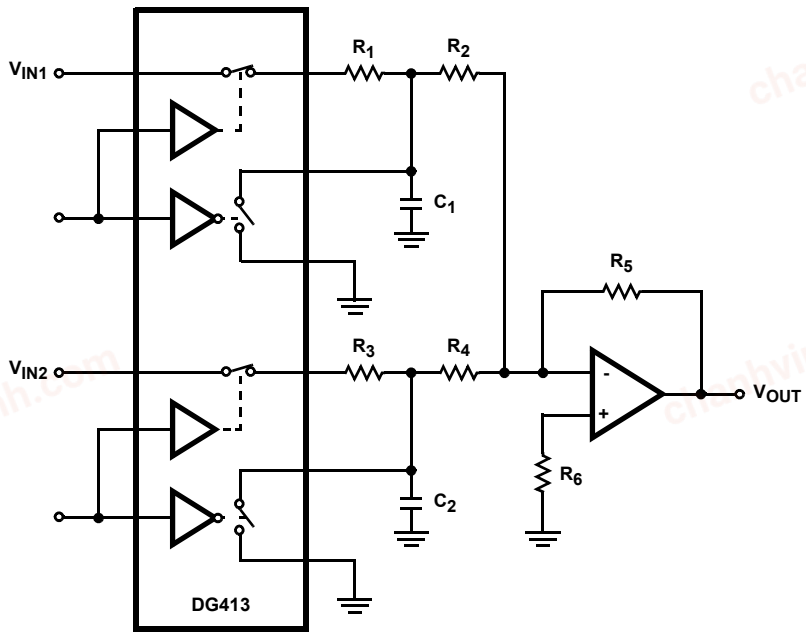


FIGURE 7. SUMMING AMPLIFIER

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Typical Performance Curves

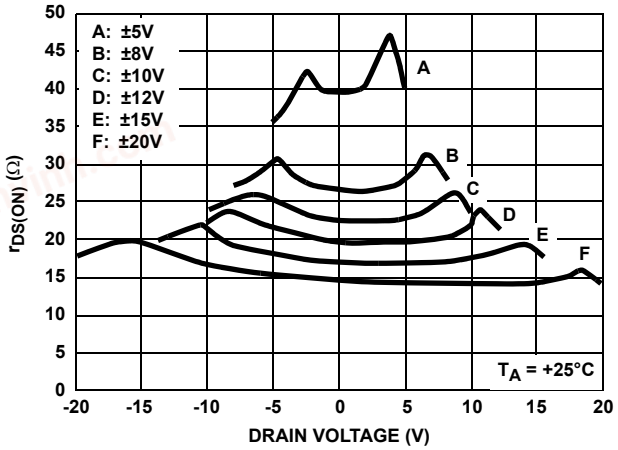


FIGURE 8. ON RESISTANCE vs V_D AND POWER SUPPLY VOLTAGE

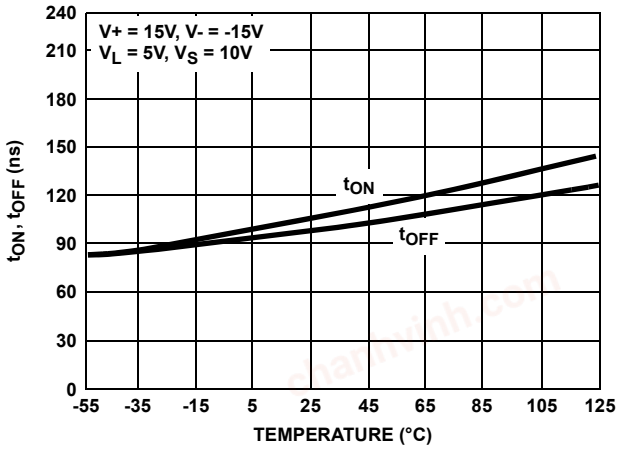


FIGURE 9. SWITCHING TIME vs TEMPERATURE

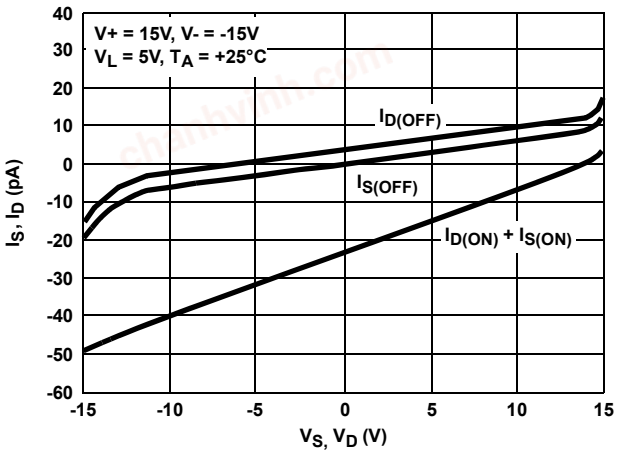


FIGURE 10. LEAKAGE CURRENTS vs ANALOG VOLTAGE

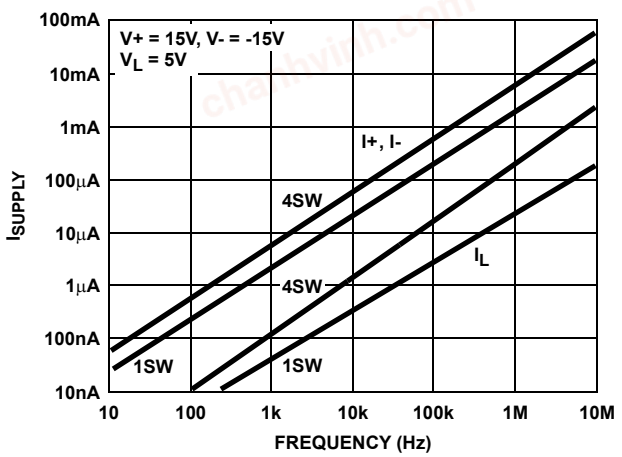


FIGURE 11. SUPPLY CURRENT vs INPUT SWITCHING FREQUENCY

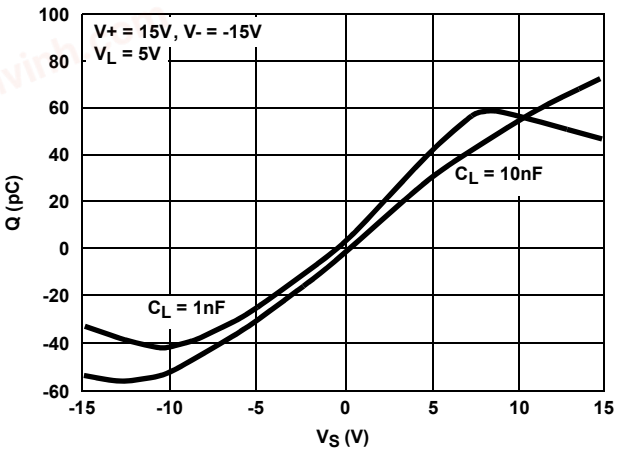


FIGURE 12. CHARGE INJECTION vs SOURCE VOLTAGE

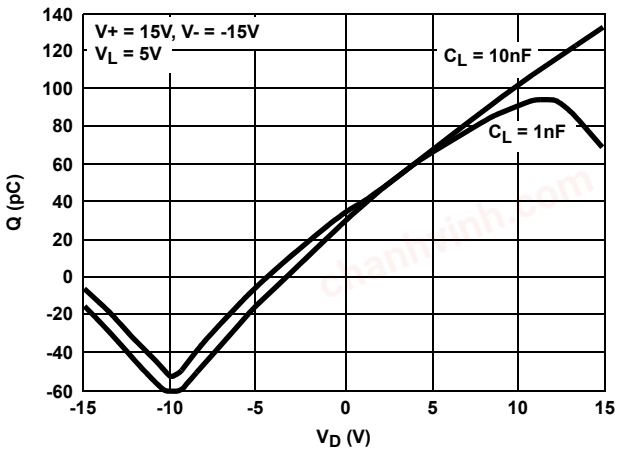


FIGURE 13. CHARGE INJECTION vs DRAIN VOLTAGE

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Die Characteristics

DIE DIMENSIONS:

2760mm x 1780mm x 485mm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

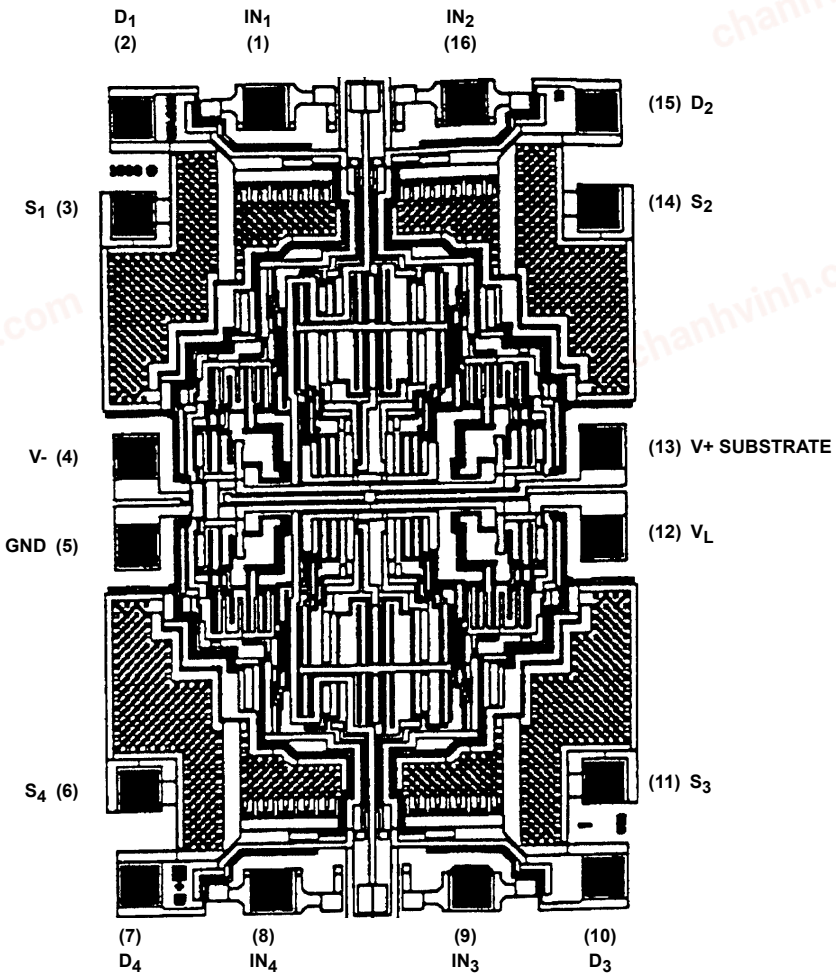
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.5×10^5 A/cm^2

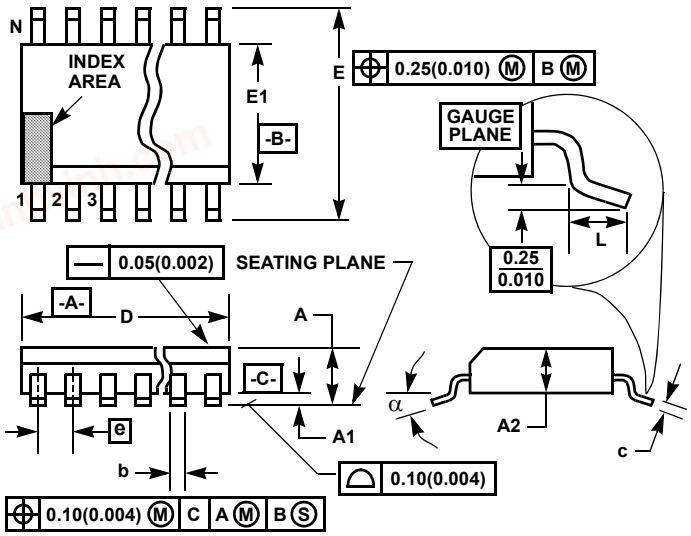
Metallization Mask Layout

DG411, DG412, DG413



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Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M16.173

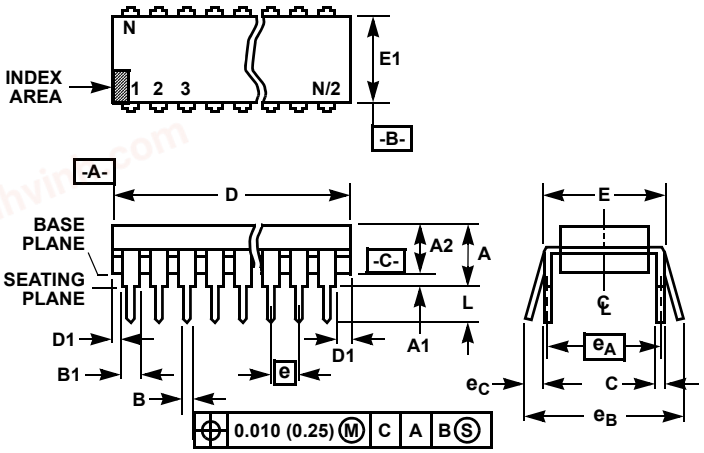
16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
a	0^o	8^o	0^o	8^o	-

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Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

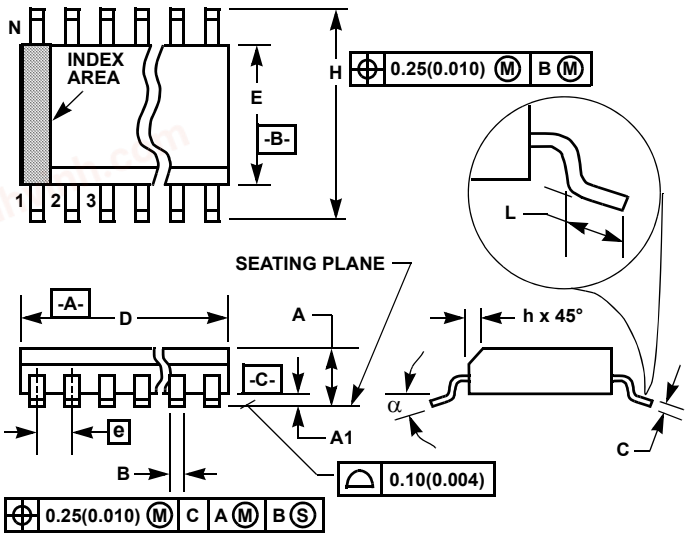
E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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(Rev.1.0 Mar 2020)

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