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2:12 DB1200ZL Derivative for PCIe Gen1–4 and UPI

9ZML1232E / 9ZML1252E Datasheet

Description

The 9ZML1232E / 9ZML1252E are a second generation 2-input/12-output differential mux for Intel Purley and newer platforms. It exceeds the demanding DB1200ZL performance specifications and is backwards compatible to the 9ZML1232B. It utilizes Low-Power HCSL-compatible outputs to reduce power consumption and termination resistors. It is suitable for PCI-Express Gen1–4 or QPI/UPI applications, and provides 2 configurable low-drift I2O settings, one for each input channel, to allow I2O tuning for various topologies.

PCIe Clocking Architectures Supported

- Common Clocked (CC)
- Separate Reference No Spread (SRNS)
- Separate Reference Independent Spread (SRIS)

Typical Applications

Servers, Storage, Networking, SSDs

Output Features

- 12 Low-power HCSL (LP-HCSL) output pairs (9ZML1232E)
- 12 Low-power HCSL (LP-HCSL) output pairs with 85Ω Zout (9ZML1252E)

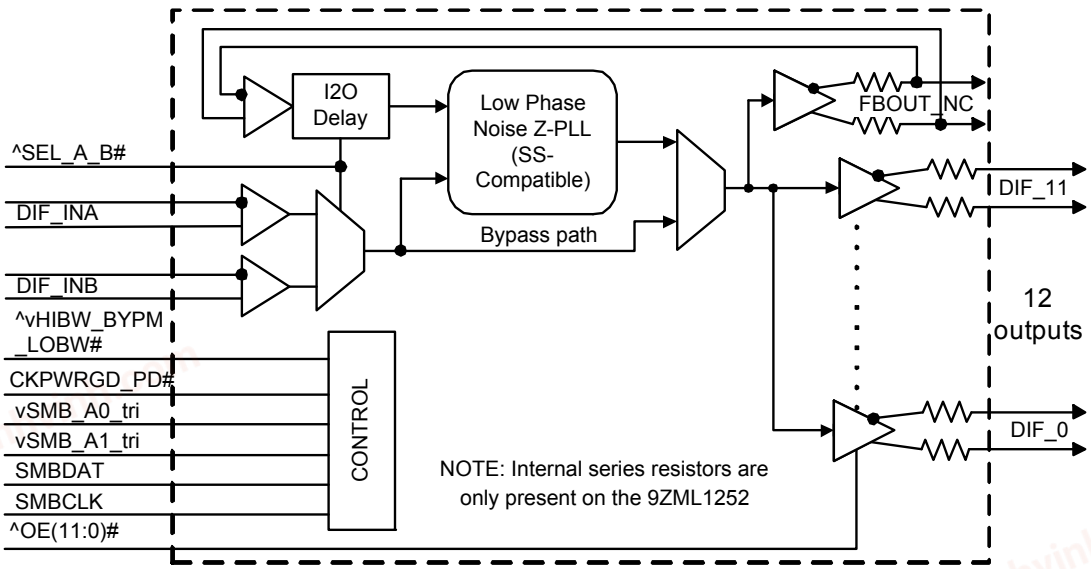
Features

- 2 configurable low drift I2O delays up to 2.9ns; maintain transport delay for various topologies
- LP-HCSL outputs; eliminate 24 resistors (9ZML1232E)
- LP-HCSL outputs with Zout = 85Ω; eliminate 48 resistors (9ZML1252E)
- 9 selectable SMBus addresses; multiple devices can share same SMBus segment
- Separate VDDIO for outputs; allows maximum power savings
- PLL or Bypass Mode; PLL can dejitter incoming clock
- Hardware or software-selectable PLL BW; minimizes jitter peaking in downstream PLLs
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- SMBus interface; software can modify device settings without hardware changes
- 10 x 10 mm 72-QFN package; small board footprint

Key Specifications

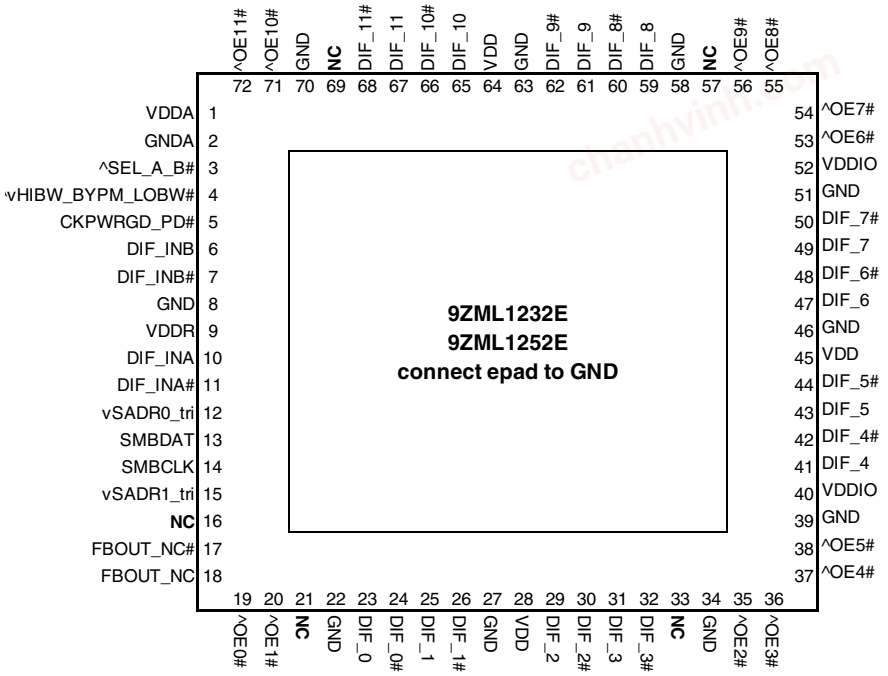
- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps
- Input-to-output delay: Fixed at 0 ps
- Input-to-output delay variation < 50ps
- Phase jitter: PCIe Gen4 < 0.5ps rms
- Phase jitter: UPI > 9.6GB/s < 0.1ps rms

Block Diagram



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Pin Configuration



^ prefix indicates internal 120Kohm Pull Up
v prefix indicates internal 120Kohm Pull down
10mm x 10mm 72-VFQFPN 0.5mm pin pitch

Power Management Table

Inputs		Control Bits	Outputs		PLL State
CKPWRGD_PD#	DIF_IN	SMBus EN bit	DIF_x	FBOUT_NC	
0	X	X	Low/Low	Low/Low	OFF
1	Running	0	Low/Low	Running	ON
		1	Running	Running	ON

PLL Operating Mode Table

HIBW_BYPM_LOBW#	Byte0[7:6]
Low (PLL Low BW)	00
Mid (Bypass)	01
High (PLL High BW)	11

NOTE: PLL is off in Bypass mode

Power Connections

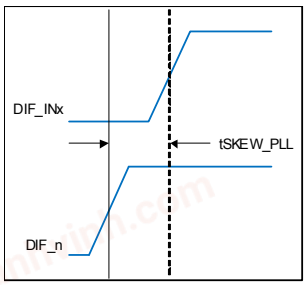
Pin Number			Description
VDD	VDDIO	GND	
1		2	Analog PLL
9		8	Analog Input
28, 45, 64	40, 52	22, 27, 34, 39, 46, 51, 58, 63, 70	DIF clocks

Power Connections (for pin compatibility with 9ZML12xxB)

Pin Number			Description
VDD	VDDIO	GND	
1		2	Analog PLL
9		8	Analog Input
28, 45, 64	**21**, **33**, 40, 52, **57**, **69**	**16**, 22, 27, 34, 39, 46, 51, 58, 63, 70	DIF clocks

Skew Programming Table

Skew[2:0]	Skew Steps	Skew (ps)
000	0	0
001	1	-416.67
010	2	-833.33
011	3	-1250.00
100	4	-1666.67
101	5	-2083.33
110	6	-2500.00
111	7	-2916.67



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Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	Power supply for PLL core.
2	GNDA	GND	Ground pin for the PLL core.
3	^SEL_A_B#	IN	Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected.
4	^vHIBW_BYPM_LOBW#	LATCHED IN	Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull up/pull down resistors. See PLL Operating Mode Table for Details.
5	CKPWRGD_PD#	IN	3.3V input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
6	DIF_INB	IN	True input of differential clock
7	DIF_INB#	IN	Complement input of differential clock
8	GND	GND	Ground pin.
9	VDDR	PWR	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
10	DIF_INA	IN	True input of differential clock
11	DIF_INA#	IN	Complement input of differential clock
12	vSADR0_tri	IN	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull down resistor. See the SMBus Address Selection Table.
13	SMBDAT	I/O	Data pin of SMBUS circuitry
14	SMBCLK	IN	Clock pin of SMBUS circuitry
15	vSADR1_tri	IN	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull down resistor. See the SMBus Address Selection Table.
16	NC	N/A	No connection.
17	FBOUT_NC#	OUT	Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
18	FBOUT_NC	OUT	True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
19	^OE0#	IN	Active low input for enabling output 0. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
20	^OE1#	IN	Active low input for enabling output 1. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
21	NC	N/A	No connection.
22	GND	GND	Ground pin.
23	DIF_0	OUT	HCSL true clock output.
24	DIF_0#	OUT	HCSL complementary clock output.
25	DIF_1	OUT	HCSL true clock output.
26	DIF_1#	OUT	HCSL complementary clock output.
27	GND	GND	Ground pin.
28	VDD	PWR	Power supply, nominally 3.3V.
29	DIF_2	OUT	HCSL true clock output.
30	DIF_2#	OUT	HCSL complementary clock output.
31	DIF_3	OUT	HCSL true clock output.
32	DIF_3#	OUT	HCSL complementary clock output.
33	NC	N/A	No connection.
34	GND	GND	Ground pin.
35	^OE2#	IN	Active low input for enabling output 2. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.

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Pin Descriptions (cont.)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
36	^OE3#	IN	Active low input for enabling output 3. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
37	^OE4#	IN	Active low input for enabling output 4. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
38	^OE5#	IN	Active low input for enabling output 5. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
39	GND	GND	Ground pin.
40	VDDIO	PWR	Power supply for differential outputs.
41	DIF_4	OUT	HCSL true clock output.
42	DIF_4#	OUT	HCSL complementary clock output.
43	DIF_5	OUT	HCSL true clock output.
44	DIF_5#	OUT	HCSL complementary clock output.
45	VDD	PWR	Power supply, nominally 3.3V.
46	GND	GND	Ground pin.
47	DIF_6	OUT	HCSL true clock output.
48	DIF_6#	OUT	HCSL complementary clock output.
49	DIF_7	OUT	HCSL true clock output.
50	DIF_7#	OUT	HCSL complementary clock output.
51	GND	GND	Ground pin.
52	VDDIO	PWR	Power supply for differential outputs.
53	^OE6#	IN	Active low input for enabling output 6. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
54	^OE7#	IN	Active low input for enabling output 7. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
55	^OE8#	IN	Active low input for enabling output 8. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
56	^OE9#	IN	Active low input for enabling output 9. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
57	NC	N/A	No connection.
58	GND	GND	Ground pin.
59	DIF_8	OUT	HCSL true clock output.
60	DIF_8#	OUT	HCSL complementary clock output.
61	DIF_9	OUT	HCSL true clock output.
62	DIF_9#	OUT	HCSL complementary clock output.
63	GND	GND	Ground pin.
64	VDD	PWR	Power supply, nominally 3.3V.
65	DIF_10	OUT	HCSL true clock output.
66	DIF_10#	OUT	HCSL complementary clock output.
67	DIF_11	OUT	HCSL true clock output.
68	DIF_11#	OUT	HCSL complementary clock output.
69	NC	N/A	No connection.
70	GND	GND	Ground pin.
71	^OE10#	IN	Active low input for enabling output 10. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
72	^OE11#	IN	Active low input for enabling output 11. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
73	epad	GND	Connect to ground

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZML1232E / 9ZML1252E. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx				3.9	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5	V	1,3
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 3.9V.

Electrical Characteristics–DIF_IN Clock Input Parameters

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage	V_{CROSS}	Cross Over Voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.35		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–SMBus

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			400	kHz	5

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

[4]DIF_IN input

[5]The differential input clock must be running for the SMBus to be active

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Electrical Characteristics–Input/Supply/Common Parameters

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	3.135	3.3	3.465	V	
	VDDIO	Supply voltage for differential outputs	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range	-40		85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, tri-level inputs	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, tri-level inputs	GND - 0.3		0.8	V	
Input High Voltage	V_{IH}	Tri-Level Inputs (_tri suffix)	2.2		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IL}	Tri-Level Inputs (_tri suffix)	1.2	VDD/2	1.8	V	
Input Low Voltage	V_{IL}	Tri-Level Inputs (_tri suffix)	GND - 0.3		0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-100		100	uA	
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	1		400	MHz	
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	98.5	100.00	102	MHz	5
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		1.2	1.8	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable Frequency for PCIe Applications (Triangular Modulation)	30	31.6	33	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4	5	10	clocks	1,2,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion		85	300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	2
Trise	t_R	Rise time of control inputs			5	ns	2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV, PLL mode.

[4]DIF_IN input

[5] This parameter reflects the operating range after locking to a 100MHz input.

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Electrical Characteristics–DIF HCSL/LP-HCSL Outputs

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on	2.0	2.8	4.0	0.6 - 4.0	V/ns	1,2,3
Slew rate matching	ΔdV/dt	Slew rate matching, Scope averaging on		4	15	20	%	1,2,4,7
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)	660	794	870	1150	mV	7,8
Min Voltage	Vmin		-111	-49		-300		7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	302	367	453	250 - 550	mV	1,5,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		32	74	140	mV	1,6,7

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

[8] If driving a receiver with input terminations, the Vmax and Vmin values will be halved.

Electrical Characteristics–Current Consumption

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DDx}	All other VDD pins, All outputs @100MHz, CL = 2pF; Zo=85Ω		22	30	mA	2
	I_{DDA+R}	VDDA+VDDR pins, All outputs @100MHz, CL = 2pF; Zo=85Ω		56	65	mA	1,2
	I_{DDO}	VDDIO pins, All outputs @100MHz, CL = 2pF; Zo=85Ω		84	100	mA	2
Powerdown Current	I_{DDx}	All other VDD pins, all outputs Low/Low		0.9	2	mA	1,2
	I_{DDA+R}	VDDA+VDDR pins, all outputs Low/Low		4.3	6	mA	1,2
	I_{DDO}	VDDIO pins, all outputs Low/Low		0.1	0.2	mA	1,2

[1.] Includes VDDR if applicable

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Electrical Characteristics–Skew and Differential Jitter Parameters

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CLK_IN, DIF[x:0]	t_{SKEW_PLL}	Input-to-Output Skew in PLL mode @100MHz, nominal temperature and voltage	-100	-4	100	ps	1,2,4,5,6, 8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode @100MHz, nominal temperature and voltage	2.2	2.9	3.6	ns	1,2,3,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-Output Skew Variation in PLL mode @100MHz, across voltage and temperature	-50	0.0	50	ps	1,2,3,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	Input-to-Output Skew Variation in Bypass mode @100MHz, across voltage and temperature, T_{AMB} = 0C to 70C, default slew rate	-250	0.0	250	ps	1,2,3,8
		Input-to-Output Skew Variation in Bypass mode @100MHz, across voltage and temperature, T_{AMB} = -40C to 85C, default slew rate	-350	0.0	350	ps	1,2,3,8
DIF[x:0]	t_{SKEW_ALL}	Output-to-Output Skew across all outputs, common to PLL and Bypass mode, @100MHz, default slew rate		30	50	ps	1,2,3,8
PLL Jitter Peaking	$j_{peak\text{-}hibw}$	LOBW#_BYPASS_HIBW = 1	0	1.3	2.5	dB	7,8
PLL Jitter Peaking	$j_{peak\text{-}lobw}$	LOBW#_BYPASS_HIBW = 0	0	1.3	2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1	2	2.6	4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0	0.7	1.0	1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz	-1	-0.2	0	%	1,10
Jitter, Cycle to cycle	$t_{jcyc\text{-}cyc}$	PLL mode		13	50	ps	1,11
		Additive Jitter in Bypass Mode		0.2	5	ps	1,11

[1] Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device

[5] Measured with scope averaging on to find mean value.

[6] This value is programmable, see I2O Programming Table.

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3 db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[11] Measured from differential waveform.

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Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		13	30	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.3	0.7	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		1.0	1.6	3.1	ps (rms)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.24	0.35	1	ps (rms)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.24	0.30	0.5	ps (rms)	1,2
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		0.01	0.05	n/a	ps (p-p)	1,2
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.01	0.05		ps (rms)	1,2,4
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.000	0.05		ps (rms)	1,2,4
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.01	0.05		ps (rms)	1,2,4
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.01	0.05		ps (rms)	1,2,4

[1] Applies to all outputs, when driven by 9SQL4958 or equivalent.

[2] Based on PCIe Base Specification Rev4.0 version 0.7 draft. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] For RMS values additive jitter is calculated by solving the following equation for b [*a^2 + b^2 = c^2*] where "a" is rms input jitter and "c" is rms total jitter.

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Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1-SRIS}$	PCIe Gen 1	n/a			n/a	ps (p-p)	1,2,3
	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.8	1.2	2	ps (rms)	1,2
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.6	0.68	0.7	ps (rms)	1,2
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)	n/a			n/a	ps (rms)	1,2
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG1-SRIS}$	PCIe Gen 1	n/a			n/a	ps (p-p)	1,2,5
	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.0	0.02		ps (rms)	1,2,4
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.0	0.02		ps (rms)	1,2,4
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)	n/a				ps (rms)	1,2,4,5

[1] Applies to all outputs, when driven by 9SQL4958 or equivalent

[2] Based on PCIe Base Specification Rev3.1a. These filters are different than Common Clock filters. See http://www.pcisig.com for latest specifications. 0.7ps is the Intel specified limit, which may differ from the PCI SIG limit.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] For RMS values, additive jitter is calculated by solving the following equation for b [*a^2 + b^2 = c^2*] where "a" is rms input jitter and "c" is rms total jitter.

[5] SRIS is not currently defined for PCIe Gen1 and Gen4.

Electrical Characteristics–Filtered Phase Jitter Parameters - QPI/UPI

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	IND.LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	t_{jphQPI_UPI}	QPI & SMI (100MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.15	0.3	0.5	ps (rms)	1,2
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.08	0.1	0.3	ps (rms)	1,2
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.07	0.1	0.2	ps (rms)	1,2
Additive Phase Jitter, Bypass mode	t_{jphQPI_UPI}	QPI & SMI (100MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.00	0.05	n/a	ps (rms)	1,2,3
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.02	0.09		ps (rms)	1,2,3
		QPI & SMI (100MHz, ? 9.6Gb/s, 12UI)		0.02	0.08		ps (rms)	1,2,3

[1] Applies to all outputs, when driven by 9SQL4958 or equivalent

[2] Calculated from Intel-supplied Clock Jitter Tool

[3] For RMS values additive jitter is calculated by solving the following equation for b [*a^2 + b^2 = c^2*] where "a" is rms input jitter and "c" is rms total jitter.

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Electrical Characteristics–Unfiltered Phase Jitter Parameters - 12kHz to 20MHz

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	IND.LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jph12k-20MHi}$	PLL High BW, SSC OFF, 100MHz		171	250	n/a	fs (rms)	1,2
Phase Jitter, PLL Mode	$t_{jph12k-20MLo}$	PLL Low BW, SSC OFF, 100MHz		183	250	n/a	fs (rms)	1,2
Additive Phase Jitter, Bypass mode	$t_{jph12k-20MByp}$	Bypass Mode, SSC OFF, 100MHz		109	150	n/a	fs (rms)	1,2,3

[1] Applies to all outputs. Wenzel clock source.

[2] 12kHz to 20MHz brick wall filter.

[3] For RMS values additive jitter is calculated by solving the following equation for b [*a^2 + b^2 = c^2*] where "a" is rms input jitter and "c" is rms total jitter.

Clock Periods–Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2,3

Clock Periods–Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3

Notes:

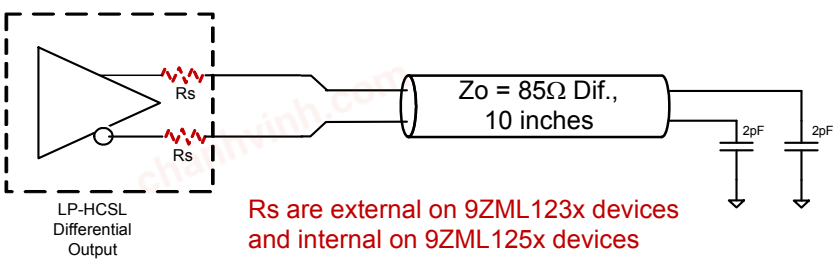
[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ accuracy requirements (+/-100ppm). The 9ZML12xx does not contribute to ppm error.

[3] Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

Test Loads

9ZML Differential Test Loads



Differential Output Terminations*

Device	DIF Zo (Ω)	Rs (Ω)
9ZML123x	85	27
9ZML123x	100	33
9ZML125x	85	Internal
9ZML125x	100	7.5

*Contact factory for versions of this device with Zo=100Ω

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General SMBus Serial Interface Information for 9ZML1232E / 9ZML1252E

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

9ZML1232E / 9ZML1252E SMBus Addressing

SMB_A(1:0)_tri	SMBus Address (Rd/Wrt bit = 0)
00	D8
0M	DA
01	DE
M0	C2
MM	C4
M1	C6
10	CA
1M	CC
11	CE

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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SMBusTable: PLL Mode, and Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		PLL Mode bit [1]	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback Table		Latch
Bit 6		PLL Mode bit [0]	PLL Operating Mode Rd back 0	R			Latch
Bit 5		SEL_A_B#	Input Select Readback	R	DIF_INB	DIF_INA	Real
Bit 4		Reserved					0
Bit 3		PLL_InSEL_SW_EN	Enable S/W control of PLL BW and Input select	RW	Pin Control	SMBus Control	0
Bit 2		PLL Mode bit [1]	PLL Operating Mode 1	RW	See PLL Operating Mode Readback Table[1]		1
Bit 1		PLL Mode bit [0]	PLL Operating Mode 1	RW			1
Bit 0		Reserved					1

1. Note, Changing the PLL operating mode between HiBW or LoBW and Bypass mode or between Bypass mode and HiBW or LoBW requires a system reset. Changing the PLL operating mode between HiBW and LoBw or between LoBW and HiBW does not require a system reset.

SMBusTable: Output Disable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		DIF_7_En	Output Control overrides OE# pin	RW	Low/Low	Pin Control	1
Bit 6		DIF_6_En	Output Control overrides OE# pin	RW			1
Bit 5		DIF_5_En	Output Control overrides OE# pin	RW			1
Bit 4		DIF_4_En	Output Control overrides OE# pin	RW			1
Bit 3		DIF_3_En	Output Control overrides OE# pin	RW			1
Bit 2		DIF_2_En	Output Control overrides OE# pin	RW			1
Bit 1		DIF_1_En	Output Control overrides OE# pin	RW			1
Bit 0		DIF_0_En	Output Control overrides OE# pin	RW			1

SMBusTable: Output Disable Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		DIF_11_En	Output Control overrides OE# pin	RW	Low/Low	Pin Control	1
Bit 2		DIF_10_En	Output Control overrides OE# pin	RW			1
Bit 1		DIF_9_En	Output Control overrides OE# pin	RW			1
Bit 0		DIF_8_En	Output Control overrides OE# pin	RW			1

SMBusTable: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBusTable: Reserved Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

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SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	E rev = 0100		0
Bit 6	-	RID2		R			1
Bit 5	-	RID1		R			0
Bit 4	-	RID0		R			0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		R	9ZML1232=EC 9ZML1233=ED 9ZML1252=FC 9ZML1253=FD		1
Bit 6	-	Device ID 6		R			1
Bit 5	-	Device ID 5		R			1
Bit 4	-	Device ID 4		R			X
Bit 3	-	Device ID 3		R			1
Bit 2	-	Device ID 2		R			1
Bit 1	-	Device ID 1		R			0
Bit 0	-	Device ID 0		R			X

SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4	-	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			0

SMBusTable:Output Skew RegisterA (when Input Clock A is selected)

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		I2O_FB_ASkew2	Channel A Output delay programming (early)		Binary value of number of VCO periods that outputs will be pulled earlier than input.		0
Bit 1		I2O_FB_ASkew1		RW			0
Bit 0		I2O_FB_ASkew0		RW			0

Note: For example, at 2.4GHz, each VCO period is 416.7ps and there are 24 VCO periods in a 100MHz output. Each write to bits [2:0] will pull the output a early by that number of VCO periods. Writing '110' 4 times would pull the output back in phase with the input. Writing '001' twice will accomplish the same result as writing '010' once - pulling the output 2 VCO periods earlier.

SMBusTable:Output Skew RegisterA (when Input Clock B is selected)

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		I2O_FB_BSkew2	Channel B Output delay programming (early)	RW	Binary value of number of VCO periods that outputs will be earlier than input. Default is 0.		0
Bit 1		I2O_FB_BSkew1		RW			0
Bit 0		I2O_FB_BSkew0		RW			0

Note: For example, at 2.4GHz, each VCO period is 416.7ps and there are 24 VCO periods in a 100MHz output. Each write to bits [2:0] will pull the output a early by that number of VCO periods. Writing '110' 4 times would pull the output back in phase with the input. Writing '001' twice will accomplish the same result as writing '010' once - pulling the output 2 VCO periods earlier.

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Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/nlnlg72-package-outline-100-x-100-mm-body-epad-59-mm-sq-050-mm-pitch-vfqfpn-sawn

Ordering Information

Part Number	Shipping Package	Package	Temperature
9ZML1232EKILF	Trays	72-pin QFN	-40 to +85°C
9ZML1232EKILFT	Tape and Reel	72-pin QFN	-40 to +85°C
9ZML1252EKILF	Trays	72-pin QFN	-40 to +85°C
9ZML1252EKILFT	Tape and Reel	72-pin QFN	-40 to +85°C

“LF” designates PB-free configuration, RoHS compliant.
“E” is the device revision designator (will not correlate with the datasheet revision).

Marking Diagrams





1. “L” denotes RoHS compliant package.
2. “LOT” denotes the lot number.
3. “COO” denotes country of origin.
4. “YYWW” denotes the last two digits of the year and week the part was assembled.

Revision History

Issue Date	Description
1/27/2017	1. Updated electrical tables with characterization data. 2. Updated VDDIO minimum VDDIO value from 1.05V to 3.135V 3. Updated block diagrams to remove color fill. 4. Moved to Preliminary.
1/31/2017	1. Finalized Electrical Tables. 2. Removed Byte 0, bit 0 from SMBus - only Hardware can select A or B input. 3. Added notes about functionality of Byte 0 [2:1]. 4. Move to final
4/17/2017	1. Reverted back to original Device ID Scheme, byte 6 updated accordingly: 9ZML1232=EC 9ZML1252=FC
12/1/2017	Removed "5V tolerant" reference on pins 13 and 14 descriptions.
4/12/2018	Updated absolute maximum supply voltage rating and VIHSMB to 3.9V.

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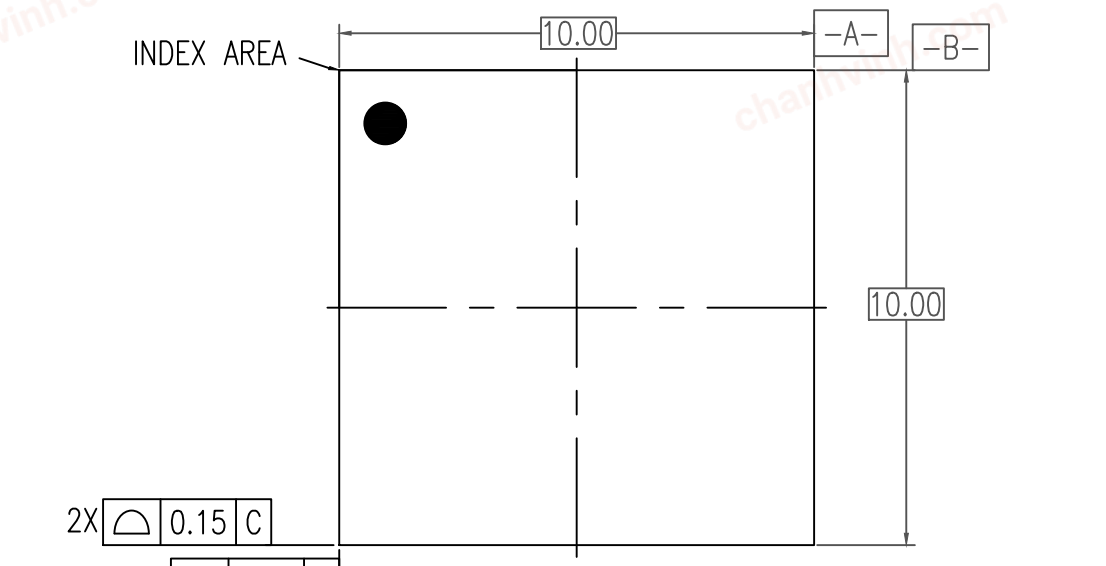
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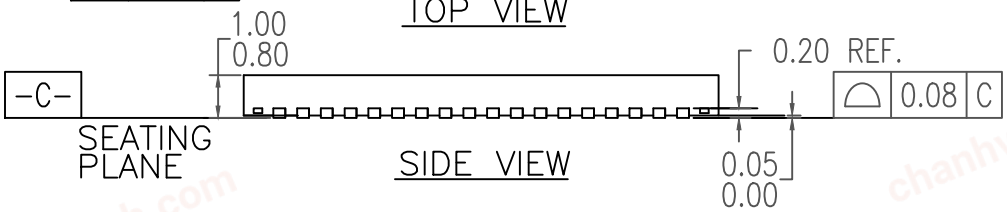
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72-VFQFPN, Package Outline Drawing

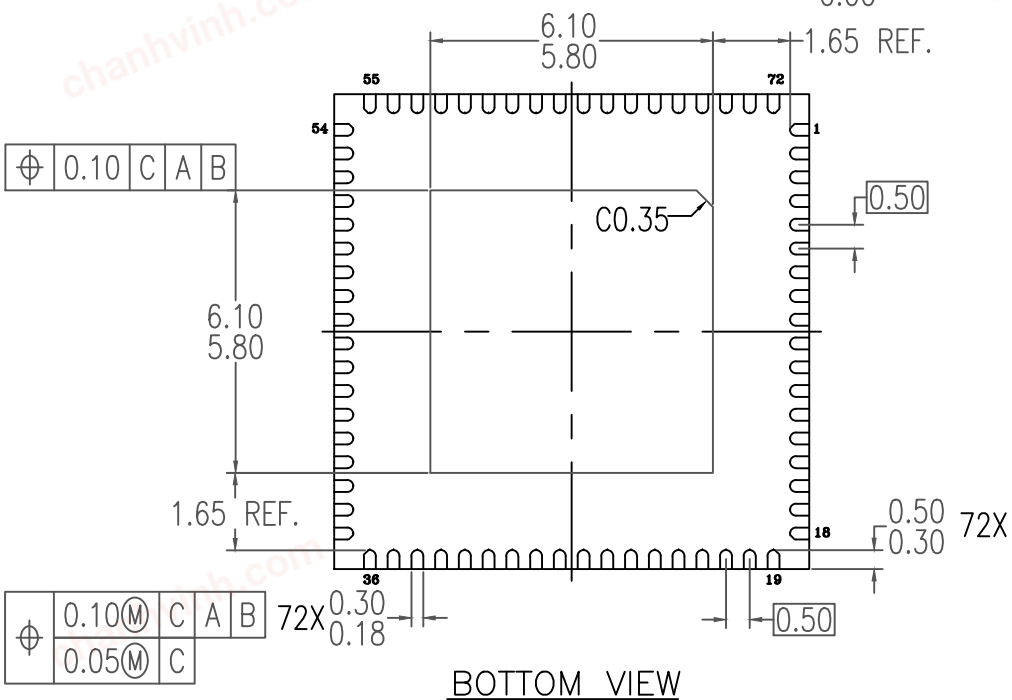
10.0 x 10.0 x 0.90 mm Body, Epad 5.95 x 5.95 mm 0.50mm Pitch



TOP VIEW



SIDE VIEW



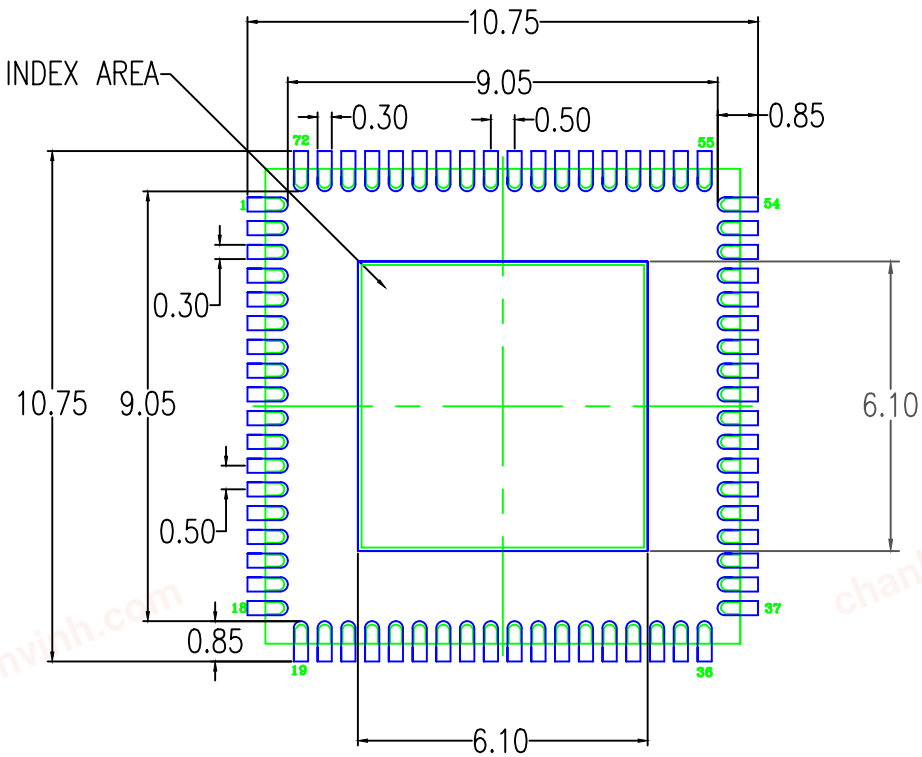
BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1994
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. INDEX AREA (PIN1 IDENTIFIER)

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 3, 2019	Rev 03	Update P1 Dimension from 5. 8 to 5.95 mm SQ
May 8, 2017	Rev 02	Change Package Code QFN to VFQFPN

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(Rev.1.0 Mar 2020)

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