chanhvinh.com

2:4 3.3V PCIe Gen1–5 Clock Mux 9DML0441 / 9DML0451

DATASHEET

Description

The 9DML0441 and 9DML0451 devices are 3.3V members of IDT's Full-Featured PCIe family. They support PCIe Gen1–5 Common Clocked (CC), Separate Reference no Spread (SRnS), and Separate Reference Independent Spread (SRIS) architectures. The parts provide a choice of asynchronous or glitch-free, gapped-clock switching modes, and offer a choice of integrated output terminations for direct connection to 85Ω or 100Ω transmission lines.

Typical Applications

- Servers
- ATE
- Storage
- Master/Slave applications

Output Features

- Four 1–200MHz Low-Power HCSL (LP-HCSL) DIF pairs
- 9DML0441 default ZOUT = 100Ω
- 9DML0451 default ZOUT = 85Ω
- See AN-891 for easy termination to other logic levels

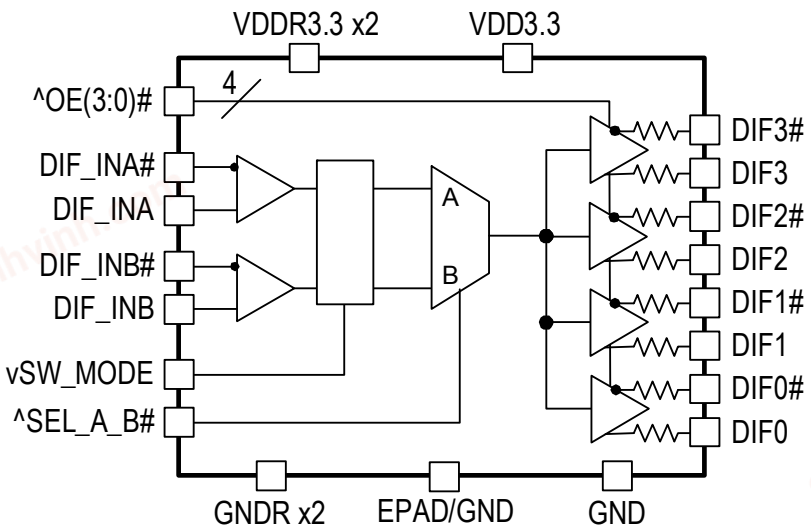
Features

- Direct connection to 100Ω (xx41) or 85Ω (xx51) transmission lines saves up to 16 resistors
- 79mW typical power consumption
- Spread Spectrum Clocking (SSC) compatible
- OE# pins for each output
- HCSL-compatible differential inputs
- Selectable asynchronous or glitch-free, gapped-clock switching; allows the mux to be selected at power up even if both inputs are not running, then transition to glitch-free switching mode
- Space saving 4 × 4 mm 24-VFQFPN
- Contact factory for customized versions

Key Specifications

- PCIe Gen1–5 CC support
- PCIe Gen1–5 SRIS support
- Output-to-output skew < 50ps
- PCIe Gen5 additive jitter (CC) is < 0.06 ps rms
- 12kHz–20MHz additive phase jitter 285fs rms typical at156.25MHz

Block Diagram

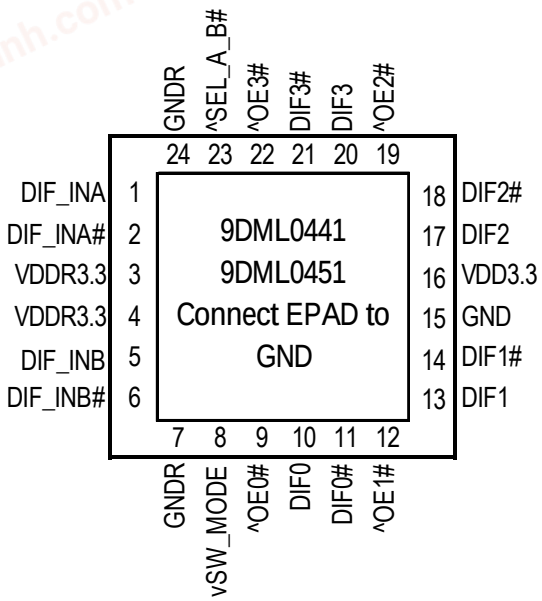


Note: Default resistors are internal on 41/51 devices.

© 2019 Renesas Electronics Corporation

chanhvinh.com

Pin Configuration



24-VFQFPN, 4 x 4 mm, 0.5mm pitch
^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor

Power Management Table

OEx# Pin	DIF_IN	DIFx	
		True O/P	Comp. O/P
0	Running	Running	Running
1	Running	Low	Low

Power Connections

Pin Number		Description
VDD	GND	
3	24	Input A receiver analog
4	7	Input B receiver analog
16	15	DIF outputs

© 2019 Renesas Electronics Corporation

chanhvinh.com

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	DIF_INA	IN	True input of differential clock
2	DIF_INA#	IN	Complement input of differential clock
3	VDDR3.3	PWR	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
4	VDDR3.3	PWR	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
5	DIF_INB	IN	True input of differential clock
6	DIF_INB#	IN	Complement input of differential clock
7	GNDR	GND	Analog ground pin for the differential input (receiver).
8	vSW_MODE	IN	Switch Mode. This pin selects either asynchronous or glitch-free, gapped clock switching of the mux. Use asynchronous mode if 0 or 1 of the input clocks is running. Glitch-free, gapped clock mode may be used if both input clocks are running. This pin has an internal pull down resistor. 0 = asynchronous switching mode 1 = glitch-free, gapped clock switching mode
9	^OE0#	IN	Active low input for enabling output 0. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output
10	DIF0	OUT	Differential true clock output.
11	DIF0#	OUT	Differential complementary clock output.
12	^OE1#	IN	Active low input for enabling output 1. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output
13	DIF1	OUT	Differential true clock output.
14	DIF1#	OUT	Differential complementary clock output.
15	GND	GND	Ground pin.
16	VDD3.3	PWR	Power supply, nominally 3.3V
17	DIF2	OUT	Differential true clock output.
18	DIF2#	OUT	Differential complementary clock output.
19	^OE2#	IN	Active low input for enabling output 2. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output
20	DIF3	OUT	Differential true clock output.
21	DIF3#	OUT	Differential complementary clock output.
22	^OE3#	IN	Active low input for enabling output 3. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output
23	^SEL_A_B#	IN	Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected.
24	GNDR	GND	Analog ground pin for the differential input (receiver).
25	EPAD	GND	Connect to Ground.

© 2019 Renesas Electronics Corporation

chanhvinh.com

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DML0441 / 9DML0451. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	VDDx				4.6	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD}+0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2500			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these Conditions is neither implied nor guaranteed.

[3] Not to exceed 4.6V.

Electrical Characteristics–Clock Input Parameters

$T_A = T_{AMB}$, Supply Voltages per normal operation Conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero.

Electrical Characteristics–Current Consumption

$T_A = T_{AMB}$, Supply Voltages per normal operation Conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DD}	VDD, All outputs active at 100MHz		24	31	mA	
Powerdown Current	I_{DDPD}	VDD, all outputs disabled		2	3	mA	1

[1] Input clock stopped.

© 2019 Renesas Electronics Corporation

chanhvinh.com

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

$T_A = T_{AMB}$, Supply Voltages per normal operation Conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	VDDx	Supply voltage for core and analog	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75 V_{DD}		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus	-0.3		0.25 V_{DD}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-50		50	uA	
Input Frequency	F_{ibyp}		1		200	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.74	1	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable Frequency for PCIe Applications (Triangular Modulation)	30	31.5	33	kHz	
Input SS Modulation Frequency non-PCIe	f_{MODIN}	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1	2	3	clocks	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	2
Trise	t_R	Rise time of single-ended control inputs			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200 mV.

© 2019 Renesas Electronics Corporation

chanhvinh.com

Electrical Characteristics–DIF Low-Power HCSL Outputs

$T_A = T_{AMB}$, Supply Voltages per normal operation Conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew rate	dV/dt	Scope averaging on, default settings	1.5	2.4	4	V/ns	1, 2, 3
Slew rate matching	ΔdV/dt	Slew rate matching		8.1	20	%	1, 4
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	783	850	mV	7
Voltage Low	V_{LOW}		-150	-24	150		7
Maximum Voltage	VMaximum	Measurement on single ended signal using absolute value. (Scope averaging off)		814	1150	mV	7
Minimum Voltage	VMinimum		-300	-66			7
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	368	550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		17	140	mV	1, 6

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V. These are defaults for the 41/51 devices, alternate settings are available in the P1 device.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_Minimum/Maximum (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] These are defaults for the 41/51 devices. They are factory adjustable in the P1 device.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

$T_A = T_{AMB}$, Supply Voltages per normal operation Conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Duty Cycle Distortion	t_{DCD}	Measured differentially, at 100MHz	0	0.2	0.7	%	1,3
Skew, Input to Output	t_{pd}	V_T = 50%	2637	3381	4273	ps	1
Skew, Output to Output	t_{sk3}	V_T = 50%		23	50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	*Additive* Jitter			1	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock.

© 2019 Renesas Electronics Corporation

chanhvinh.com

Electrical Characteristics–Additive PCIe Phase Jitter

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Units	Notes
Additive PCIe Phase Jitter (Common Clocked Architecture)	$t_{jphPCIeG1-CC}$	PCIe Gen 1 (2.5 GT/s) SSC ≤ -0.5%	0.214	2.6	5.0	86	ps (pk-pk)	1, 2
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Hi Band (5.0 GT/s) SSC ≤ -0.5%	0.322	0.357	0.428	3.1	ps (RMS)	1, 2
		PCIe Gen 2 Lo Band (5.0 GT/s) SSC ≤ -0.5%	0.008	0.023	0.033	3	ps (RMS)	1, 2
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (8.0 GT/s) SSC ≤ -0.5%	0.036	0.091	0.149	1	ps (RMS)	1, 2
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (16.0 GT/s) SSC ≤ -0.5%	0.036	0.092	0.156	0.5	ps (RMS)	1, 2, 3, 4
	$t_{jphPCIeG5-CC}$	PCIe Gen 5 (32.0 GT/s) SSC ≤ -0.5%	0.010	0.031	0.059	0.15	ps (RMS)	1, 2, 3, 5
Additive PCIe Phase Jitter (SRIS Architecture)	$t_{jphPCIeG1-SRIS}$	PCIe Gen 1 (2.5 GT/s) SSC ≤ -0.3%	n/a	n/a	n/a	n/a	ps (pk-pk)	1, 2, 6
	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 Band (5.0 GT/s) SSC ≤ -0.3%	0.436	0.455	0.524	n/a	ps (RMS)	1, 2, 6
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (8.0 GT/s) SSC ≤ -0.3%	0.126	0.131	0.150	n/a	ps (RMS)	1, 2, 6
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (16.0 GT/s) SSC ≤ -0.3%	0.107	0.111	0.128	n/a	ps (RMS)	1, 2, 6
	$t_{jphPCIeG5-SRIS}$	PCIe Gen 5 (32.0 GT/s) SSC ≤ -0.3%	0.038	0.040	0.045	n/a	ps (RMS)	1, 2, 6

Notes:

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The **total** Ref Clk jitter limits for each data rate are listed for convenience. The addtiive jitter may be subtracted from the limit using RSS subtraction to determine remaining margin.

2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data ratem the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

4. Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.

5. Note that 0.25 ps RMS is to be used in channel simulations to account for additional noise in a real system.

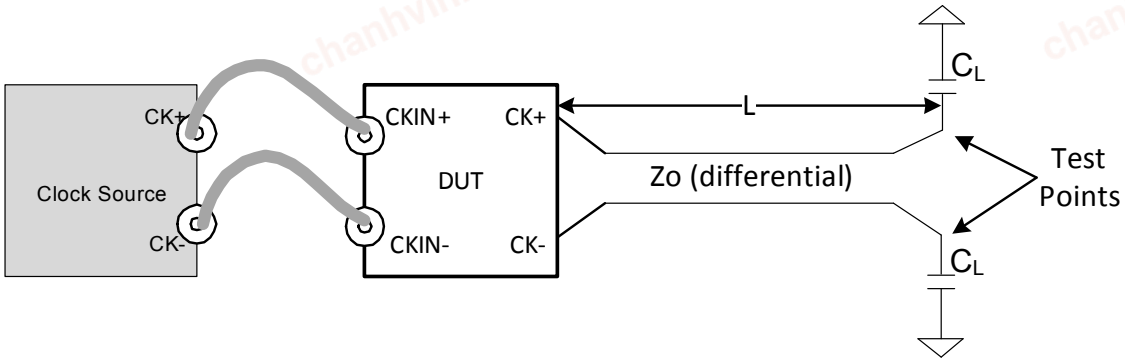
6. While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specifcation limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by $\sqrt{2}$.

© 2019 Renesas Electronics Corporation

chanhvinh.com

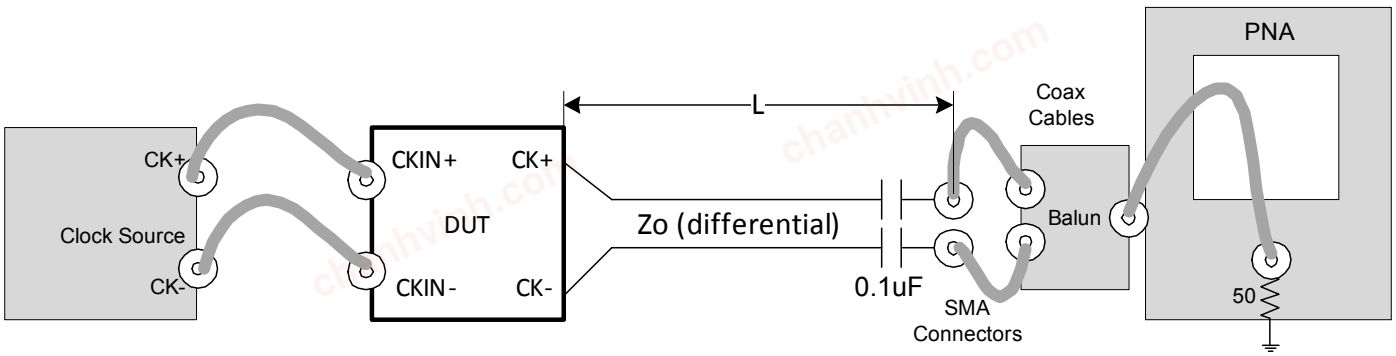
Test Loads

Test Load for AC/DC Measurements



Clock Source	DUT	L (cm)	Differential Zo (ohms)	C_L (pF)
SMA100B	9DML0451	12.7	85	2
SMA100B	9DML0441	12.7	100	2

Test Load for Phase Jitter Measurements



Clock Source	DUT	L (cm)	Differential Zo (ohms)
SMA100B	9DML0451	25.4	85
SMA100B	9DML0441	25.4	100

Alternate HCSL Terminations

Device	Differential Zo (Ω)	Rs (Ω)
9DML0441	85	N/A
9DML0441	100	None needed
9DML0451	85	None needed
9DML0451	100	7.5

Alternate Terminations

The 9DML family can easily drive LVPECL, LVDS, and CML logic. See “AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs” for details.

© 2019 Renesas Electronics Corporation

chanhvinh.com

Marking Diagrams





Notes:
1. Line 1: “LOT” is the lot sequence number.
2. Line 2: truncated part number.
3. Line 3: “YYWW” is the digits of the year and work-week that the part was assembled.

Thermal Characteristics

Parameter	Symbol	Conditions	PKG	Typical VALUE	Units	Notes
Thermal Resistance	θ_{JC}	Junction to Case	NLG24	42	°C/W	1
	θ_{Jb}	Junction to Base		2.4	°C/W	1
	θ_{JA0}	Junction to Air, still air		39	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		33	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		28	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		27	°C/W	1

[1] EPAD soldered to board.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/24-vfqfpn-package-outline-drawing-40-x-40-x-090-mm-body050mm-pitchepad-245-x-245-mm-nlg24p1

Ordering Information

Part / Order Number	Notes	ShippingPackaging	Package	Temperature
9DML0441AKILF	100Ω	Trays	24-VFQFPN	-40 to +85° C
9DML0441AKILFT		Tape and Reel	24-VFQFPN	-40 to +85° C
9DML0451AKILF	85Ω	Trays	24-VFQFPN	-40 to +85° C
9DML0451AKILFT		Tape and Reel	24-VFQFPN	-40 to +85° C

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.
“A” is the device revision designator (will not correlate with the datasheet revision).

© 2019 Renesas Electronics Corporation

chanhvinh.com

Revision History

Issue Date	Description
5/22/2019	1. Added PCIe Gen5 parameters to electrical tables 2. Removed 'P' devices from data sheet.
8/27/2018	1. Minor updates to electrical tables. 2. Updated front page text. 3. Updated block diagram.
6/6/2016	1. Updated leakage current spec for inputs with pull/up/down to +/-50µA. 2. Updated electrical tables with characterization data. 3. Update Front page text. 4. Updated ordering information. 5. Move to Final.

chanhvinh.com

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.