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Low Skew, 1-to-6, Differential-to-LVDS Fanout Buffer

854S006
Datasheet

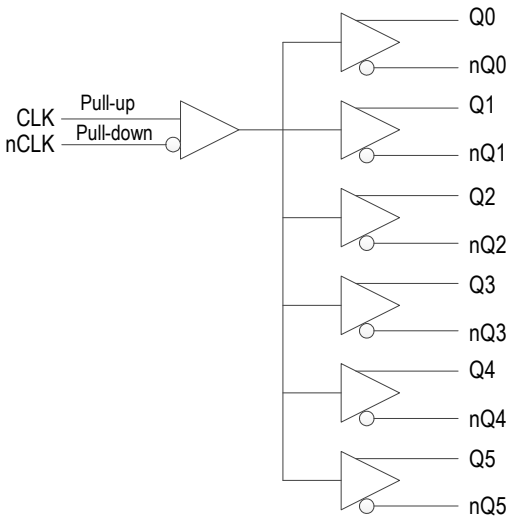
Description

The 854S006 is a low skew, high performance 1-to-6, Differential-to-LVDS fanout buffer. The CLK, nCLK pair can accept most standard differential input levels. The 854S006 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the 854S006 ideal for those clock distribution applications demanding well defined performance and repeatability.

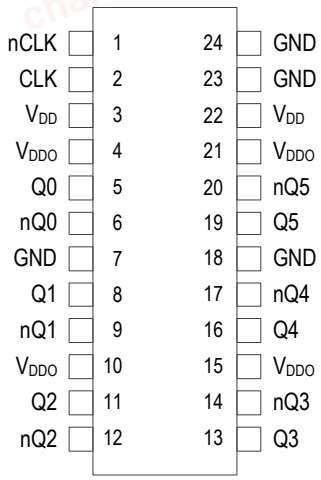
Features

- Six differential LVDS outputs
- One differential clock input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 1.7GHz
- Translates any single-ended input signal to LVDS levels with resistor bias on nCLK input
- Output Skew: 55ps (maximum)
- Propagation delay: 850ps (maximum)
- Additive phase jitter, RMS: 0.067ps (typical)
- Full 3.3V or 2.5V supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



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Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type[a]	Description
1	nCLK	Input (PD)	Inverting differential clock input.
2	CLK	Input (PU)	Non-inverting differential clock input.
3, 22	V_{DD}	Power	Positive supply pins.
4, 10, 15, 21	V_{DDO}	Power	Output supply pins.
5, 6	Q0, nQ0	Output	Differential output pair. LVDS interface levels.
7, 18, 23, 24	GND	Power	Power supply ground.
8, 9	Q1, nQ1	Output	Differential output pair. LVDS interface levels.
11, 12	Q2, nQ2	Output	Differential output pair. LVDS interface levels.
13, 14	Q3, nQ3	Output	Differential output pair. LVDS interface levels.
16, 17	Q4, nQ4	Output	Differential output pair. LVDS interface levels.
19, 20	Q5, nQ5	Output	Differential output pair. LVDS interface levels.

[a] Pull-up (PU) and pull-down (PD) refer to internal input resistors, and are indicated in parentheses.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. Clock Input Function Table

Inputs		Outputs		Input-to-Output Mode	Polarity
CLK	nCLK	Q[0:5]	nQ[0:5]		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased[a]	LOW	HIGH	Single-ended to Differential	Non-Inverting
1	Biased[a]	HIGH	LOW	Single-ended to Differential	Non-Inverting
Biased[a]	0	HIGH	LOW	Single-ended to Differential	Inverting
Biased[a]	1	LOW	HIGH	Single-ended to Differential	Inverting

[a] Refer to the Application Information section, Wiring the Differential Input to Accept Single-ended Levels.

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Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 854S006 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD}+0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	70°C/W (0mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 5. Power Supply DC Characteristics, V_{DD} = V_{DDO} = 3.3V ±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				55	mA
I_{DDO}	Output Supply Current				105	mA

Table 6. Power Supply DC Characteristics, V_{DD} = V_{DDO} = 2.5V ±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				55	mA
I_{DDO}	Output Supply Current				102	mA

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Table 7. Differential DC Characteristics, V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V or 2.625V			10	µA
		nCLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = V_{IN} = 3.465V or 2.625V	-150			µA
		nCLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
V_{PP}	Peak-to-Peak Input Voltage[a]			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage[a][b]			GND +0.5		V_{DD} – 0.85	V

[a] V_{IL} should not be less than -0.3V.

[b] Common mode voltage is defined as V_{IH}.

Table 8. LVDS DC Characteristics, V_{DD} = V_{DDO} = 3.3V ±5%, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		326		526	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.28		1.44	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

[a] For output information, refer to the Parameter Measurement Information.

Table 9. LVDS DC Characteristics, V_{DD} = V_{DDO} = 2.5V ±5%, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		305		505	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.1		1.45	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

[a] For output information, refer to the Parameter Measurement Information.

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AC Electrical Characteristics

Table 10. AC Characteristics, V_{DD} = V_{DDO} = 3.3V ±5%, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		0		1.7	GHz
t_{PD}	Propagation Delay[b]		300		850	ps
*t*sk(o)	Output Skew[c][d]				55	ps
*t*sk(pp)	Part-to-Part Skew[d][e]				150	ps
*t*jit	Buffer Additive Phase Jitter, RMS; see Additive Phase Jitter	622.08MHz, Integration Range: 12kHz – 5MHz		0.067		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		250	ps
odc	Output Duty Cycle	≤1.2GHz	47		53	%

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Measured from the differential input crossing point to the differential output crossing point.

[c] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing point.

[d] This parameter is defined in accordance with JEDEC Standard 65.

[e] Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Table 11. AC Characteristics, V_{DD} = V_{DDO} = 2.5V ±5%, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		0		1.7	GHz
t_{PD}	Propagation Delay[b]		300		800	ps
*t*sk(o)	Output Skew[c][d]				55	ps
*t*sk(pp)	Part-to-Part Skew[d][e]				150	ps
*t*jit	Buffer Additive Phase Jitter, RMS; see Additive Phase Jitter	622.08MHz, Integration Range: 12kHz – 5MHz		0.067		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		250	ps
odc	Output Duty Cycle	≤1.2GHz	47		53	%

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Measured from the differential input crossing point to the differential output crossing point.

[c] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing point.

[d] This parameter is defined in accordance with JEDEC Standard 65.

[e] Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

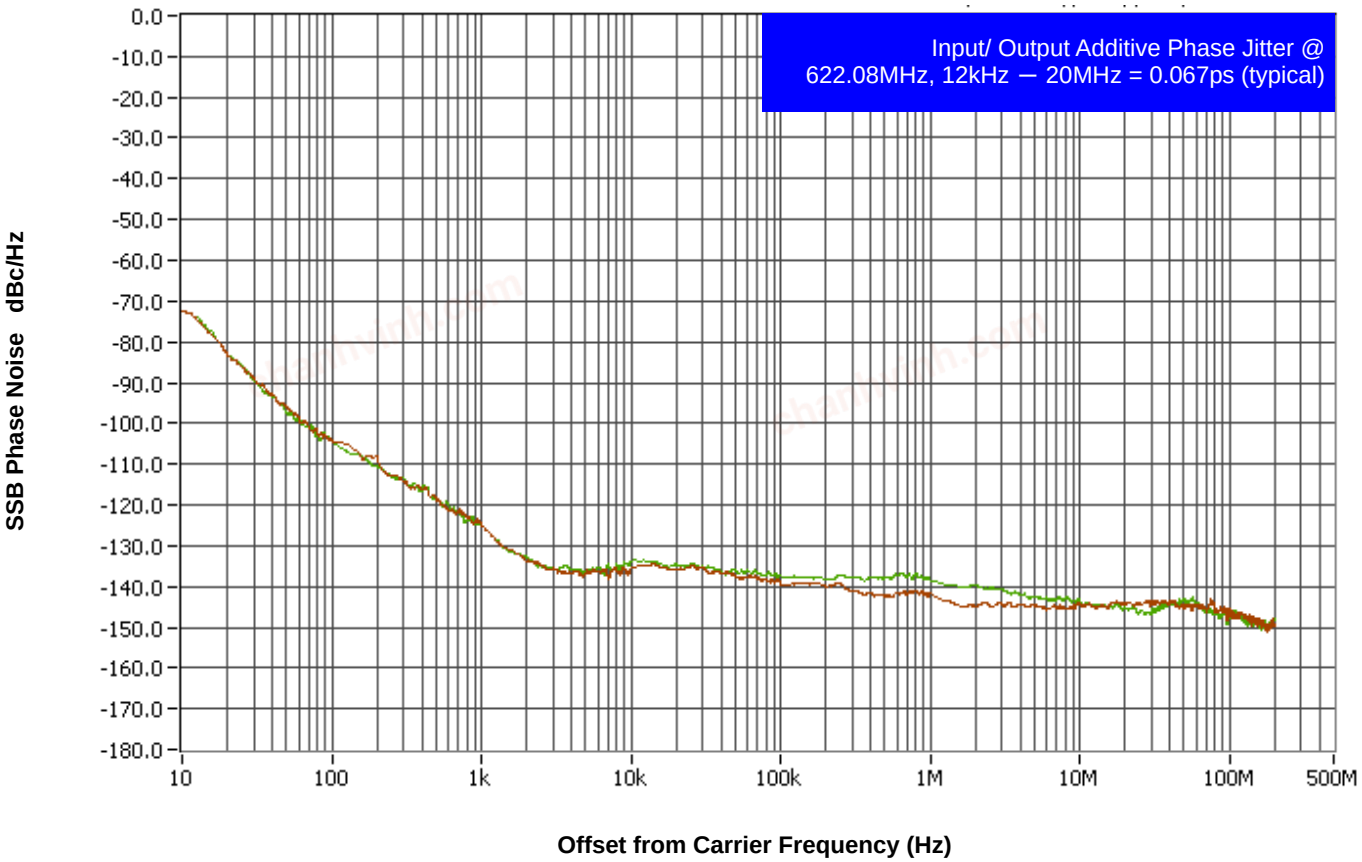
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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Figure 1. Additive Phase Jitter Plot



As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

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Parameter Measurement Information

Figure 2. 3.3V Core/ 3.3V Output Load AC Test Circuit

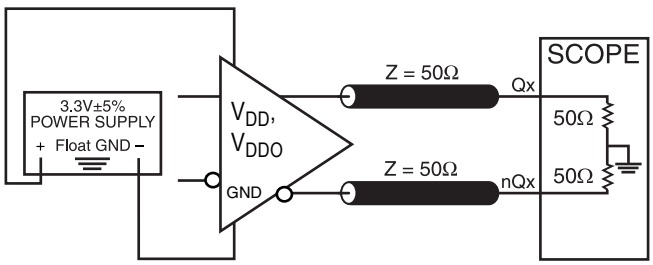


Figure 3. 2.5V Core/ 2.5V Output Load AC Test Circuit

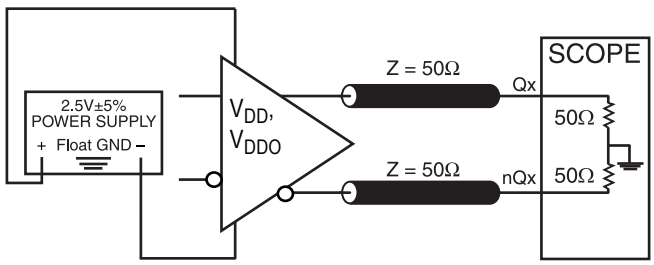


Figure 4. Differential Input Level

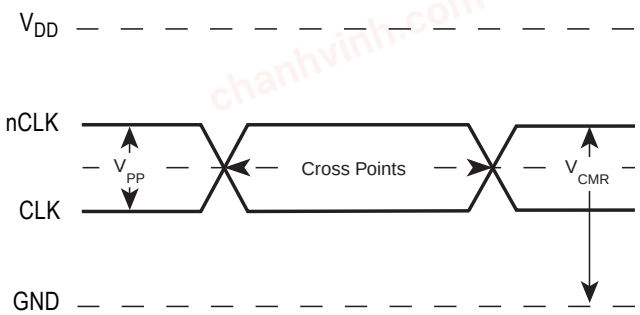


Figure 5. Output Skew

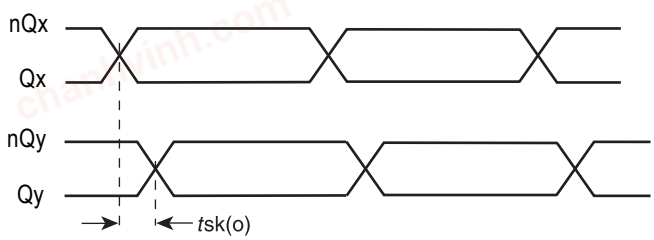


Figure 6. Output Rise/ Fall Time

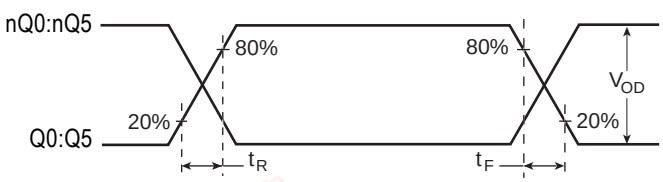
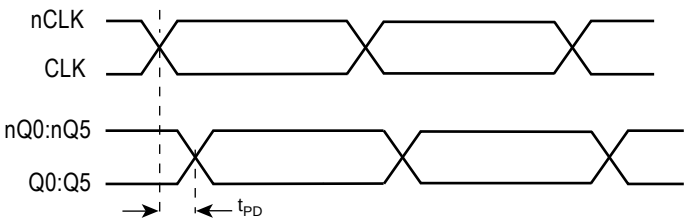


Figure 7. Propagation Delay



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Parameter Measurement Information

Figure 8. Output Duty Cycle/ Pulse Width/ Period

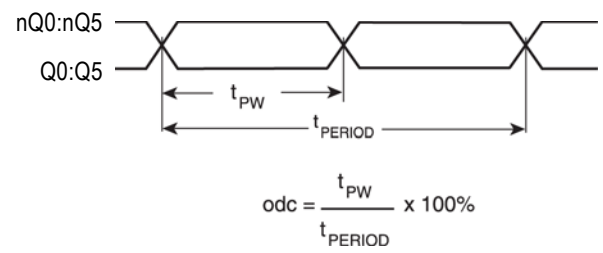


Figure 9. Part-to-Part Skew

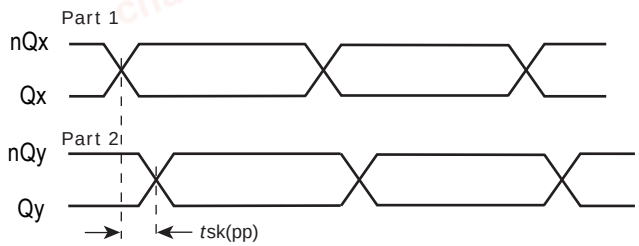


Figure 10. Differential Output Voltage Setup

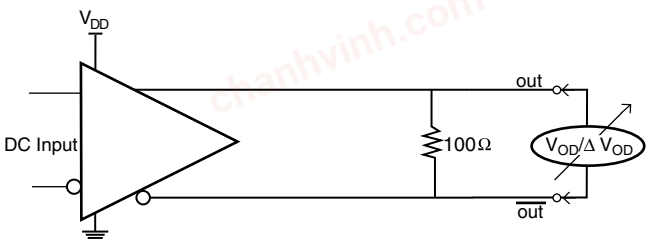
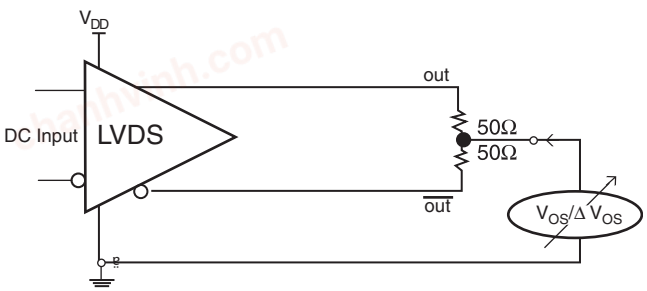


Figure 11. Offset Voltage Setup



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Applications Information

Recommendations for Unused Input and Output Pins

Outputs:

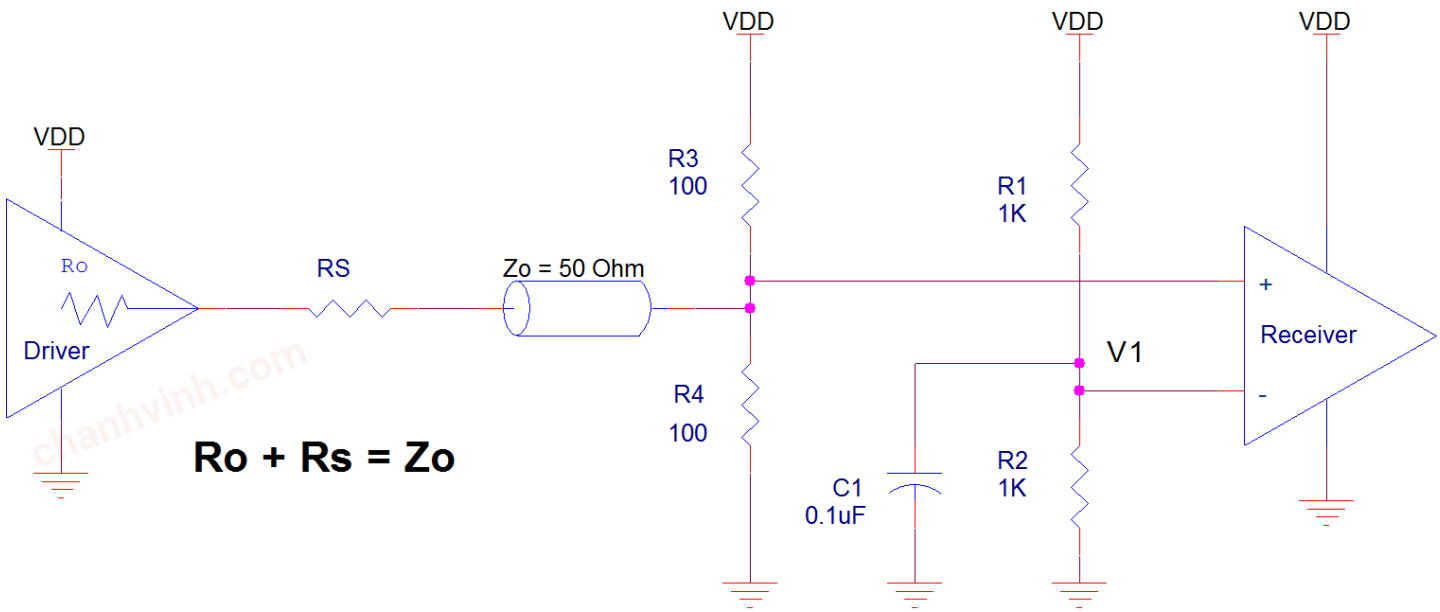
LVDS Outputs

Any unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

Wiring the Differential Input to Accept Single-ended Levels

Figure 12 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} +0.3V. Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 12. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



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3.3V Differential Clock Input Interface

CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figure 13 to Figure 18 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 13, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 13. CLK/ nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

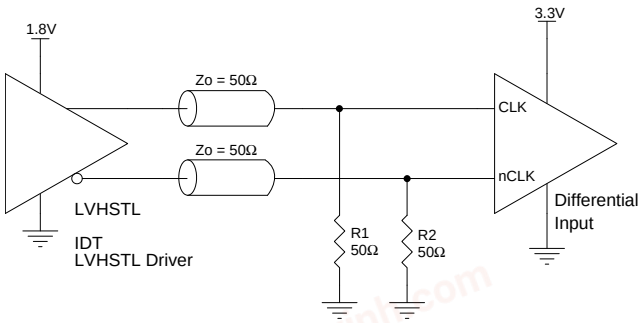


Figure 14. CLK/ nCLK Input Driven by a 3.3V LVPECL Driver

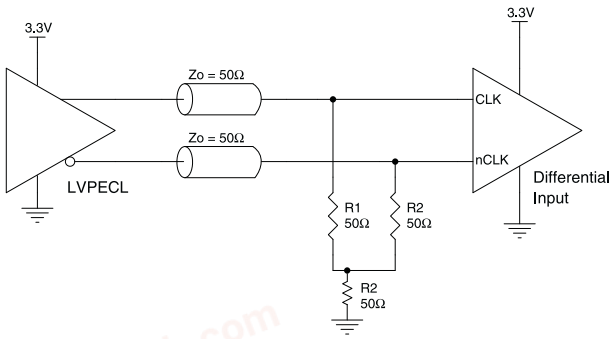


Figure 15. CLK/ nCLK Input Driven by a 3.3V LVPECL Driver

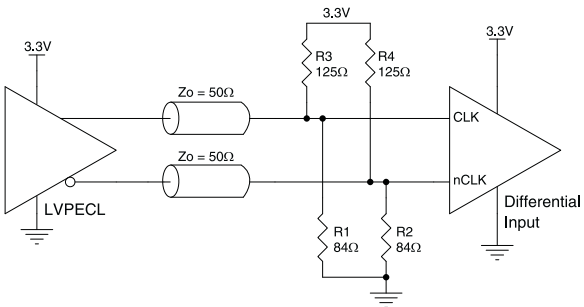


Figure 16. CLK/ nCLK Input Driven by a 3.3V LVDS Driver

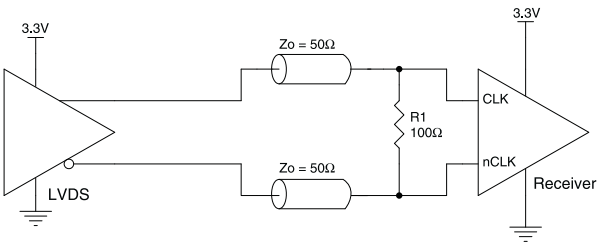


Figure 17. CLK/ nCLK Input Driven by a 3.3V HCSL Driver

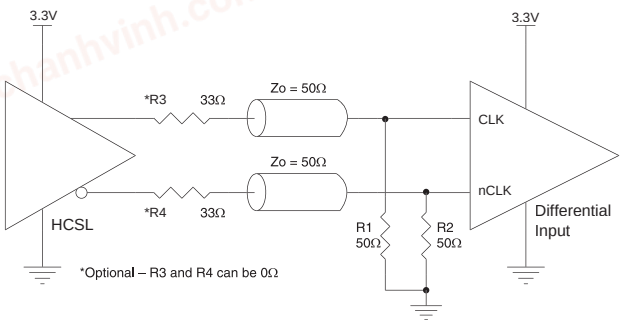
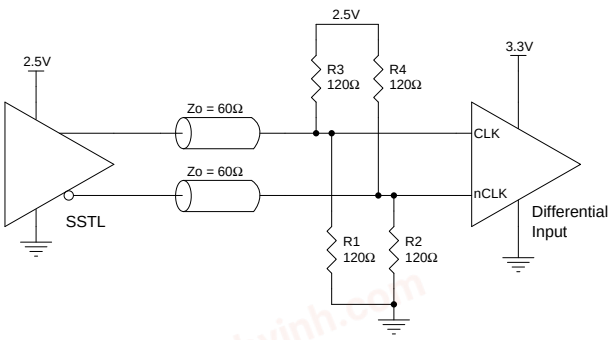


Figure 18. CLK/ nCLK Input Driven by a 2.5V SSTL Driver



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2.5V Differential Clock Input Interface

CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figure 19 to Figure 24 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 19, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 19. CLK/ nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

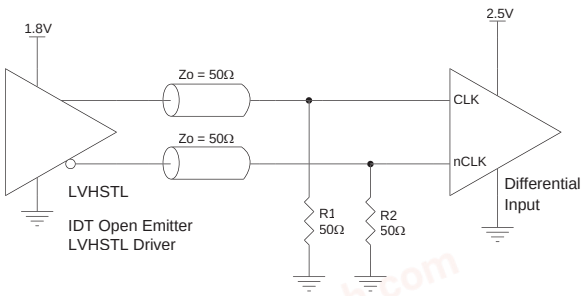


Figure 20. CLK/ nCLK Input Driven by a 2.5V LVPECL Driver

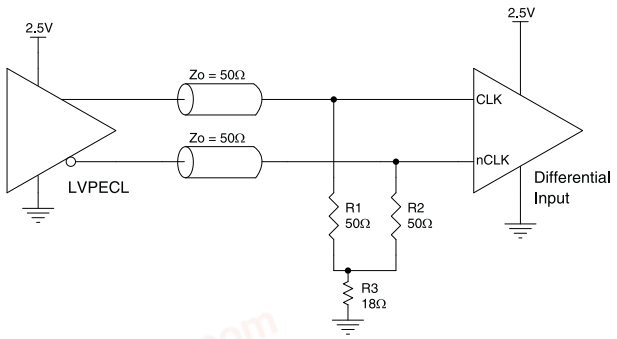


Figure 21. CLK/ nCLK Input Driven by a 2.5V LVPECL Driver

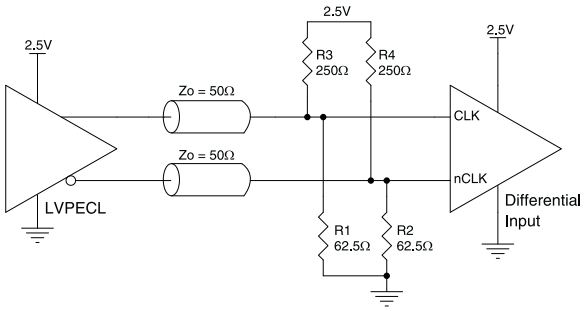


Figure 22. CLK/ nCLK Input Driven by a 2.5V LVDS Driver

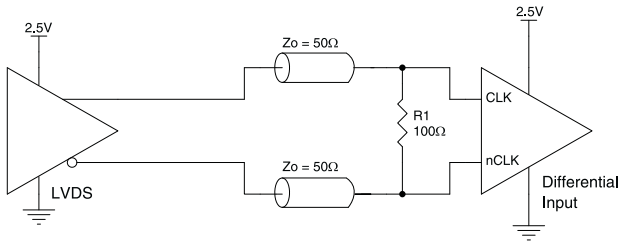


Figure 23. CLK/ nCLK Input Driven by a 2.5V HCSL Driver

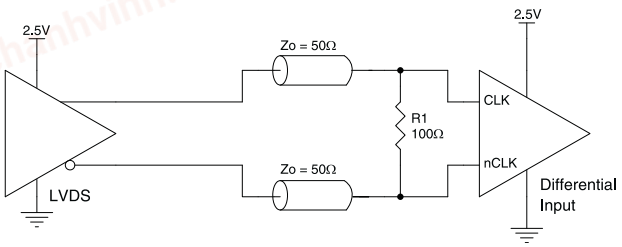
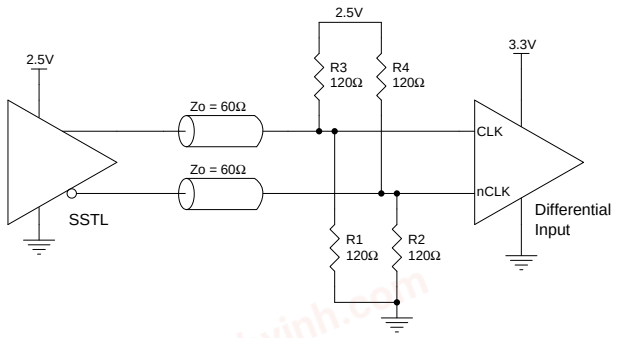


Figure 24. CLK/ nCLK Input Driven by a 2.5V SSTL Driver



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LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 25 can be used with either type of output structure. Figure 26, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 25. Standard LVDS Termination

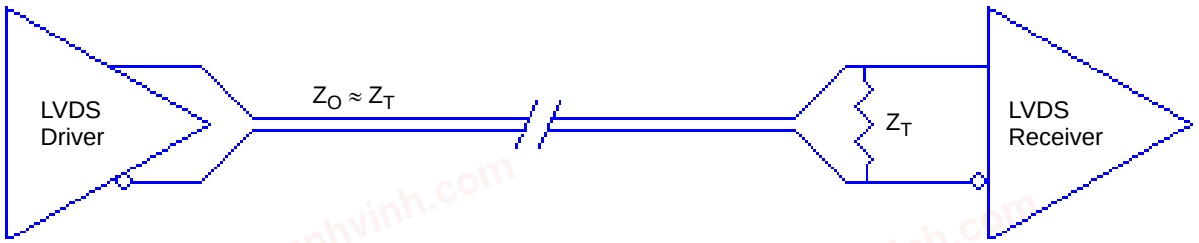
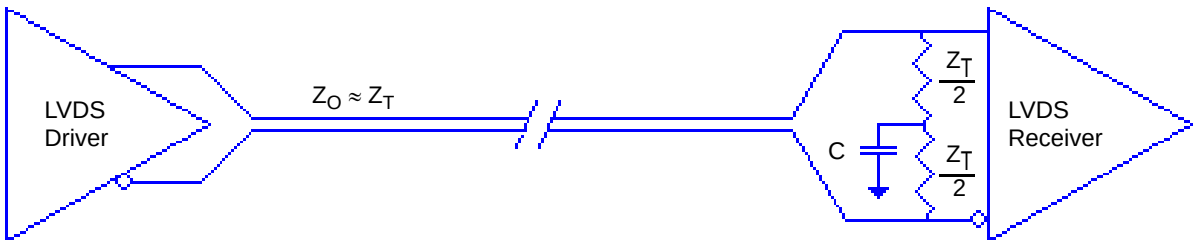


Figure 26. Optional LVDS Termination



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Power Considerations

This section provides information on power dissipation and junction temperature for the 854S006.
Equations and example calculations are also provided.

1. Power Dissipation

The total power dissipation for the 854S006 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V +5% = 3.465V, which gives worst case results.

Power $(core)_{MAX} = V_{DD_MAX} \times I_{DD_MAX}$ = 3.465V x 55mA = 190.575mW

Power $(outputs)_{MAX} = V_{DDO_MAX} \times I_{DDO_MAX}$ = 3.465V x 105mA = 363.825mW

Total $Power_{MAX}$ = 190.575mW x 363.825mW = 554.4mW

2. Junction Temperature

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} \times Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 70°C/W Table 12 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.554W x 70°C/W = 123.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 12. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

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Reliability Information

Table 13. θ_{JA} vs. Air Flow for 24-Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

Transistor Count

854S006 transistor count: 293

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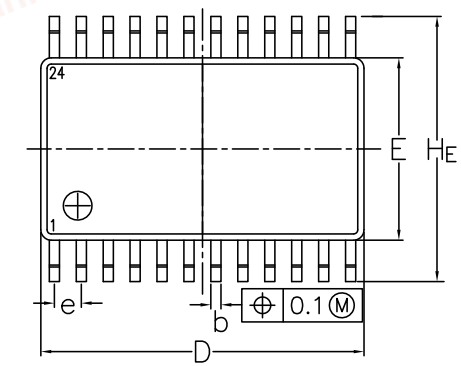
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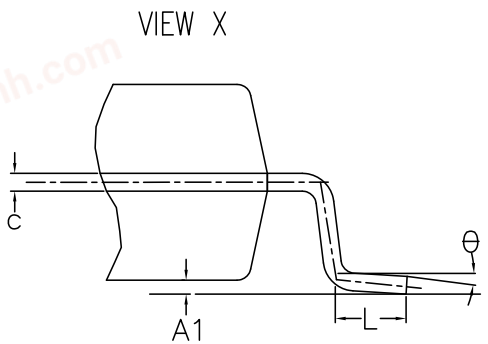
BASED ON JEDEC JEP95: MO-153

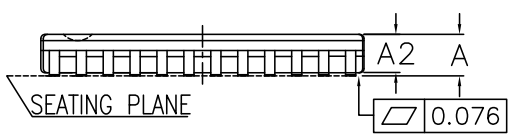
DIMENSIONS IN MILLIMETERS

1. DIMENSIONS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	2/29/16	J.H







DIMENSIONS	min	max
A	0.90	1.10
A1	0.05	0.15
A2	0.85	0.95
b	0.19	0.30
c	0.09	0.20
D	7.7	7.9
E	4.3	4.5
e	0.65nom	
H_E	6.3	6.5
L	0.5	0.7
θ	0°	8°

* WITHOUT MOLD FLASH

2. WEIGHT ≤ 0.09 g
3. BODY MATERIAL LOW STRESS EPOXY
4. LEAD MATERIAL Cu-ALLOY
5. LEAD FINISH SOLDER PLATING
6. LEAD FORM Z-BENDS

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572	
APPROVALS	DATE	TITLE	PG24 PACKAGE OUTLINE 4.4mm TSSOP
DRAWN PAC	2/29/16		
CHECKED			
		SIZE C	DRAWING No. PSC-4056-03 REV 00
		DO NOT SCALE DRAWING	SHEET 1 OF 1

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Ordering Information

Orderable Part Number	Marking	Package	Carrier Type	Temperature
854S006AGILF	ICS854S006AIL	4.4 x 7.8 x 0.925 mm 24-TSSOP	Tray	-40° to +85°C
854S006AGILFT	ICS854S006AIL	4.4 x 7.8 x 0.925 mm 24-TSSOP	Tape and Reel	-40° to +85°C

Revision History

Revision Date	Description of Change
April 11, 2017	▪ Table 10 and Table 11 AC Characteristics: – added part-to-part skew spec – added minimum f_{MAX} spec. ▪ Parameter Measurement Information — Figure 9 added part-to-part skew diagram. ▪ Applications Information: – Updated Wiring the Differential Input to Accept Single-ended Levels – Updated LVDS Driver Termination ▪ Updated Package Drawings ▪ Updated datasheet format.
January 19, 2016	▪ Removed ICS from the part numbers where needed. ▪ General Description — removed ICS chip. ▪ Ordering Information — removed quantity from tape and reel. Deleted the LF note below the table. ▪ Updated header and footer.
January 18, 2010	▪ Block Diagram — changed CLK to “pullup” and nCLK to “pulldown”. ▪ Pin Descriptions — changed CLK and nCLK “Type” to reflect block diagram. ▪ Differential DC Characteristics Table – I_{IH} parameters, changed CLK levels from 150uA max. to 10uA max.; nCLK levels from 5uA max. to 150uA max. – I_{IL} parameters, changed CLK levels from -5uA min. to -150uA min.; nCLK levels from -150uA min. to -10uA min. ▪ Added thermal note. ▪ Updated Differential Clock Input Interface section.
July 20, 2009	▪ LVDS DC Characteristics Table — changed V_{OD} units from V to mV. ▪ Ordering Information Table — deleted “ICS” prefix from Part/Order column. ▪ Changed style of header/footer.

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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