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4:1, Differential-To-3.3V, 2.5V LVPECL/ECL Clock Data Multiplexer

853S057

DATASHEET

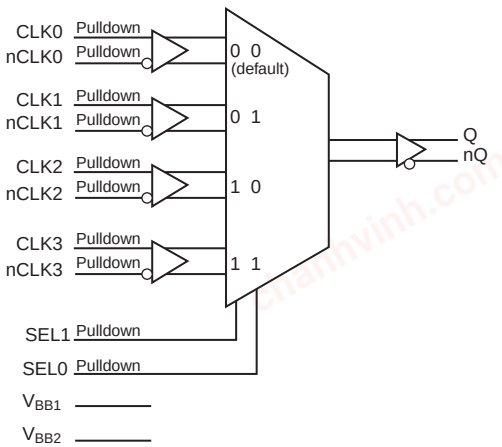
Description

The 853S057 is a 4:1 Differential-to-3.3V or 2.5V LVPECL/ECL Clock/Data Multiplexer which can operate up to 3GHz. The 853S057 has 4 differential selectable clock input pairs. The CLK, nCLK input pairs can accept LVPECL, LVDS, CML or SSTL levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The multiplexer select control inputs have ECL/LVPECL interface levels. The select pins have internal pull-down resistors.

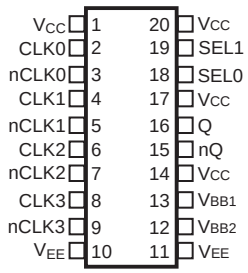
Features

- High speed 4:1 differential multiplexer
- One differential 3.3V, 2.5V LVPECL/ECL output
- Four differential CLKx, nCLKx input pairs
- Differential CLKx, nCLKx pairs can accept the following interface levels: LVPECL, LVDS, CML, SSTL
- Maximum input/output frequency: 3GHz
- Additive phase jitter, RMS at 622.08MHz: 0.073ps (typical)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 615ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.465V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



853S057

20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 14, 17, 20	V_{CC}	Power		Positive supply pins.
2	CLK0	Input	Pulldown	Non-inverting differential clock input.
3	nCLK0	Input	Pulldown	Inverting differential clock input.
4	CLK1	Input	Pulldown	Non-inverting differential clock input.
5	nCLK1	Input	Pulldown	Inverting differential clock input.
6	CLK2	Input	Pulldown	Non-inverting differential clock input.
7	nCLK2	Input	Pulldown	Inverting differential clock input.
8	CLK3	Input	Pulldown	Non-inverting differential clock input.
9	nCLK3	Input	Pulldown	Inverting differential clock input.
10, 11	V_{EE}	Power		Negative supply pins.
12, 13	V_{BB2}, V_{BB1}	Output		ECL reference outputs.
15, 16	nQ, Q	Output		Differential output pair. ECL/LVPECL interface levels.
18, 19	SEL0, SEL1	Input	Pulldown	Clock select inputs. ECL/LVPECL or LVCMOS interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. Control Input Function Table

Control Inputs		Clock Out
SEL1	SEL0	Q, nQ
0	0 (default)	CLK0, nCLK0
0	1	CLK1, nCLK1
1	0	CLK2, nCLK2
1	1	CLK3, nCLK3

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	87.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.465V; V_{EE} = 0V, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.465	V
I_{EE}	Power Supply Current				25	mA

Table 4B. DC Characteristics, V_{CC} = 2.375V to 3.465V; V_{EE} = 0V, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{PP}	Input Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Range; NOTE 1, 2			1.2		V_{CC}	V
I_{IH}	Input High Current	CLK[0:3], nCLK[0:3]	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK[0:3], nCLK[0:3]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

Table 4C. LVPECL DC Characteristics, V_{CC} = 2.375V to 3.465V; V_{EE} = 0V, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{swing}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

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Table 4D. ECL DC Characteristics, V_{CC} = 0V; V_{EE} = -2.375V to -3.465V, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		-1.125		-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895		-1.67	V
V_{BB1}, V_{BB2}	Output Voltage Reference; NOTE 2			-1.3		V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.

AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 2.375V to 3.465V; V_{EE} = 0V or V_{CC} = 0V; V_{EE} = -3.8V to -2.375V, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				3	GHz
*t*jit	Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	622.08MHz, 12kHz – 20MHz		0.073		ps
t_{PD}	Propagation Delay; NOTE 1		300		615	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				250	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	70		220	ps
$MUX_{ISOLATION}$	MUX Isolation	622.08MHz, V_{IN} 1.6V to 2.4V		-59		dB

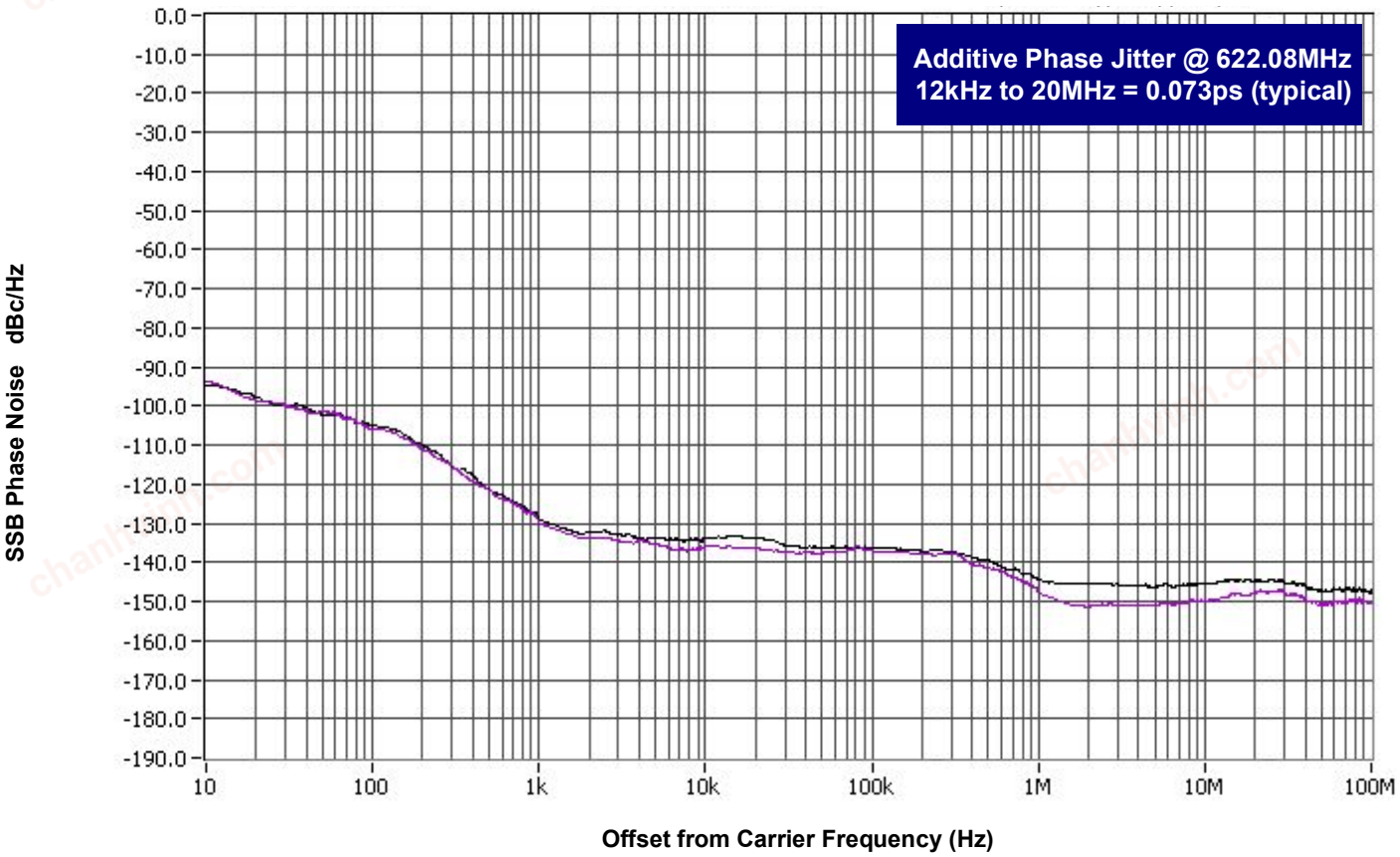
All parameters measured up to 1.5GHz, unless otherwise noted.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined according with JEDEC Standard 65.

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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

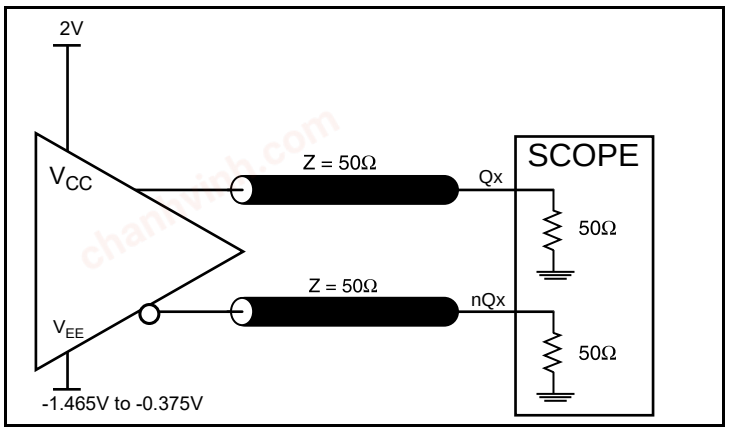


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

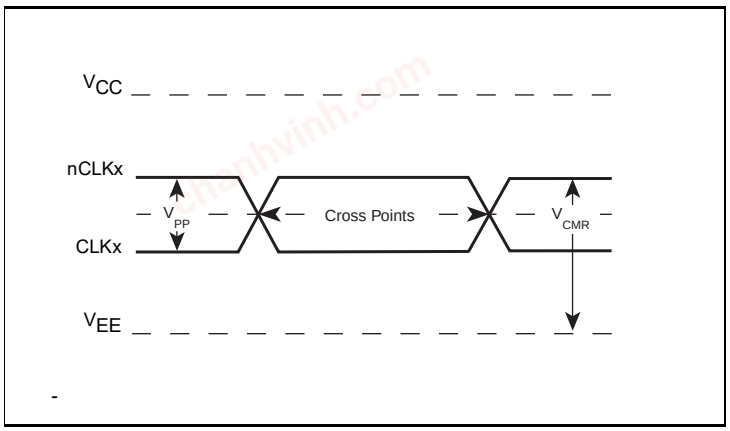
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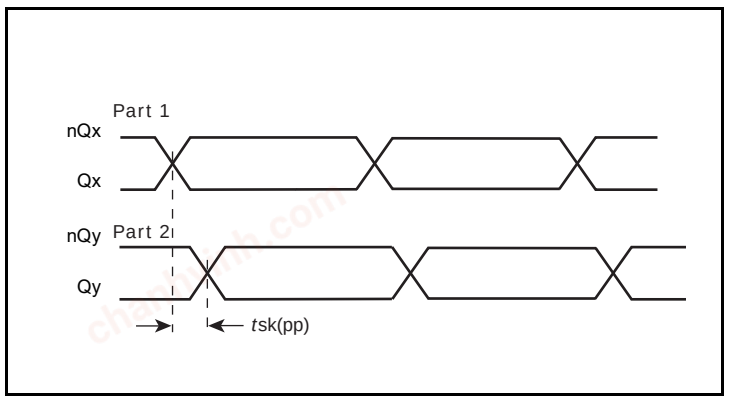
Parameter Measurement Information



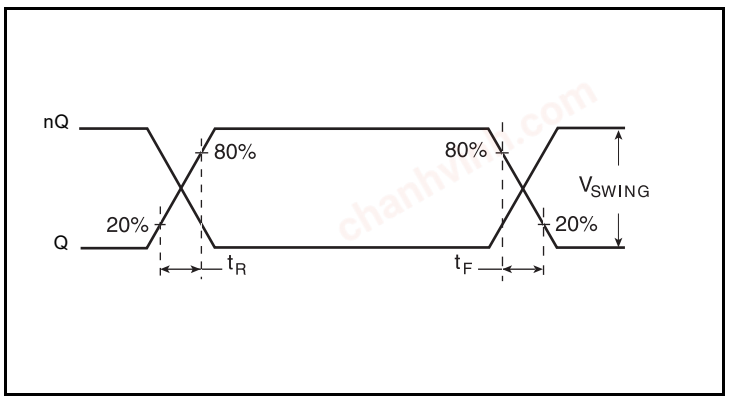
LVPECL Output Load AC Test Circuit



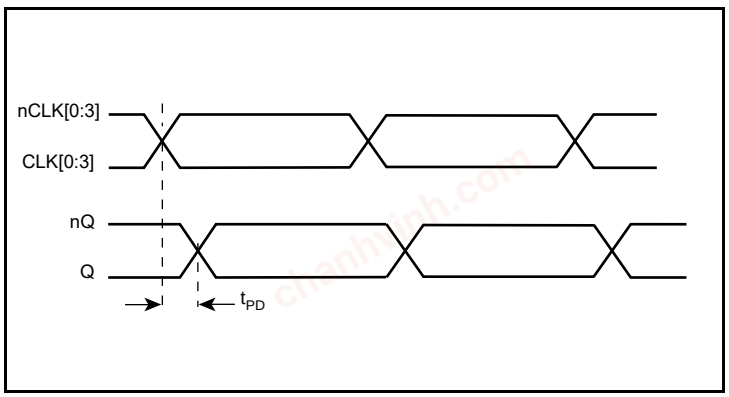
Differential Input Level



Part-to-Part Skew



Output Rise/Fall Time



Propagation Delay

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Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

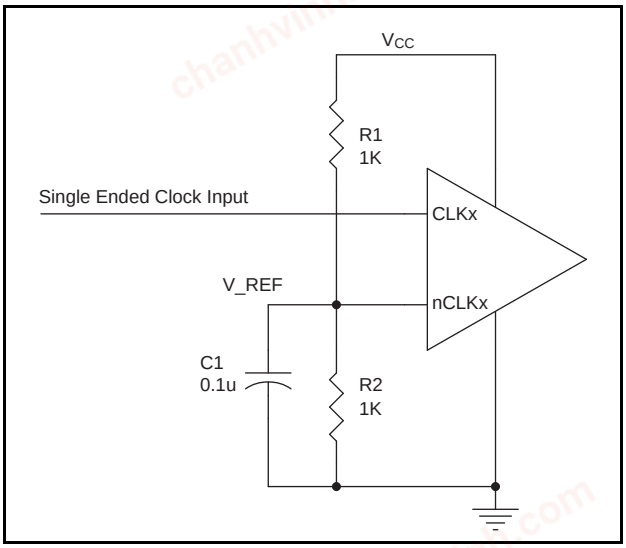


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, a 1kΩ resistor should be tied from nCLK to V_{CC}.

Single-ended LVPECL Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

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Clock Input Interface

The CLK/nCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to2E* show interface examples for the HiPerClockS CLK /nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

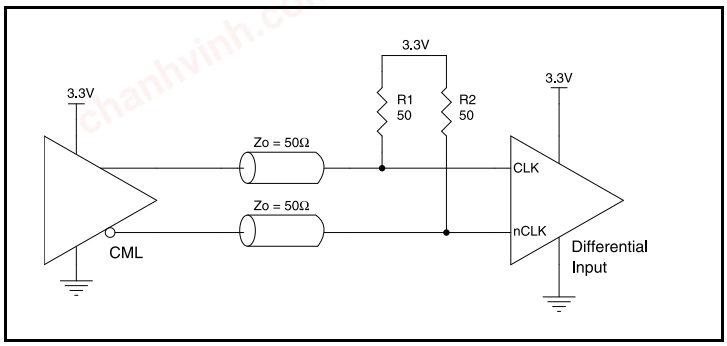


Figure 2A. HiPerClockS CLK/nCLK Input Driven by a CML Driver

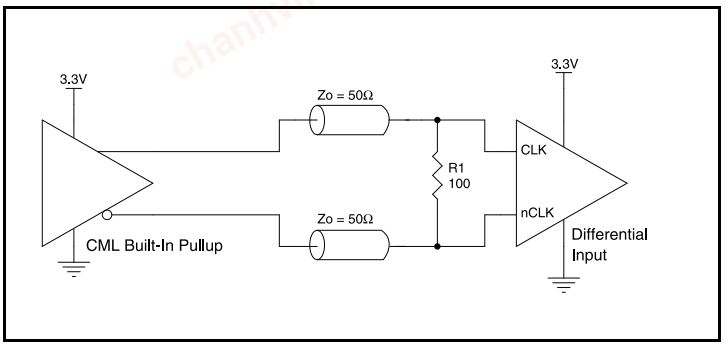


Figure 2B. HiPerClockS CLK/nCLK Input Driven by a Built-In Pullup CML Driver

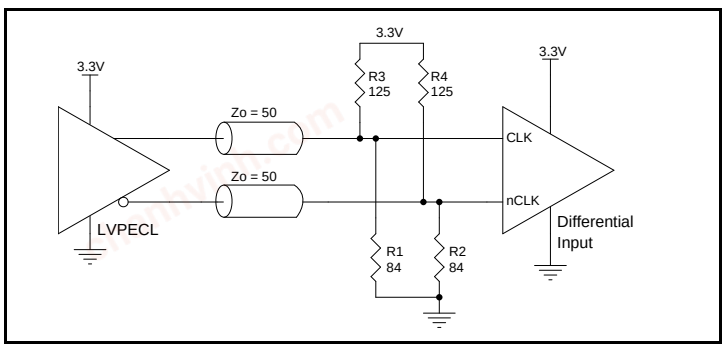


Figure 2C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

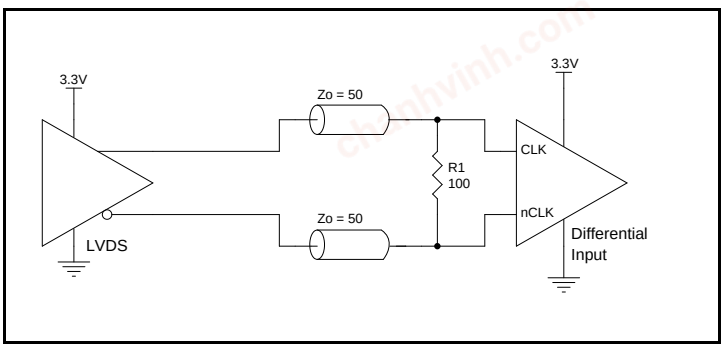


Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

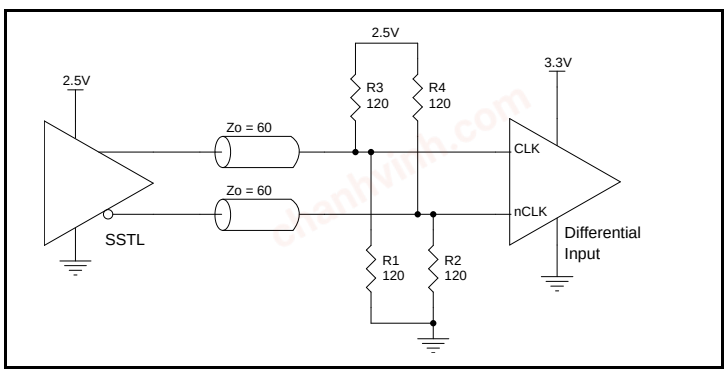


Figure 2E. HiPerClockS CLK/nCLK Input Driven by an SSTL Driver

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Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines.

Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

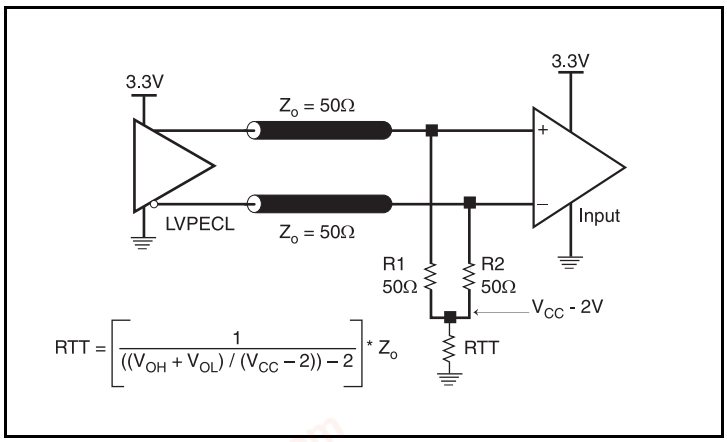


Figure 3A. 3.3V LVPECL Output Termination

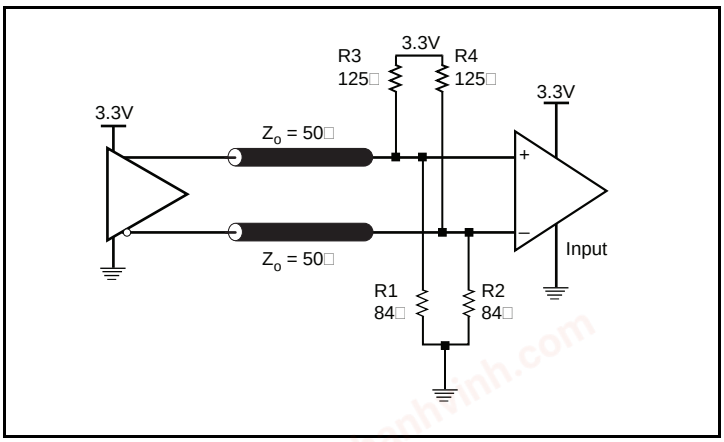


Figure 3B. 3.3V LVPECL Output Termination

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Termination for 2.5V LVPECL Outputs

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

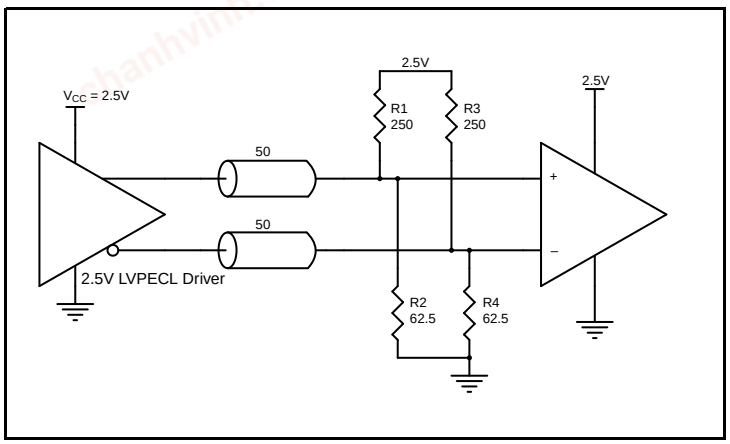


Figure 4A. 2.5V LVPECL Driver Termination Example

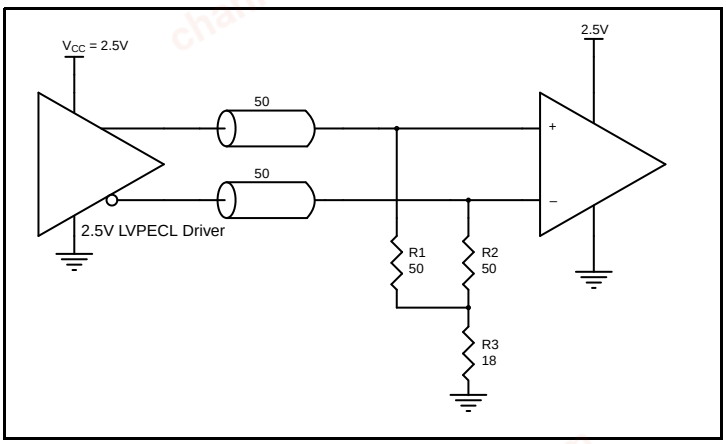


Figure 4B. 2.5V LVPECL Driver Termination Example

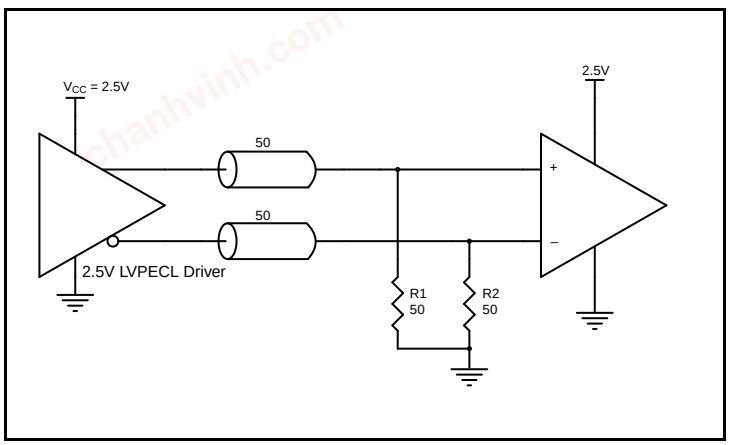


Figure 4C. 2.5V LVPECL Driver Termination Example

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS53S057I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS53S057I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.465V * 25mA = **86.625mW**
- Power $(outputs)_{MAX}$ = **31.1mW/Loaded Output pair**

Total Power$_{MAX}$ (3.3V, with all outputs switching) = 86.625mW + 31.1mW = **117.725mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 87.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.118W * 87.2°C/W = 95.3°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.2°C/W	82.9°C/W	80.7°C/W

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3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

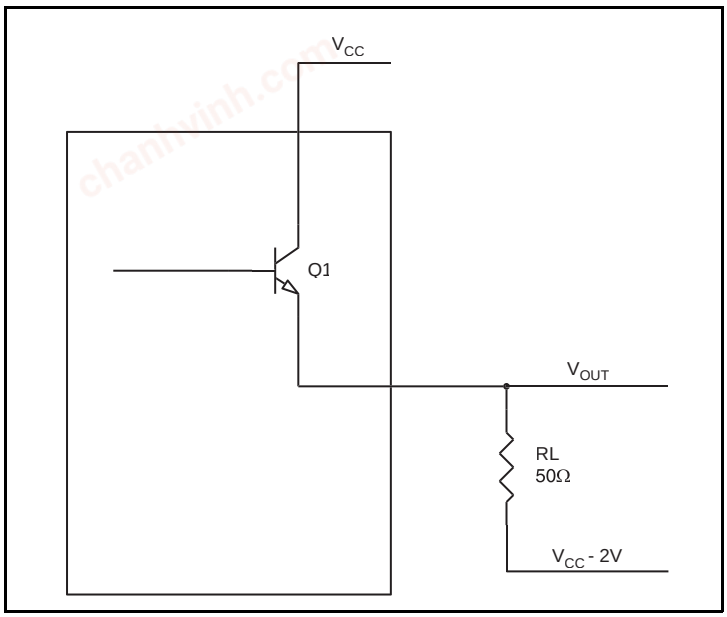


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} – 0.935V}$
  $(V_{CC_MAX} – V_{OH_MAX}) = \mathbf{0.935V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} – 1.67V}$
  $(V_{CC_MAX} – V_{OL_MAX}) = \mathbf{1.67V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) = [(2V – (V_{CC_MAX} – V_{OH_MAX}))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) =$
$[(2V – 0.935V)/50Ω] * 0.935V =$ **19.9mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) = [(2V – (V_{CC_MAX} – V_{OL_MAX}))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) =$
$[(2V – 1.67V)/50Ω] * 1.67V =$ **11.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.1mW**

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.2°C/W	82.9°C/W	80.7°C/W

Transistor Count

The transistor count for 853S057 is: 251

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S057AGILF	ICS53S057AIL	"Lead-Free" 20-TSSOP	Tube	-40°C to +85°C
853S057AGILFT	ICS53S057AIL		2500 Tape & Reel	-40°C to +85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

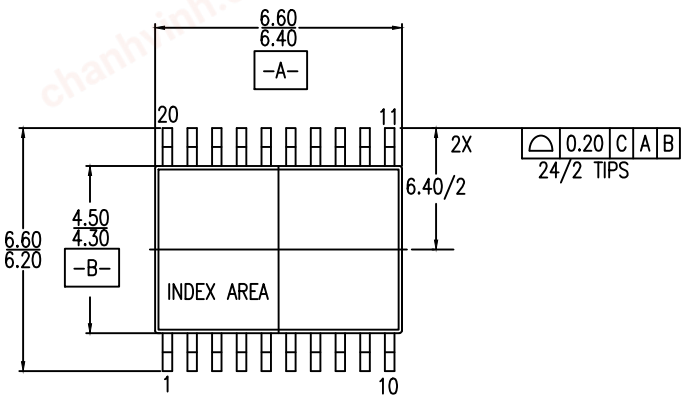
Revision Date	Description of Change
August 13, 2021	Updated VCMR specifications in table 4B.
May 28, 2020	• Updated the title description for Table 4D. • Added a link to the latest package outline drawing; however, no technical changes
May 16, 2012	Pin Description Table - Pins 18 and 19 (SELx description) added LVCMOS levels.
July 30, 2009	AC Characteristics Table - added Thermal Note. Recommendations for Unused Input Pins - modified CLK/nCLK Input paragraph. Changed datasheet Header/Footer.

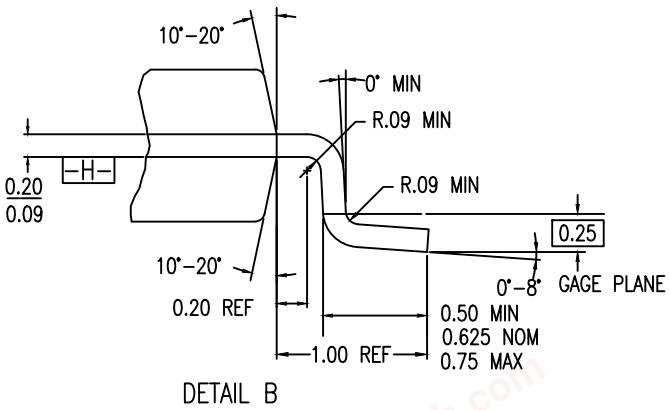
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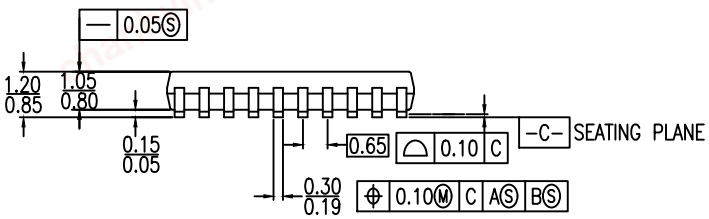
20-TSSOP Package Outline Drawing

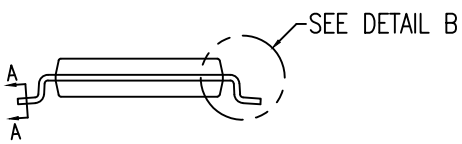
4.4 mm Body 0.65mm Pitch

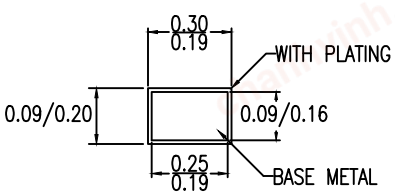




DETAIL B







SECTION A-A

NOTES:

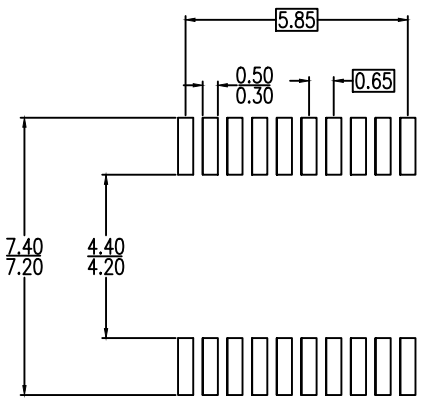
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSION ARE IN MM.

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20-TSSOP Package Outline Drawing

4.4 mm Body 0.65mm Pitch



RECOMMENDED LAND PATTERN DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
July 24, 2018	Rev 00	Initial Release

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