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LOW-VOLTAGE OCTAL BUS SWITCH

74CBTLV3245

FEATURES:

- **Pin-out compatible with standard '245 Logic products**
- **5Ω A/B bi-directional switch**
- **Isolation under power-off conditions**
- **Over-voltage tolerant**
- **Latch-up performance exceeds 100mA**
- **Vcc = 2.3V - 3.6V, Normal Range**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Available in QSOP and TSSOP packages**

APPLICATIONS:

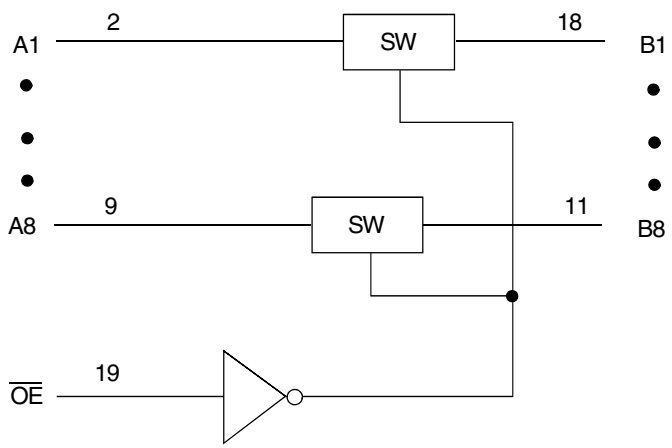
- **3.3V High Speed Bus Switching and Bus Isolation**

DESCRIPTION:

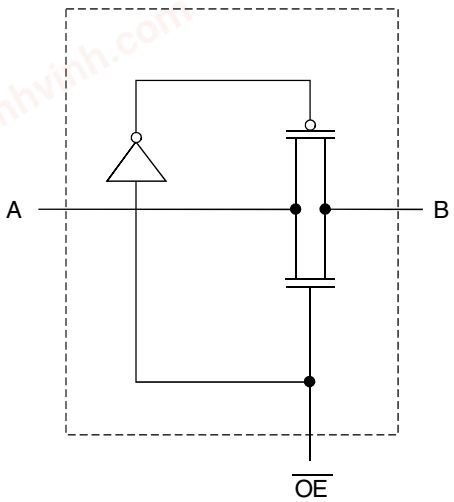
The octal bus switch has standard 245 pinouts. The CBTLV3245 is designed for asynchronous communication between data buses. When Output Enable ($\overline{OE}$) is low, the 8-bit bus switch is on and port A is connected to Port B. When $\overline{OE}$ is high, the switch is off and a high impedance exists between Port A and Port B.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to Vcc through a pullup resistor.

FUNCTIONAL BLOCK DIAGRAM



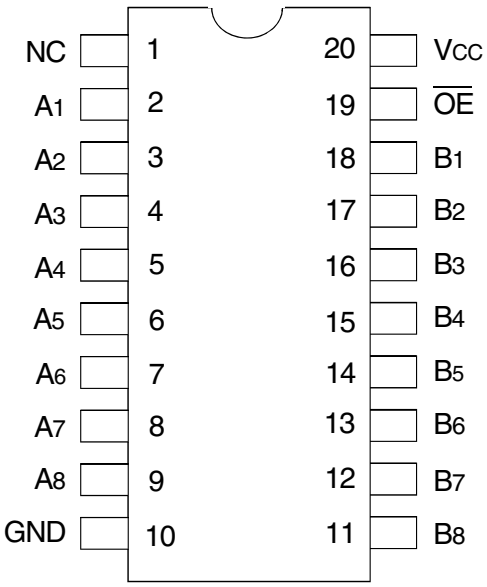
SIMPLIFIED SCHEMATIC, EACH SWITCH



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PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
TSSOP	PGG20	PGG
QSOP	PCG20	QG

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{CC}	SupplyVoltage Range	–0.5 to +4.6	V
V_I	Input Voltage Range	–0.5 to +4.6	V
	Continuous Channel Current	128	mA
I_{IK}	Input Clamp Current, $V_{I/O} < 0$	–50	mA
T_{STG}	Storage Temperature	–65 to +150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable (Active LOW)
Ax	Port A Inputs or Outputs
Bx	Port B Inputs or Outputs

FUNCTION TABLE(1)

Input $\overline{OE}$	Operation
L	A Port = B Port
H	Isolation

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level

OPERATING CHARACTERISTICS, T_A = 25°C(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		2.3	3.6	V
V_{IH}	High-Level Control Input Voltage	V_{CC} = 2.3V to 2.7V	1.7	—	V
		V_{CC} = 2.7V to 3.6V	2	—	
V_{IL}	Low-Level Control Input Voltage	V_{CC} = 2.3V to 2.7V	—	0.7	V
		V_{CC} = 2.7V to 3.6V	—	0.8	
T_A	Operating Free-Air Temperature		–40	85	°C

NOTE:
1. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IK}	Control Inputs, Data Inputs	V_{CC} = 3V, I_I = –18mA		—	—	–1.2	V
I_I	Control Inputs	V_{CC} = 3.6V, V_I = V_{CC} or GND		—	—	±1	µA
I_{OZ}	Data I/O	V_{CC} = 3.6V, V_O = 0 or 3.6V, switch disabled		—	—	5	µA
I_{OFF}		V_{CC} = 0, V_I or V_O = 0 to 3.6V		—	—	50	µA
I_{CC}		V_{CC} = 3.6V, I_O = 0, V_I = V_{CC} or GND		—	—	10	µA
ΔI_{CC}(2)	Control Inputs	V_{CC} = 3.6V, one input at 3V, other inputs at V_{CC} or GND		—	—	300	µA
C_I	Control Inputs	V_I = 3V or 0		—	4	—	pF
$C_{IO(OFF)}$		V_O = 3V or 0, $\overline{OE}$ = V_{CC}		—	6	—	pF
R_{ON}(3)	V_{CC} = 2.3V Typ. at V_{CC} = 2.5V	V_I = 0	I_O = 64mA	—	5	8	Ω
			I_O = 24mA	—	5	8	
		V_I = 1.7V	I_O = 15mA	—	27	40	
	V_{CC} = 3V	V_I = 0	I_O = 64mA	—	5	7	
			I_O = 24mA	—	5	7	
		V_I = 2.4V	I_O = 15mA	—	10	15	

NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. The increase in supply current is attributable to each current that is at the specified voltage level rather than V_{CC} or GND.
3. This is measured by the voltage drop between the A and B terminals at the indicated current through the switch.

SWITCHING CHARACTERISTICS

Symbol	Parameter	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t_{PD}(1)	Propagation Delay A to B or B to A	–	0.15	–	0.25	ns
t_{EN}	Output Enable Time $\overline{OE}$ to A or B	1	4.5	1	4.2	ns
t_{DIS}	Output Disable Time $\overline{OE}$ to A or B	1	5	1	5	ns

NOTE:
1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance driven by an ideal voltage source (zero output impedance).

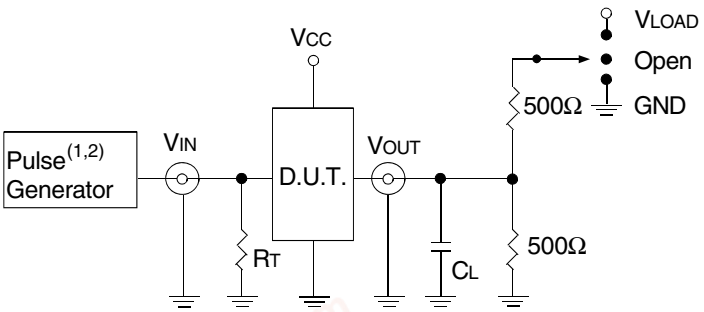
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TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$=3.3V±0.3V	$V_{CC}^{(2)}$=2.5V±0.2V	Unit
V_{LOAD}	6	2 x Vcc	V
V_{IH}	3	Vcc	V
V_T	1.5	Vcc / 2	V
V_{LZ}	300	150	mV
V_{HZ}	300	150	mV
C_L	50	30	pF



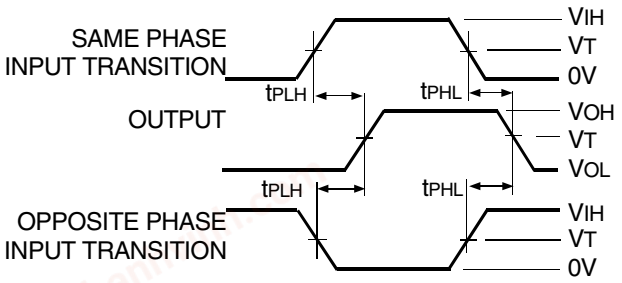
Test Circuits for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

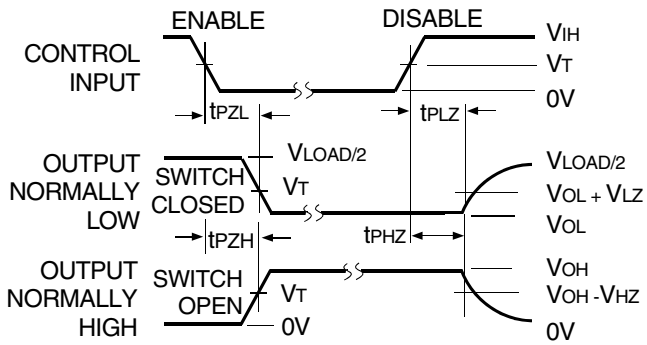
NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2.5ns.

SWITCH POSITION

Test	Switch
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
t_{PD}	Open



Propagation Delay

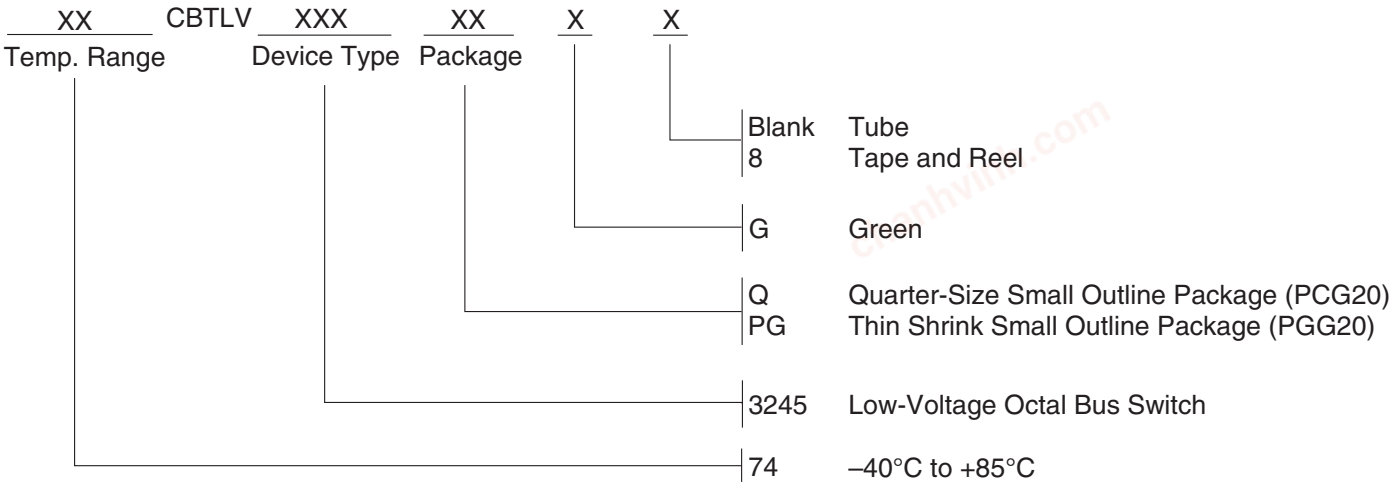


Enable and Disable Times

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ORDERING INFORMATION



Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
	74CBTLV3245PGG	PGG20	TSSOP	I
	74CBTLV3245PGG8	PGG20	TSSOP	I
	74CBTLV3245QG	PCG20	QSOP	I
	74CBTLV3245QG8	PCG20	QSOP	I

Datasheet Document History

12/18/2014	Pg. 5	Updated the ordering information by removing non RoHS part and by adding Tape and Reel information.
05/10/2019	Pg. 2,5	Added table under pin configuration diagram with detailed package information and orderable part information table. Updated the ordering information diagram in clearer detail.

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