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CMOS ASYNCHRONOUS FIFO
2,048 x 9, 4,096 x 9
8,192 x 9, 16,384 x 9
32,768 x 9 and 65,536 x 9

IDT7203
IDT7204
IDT7205
IDT7206
IDT7207
IDT7208

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

FEATURES:

- **First-In/First-Out Dual-Port memory**
- **2,048 x 9 organization (IDT7203)**
- **4,096 x 9 organization (IDT7204)**
- **8,192 x 9 organization (IDT7205)**
- **16,384 x 9 organization (IDT7206)**
- **32,768 x 9 organization (IDT7207)**
- **65,536 x 9 organization (IDT7208)**
- **High-speed: 12ns access time**
- **Low power consumption**
  - *— Active: 660mW (max.)*
  - *— Power-down: 44mW (max.)*
- **Asynchronous and simultaneous read and write**
- **Fully expandable in both word depth and width**
- **720x family is pin and functionally compatible from 256 x 9 to 64k x 9**
- **Status Flags: Empty, Half-Full, Full**
- **Retransmit capability**
- **High-performance CMOS technology**
- **Military product compliant to MIL-STD-883, Class B**
- **Standard Military Drawing for #5962-88669 (IDT7203), 5962-89567 (IDT7203), and 5962-89568 (IDT7204) are listed on this function**
- **Industrial temperature range (–40°C to +85°C) is available (plastic packages only)**
- **Green parts available, see ordering information**

DESCRIPTION:

The IDT7203/7204/7205/7206/7207/7208 are dual-port memory buffers with internal pointers that load and empty data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

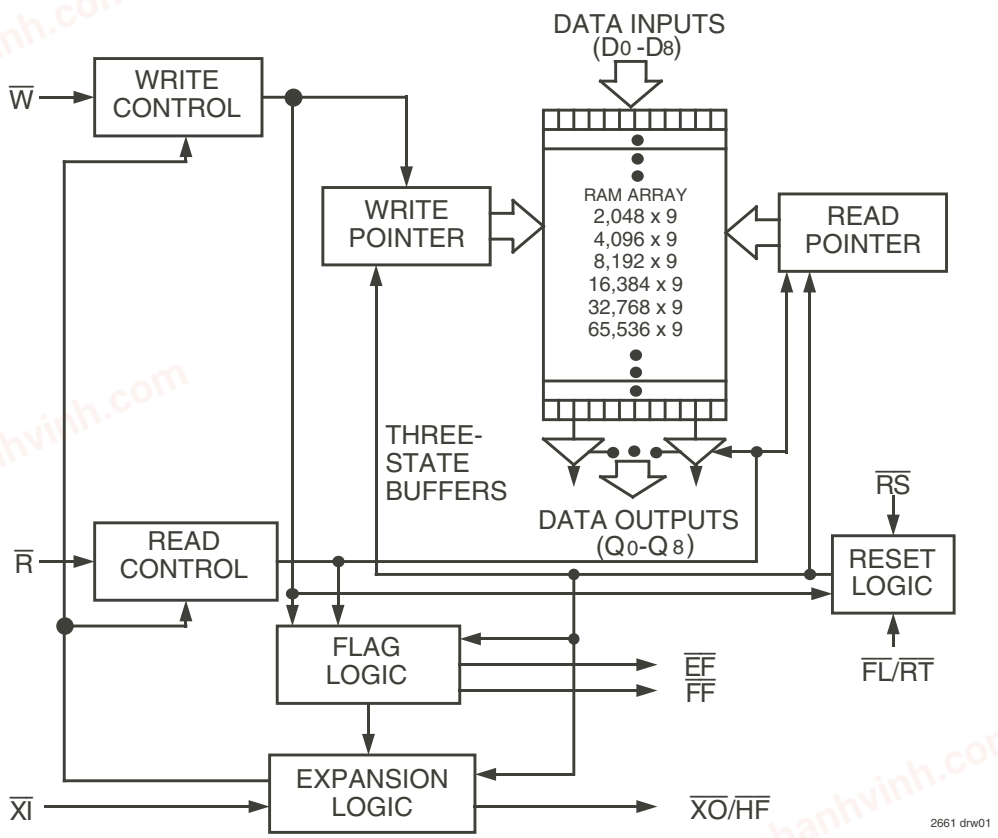
Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins.

The device's 9-bit width provides a bit for a control or parity at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows the read pointer to be reset to its initial position when $\overline{RT}$ is pulsed LOW. A Half-Full Flag is available in the single device and width expansion modes.

These FIFOs are fabricated using high-speed CMOS technology. They are designed for applications requiring asynchronous and simultaneous read/writes in multiprocessing, rate buffering and other applications.

Military grade product is manufactured in compliance with MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

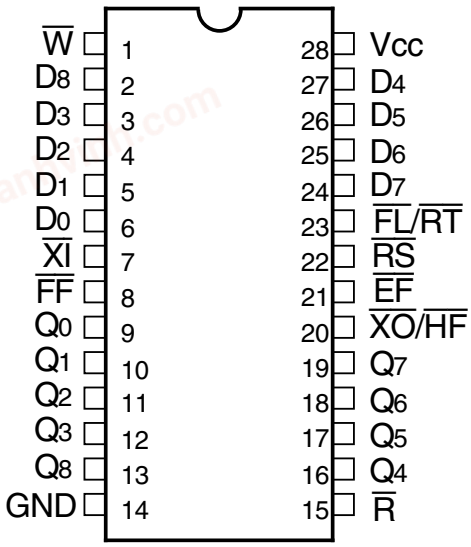


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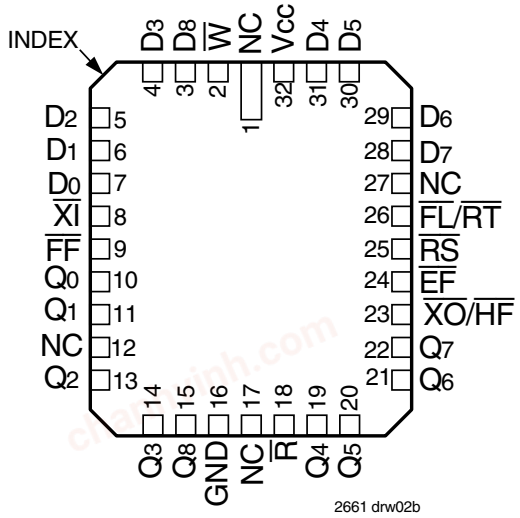
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PIN CONFIGURATIONS



TOP VIEW



TOP VIEW

Package Type	Reference Identifier	Order Code	Device Availability
PLASTIC DIP	P28-1	P	All devices
PLASTIC THIN DIP	P28-2	TP	All except IDT7207/7208
CERDIP	D28-1	D	All except IDT7208
THIN CERDIP	D28-3	TD	Only for IDT7203/7204/7205
SOIC	SO28-3	SO	Only for IDT7204

Package Type	Reference Identifier	Order Code	Device Availability
PLCC	J32-1	J	All devices
LCC(1)	L32-1	L	All except IDT7208

NOTE:
1. This package is only available in the military temperature range.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TSTG	Storage Temperature	–55 to + 125	–65 to +155	°C
IOUT	DC Output +Current	–50 to +50	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage Commercial/Industrial/Military	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial/Industrial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(2)	Input Low Voltage Commercial/Industrial/Military	—	—	0.8	V
TA	Operating Temperature Commercial	0	—	70	°C
TA	Operating Temperature Industrial	–40	—	85	°C
TA	Operating Temperature Military	–55	—	125	°C

NOTES:
1. For $\overline{RT}/\overline{RS}/\overline{XI}$ input, VIH = 2.6V (commercial).
   For $\overline{RT}/\overline{RS}/\overline{XI}$ input, VIH = 2.6V (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

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DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Industrial: V_{CC} = 5V ± 10%, T_A = –40°C to +85°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT7203[1] IDT7204[1] Commercial and Industrial t_A = 12, 15, 20, 25, 35, 50 ns			IDT7203 IDT7204 Military[3] t_A = 20, 30, 40 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[6]	Input Leakage Current (Any Input)	–1	—	1	–1	—	1	µA
I_{LO}[7]	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}[8,9,10]	Active Power Supply Current	—	—	120	—	—	150	mA
I_{CC2}[8,10,11]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	—	12	—	—	25	mA
I_{CC3}[8,10,12]	Power Down Current	—	—	2	—	—	4	mA

Symbol	Parameter	IDT7205[1] IDT7206[2,4] IDT7207[2,4] IDT7208[2,5] Commercial and Industrial t_A = 12, 15, 20, 25, 35, 50 ns			IDT7205 IDT7206 IDT7207 Military t_A = 20, 30 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[6]	Input Leakage Current (Any Input)	–1	—	1	–1	—	1	µA
I_{LO}[7]	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}[8,9,10]	Active Power Supply Current	—	—	120	—	—	150	mA
I_{CC2}[8,10,11]	Standby Current ($\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	—	12	—	—	25	mA
I_{CC3}[8,10,12]	Power Down Current	—	—	8	—	—	12	mA

NOTES:
1. Industrial temperature range product for 15ns and 25ns speed grades are available as a standard device.
2. Industrial temperature range product for 25ns speed grade only is available as a standard device. All other speed grades are available by special order.
3. Military temperature range product for the 40ns is only available for 7203.
4. Commercial temperature range product for the 12ns not available.
5. Commercial temperature range product for the 12ns, 15ns and 50ns not available.
6. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
7. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
8. Tested with outputs open (I_{OUT} = 0).
9. $\overline{R}$ and $\overline{W}$ toggle at 20 MHz and data inputs switch at 10 MHz.
10. I_{CC} measurements are made with outputs open.
11. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except $\overline{R}$ and $\overline{W}$, which toggle at 20MHz.
12. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except $\overline{R}$ and $\overline{W}$ = V_{CC} -0.2V.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:
1. This parameter is sampled and not 100% tested.
2. With output deselected.

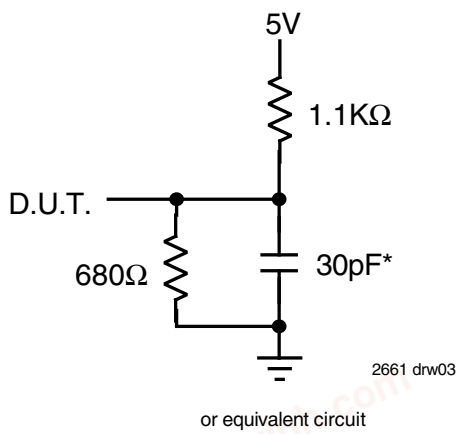


Figure 1. Output Load
*Includes jig and scope capacitances.

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AC ELECTRICAL CHARACTERISTICS(1)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Industrial: V_{CC} = 5V ± 10%, T_A = –40°C to +85°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commercial		Com'l & Ind'l		Com'l & Military		Commercial		Com'l & Ind'l		
		IDT7203L12 IDT7204L12 IDT7205L12		IDT7203L15(2) IDT7204L15(2) IDT7205L15(2) IDT7206L15 IDT7207L15		IDT7203L20 IDT7204L20 IDT7205L20 IDT7206L20 IDT7207L20		IDT7208L20		IDT7203L25(2) IDT7204L25(2) IDT7205L25(2) IDT7206L25(3) IDT7207L25(3) IDT7208L25(3)		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	50	—	40	—	33.3	—	33.3	—	28.5	MHz
t_{RC}	Read Cycle Time	20	—	25	—	30	—	30	—	35	—	ns
t_A	Access Time	—	12	—	15	—	20	—	20	—	25	ns
t_{RR}	Read Recovery Time	8	—	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width(4)	12	—	15	—	20	—	20	—	25	—	ns
t_{RLZ}	Read LOW to Data Bus LOW(5)	3	—	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write HIGH to Data Bus Low-Z(5,6)	3	—	5	—	5	—	5	—	5	—	ns
t_{DV}	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read HIGH to Data Bus High-Z(5)	—	12	—	15	—	15	—	15	—	18	ns
t_{WC}	Write Cycle Time	20	—	25	—	30	—	30	—	35	—	ns
t_{WPW}	Write Pulse Width(4)	12	—	15	—	20	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	8	—	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	9	—	11	—	12	—	12	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	20	—	25	—	30	—	30	—	35	—	ns
t_{RS}	Reset Pulse Width(4)	12	—	15	—	20	—	20	—	25	—	ns
t_{RSS}	Reset Set-up Time(5)	12	—	15	—	20	—	20	—	25	—	ns
t_{RTR}	Reset Recovery Time	8	—	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	20	—	25	—	30	—	30	—	35	—	ns
t_{RT}	Retransmit Pulse Width(4)	12	—	15	—	20	—	20	—	25	—	ns
t_{RTS}	Retransmit Set-up Time(5)	12	—	15	—	20	—	20	—	25	—	ns
t_{RTR}	Retransmit Recovery Time	8	—	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to $\overline{EF}$ LOW	—	12	—	25	—	30	—	30	—	35	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	17	—	25	—	30	—	30	—	35	ns
t_{RTF}	Retransmit LOW to Flags Valid	—	20	—	25	—	30	—	30	—	35	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW	—	12	—	15	—	20	—	20	—	25	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH	—	14	—	15	—	20	—	20	—	25	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ HIGH	12	—	15	—	20	—	20	—	25	—	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH	—	12	—	15	—	20	—	20	—	25	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW	—	14	—	15	—	20	—	20	—	25	ns
t_{WHF}	Write LOW to $\overline{HF}$ Flag LOW	—	17	—	25	—	30	—	30	—	35	ns
t_{RHF}	Read HIGH to $\overline{HF}$ Flag HIGH	—	17	—	25	—	30	—	30	—	35	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ HIGH	12	—	15	—	20	—	20	—	25	—	ns
t_{XOL}	Read/Write LOW to $\overline{XO}$ LOW	—	12	—	15	—	20	—	20	—	25	ns
t_{XOH}	Read/Write HIGH to $\overline{XO}$ HIGH	—	12	—	15	—	20	—	20	—	25	ns
t_{XI}	$\overline{XI}$ Pulse Width(4)	12	—	15	—	20	—	20	—	25	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	8	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	8	—	10	—	10	—	10	—	10	—	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Industrial temperature range product for 15ns and 25ns speed grades are available as a standard device.
3. Industrial temperature range product for 25ns speed grade only is available as a standard device. All other speed grades are available by special order.
4. Pulse widths less than minimum are not allowed.
5. Values guaranteed by design, not currently tested.
6. Only applies to read data flow-through mode.

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AC ELECTRICAL CHARACTERISTICS(1) (CONTINUED)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Industrial: V_{CC} = 5V ± 10%, T_A = –40°C to +85°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Military IDT7203L30 IDT7204L30 IDT7205L30 IDT7206L30 IDT7207L30		Commercial IDT7203L35 IDT7204L35 IDT7205L35 IDT7206L35 IDT7207L35 IDT7208L35		Military IDT7203L40		Commercial IDT7203L50 IDT7204L50 IDT7205L50 IDT7206L50 IDT7207L50		
Symbol	**Parameters**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Shift Frequency	—	25	—	22.22	—	20	—	15	MHz
t_{RC}	Read Cycle Time	40	—	45	—	50	—	65	—	ns
t_A	Access Time	—	30	—	35	—	40	—	50	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	15	—	ns
t_{RPW}	Read Pulse Width(2)	30	—	35	—	40	—	50	—	ns
t_{RLZ}	Read LOW to Data Bus LOW(3)	5	—	5	—	5	—	10	—	ns
t_{WLZ}	Write HIGH to Data Bus Low-Z(3,4)	5	—	10	—	10	—	15	—	ns
t_{DV}	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read HIGH to Data Bus High-Z(3)	—	20	—	20	—	25	—	30	ns
t_{WC}	Write Cycle Time	40	—	45	—	50	—	65	—	ns
t_{WPW}	Write Pulse Width(2)	30	—	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	15	—	ns
t_{DS}	Data Set-up Time	18	—	18	—	20	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	5	—	ns
t_{RSC}	Reset Cycle Time	40	—	45	—	50	—	65	—	ns
t_{RS}	Reset Pulse Width(2)	30	—	35	—	40	—	50	—	ns
t_{RSS}	Reset Set-up Time(3)	30	—	35	—	40	—	50	—	ns
t_{RTR}	Reset Recovery Time	10	—	10	—	10	—	15	—	ns
t_{RTC}	Retransmit Cycle Time	40	—	45	—	50	—	65	—	ns
t_{RT}	Retransmit Pulse Width(2)	30	—	35	—	40	—	50	—	ns
t_{RTS}	Retransmit Set-up Time(3)	30	—	35	—	40	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	10	—	15	—	ns
t_{EFL}	Reset to $\overline{EF}$ LOW	—	40	—	45	—	50	—	65	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	40	—	45	—	50	—	65	ns
t_{RTF}	Retransmit LOW to Flags Valid	—	40	—	45	—	50	—	65	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW	—	30	—	30	—	35	—	45	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH	—	30	—	30	—	35	—	45	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ HIGH	30	—	35	—	40	—	50	—	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH	—	30	—	30	—	35	—	45	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW	—	30	—	30	—	35	—	45	ns
t_{WHF}	Write LOW to $\overline{HF}$ Flag LOW	—	40	—	45	—	50	—	65	ns
t_{RHF}	Read HIGH to $\overline{HF}$ Flag HIGH	—	40	—	45	—	50	—	65	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ HIGH	30	—	35	—	40	—	50	—	ns
t_{XOL}	Read/Write LOW to $\overline{XO}$ LOW	—	30	—	35	—	40	—	50	ns
t_{XOH}	Read/Write HIGH to $\overline{XO}$ HIGH	—	30	—	35	—	40	—	50	ns
t_{XI}	$\overline{XI}$ Pulse Width(2)	30	—	35	—	40	—	50	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	15	—	15	—	15	—	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

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SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D_0–D_8) — Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$.**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered-to, with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW, and will remain set until the difference between the write pointer and read pointer is less-than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW on the falling edge of the last write signal, which inhibits further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF}, allowing a new valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$), provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (Q_0 through Q_8) will return to a high-impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high-impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204/7205/7206/7207/7208 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. The status of the Flags will change depending on the relative locations of the read and write pointers. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than 2,048/4,096/8,192/16,384/32,768/65,536 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION IN ($\overline{XI}$) — This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy-Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations, when the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 2,048/4,096/8,192/16,384/32,768/65,536 writes.

EMPTY FLAG ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$) — This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

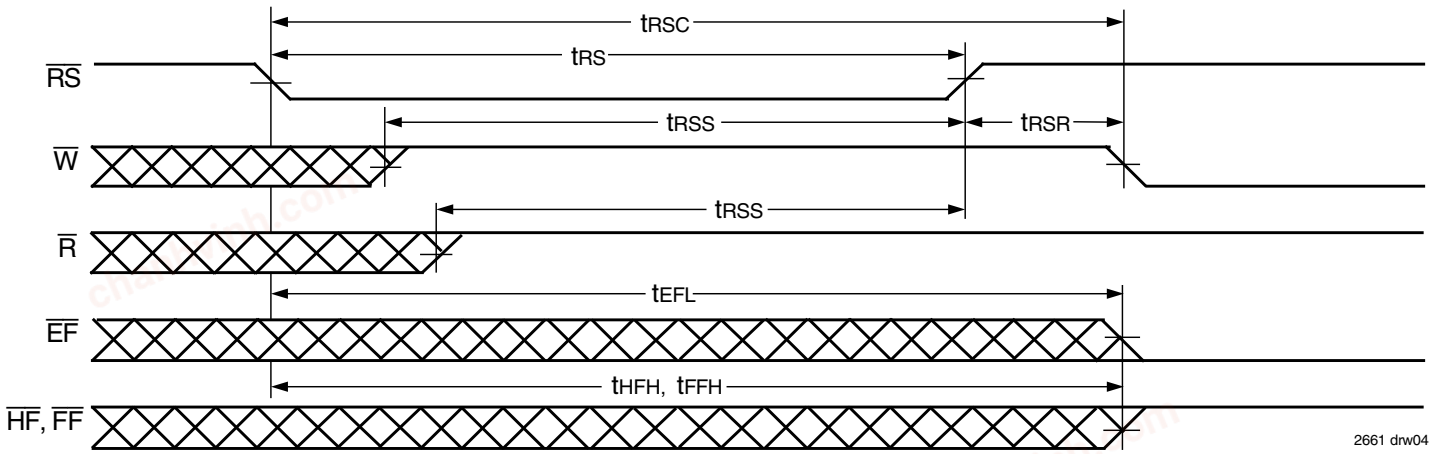
After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the Write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the Read pointer reaches the last location of memory.

DATA OUTPUTS (Q_0-Q_8) — Q_0-Q_8 are data outputs for 9-bit wide data. These outputs are in a high-impedance condition whenever Read ($\overline{R}$) is in a HIGH state.

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NOTE:
1. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

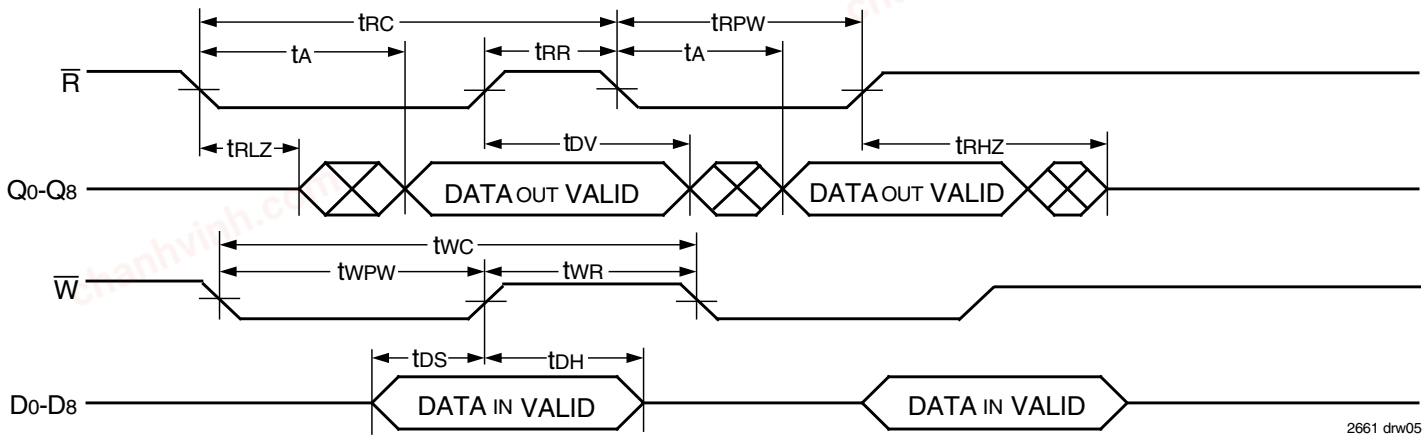


Figure 3. Asynchronous Write and Read Operation

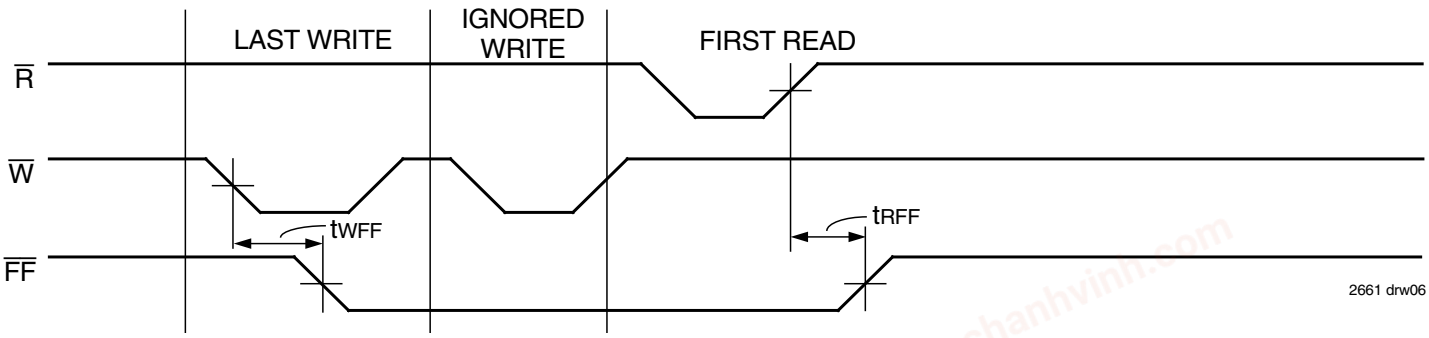


Figure 4. Full Flag Timing From Last Write to First Read

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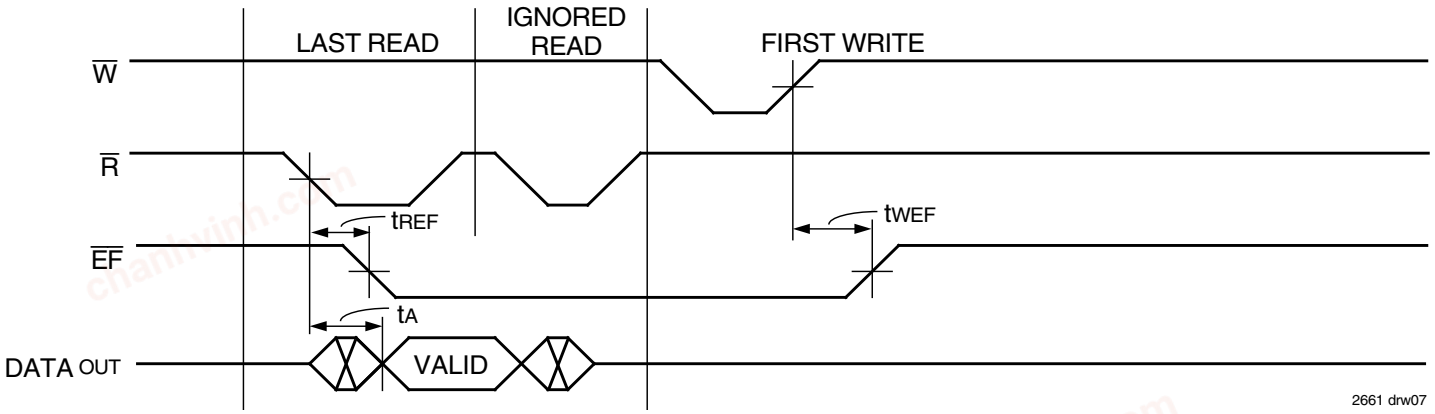
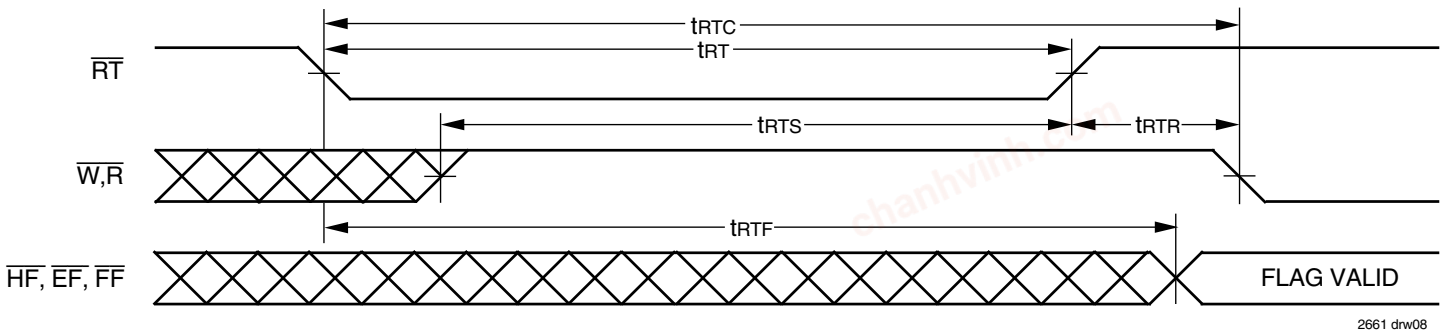


Figure 5. Empty Flag Timing From Last Read to First Write



NOTE:
1. EF, FF and HF may change status during Retransmit, but flags will be valid at tRTC.

Figure 6. Retransmit

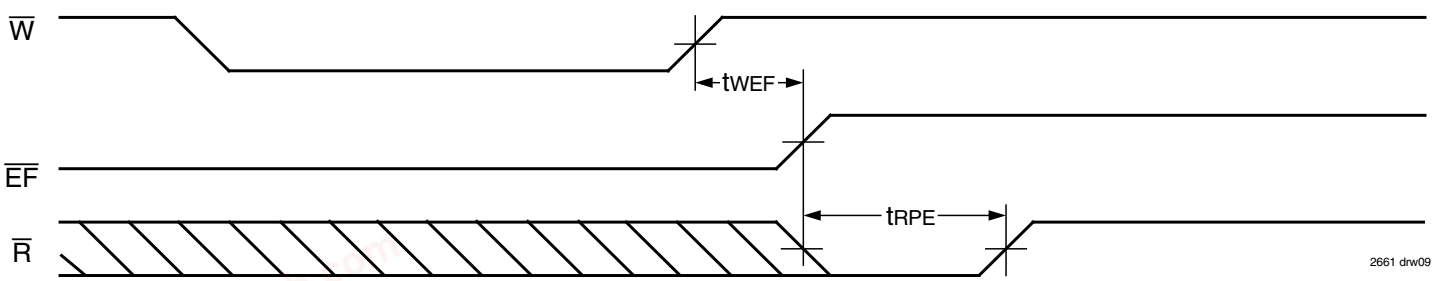


Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse.

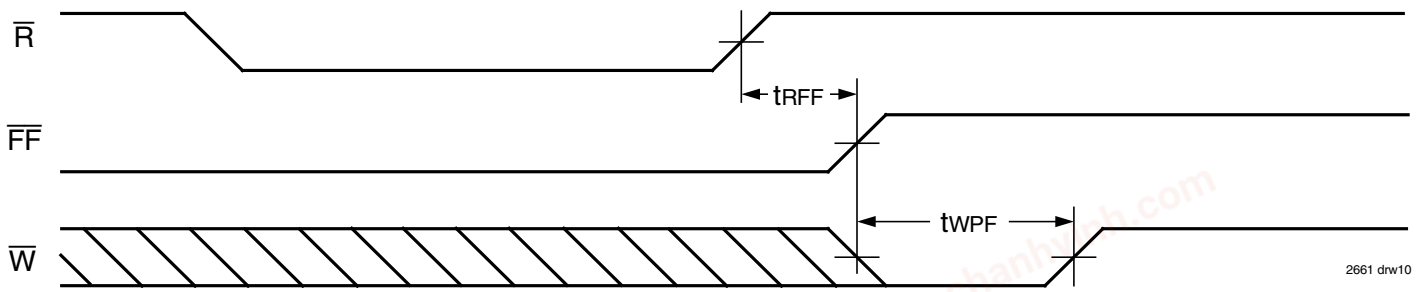


Figure 8. Minimum Timing for a Full Flag Coincident Write Pulse.

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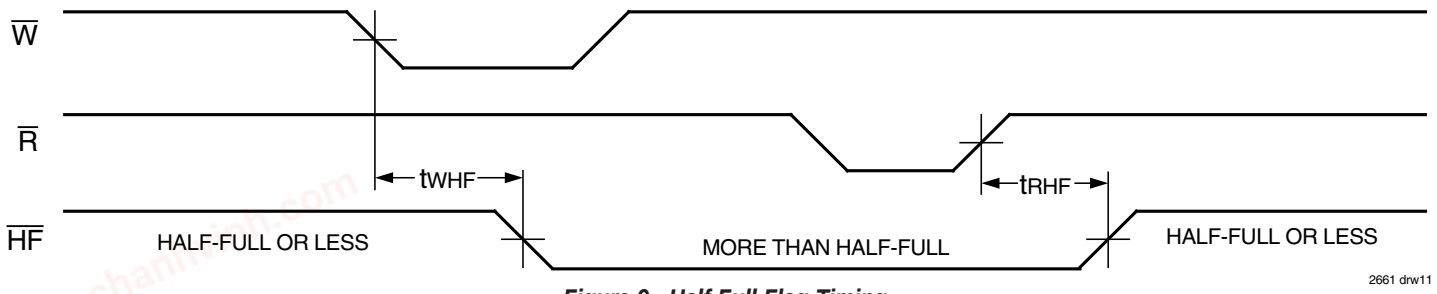


Figure 9. Half-Full Flag Timing

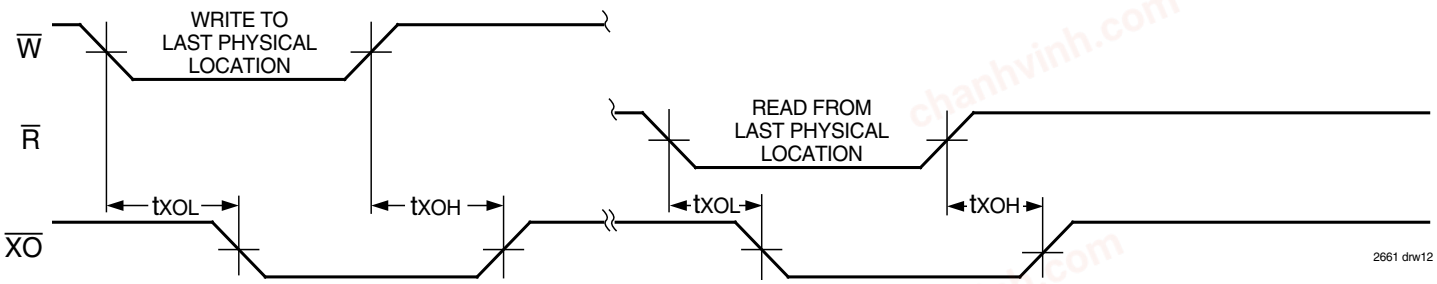


Figure 10. Expansion Out

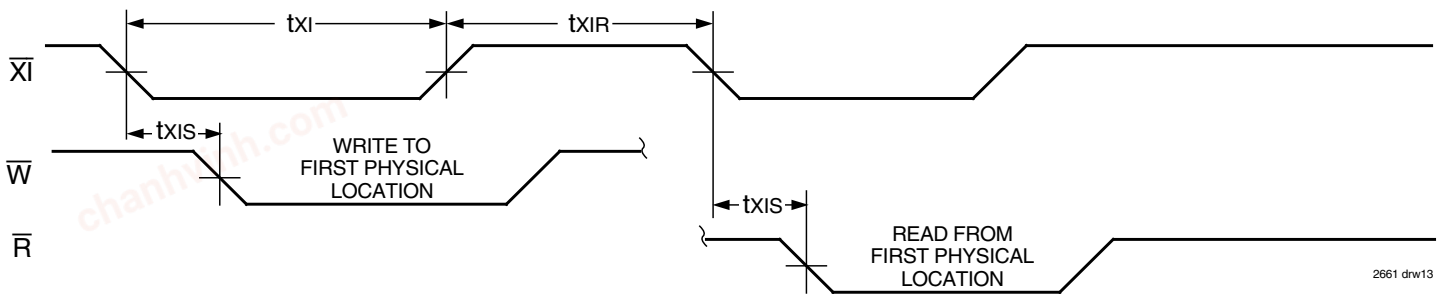


Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information on the IDT7203/7204/7205/7206/7207, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Single Device Mode

A single IDT7203/7204/7205/7206/7207/7208 may be used when the application requirements are for 2,048/4,096/8,192/16,384/32,768/65,536 words or less. These FIFOs are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

These FIFOs can easily be adapted to applications when the requirements are for greater than 2,048/4,096/8,192/16,384/32,768/65,536 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204/7205/7206/7207/7208s. Any depth can be attained by adding additional IDT7203/7204/7205/7206/7207/7208s. These devices operate in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information on the IDT7203/7204/7205/7206/7207, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

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USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204/7205/7206/7207/7208s. Any word width can be attained by adding additional IDT7203/7204/7205/7206/7207/7208s (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204/7205/7206/7207/7208s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

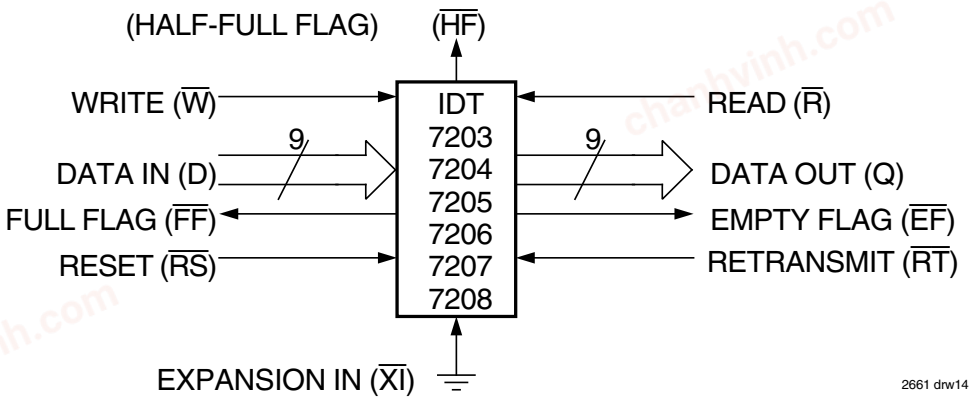
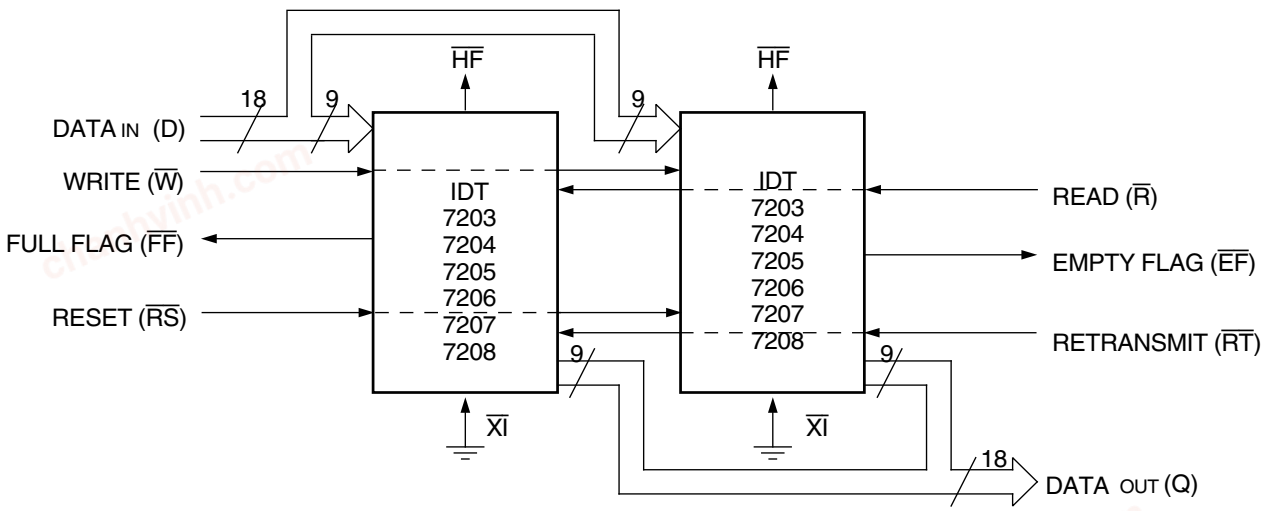


Figure 12. Block Diagram of 2,048 x 9, 4,096 x 9, 8,192 x 9, 16,384 x 9, 32,768 x 9, 65,536 x 9 FIFO Used in Single Device Mode



NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

Figure 13. Block Diagram of 2,048 x 18, 4,096 x 18, 8,192 x 18, 16,384 x 18, 32,768 x 18, 65,536 x 18 FIFO Memory Used in Width Expansion Mode

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TRUTH TABLES

TABLE 1 – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will Increment if flag is HIGH.

TABLE 2 – RESET AND FIRST LOAD

DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

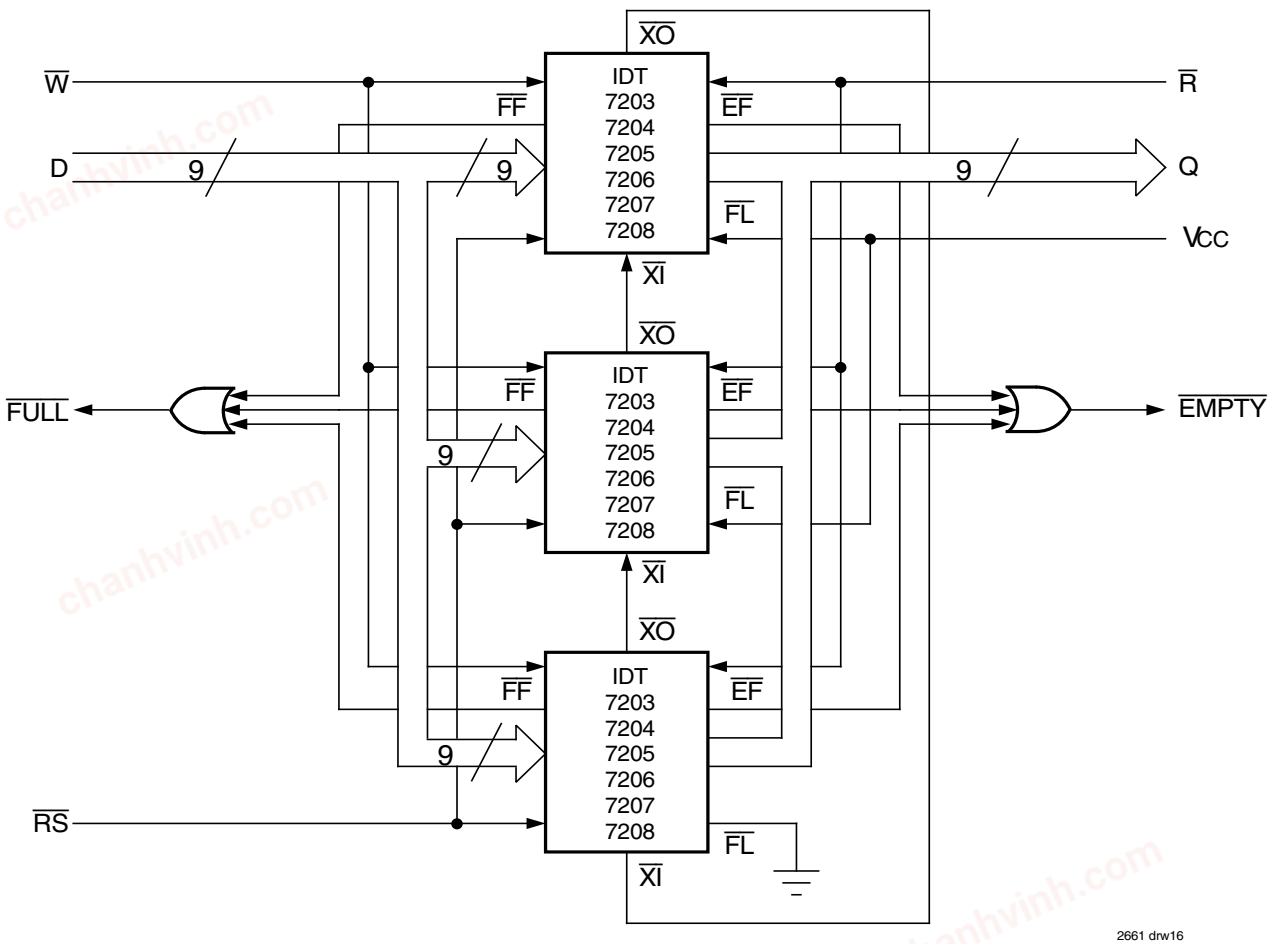
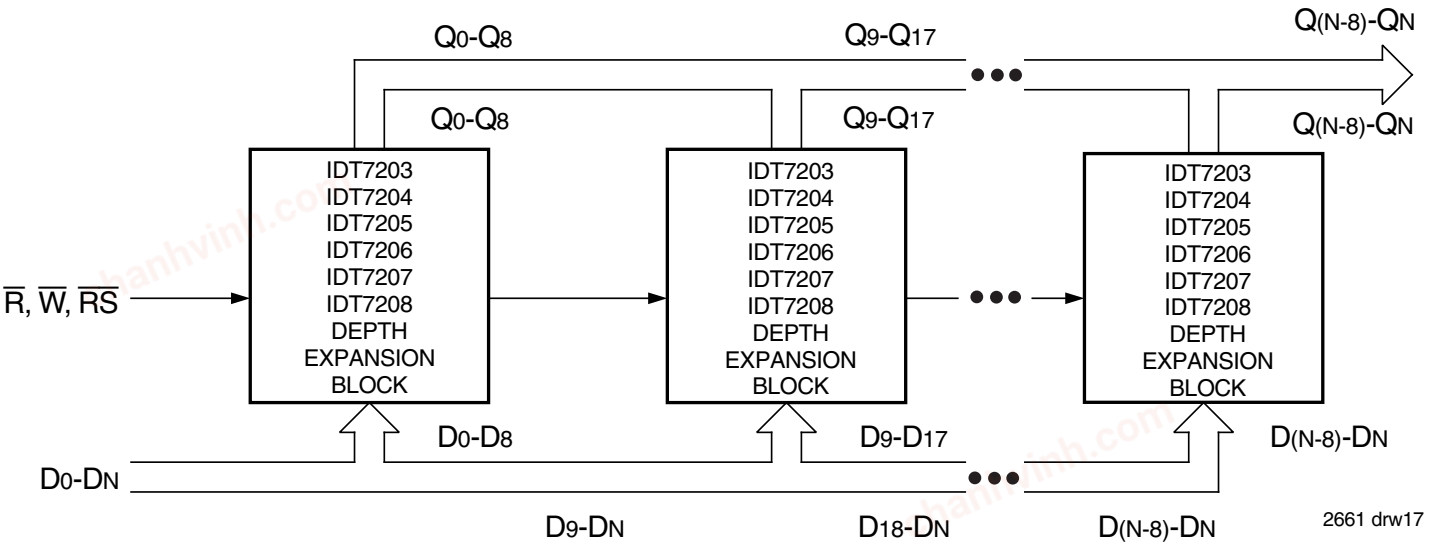


Figure 14. Block Diagram of 6,144 x 9, 12,288 x 9, 24,576 x 9, 49,152 x 9, 98,304 x 9, 196,608 x 9 FIFO Memory (Depth Expansion)

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NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13..

Figure 15. Compound FIFO Expansion

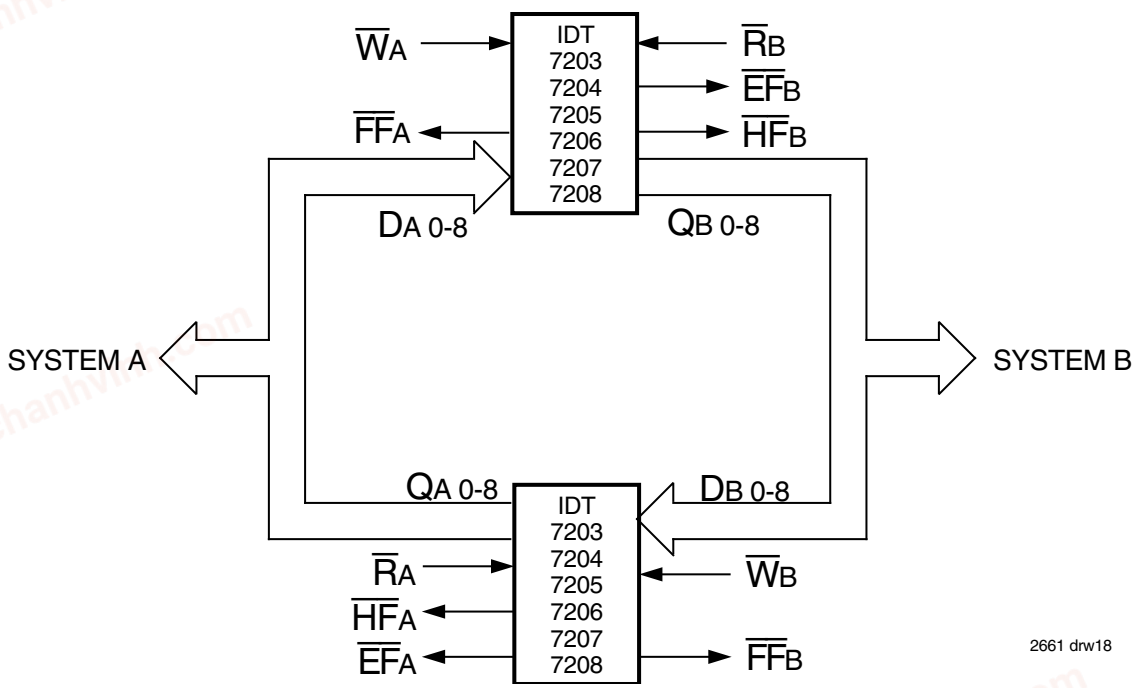


Figure 16. Bidirectional FIFO Operation

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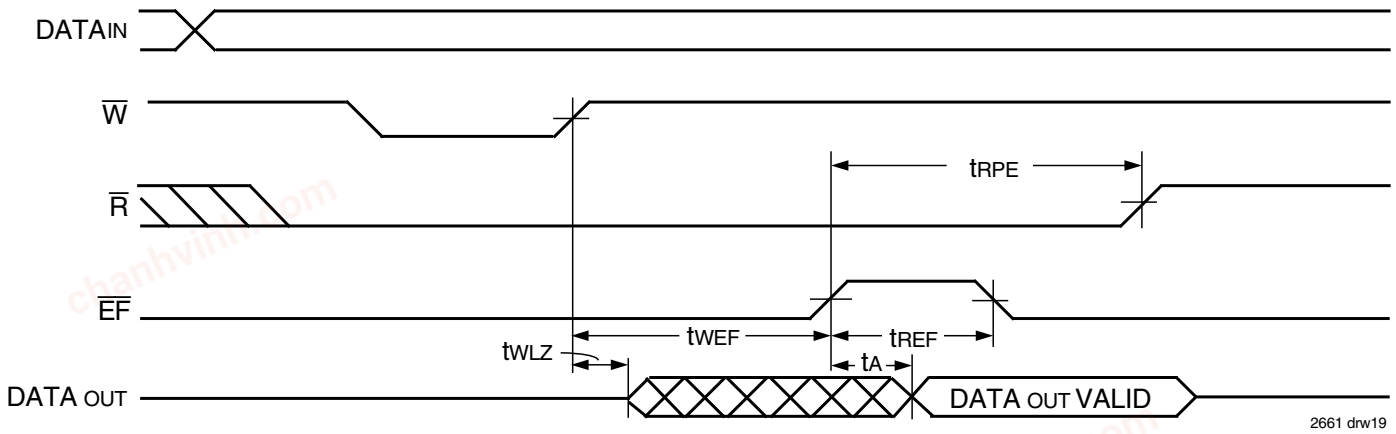


Figure 17. Read Data Flow-Through Mode

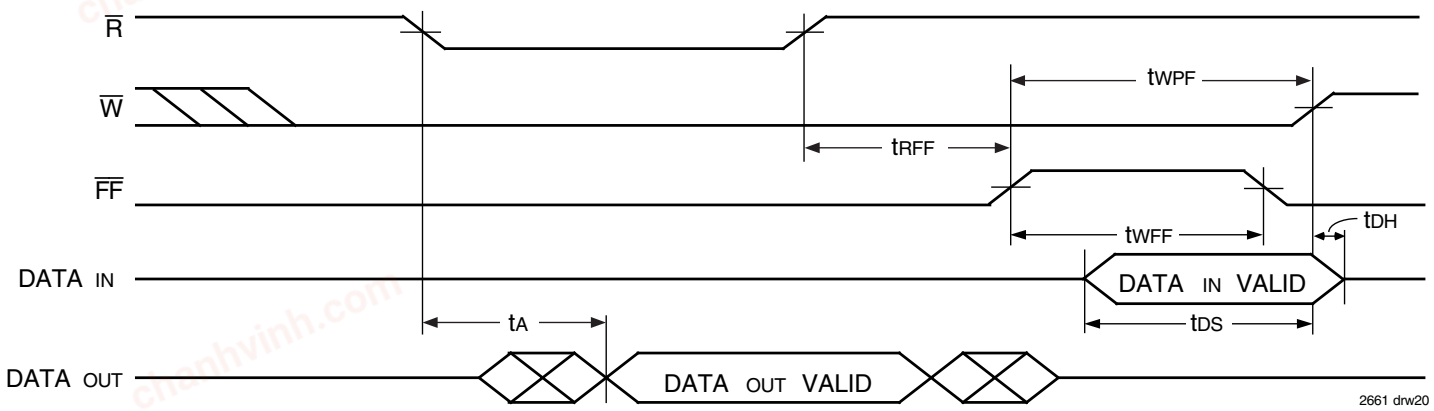
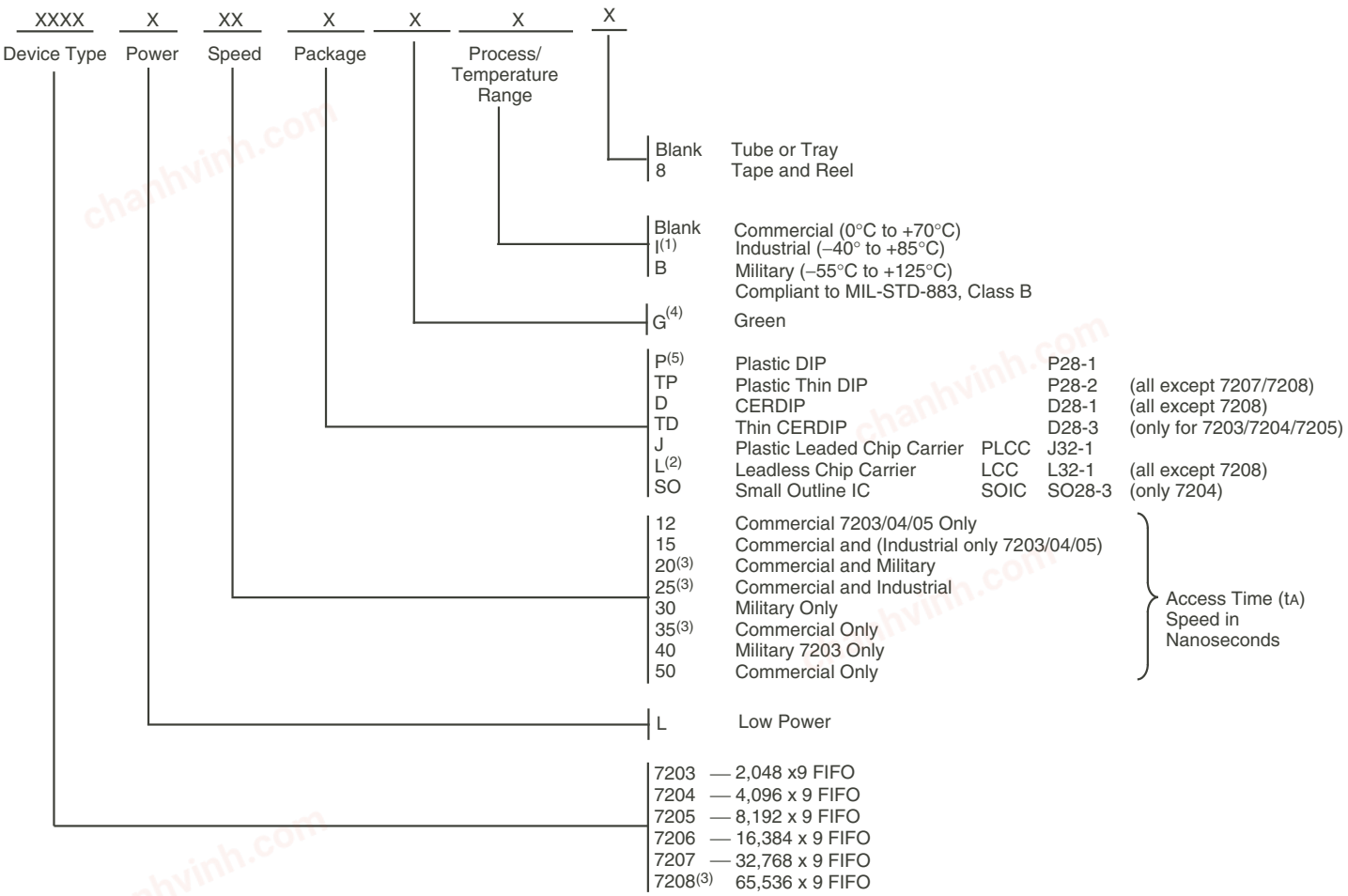


Figure 18. Write Data Flow-Through Mode

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ORDERING INFORMATION



2661 drw21

NOTES:

1. Industrial temperature range product for 15ns and 25ns speed grades are available as a standard device for IDT7203/7204/7205, and 25ns speed grade only is available as a standard device for IDT7206/7207/7208. All other speed grades are available by special order.
2. The LCC is only available in the military temperature range.
3. The IDT7208 is only available in commercial speed grades of 20, 25 and 35 ns.
4. Green parts are available. For specific speeds and packages contact your local sales office.
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02
5. For "P", Plastic Dip, when ordering green package, the suffix is "PDG".

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