chanhvinh.com

3.3V CMOS Static RAM 4 Meg (512K x 8-Bit)

71V424S
71V424L

Features

- **512K x 8 advanced high-speed CMOS Static RAM**
- **JEDEC Center Power / GND pinout for reduced noise**
- **Equal access and cycle times**
  - *Commercial and Industrial: 10/12/15ns*
- **Single 3.3V power supply**
- **One Chip Select plus one Output Enable pin**
- **Bidirectional data inputs and outputs directly TTL-compatible**
- **Low power consumption via chip deselect**
- **Available in 36-pin, 400 mil plastic SOJ package and 44-pin, 400 mil TSOP.**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**

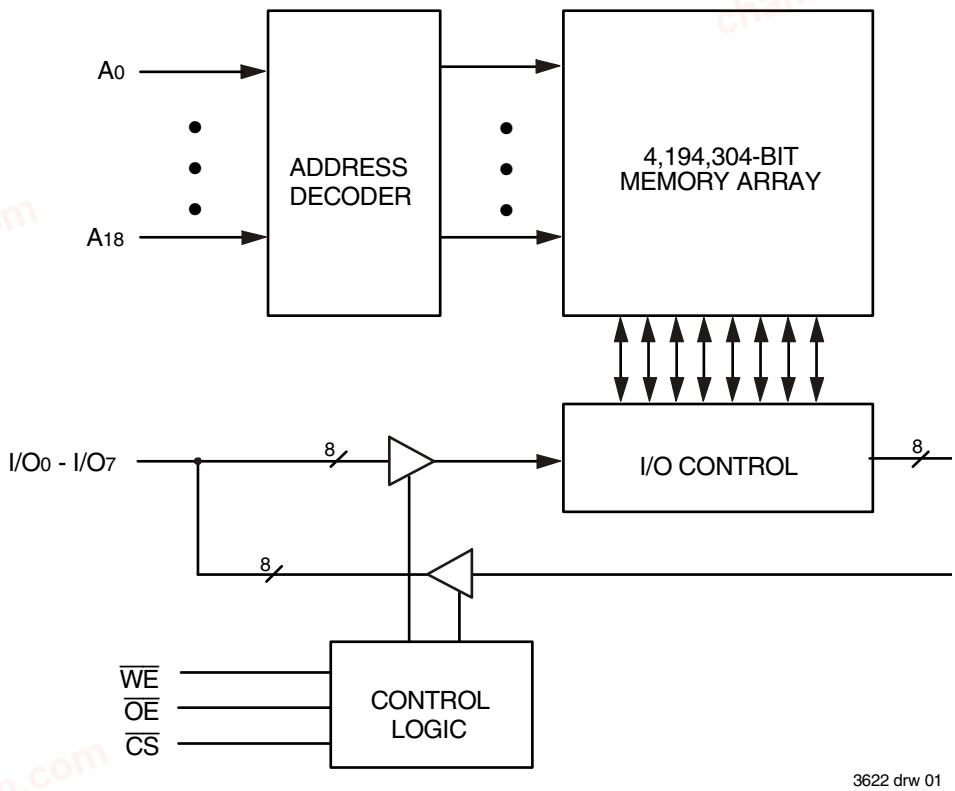
Description

The IDT71V424 is a 4,194,304-bit high-speed Static RAM organized as 512K x 8. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71V424 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71V424 are TTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71V424 is packaged in a 36-pin, 400 mil Plastic SOJ and 44-pin, 400 mil TSOP.

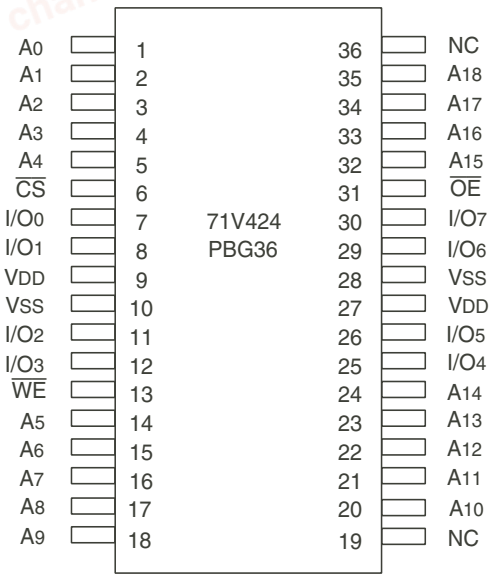
Functional Block Diagram



3622 drw 01

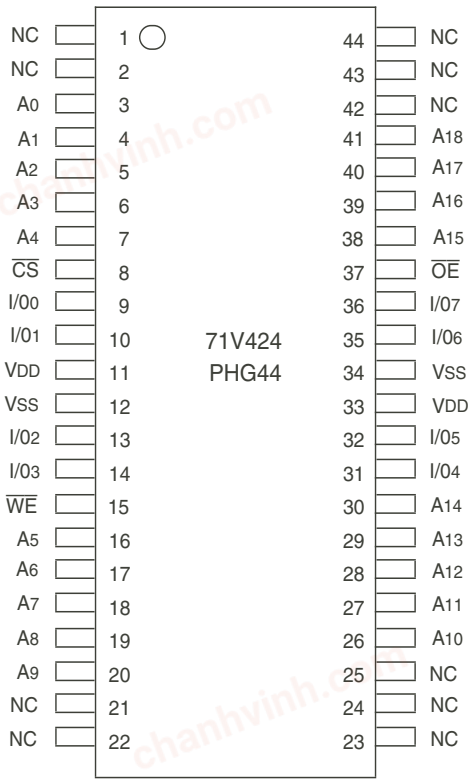
chanhvinh.com

Pin Configurations[1]



SOJ
Top View

3622 drw 02



TSOP
Top View

3622 drw 11

NOTE:

1. This text does not indicate orientation of actual part-marking.

Pin Description

$A_0 - A_{18}$	Address Inputs	Input
$\overline{CS}$	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
$I/O_0 - I/O_7$	Data Input/Output	I/O
V_{DD}	3.3V Power	Power
V_{SS}	Ground	Gnd

3622 tbl 02

Capacitance

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

3622 tbl 03

NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

Truth Table[1,2]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}[3]	X	X	High-Z	Deselected - Standby (I_{SB1})

3622 tbl 01

NOTES:

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{DD} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

chanhvinh.com

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{DD}	Supply Voltage Relative to V_{SS}	-0.5 to +4.6	V
V_{IN}, V_{OUT}	Terminal Voltage Relative to V_{SS}	-0.5 to V_{DD}+0.5	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1	W
I_{OUT}	DC Output Current	50	mA

3622 tbl 04

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	Vss	VDD
Commercial	0°C to +70°C	0V	See Below
Industrial	–40°C to +85°C	0V	See Below

3622 tbl 05

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3(1)	V
V_{IL}	Input Low Voltage	-0.3(2)	—	0.8	V

3622 tbl 06

NOTES:

1. V_{IH} (max.) = V_{DD}+2V for pulse width less than 5ns, once per cycle.
2. V_{IL} (min.) = –2V for pulse width less than 5ns, once per cycle.

DC Electrical Characteristics

(V_{DD} = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Condition	IDT71V424		
			Min.	Max. Unit	
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = V_{SS} to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{DD} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{DD}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{DD} = Min.	2.4	—	V

3622 tbl 07

DC Electrical Characteristics(1, 2, 3)

(V_{DD} = Min. to Max., V_{LC} = 0.2V, V_{HC} = V_{DD} – 0.2V)

Symbol	Parameter		71V424S/L 10		71V424S/L 12		71V424S/L 15		Unit
			Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{LC}$, Outputs Open, V_{DD} = Max., f = f_{MAX}(4)	S	180	180	170	170	160	160	mA
		L	165	165	155	155	145	145	mA
I_{SB}	Dynamic Standby Power Supply Current $\overline{CS} \geq V_{HC}$, Outputs Open, V_{DD} = Max., f = f_{MAX}(4)	S	60	60	55	55	50	50	mA
		L	55	55	50	50	45	45	mA
I_{SB1}	Full Standby Power Supply Current (static) $\overline{CS} \geq V_{HC}$, Outputs Open, V_{DD} = Max., f = 0(4)	S	20	20	20	20	20	20	mA
		L	10	10	10	10	10	10	mA

3622 tbl 08

NOTES:

1. All values are maximum guaranteed values.
2. All inputs switch between 0.2V (Low) and V_{DD} - 0.2V (High).
3. Power specifications are preliminary.
4. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

chanhvinh.com

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1, 2 and 3

3622 tbl 09

AC Test Loads

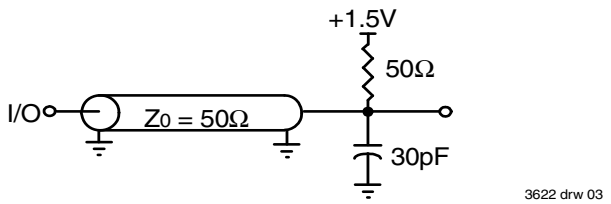
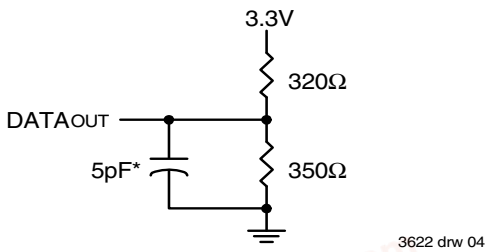


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

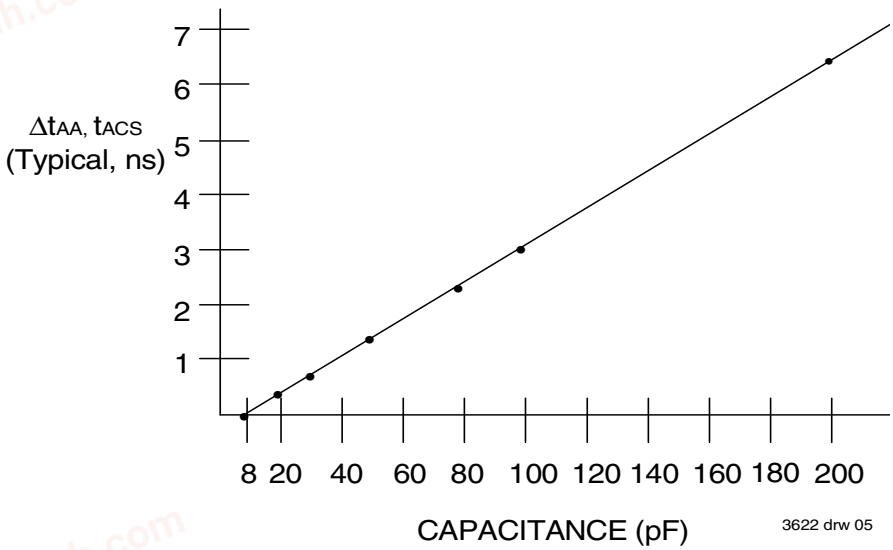


Figure 3. Output Capacitive Derating

chanhvinh.com

AC Electrical Characteristics

(VCC = 3.3V ± 10%, Commercial and Industrial Temperature Ranges)

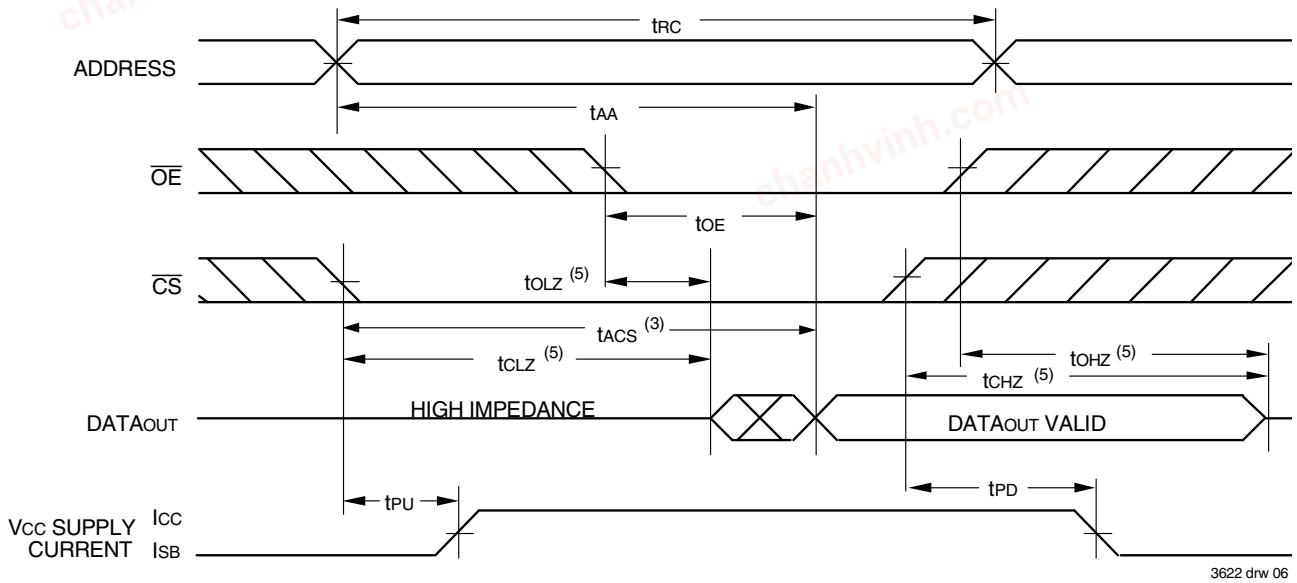
Symbol	Parameter	71V424S/L10		71V424S/L12		71V424S/L15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	4	—	4	—	4	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	—	5	—	6	—	7	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	5	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	10	—	12	—	15	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	8	—	8	—	10	—	ns
t_{CW}	Chip Select to End of Write	8	—	8	—	10	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	8	—	10	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	6	—	6	—	7	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	3	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	—	6	—	7	—	7	ns

3622 tbl 10

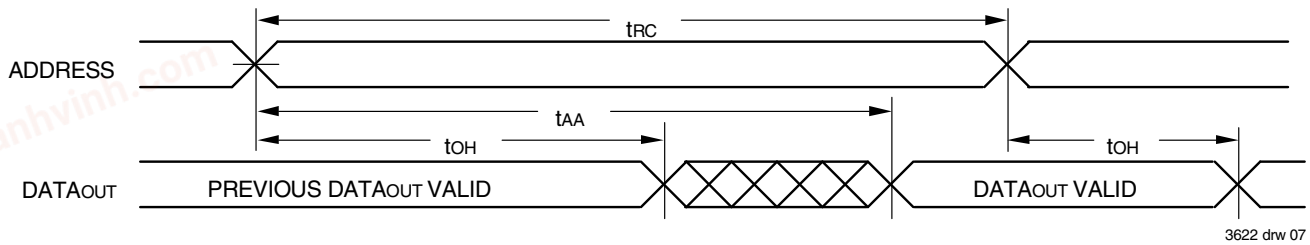
NOTE:
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

chanhvinh.com

Timing Waveform of Read Cycle No. 1(1)



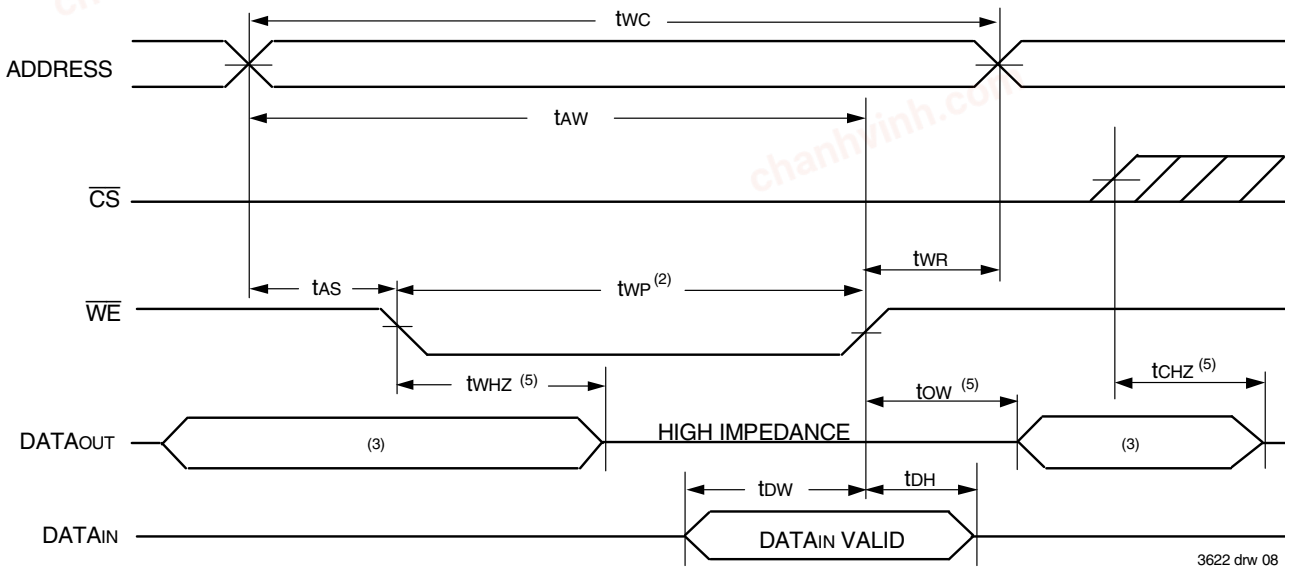
Timing Waveform of Read Cycle No. 2(1, 2, 4)



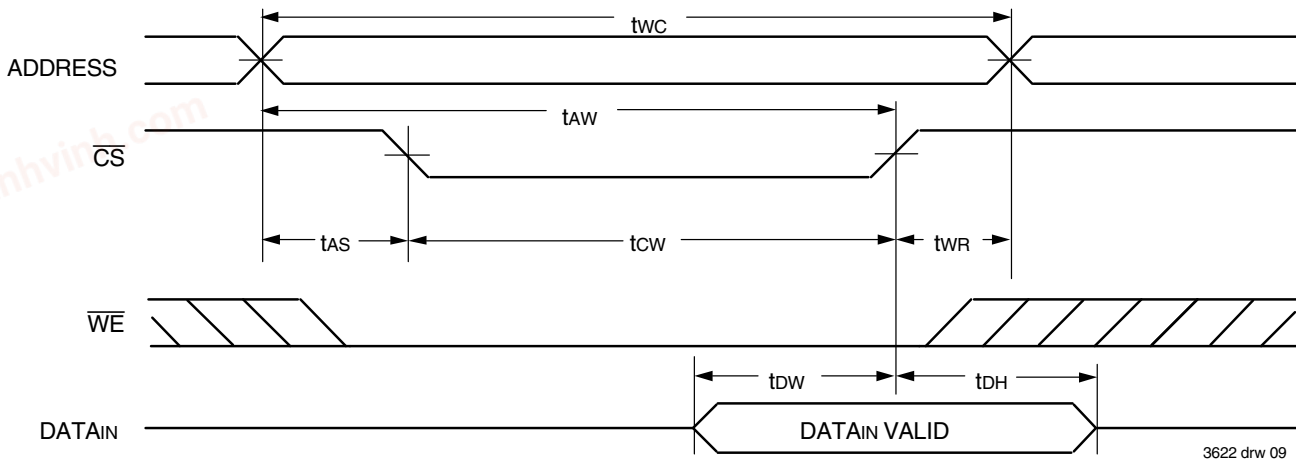
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

chanhvinh.com

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1, 2, 4)



Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1, 4)

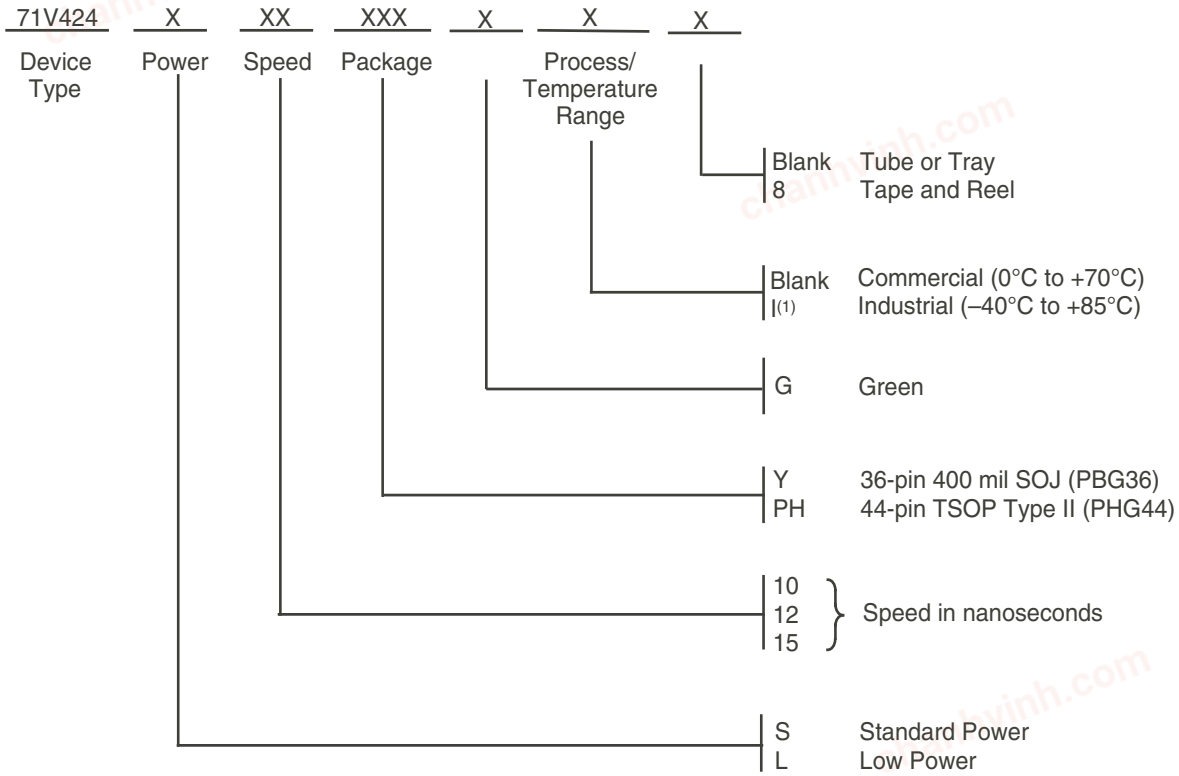


NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS}$ must be active during the t_{CW} write period.
5. Transition is measured ±200mV from steady state.

chanhvinh.com

Ordering Information



NOTE:
1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.

3622 drw 10

chanhvinh.com

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
10	71V424L10PHG	PHG44	TSOP	C
	71V424L10PHG8	PHG44	TSOP	C
	71V424L10PHGI	PHG44	TSOP	I
	71V424L10PHGI8	PHG44	TSOP	I
	71V424L10YG	PBG36	SOJ	C
	71V424L10YG8	PBG36	SOJ	C
	71V424L10YGI	PBG36	SOJ	I
	71V424L10YGI8	PBG36	SOJ	I
12	71V424L12PHG	PHG44	TSOP	C
	71V424L12PHG8	PHG44	TSOP	C
	71V424L12PHGI	PHG44	TSOP	I
	71V424L12PHGI8	PHG44	TSOP	I
	71V424L12YG	PBG36	SOJ	C
	71V424L12YG8	PBG36	SOJ	C
	71V424L12YGI	PBG36	SOJ	I
	71V424L12YGI8	PBG36	SOJ	I
15	71V424L15PHG	PHG44	TSOP	C
	71V424L15PHG8	PHG44	TSOP	C
	71V424L15PHGI	PHG44	TSOP	I
	71V424L15PHGI8	PHG44	TSOP	I
	71V424L15YG	PBG36	SOJ	C
	71V424L15YG8	PBG36	SOJ	C
	71V424L15YGI	PBG36	SOJ	I
	71V424L15YGI8	PBG36	SOJ	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
10	71V424S10PHG	PHG44	TSOP	C
	71V424S10PHG8	PHG44	TSOP	C
	71V424S10PHGI	PHG44	TSOP	I
	71V424S10PHGI8	PHG44	TSOP	I
	71V424S10YG	PBG36	SOJ	C
	71V424S10YG8	PBG36	SOJ	C
	71V424S10YGI	PBG36	SOJ	I
	71V424S10YGI8	PBG36	SOJ	I
12	71V424S12PHG	PHG44	TSOP	C
	71V424S12PHG8	PHG44	TSOP	C
	71V424S12PHGI	PHG44	TSOP	I
	71V424S12PHGI8	PHG44	TSOP	I
	71V424S12YG	PBG36	SOJ	C
	71V424S12YG8	PBG36	SOJ	C
	71V424S12YGI	PBG36	SOJ	I
	71V424S12YGI8	PBG36	SOJ	I
15	71V424S15PHG	PHG44	TSOP	C
	71V424S15PHG8	PHG44	TSOP	C
	71V424S15PHGI	PHG44	TSOP	I
	71V424S15PHGI8	PHG44	TSOP	I
	71V424S15YG	PBG36	SOJ	C
	71V424S15YG8	PBG36	SOJ	C
	71V424S15YGI	PBG36	SOJ	I
	71V424S15YGI8	PBG36	SOJ	I

chanhvinh.com

Datasheet Document History

8/13/99		Updated to new format
	Pg. 2	Removed SO44-1 from TSOP pinout
	Pg. 7	Revised footnotes on Write Cycle No. 1 diagram
		Removed footnote for t_{WR} on Write Cycle No. 2 diagram
	Pg. 9	Added Datasheet Document History
8/31/99	Pg. 1–9	Added Industrial temperature range offerings
11/22/02	Pg. 8	Added die revision option to ordering information
07/31/03	Pg. 8	Updated note, L10 speed grade commercial temperature only and updated die stepping from YF to Y.
07/28/04	Pg. 3	Increased ISB for all "L" and S15 speeds by 10mA and increased for S12 speed by 5mA (refer to PCN# SR-0402-02).
	Pg. 8	Added "Restricted hazardous substance device" to the ordering information.
09/20/08	Pg. 1, 8	Added Y and V step part numbers to front page and ordering information. Updated the ordering information by removing the "IDT" notation.
05/12/09	Pg. 3,5,8	Add Industrial grade for 10ns Low Power.
06/11/09	Pg.1,8	Removed VS, VL from datasheet and ordering information.
09/26/13:	Pg.1-9	Removed the /YS & /YL from the device name for the entire datasheet.
	Pg.1	Removed IDT's reference to fabrication.
	Pg.8	Updated ordering information by adding T&R, updated Restricted Hazardous Substance Device wording to Green and removed the Die Stepping Revision, the"Y" designator.
05/04/21	Pg.1-11	Rebranded as Renesas datasheet
	Pg.2 & 8	Updated package codes
	Pg.8	Added Industrial temp footnote to Ordering Information
	Pg.9	Added Orderable Part Information tables

chanhvinh.com

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.