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## Description

The 5PB11xx is a high-performance LVCMOS clock buffer family of devices. It has an additive phase jitter of 50fs RMS.

There are five different fan-out variations available: 1:2 to 1:10.

The 5PB11xx supports a synchronous glitch-free output enable (OE) function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It can operate from a 1.8V to 3.3V supply.

The 5PB1104 is also available in an Automotive Grade 1, AEC-Q100 qualified version.

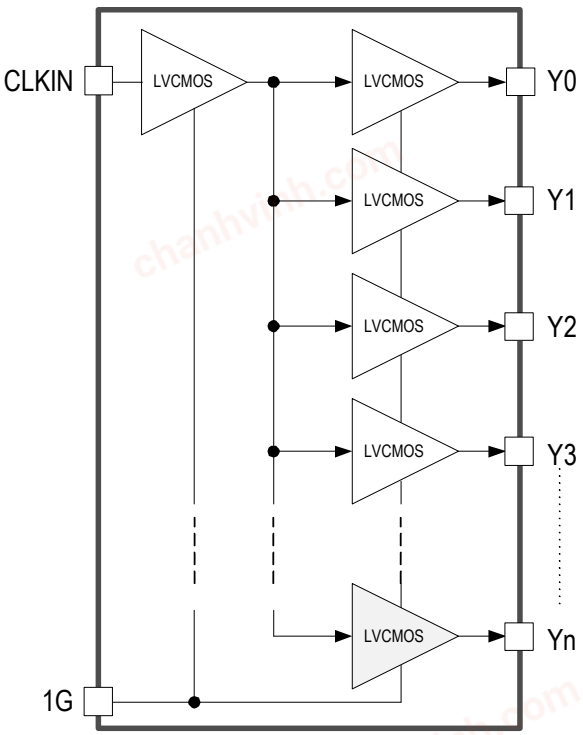
## Typical Applications

- Industrial applications
- Automotive applications

## Features

- High-performance 1:2, 1:4, 1:6, 1:8, 1:10 LVCMOS clock buffer
- Very low pin-to-pin skew: < 50ps
- Very low additive jitter: < 50fs
- Supply voltage: 1.8V to 3.3V
- 3.3V tolerant input clock
- $f_{MAX}$ = 200MHz
- Integrated serial termination for 50Ω channel
- Packaged in 8-, 14-, 16-, 20-pin TSSOP and as small as 2 × 2 mm DFN and VFQFPN packages
- Industrial (-40°C to +85°C) and extended (-40°C to +105°C) temperature ranges
- 5PB1104 available in AEC-Q100 qualified, Automotive Grade 1 (-40°C to +125°C)

## Block Diagram



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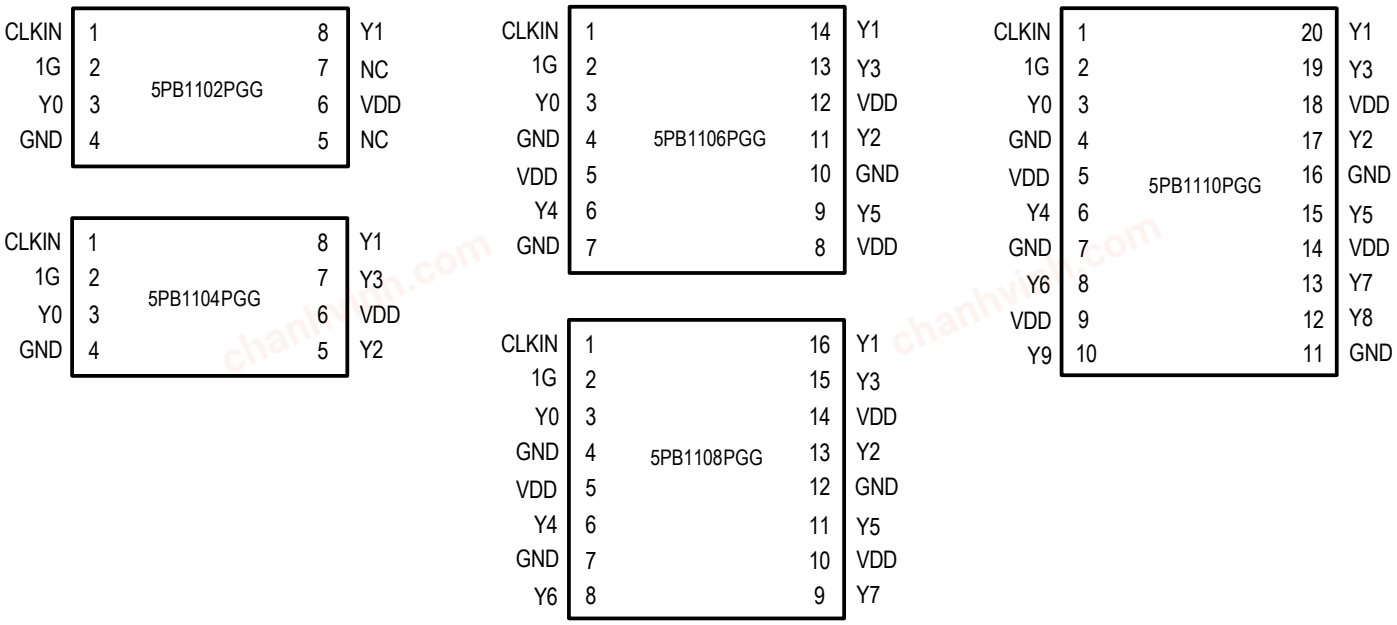
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## Pin Assignments – TSSOP Packages

Figure 1. Pin Assignments for TSSOP Packages




## Pin Descriptions – TSSOP Packages

Table 1. Pin Descriptions for TSSOP Packages

| Device Number | LVCMOS Clock Input | Clock Output Enable | LVCMOS Clock Output | Supply Voltage | Ground |
|---|---|---|---|---|---|
| | CLKIN | 1G | Y0, Y1, ... Y9 | $V_{DD}$ | GND |
| 5PB1102PGG | 1 | 2 | 3, 8 | 6 | 4 |
| 5PB1104PGG | 1 | 2 | 3, 8, 5, 7 | 6 | 4 |
| 5PB1106PGG | 1 | 2 | 3, 14, 11, 13, 6, 9 | 5, 8, 12 | 4, 7, 10 |
| 5PB1108PGG | 1 | 2 | 3, 16, 13, 15, 6, 11, 8, 9 | 5, 10, 14 | 4, 7, 12 |
| 5PB1110PGG | 1 | 2 | 3, 20, 17, 19, 6, 15, 8, 13, 12, 10 | 6 | 4, 7, 11, 16 |

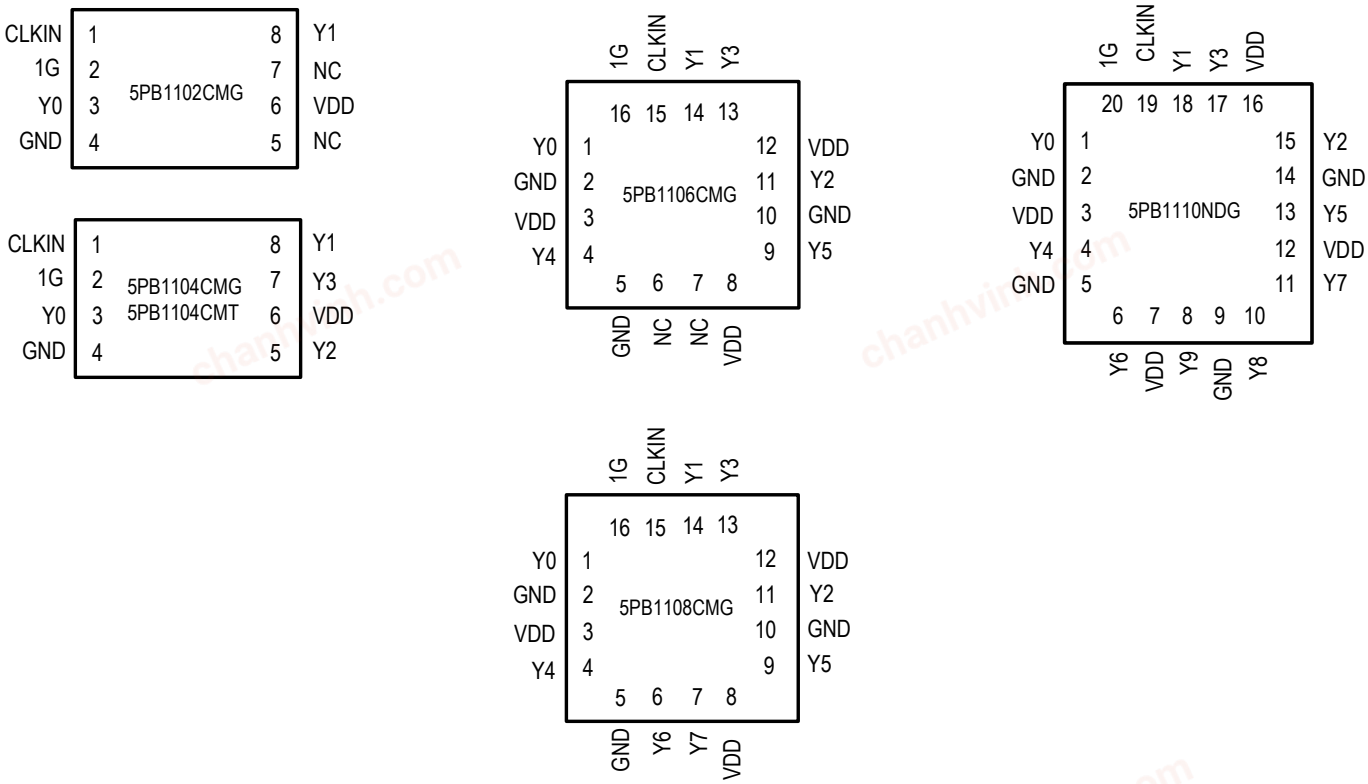
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## Pin Assignments – DFN/VFQFPN Packages

Figure 2. Pin Assignments for DFN/QFN Packages




## Pin Descriptions – DFN/VFQFPN Packages

Table 2. Pin Descriptions for DFN/VFQFPN Packages

| Device Number | LVCMOS Clock Input | Clock Output Enable | LVCMOS Clock Output | Supply Voltage | Ground |
|---|---|---|---|---|---|
| | CLKIN | 1G | Y0, Y1, ... Y9 | $V_{DD}$ | GND |
| 5PB1102CMG | 1 | 2 | 3, 8 | 6 | 4 |
| 5PB1104CMG<br>5PB1104CMT | 1 | 2 | 3, 5, 7, 8 | 6 | 4 |
| 5PB1106CMG | 15 | 16 | 1, 4, 9, 11, 13, 14 | 3, 8, 12 | 2, 5, 10 |
| 5PB1108CMG | 15 | 16 | 1, 4, 6, 7, 9, 11, 13, 14 | 3, 8, 12 | 2, 5, 10 |
| 5PB1110NDG | 19 | 20 | 1, 4, 6, 8, 10, 11, 13, 15, 17, 18 | 3, 7, 12, 16 | 2, 5, 9, 14 |

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## Output Logic Table

| Inputs | | Output |
|---|---|---|
| CLKIN | 1G | Yn |
| X | L | L |
| L | H | L |
| H | H | H |

After at least three cycles of input clock toggling. Output Enable function is asynchronous to eliminate any intermediate incorrect output clock cycles during transition which may cause frequency peaking to the downstream device.

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 5PB11xx at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 3.8V |
| Output Enable and All Outputs | -0.4 V to $V_{DD}$ + 0.5 V |
| Input Voltage, CLKIN | -0.4 V to 3.465V |
| Ambient Operating Temperature (Industrial) | -40 to +85°C |
| Ambient Operating Temperature (Extended) | -40 to +105°C |
| Ambient Operating Temperature (Automotive Grade 1) | -40 to +125°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |

## Recommended Operating Conditions

Table 4. Recommended Operating Conditions

| Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|
| Ambient Operating Temperature (Industrial) | -40 | | +85 | |
| Ambient Operating Temperature (Extended) | -40 | | +105 | |
| Ambient Operating Temperature (Automotive Grade 1) | -40 | | +125 | °C |
| Power Supply Voltage (measured in respect to GND) | +1.71 | | +3.465 | V |

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# Thermal Characteristics

Table 5. Thermal Characteristics

| Package | Applies to | $\Theta_{JA}$ | $\Theta_{JC}$ | $\Theta_{JB}$ | Units |
|---|---|---|---|---|---|
| 8-TSSOP | 5PB1102PGG, 5PB1104PGG | 122.0 | 58.2 | 139.3 | °C/W; still air |
| 14-TSSOP | 5PB1106PGG | 84.5 | 44.2 | 64.5 | °C/W; still air |
| 16-TSSOP | 5PB1108PGG | 80.9 | 43.3 | 60.1 | °C/W; still air |
| 20-TSSOP | 5PB1110PGG | 72.5 | 37.9 | 49.8 | °C/W; still air |
| 8-DFN | 5PB1102CMG, 5PB1104CMG 5PB1104CMT | 120.2 | 99.4 | 63.3 | °C/W; still air |
| 16-VFQFPN | 5PB1106CMG, 5PB1108CMG | 115.6 | 83.1 | 61.8 | °C/W; still air |
| 20-VFQFPN | 5PB1110NDG | 49.6 | 94.7 | 5.1 | °C/W; still air |

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# DC Electrical Characteristics

$V_{DD}$ = 1.8V, 2.5V, or 3.3V (see tables below)

Table 6. DC Electrical Characteristics – $V_{DD}$ = 1.8V ±5%

| Symbol | Parameter | Applies to | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating Voltage | All devices | | 1.71 | 1.8 | 1.89 | V |
| $V_{IH}$ | Input High Voltage, CLKIN [1] | All devices | | 0.7 × $V_{DD}$ | | | V |
| $V_{IL}$ | Input Low Voltage, CLKIN [1] | All devices | | | | 0.3 × $V_{DD}$ | V |
| $V_{IH}$ | Input High Voltage, 1G | All devices | | 1.6 | | $V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage, 1G | All devices | | | | 0.6 | V |
| $V_{OH}$ | Output High Voltage | Industrial and Extended [2] | $I_{OH}$ = -5mA. | 1.4 | | | V |
| | Output High Voltage | Automotive [3] | $I_{OH}$ = -5mA. | 1.2 | | | V |
| $V_{OL}$ | Output Low Voltage | Industrial and Extended [2] | $I_{OL}$ = 5mA. | | | 0.4 | V |
| | Output Low Voltage | Automotive [3] | $I_{OL}$ = 5mA. | | | 0.45 | V |
| $Z_O$ | Nominal Output Impedance | All devices | | | 50 | | Ω |
| $C_{IN}$ | Input Capacitance | All devices | CLKIN, 1G pin. | | 5 | | pF |
| $I_{DD}$ | Operating Supply Current, 5PB1102 | Industrial and Extended [2] | 100MHz, no load, 25°C. | | 6 | 8 | mA |
| | Operating Supply Current, 5PB1104 | | | | 12 | 13 | |
| | Operating Supply Current, 5PB1106 | | | | 15 | 18 | |
| | Operating Supply Current, 5PB1108 | | | | 20 | 23 | |
| | Operating Supply Current, 5PB1110 | | | | 23 | 27 | |
| $I_{DD}$ | Operating Supply Current | Automotive [3] | 0.001MHz, $C_L$ = 5pF. | | 0.7 | 1 | mA |
| | | | 0.008MHz, $C_L$ = 5pF. | | 0.7 | 1 | |
| | | | 40MHz, $C_L$ = 5pF. | | 11 | 13 | |
| | | | 100MHz, $C_L$ = 5pF. | | 25 | 30 | |
| | | | 156.25MHz, $C_L$ = 5pF. | | 37 | 47 | |
| | | | 200MHz, $C_L$ = 5pF. | | 39 | 57 | |
| $I_{IH}$ | Input High Leakage | All devices | $V_{IN}$ = $V_{DD}$ | | | 5 | µA |
| $I_{IL}$ | Input Low Leakage | All devices | $V_{IN}$ = 0V | | | 5 | µA |

[1] Nominal switching threshold is $V_{DD}/2$.

[2] 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK. $T_A$ = -40°C to +105°C unless stated otherwise.

[3] 5PB1104CMG1 and 5PB1104CMT1 only. $T_A$ = -40°C to +125°C unless stated otherwise.

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Table 7. DC Electrical Characteristics – $V_{DD}$ = 2.5V ±5%

| Symbol | Parameter | Applies to | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating Voltage | All devices | | 2.375 | 2.5 | 2.625 | V |
| $V_{IH}$ | Input High Voltage, CLKIN [1] | All devices | | 0.7 × $V_{DD}$ | | | V |
| $V_{IL}$ | Input Low Voltage, CLKIN [1] | All devices | | | | 0.3 × $V_{DD}$ | V |
| $V_{IH}$ | Input High Voltage, 1G | All devices | | 1.8 | | $V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage, 1G | All devices | | | | 0.7 | V |
| $V_{OH}$ | Output High Voltage | Industrial and Extended [2] | $I_{OH}$ = -8mA. | 1.9 | | | V |
| | Output High Voltage | Automotive [3] | $I_{OH}$ = -8mA. | 1.6 | | | V |
| $V_{OL}$ | Output Low Voltage | Industrial and Extended [2] | $I_{OL}$ = 8mA. | | | 0.5 | V |
| | Output Low Voltage | Automotive [3] | $I_{OL}$ = 8mA. | | | 0.625 | V |
| $Z_O$ | Nominal Output Impedance | All devices | | | 50 | | Ω |
| $C_{IN}$ | Input Capacitance | All devices | CLKIN, 1G pin. | | 5 | | pF |
| $I_{DD}$ | Operating Supply Current, 5PB1102 | Industrial and Extended [2] | 100MHz, no load, 25°C. | | 9 | 11 | mA |
| | Operating Supply Current, 5PB1104 | | | | 15 | 18 | |
| | Operating Supply Current, 5PB1106 | | | | 21 | 24 | |
| | Operating Supply Current, 5PB1108 | | | | 27 | 31 | |
| | Operating Supply Current, 5PB1110 | | | | 32 | 37 | |
| $I_{DD}$ | Operating Supply Current | Automotive [3] | 0.001MHz, $C_L$ = 5pF. | | 0.9 | 1.3 | mA |
| | | | 0.008MHz, $C_L$ = 5pF. | | 0.9 | 1.3 | |
| | | | 40MHz, $C_L$ = 5pF. | | 15 | 17 | |
| | | | 100MHz, $C_L$ = 5pF. | | 35 | 42 | |
| | | | 156.25MHz, $C_L$ = 5pF. | | 52 | 67 | |
| | | | 200MHz, $C_L$ = 5pF. | | 56 | 80 | |
| $I_{IH}$ | Input High Leakage | All devices | $V_{IN}$ = $V_{DD}$ | | | 5 | µA |
| $I_{IL}$ | Input Low Leakage | All devices | $V_{IN}$ = 0V | | | 5 | µA |

[1] Nominal switching threshold is $V_{DD}$/2.

[2] 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK. $T_A$ = -40°C to +105°C unless stated otherwise.

[3] 5PB1104CMG1 and 5PB1104CMT1 only. $T_A$ = -40°C to +125°C unless stated otherwise.

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Table 8. DC Electrical Characteristics – $V_{DD}$ = 3.3V ±5%

| Symbol | Parameter | Applies to | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating Voltage | All devices | | 3.135 | 3.3 | 3.465 | V |
| $V_{IH}$ | Input High Voltage, CLKIN [1] | All devices | | 0.7 × $V_{DD}$ | | | V |
| $V_{IL}$ | Input Low Voltage, CLKIN [1] | All devices | | | | 0.3 × $V_{DD}$ | V |
| $V_{IH}$ | Input High Voltage, 1G | Industrial and Extended [2] | | 2.0 | | $V_{DD}$ | V |
| $V_{IH}$ | Input High Voltage, 1G | Automotive [3] | | 2.1 | | $V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage, 1G | All devices | | | | 0.8 | V |
| $V_{OH}$ | Output High Voltage | Industrial and Extended [2] | $I_{OH}$ = -12mA. | 2.4 | | | V |
| | Output High Voltage | Automotive [3] | $I_{OH}$ = -12mA. | 2.1 | | | V |
| $V_{OL}$ | Output Low Voltage | Industrial and Extended [2] | $I_{OL}$ = 12mA. | | | 0.7 | V |
| | Output Low Voltage | Automotive [3] | $I_{OL}$ = 12mA. | | | 0.825 | V |
| $Z_O$ | Nominal Output Impedance | All devices | | | 50 | | Ω |
| $C_{IN}$ | Input Capacitance | All devices | CLKIN, 1G pin. | | 5 | | pF |
| $I_{DD}$ | Operating Supply Current, 5PB1102 | Industrial and Extended [2] | 100MHz, no load, 25°C. | | 12 | 13 | mA |
| | Operating Supply Current, 5PB1104 | | | | 20 | 22 | |
| | Operating Supply Current, 5PB1106 | | | | 25 | 30 | |
| | Operating Supply Current, 5PB1108 | | | | 35 | 38 | |
| | Operating Supply Current, 5PB1110 | | | | 40 | 45 | |
| $I_{DD}$ | Operating Supply Current | Automotive [3] | 0.001MHz, $C_L$ = 5pF. | | 1.2 | 1.7 | mA |
| | | | 0.008MHz, $C_L$ = 5pF. | | 1.2 | 1.7 | |
| | | | 40MHz, $C_L$ = 5pF. | | 19 | 22 | |
| | | | 100MHz, $C_L$ = 5pF. | | 45 | 54 | |
| | | | 156.25MHz, $C_L$ = 5pF. | | 67 | 87 | |
| | | | 200MHz, $C_L$ = 5pF. | | 75 | 107 | |
| $I_{IH}$ | Input High Leakage | All devices | $V_{IN}$ = $V_{DD}$ | | | 5 | µA |
| $I_{IL}$ | Input Low Leakage | All devices | $V_{IN}$ = 0V | | | 5 | µA |

[1] Nominal switching threshold is $V_{DD}$/2.

[2] 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK. $T_A$ = -40°C to +105°C unless stated otherwise.

[3] 5PB1104CMG1 and 5PB1104CMT1 only. $T_A$ = -40°C to +125°C unless stated otherwise.

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# AC Electrical Characteristics

$V_{DD}$ = 1.8V, 2.5V, or 3.3V (see tables below).

Table 9. AC Electrical Characteristics – $V_{DD}$ = 1.8V ±5%

| Symbol | Parameter | Applies to | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| | Input Frequency | All devices | | 0 | | 200 | MHz |
| $t_{OR}$ | Output Rise Time (2pF load) | Industrial and Extended [1] | 0.36V to 1.44V, $C_L$ = 2pF. | | 0.5 | 0.75 | ns |
| $t_{OF}$ | Output Fall Time (2pF load) | Industrial and Extended [1] | 1.44V to 0.36V, $C_L$ = 2pF. | | 0.5 | 0.75 | ns |
| $t_{OR}$ | Output Rise Time (5pF load) | Industrial and Extended [1] | 0.36V to 1.44V, $C_L$ = 5pF. | | 0.8 | 1.0 | ns |
| $t_{OF}$ | Output Fall Time (5pF load) | Industrial and Extended [1] | 1.44V to 0.36V, $C_L$ = 5pF. | | 0.8 | 1.0 | ns |
| $t_{OR}$ | Output Rise Time (5pF load) | Automotive [2] | 0.36V to 1.44V, $C_L$ = 5pF. | | 0.65 | 1.2 | ns |
| $t_{OF}$ | Output Fall Time (5pF load) | Automotive [2] | 1.44V to 0.36V, $C_L$ = 5pF. | | 0.65 | 1.2 | ns |
| $t_{START-UP}$ | Start-up Time | All devices | Part start-up time for valid outputs after $V_{DD}$ ramp-up. | | | 3 | ms |
| $t_{PD}$ | Propagation Delay [3] | Industrial and Extended [1] | | 1.5 | | 2.5 | ns |
| | | Automotive [2] | | 1.0 | | 3.4 | ns |
| | Buffer Additive Phase Jitter, RMS | Industrial and Extended [1] | 156.25MHz, Integration Range: 12kHz–20MHz. | | | 0.05 | ps |
| | | Automotive [2] | 156.25MHz, Integration Range: 12kHz–20MHz. | | | 0.06 | ps |
| | Output to Output Skew, 5PB1102/04 | Industrial and Extended [1] | Rising edges at $V_{DD}$/2. [4] | | 35 | 50 | ps |
| | Output to Output Skew, 5PB1106 | Industrial and Extended [1] | Rising edges at $V_{DD}$/2. [4] | | 35 | 58 | ps |
| | Output to Output Skew, 5PB1108/10 | Industrial and Extended [1] | Rising edges at $V_{DD}$/2. [4] | | 45 | 65 | ps |
| | Output to Output Skew | Automotive [2] | Rising edges at $V_{DD}$/2. [4] | | 35 | 87 | ps |
| | Device to Device Skew | All devices | Rising edges at $V_{DD}$/2. | | | 200 | ps |
| $t_{EN}$ | Output Enable Time | All devices | $C_L \leq$ 5pF. | | | 3 | cycles |
| $t_{DIS}$ | Output Disable Time | All devices | $C_L \leq$ 5pF. | | | 3 | cycles |
| $t_{DC}$ | Duty Cycle [5] | All devices | | | 50 | | % |

[1] 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK. $T_A$ = -40°C to +105°C unless stated otherwise.

[2] 5PB1104CMG1 and 5PB1104CMT1 only. $T_A$ = -40°C to +125°C unless stated otherwise.

[3] With rail-to-rail input clock.

[4] Between any 2 outputs with equal loading.

[5] Duty cycle on outputs will match incoming clock duty cycle when VIH on CLKIN pin equals VDD power supply voltage. Consult IDT for tight duty cycle clock generators.

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Table 10. AC Electrical Characteristics – $V_{DD}$ = 2.5V ±5%

| Symbol | Parameter | Applies to | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| | Input Frequency | All devices | | 0 | | 200 | MHz |
| $t_{OR}$ | Output Rise Time (2pF load) | Industrial and Extended [1] | 0.5V to 2.0V, $C_L$ = 2pF. | | 0.4 | 0.7 | ns |
| $t_{OF}$ | Output Fall Time (2pF load) | Industrial and Extended [1] | 2.0V to 0.5V, $C_L$ = 2pF. | | 0.4 | 0.7 | ns |
| $t_{OR}$ | Output Rise Time (5pF load) | Industrial and Extended [1] | 0.5V to 2.0V, $C_L$ = 5pF. | | 0.75 | 1.0 | ns |
| $t_{OF}$ | Output Fall Time (5pF load) | Industrial and Extended [1] | 2.0V to 0.5V, $C_L$ = 5pF. | | 0.75 | 1.0 | ns |
| $t_{OR}$ | Output Rise Time (5pF load) | Automotive [2] | 0.5V to 2.0V, $C_L$ = 5pF. | | 0.63 | 1.2 | ns |
| $t_{OF}$ | Output Fall Time (5pF load) | Automotive [2] | 2.0V to 0.5V, $C_L$ = 5pF. | | 0.63 | 1.2 | ns |
| $t_{START-UP}$ | Start-up Time | All devices | Part start-up time for valid outputs after $V_{DD}$ ramp-up. | | | 3 | ms |
| $t_{PD}$ | Propagation Delay, 5PB1102/04[3] | Industrial and Extended [1] | | 1.9 | | 2.9 | ns |
| | Propagation Delay, 5PB1106/08[3] | Industrial and Extended [1] | | 2.0 | | 3.3 | ns |
| | Propagation Delay, 5PB1110 [3] | Industrial and Extended [1] | | 2.0 | | 3.0 | ns |
| | Propagation Delay [3] | Automotive [2] | | 1.0 | | 4.5 | ns |
| | Buffer Additive Phase Jitter, RMS | Industrial and Extended [1] | 156.25MHz, Integration Range: 12kHz–20MHz. | | | 0.05 | ps |
| | | Automotive [2] | 156.25MHz, Integration Range: 12kHz–20MHz. | | | 0.06 | ps |
| | Output to Output Skew, 5PB1102/04 | Industrial and Extended [1] | Rising edges at $V_{DD}$/2. [4] | | 35 | 50 | ps |
| | Output to Output Skew, 5PB1106 | Industrial and Extended [1] | Rising edges at $V_{DD}$/2. [4] | | 35 | 58 | ps |
| | Output to Output Skew, 5PB1108/10 | Industrial and Extended [1] | Rising edges at $V_{DD}$/2. [4] | | 45 | 65 | ps |
| | Output to Output Skew | Automotive [2] | Rising edges at $V_{DD}$/2. [4] | | 35 | 87 | ps |
| | Device to Device Skew | All devices | Rising edges at $V_{DD}$/2. | | | 200 | ps |
| $t_{EN}$ | Output Enable Time | All devices | $C_L \leq$ 5pF. | | | 3 | cycles |
| $t_{DIS}$ | Output Disable Time | All devices | $C_L \leq$ 5pF. | | | 3 | cycles |
| $t_{DC}$ | Duty Cycle [5] | All devices | | | 50 | | % |

[1] 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK. $T_A$ = -40°C to +105°C unless stated otherwise.

[2] 5PB1104CMG1 and 5PB1104CMT1 only. $T_A$ = -40°C to +125°C unless stated otherwise.

[3] With rail-to-rail input clock.

[4] Between any 2 outputs with equal loading.

[5] Duty cycle on outputs will match incoming clock duty cycle when VIH on CLKIN pin equals VDD power supply voltage. Consult IDT for tight duty cycle clock generators.

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Table 11. AC Electrical Characteristics – $V_{DD}$ = 3.3V ±5%

| Symbol | Parameter | Applies to | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| | Input Frequency | All devices | | 0 | | 200 | MHz |
| $t_{OR}$ | Output Rise Time (2pF load) | Industrial and Extended [1] | 0.66V to 2.64V, $C_L$ = 2pF. | | 0.45 | 0.6 | ns |
| $t_{OF}$ | Output Fall Time (2pF load) | Industrial and Extended [1] | 2.64V to 0.66V, $C_L$ = 2pF. | | 0.45 | 0.6 | ns |
| $t_{OR}$ | Output Rise Time (5pF load) | Industrial and Extended [1] | 0.66V to 2.64V, $C_L$ = 5pF. | | 0.7 | 1.0 | ns |
| $t_{OF}$ | Output Fall Time (5pF load) | Industrial and Extended [1] | 2.64V to 0.66V, $C_L$ = 5pF. | | 0.7 | 1.0 | ns |
| $t_{OR}$ | Output Rise Time (5pF load) | Automotive [2] | 0.66V to 2.64V, $C_L$ = 5pF. | | 0.61 | 1.2 | ns |
| $t_{OF}$ | Output Fall Time (5pF load) | Automotive [2] | 2.64V to 0.66V, $C_L$ = 5pF. | | 0.61 | 1.2 | ns |
| $t_{START-UP}$ | Start-up Time | All devices | Part start-up time for valid outputs after $V_{DD}$ ramp-up. | | | 3 | ms |
| $t_{PD}$ | Propagation Delay, 5PB1102/04[3] | Industrial and Extended [1] | | 1.7 | | 2.4 | ns |
| | Propagation Delay, 5PB1106/08[3] | Industrial and Extended [1] | | 1.7 | | 2.7 | ns |
| | Propagation Delay, 5PB1110 [3] | Industrial and Extended [1] | | 1.7 | | 2.5 | ns |
| | Propagation Delay [3] | Automotive [2] | | 1.0 | | 3.4 | ns |
| | Buffer Additive Phase Jitter, RMS | All devices | 156.25MHz, Integration Range: 12kHz–20MHz. | | | 0.05 | ps |
| | Output to Output Skew, 5PB1102/04 | Industrial and Extended [1] | Rising edges at $V_{DD}$/2. [4] | | 35 | 50 | ps |
| | Output to Output Skew, 5PB1106 | Industrial and Extended [1] | Rising edges at $V_{DD}$/2. [4] | | 35 | 58 | ps |
| | Output to Output Skew, 5PB1108/10 | Industrial and Extended [1] | Rising edges at $V_{DD}$/2. [4] | | 45 | 65 | ps |
| | Output to Output Skew | Automotive [2] | Rising edges at $V_{DD}$/2. [4] | | 35 | 87 | ps |
| | Device to Device Skew | All devices | Rising edges at $V_{DD}$/2. | | | 200 | ps |
| $t_{EN}$ | Output Enable Time | All devices | $C_L \leq$ 5pF. | | | 3 | cycles |
| $t_{DIS}$ | Output Disable Time | All devices | $C_L \leq$ 5pF. | | | 3 | cycles |
| $t_{DC}$ | Duty Cycle [5] | All devices | | | 50 | | % |

[1] 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK. $T_A$ = -40°C to +105°C unless stated otherwise.

[2] 5PB1104CMG1 and 5PB1104CMT1 only. $T_A$ = -40°C to +125°C unless stated otherwise.

[3] With rail-to-rail input clock.

[4] Between any 2 outputs with equal loading.

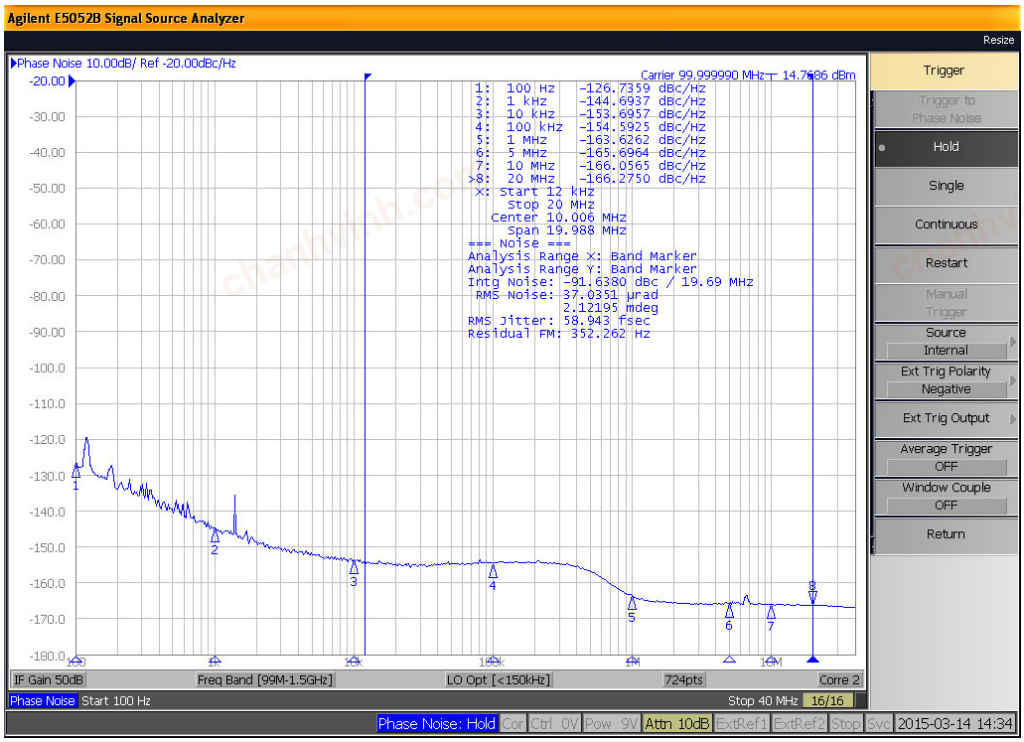
[5] Duty cycle on outputs will match incoming clock duty cycle when VIH on CLKIN pin equals VDD power supply voltage. Consult IDT for tight duty cycle clock generators.

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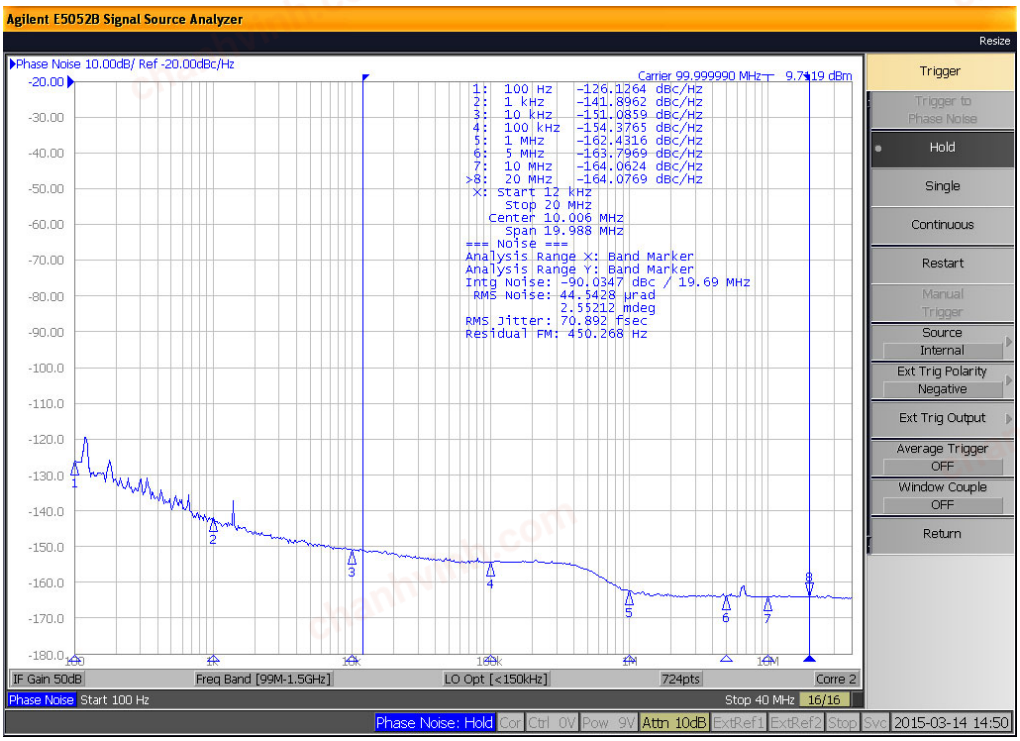


# Phase Noise Plots

The phase noise plots show the low additive jitter of the 5PB11xx high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 58.9fs of RMS phase jitter while the output of 5PB11xx has about 70.9fs of RMS phase jitter. This results in a low additive phase jitter of only 39fs.




**Reference Phase Noise 58.9fs (12kHz to 20MHz)**

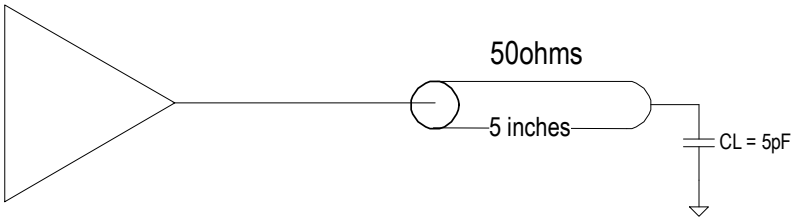



**Output Phase Noise 70.9fs (12kHz to 20MHz)**

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## Test Load and Circuit




## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/8-tssop-package-outline-drawing-44-mm-body-065mm-pitch-pgg8d1

www.idt.com/document/psc/14-tssop-package-outline-drawing-44mm-body-065mm-pitch-pgg14t1

www.idt.com/document/psc/16-tssop-package-outline-drawing-44mm-body-065mm-pitch-pgg16t1

www.idt.com/document/psc/20-tssop-package-outline-drawing-44-mm-body-065mm-pitch-pgg20d1

www.idt.com/document/psc/cmg8-package-outline-drawing-20-x-20-x-05-mm-body-05mm-pitch-dfn

www.idt.com/document/psc/cmg16-package-outline-drawing-25-x-25-x-05-mm-body-040mm-pitch-vfqfpn

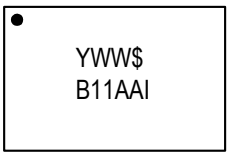
www.idt.com/document/psc/20-vfqfpn-package-outline-drawing-30-x-30-x-090-mm-040mm-pitch-165-x-165-mm-epad-ndg20p2

www.idt.com/document/psc/dfn-8-package-outline-drawing-20-x-20-x-075-mm-body-050mm-pitch-cmt8d1

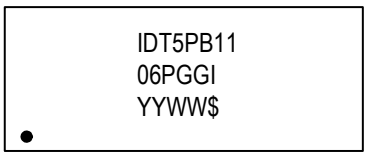
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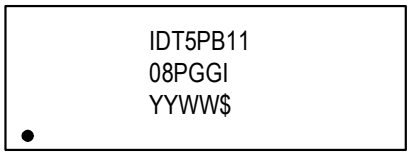
## Marking Diagrams (Industrial)



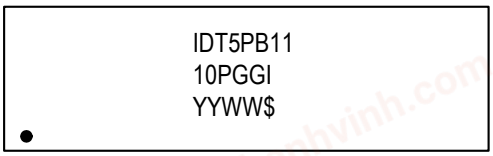

8-pin TSSOP



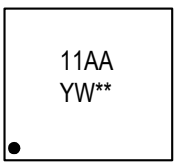

14-pin TSSOP



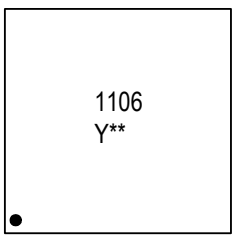

16-pin TSSOP



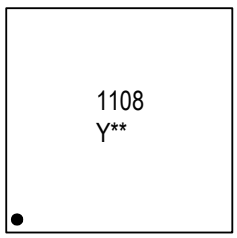

20-pin TSSOP



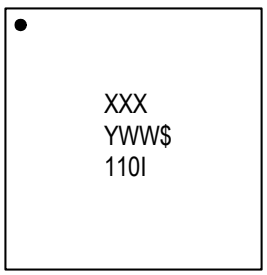

8-pin DFN




16-pin VFQFPN




16-pin VFQFPN



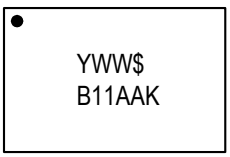

20-pin VFQFPN

- “AA” denotes the last two digits of the part number for 8-TSSOP and DFN (e.g. 02, 04).
- “**” is the lot sequence.
- “XXX” denotes the last three characters of the Asm lot (20-VFQFPN only).
- “YYWW”, “YWW”, “YW”, or “Y” is the last digit(s) of the year and work week that the part was assembled.
- “$” denotes the mark code.
- “G” after the two-letter package code denotes RoHS compliant package.
- “I” denotes industrial temperature range device.
- Bottom marking: LOT and COO (TSSOP only).

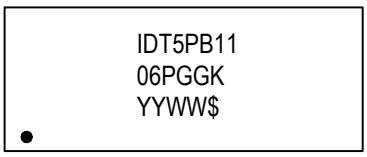
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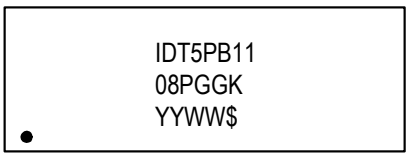
## Marking Diagrams (Extended)



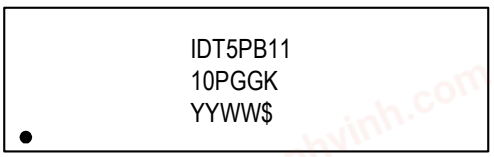

8-pin TSSOP




14-pin TSSOP



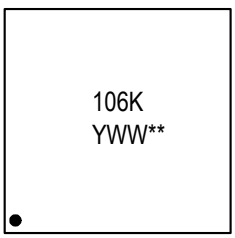

16-pin TSSOP



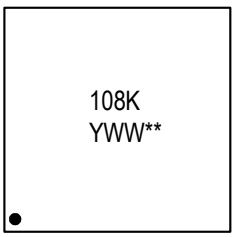

20-pin TSSOP



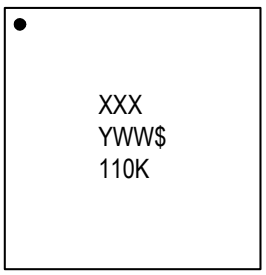

8-pin DFN




16-pin VFQFPN



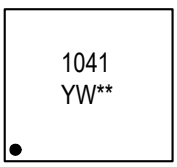

16-pin VFQFPN



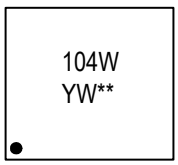

20-pin VFQFPN

- "AA" denotes the last two digits of the part number for 8-TSSOP and DFN (e.g. 02, 04).
- "**" is the lot sequence.
- "XXX" denotes the last three characters of the Asm lot (20-VFQFPN only).
- "YYWW", "YWW", "YW", or "Y" is the last digit(s) of the year and week that the part was assembled.
- "$" denotes the mark code.
- "G" after the two-letter package code denotes RoHS compliant package.
- "K" denotes extended temperature range device.
- Bottom marking: LOT and COO (TSSOP only).

## Marking Diagrams (Automotive)




8-pin DFN




8-pin DFN (wettable flank)

- Line 1: truncated part number; last number is the temperature grade: 1 = Automotive Grade 1.
- "YW" is the last digit of the year and work week that the part was assembled.
- "**" denotes the lot sequence number.

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# Ordering Information (Industrial)

| Orderable Part Number | Package | Carrier Type | Temperature |
|---|---|---|---|
| 5PB1102PGGI | 4.4mm body, 8-TSSOP | Tubes | -40 to +85°C |
| 5PB1102PGGI8 | | Tape and Reel | |
| 5PB1104PGGI | | Tubes | |
| 5PB1104PGGI8 | | Tape and Reel | |
| 5PB1106PGGI | 4.4mm body, 14-TSSOP | Tubes | |
| 5PB1106PGGI8 | | Tape and Reel | |
| 5PB1108PGGI | 4.4mm body, 16-TSSOP | Tubes | |
| 5PB1108PGGI8 | | Tape and Reel | |
| 5PB1110PGGI | 4.4mm body, 20-TSSOP | Tubes | |
| 5PB1110PGGI8 | | Tape and Reel | |
| 5PB1102CMGI | 2.0 × 2.0 × 0.5 mm, 8-DFN | Cut Tape | |
| 5PB1102CMGI8 | | Tape and Reel | |
| 5PB1104CMGI | | Cut Tape | |
| 5PB1104CMGI8 | | Tape and Reel | |
| 5PB1104CMGI/W* | | Tape and Reel | |
| 5PB1106CMGI | 2.5 × 2.5 × 0.5 mm,16-VFQFPN | Cut Tape | |
| 5PB1106CMGI8 | | Tape and Reel | |
| 5PB1108CMGI | | Cut Tape | |
| 5PB1108CMGI8 | | Tape and Reel | |
| 5PB1110NDGI | 3.0 × 3.0 × 0.90 mm, 20-VFQFPN | Tubes | |
| 5PB1110NDGI8 | | Tape and Reel | |

* “/W” stands for tape and reel with pin 1 orientation: EIA-481-D. All other tape and reels options come with EIA-481-C pin 1 orientation.

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## Ordering Information (Extended)

| Orderable Part Number | Package | Carrier Type | Temperature |
|---|---|---|---|
| 5PB1102PGGK | 4.4mm body, 8-TSSOP | Tubes | -40 to +105°C |
| 5PB1102PGGK8 | | Tape and Reel | |
| 5PB1104PGGK | | Tubes | |
| 5PB1104PGGK8 | | Tape and Reel | |
| 5PB1106PGGK | 4.4mm body, 14-TSSOP | Tubes | |
| 5PB1106PGGK8 | | Tape and Reel | |
| 5PB1108PGGK | 4.4mm body, 16-TSSOP | Tubes | |
| 5PB1108PGGK8 | | Tape and Reel | |
| 5PB1110PGGK | 4.4mm body, 20-TSSOP | Tubes | |
| 5PB1110PGGK8 | | Tape and Reel | |
| 5PB1102CMGK | 2.0 × 2.0 × 0.5 mm, 8-DFN | Cut Tape | |
| 5PB1102CMGK8 | | Tape and Reel | |
| 5PB1104CMGK | | Cut Tape | |
| 5PB1104CMGK8 | | Tape and Reel | |
| 5PB1106CMGK | 2.5 × 2.5 × 0.5 mm,16-VFQFPN | Cut Tape | |
| 5PB1106CMGK8 | | Tape and Reel | |
| 5PB1108CMGK | | Cut Tape | |
| 5PB1108CMGK8 | | Tape and Reel | |
| 5PB1110NDGK | 3.0 × 3.0 × 0.90 mm, 20-VFQFPN | Tubes | |
| 5PB1110NDGK8 | | Tape and Reel | |

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

## Ordering Information (Automotive)

| Orderable Part Number | Package | Carrier Type | Temperature |
|---|---|---|---|
| 5PB1104CMG1 | 2.0 × 2.0 × 0.5 mm, 8-DFN | Cut Tape | -40° to +125°C |
| 5PB1104CMG18 | | Tape and Reel | |
| 5PB1104CMT1 | 2.0 × 2.0 × 0.5 mm, 8-DFN, Wettable flank | Cut Tape | -40° to +125°C |
| 5PB1104CMT18 | | Tape and Reel | |

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# Revision History

| Revision Date | Description of Change |
|---|---|
| January 31, 2020 | Rebranded the document as Renesas. No technical changes were made. |
| December 4, 2019 | Added Input High and Low Leakage parameters to Table 6, Table 7, and Table 8 |
| May 31, 2019 | ▪ Added 5PB1104CMT1 wettable flank package information.<br>▪ Updated Propagation Delay values for automotive. |
| December 18, 2018 | ▪ Updated $t_{PD}$ and skew values.<br>▪ Added 5PB1104CMG1 automotive part information. |
| October 24, 2018 | Initial release. |

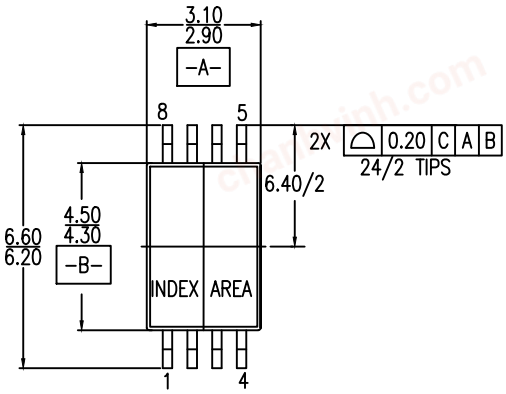
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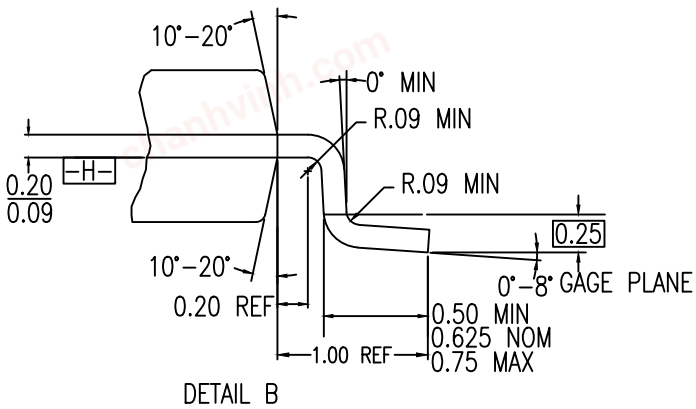
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# 8-TSSOP Package Outline Drawing

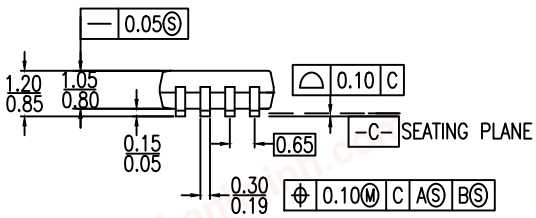
4.4 mm Body 0.65mm Pitch

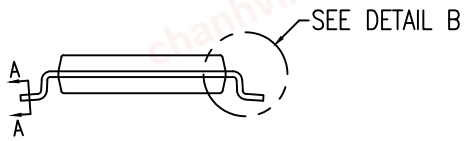


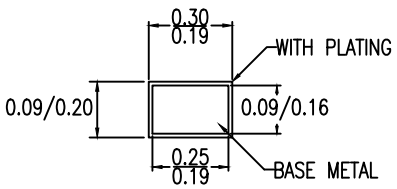



DETAIL B



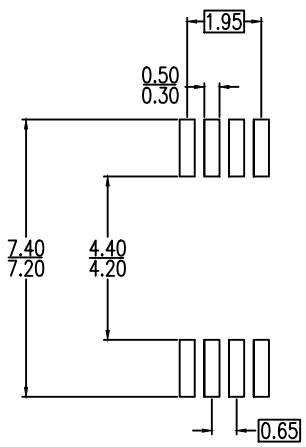

SECTION A-A

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSION ARE IN MM.

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RECOMMENDED LAND PATTERN DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| | | |
| July 27, 2018 | Rev 00 | Initial Release |

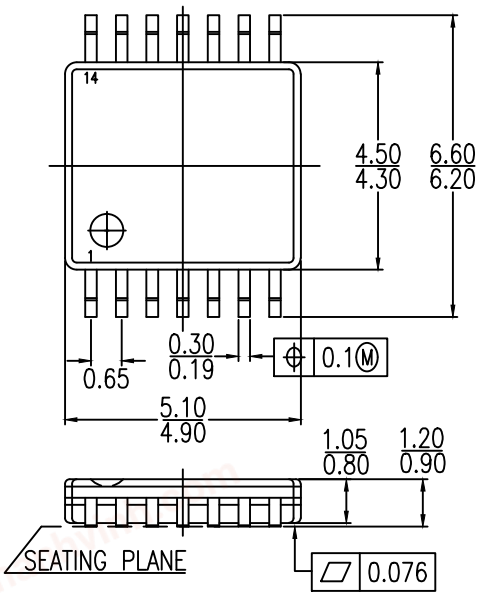
© Renesas Electronics Corporation

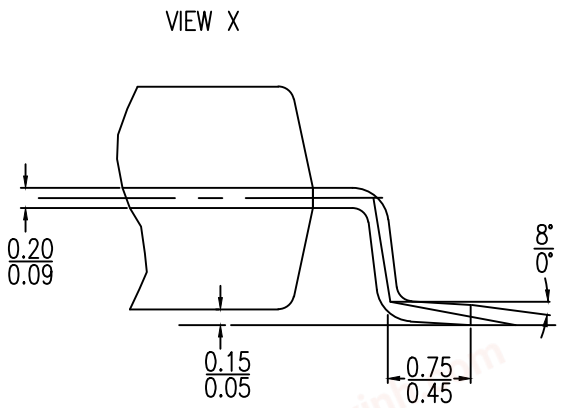
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# 14-TSSOP Package Outline Drawing

4.4mm Body, 0.65mm Pitch





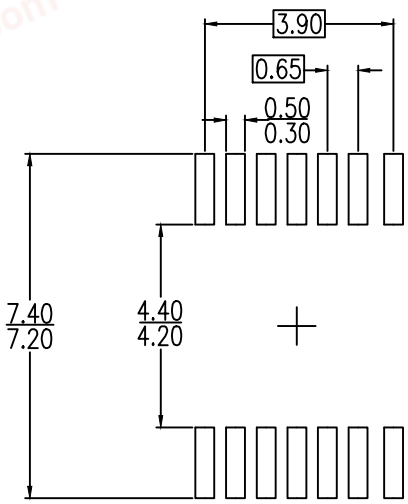

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS

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LAND PATTERN DIMENSIONS

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| Mar, 10 2017 | Rev 01 | Added Land Pattern |
| Dec, 19 2017 | Rev 02 | New Format |

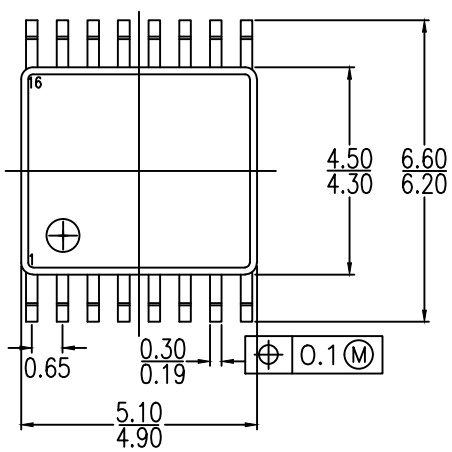
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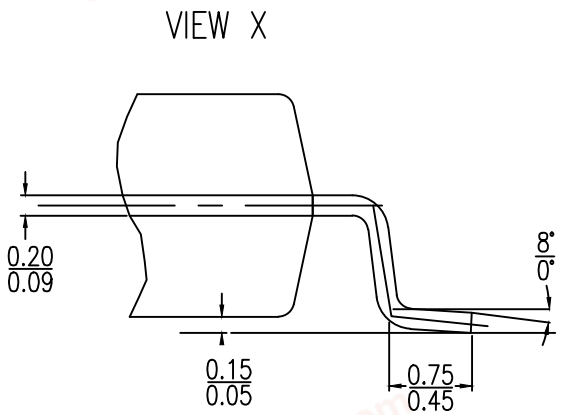
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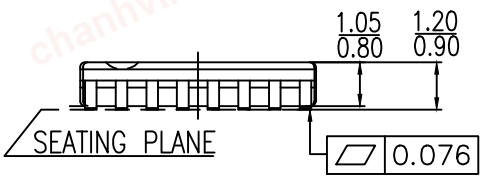
# 16-TSSOP Package Outline Drawing

4.4mm Body, 0.65mm Pitch





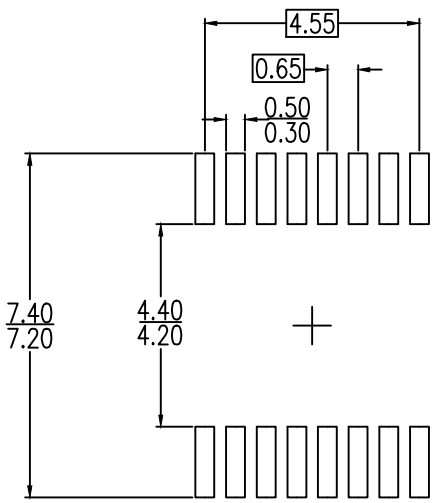

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS

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LAND PATTERN DIMENSIONS

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| | | |
| Jan 26, 2018 | Rev 00 | Revised from PSC-4056-02 PGG16 |

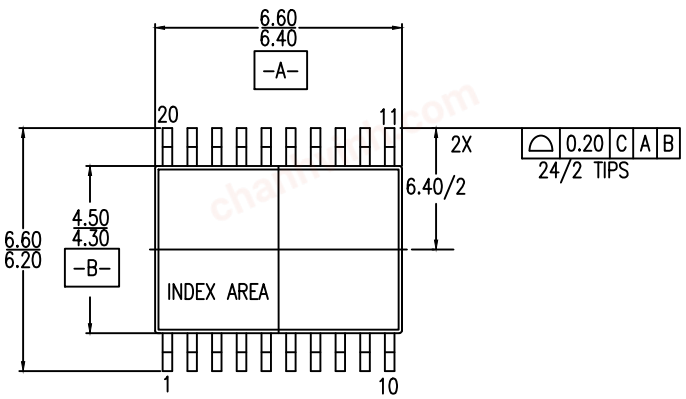
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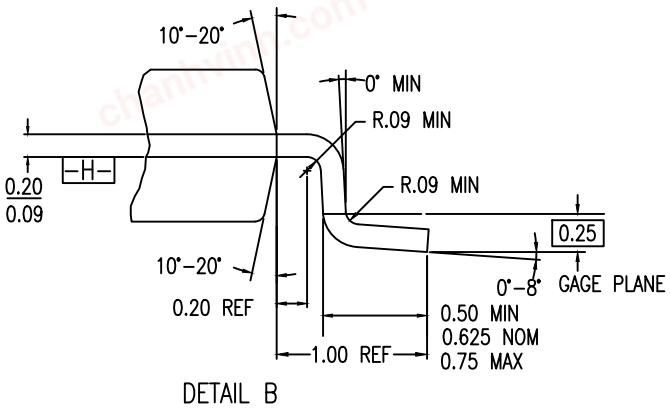
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# 20-TSSOP Package Outline Drawing

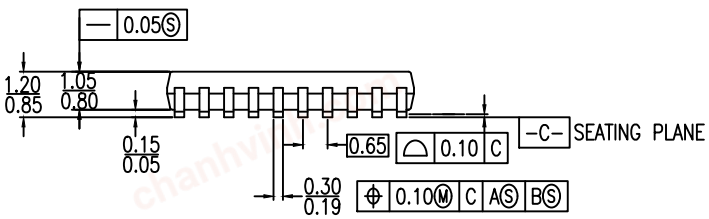
4.4 mm Body 0.65mm Pitch

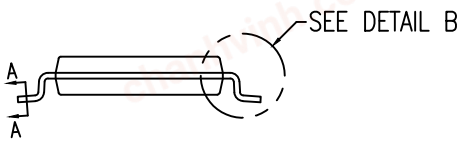


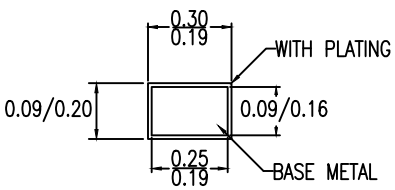



DETAIL B




SECTION A-A

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSION ARE IN MM.

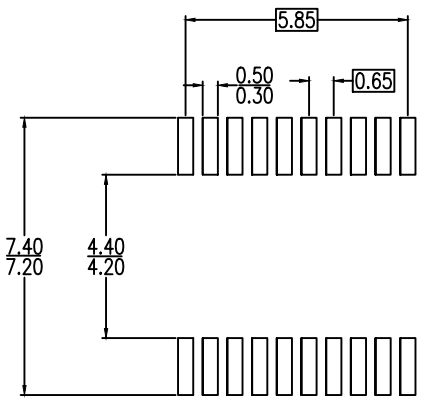
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# 20-TSSOP Package Outline Drawing

4.4 mm Body 0.65mm Pitch






RECOMMENDED LAND PATTERN DIMENSIONS

NOTES:

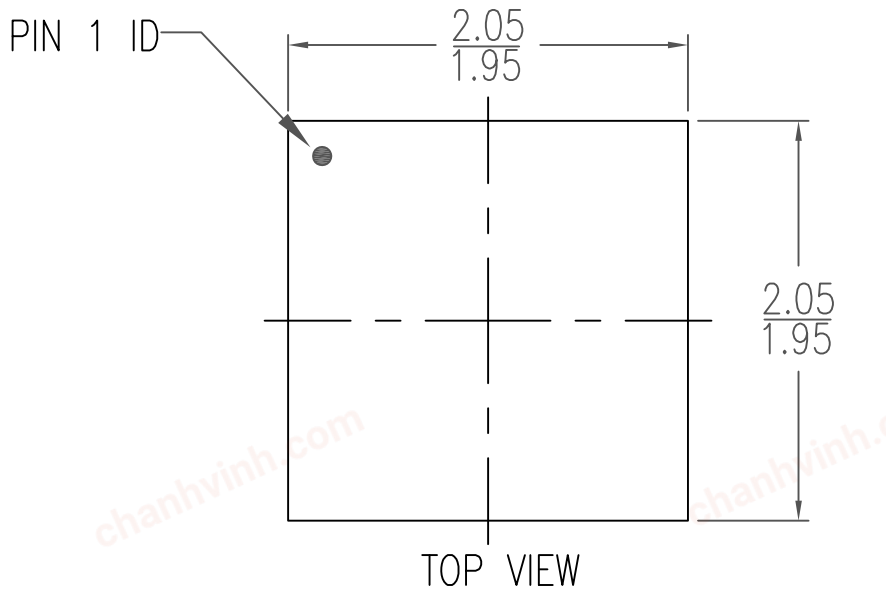
1. ALL DIMENSIONS ARE IN MILLIMETERS

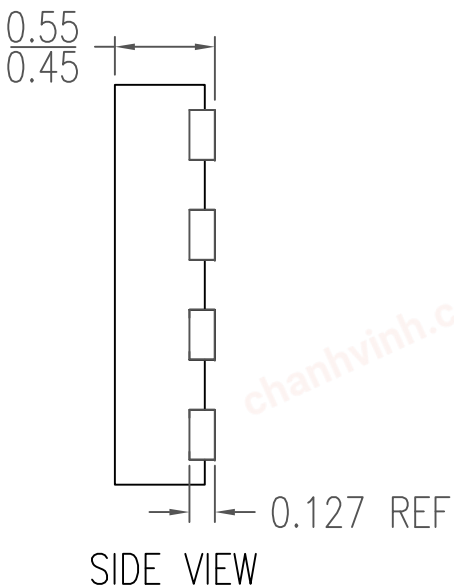
| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| | | |
| July 24, 2018 | Rev 00 | Initial Release |

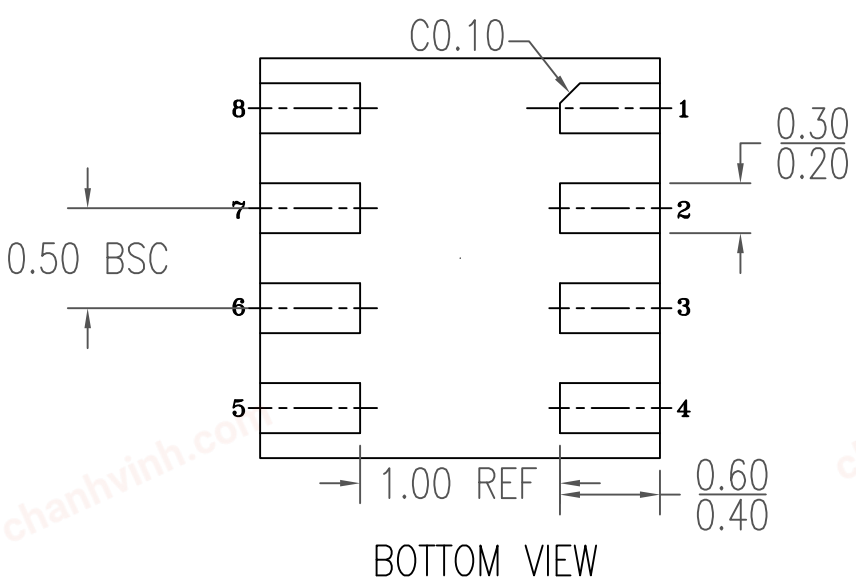
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| REVISIONS | | | |
|---|---|---|---|
| DATE CREATED | REV | DESCRIPTION | AUTHOR |
| 09/18/14 | 00 | INITIAL RELEASE | J.HUA |
| 4/5/18 | 01 | CHANGE VFQFN to DFN | R.C |
| NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE | | | |



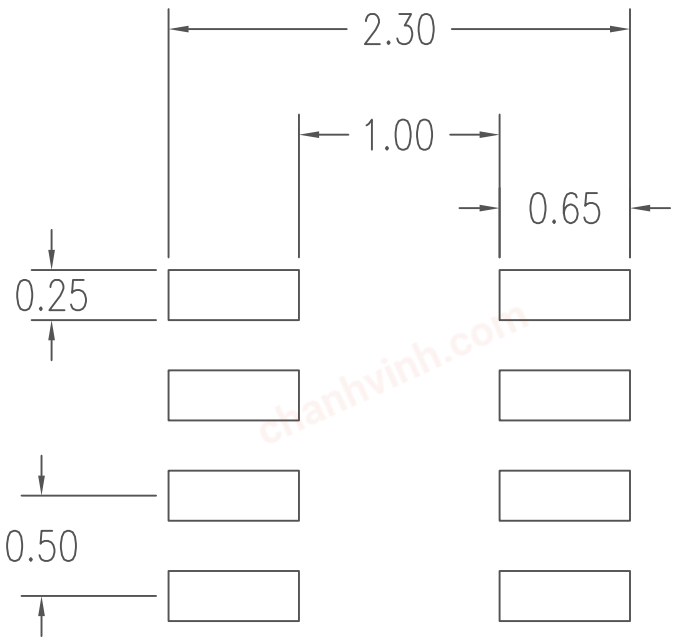




NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS

| | |
|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | IDT. www.IDT.com<br>6024 SILVER CREEK VALLEY ROAD<br>San Jose, CA 95138<br>PHONE: (408) 284–8200<br>FAX: (408) 492–8674 |
| | TITLE CMG8 Package Outline Drawing<br>2.0 x 2.0 x 0.5 mm Body<br>0.5mm Pitch DFN |
| | SIZE C \| DRAWING No. PSC–4490 \| REV 01 |
| | DO NOT SCALE DRAWING \| SHEET 1 OF 2 |

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| REVISIONS | | | |
|---|---|---|---|
| DATE CREATED | REV | DESCRIPTION | AUTHOR |
| 09/18/14 | 00 | INITIAL RELEASE | J.HUA |
| 4/5/18 | 01 | CHANGE VFQFN to DFN | R.C |
| NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE | | | |




RECOMMENDED LAND PATTERN DIMENSION

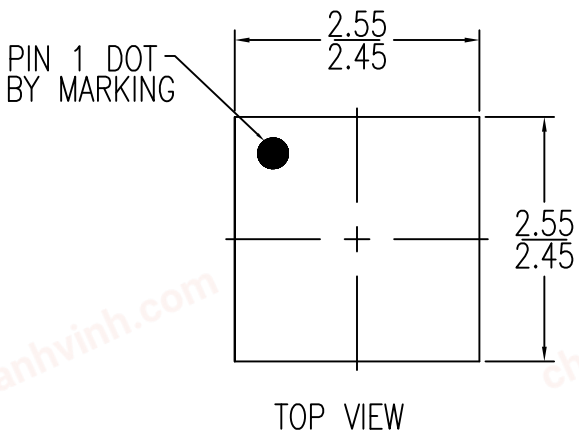
NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.

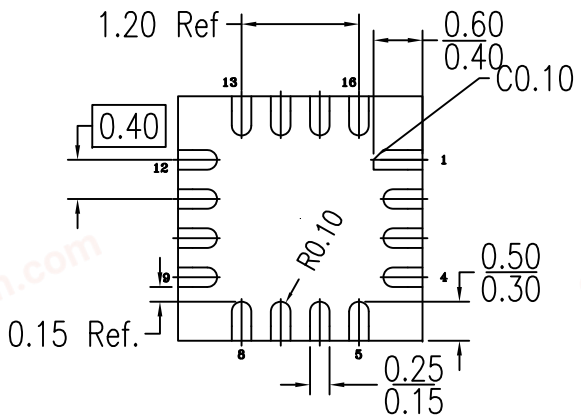
| | |
|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | IDT. www.IDT.com<br>6024 SILVER CREEK VALLEY ROAD<br>San Jose, CA 95138<br>PHONE: (408) 284-8200<br>FAX: (408) 492-8674 |
| | TITLE CMG8 Package Outline Drawing<br>2.0 x 2.0 x 0.5 mm Body<br>0.5mm Pitch DFN |
| | SIZE C \| DRAWING No. PSC-4490 \| REV 01 |
| | DO NOT SCALE DRAWING \| SHEET 2 OF 2 |

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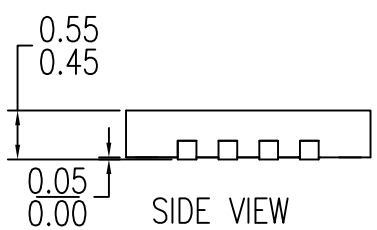
| REVISIONS | | | |
|---|---|---|---|
| DATE CREATED | REV | DESCRIPTION | AUTHOR |
| 4/3/14 | 00 | INITIAL RELEASE | JH |
| 12/11/14 | 01 | ADD PIN1 CHAMFER | JH |
| 4/5/18 | 02 | CHANGE QFN TO VFQFPN, RECALCULATE LAND PATTERN | RC |
| NOE: REFER TO DCP FOR OFFICIAL RELEASE DATE | | | |




TOP VIEW




BOTTOM VIEW



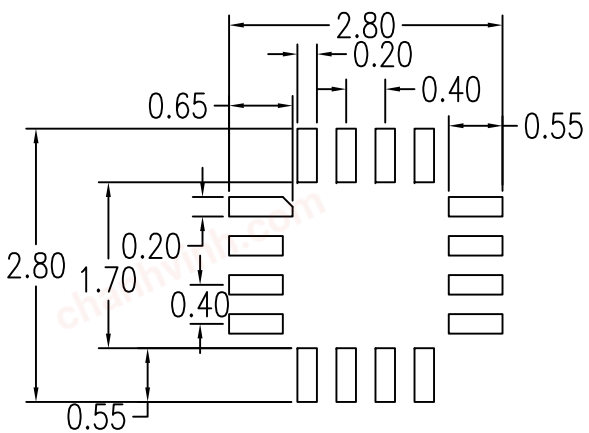

SIDE VIEW

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

| | |
|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>X± ±1°<br>XX±<br>XXX± | IDT™ www.IDT.com<br>6024 Silver Creek Valley Road<br>San Jose CA 95138<br>PHONE: (408) 284–8200<br>FAX: (408) 284–8591 |
| DRAWN | TITLE CMG16 Package Outline Drawing<br>2.5 x 2.5 x 0.5 mm Body<br>0.40mm Pitch VFQFPN |
| | SIZE C \| DRAWING No. PSC–4478 \| REV 02 |
| | DO NOT SCALE DRAWING \| SHEET 1 OF 2 |

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| REVISIONS | | | |
|---|---|---|---|
| DATE CREATED | REV | DESCRIPTION | AUTHOR |
| 4/3/14 | 00 | INITIAL RELEASE | JH |
| 12/11/14 | 01 | ADD PIN1 CHAMFER | JH |
| 4/5/18 | 02 | CHANGE QFN TO VFQFPN, RECALCULATE LAND PATTERN | RC |
| NOE: REFER TO DCP FOR OFFICIAL RELEASE DATE | | | |




RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
X± ±1°
XX±
XXX±

DRAWN

IDT™
www.IDT.com
6024 Silver Creek Valley Road
San Jose CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE CMG16 Package Outline Drawing
2.5 x 2.5 x 0.5 mm Body
0.40mm Pitch VFQFPN

| SIZE | DRAWING No. | REV |
|---|---|---|
| C | PSC-4478 | 02 |

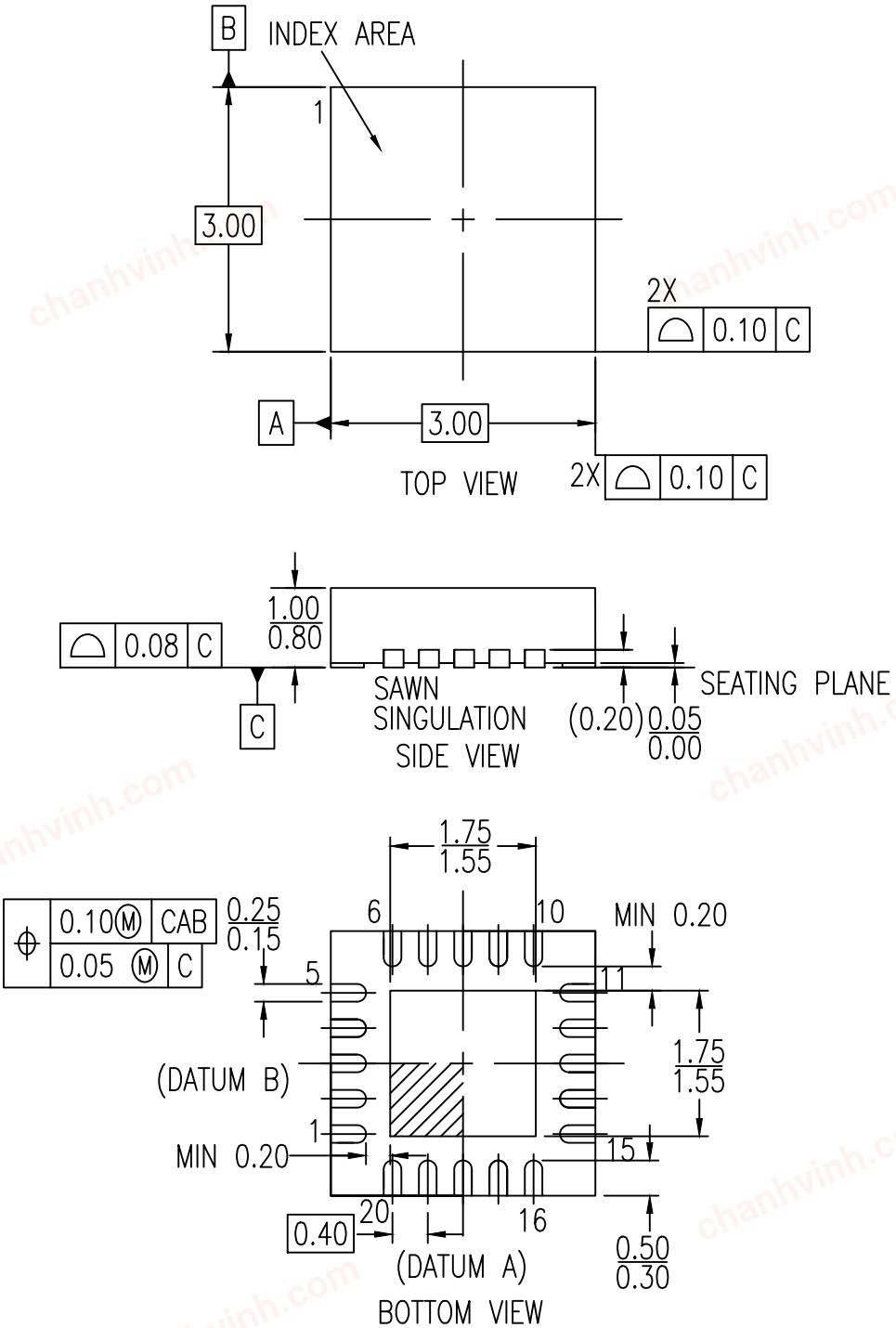
DO NOT SCALE DRAWING

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# 20-VFQFPN Package Outline Drawing

3.0 x 3.0 x 0.90 mm, 0.40mm Pitch, 1.65 x 1.65 mm Epad





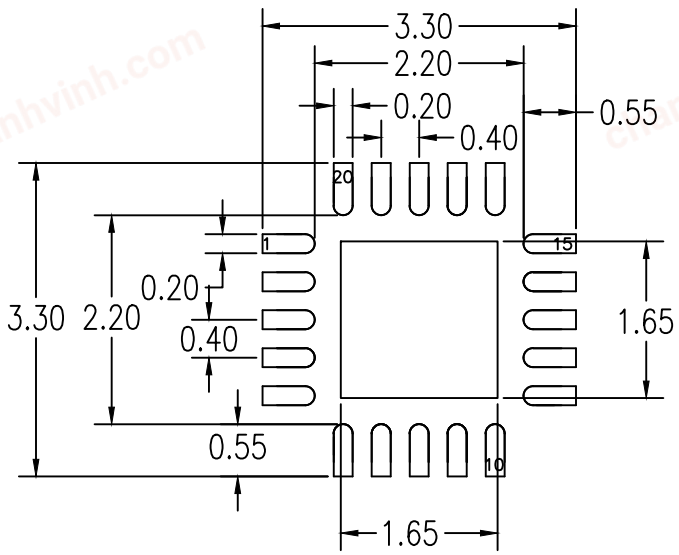

NOTE:

1. ALL DIMENSIONS ARE IN MM.
2. ALL DIMENSIONIONG AND TOLERANCING CONFORFM TOASME Y14.5–2009
3. PIN 1 LOCATION IDENTIFIER IS EITHER BY CHAMFER OR NOTCH

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| Sept 13, 2018 | Rev 01 | Change QFN to VFQFPN |
| Mar 30, 2016 | Rev 00 | Initial Release |

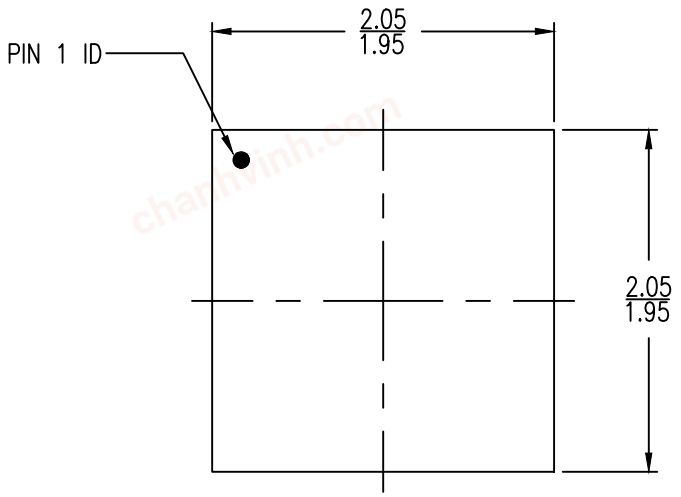
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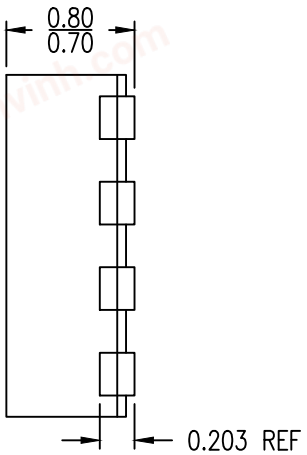
# DFN-8, Package Outline Drawing

2.0 x 2.0 x 0.75 mm Body, 0.50mm Pitch

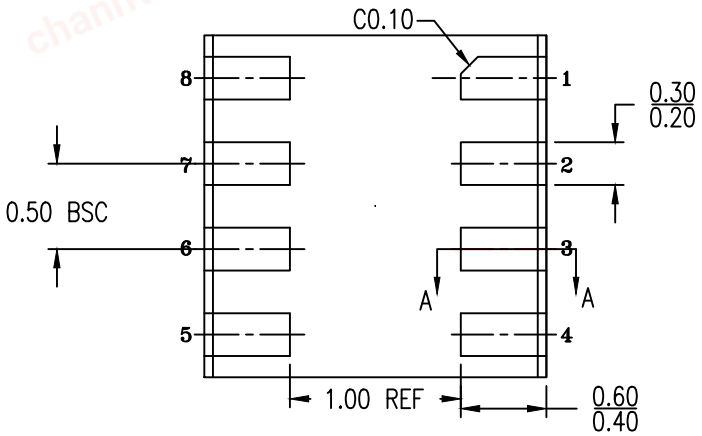




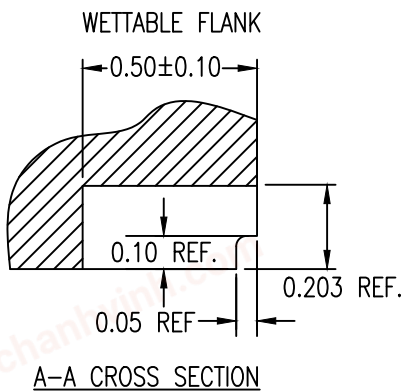

TOP VIEW




SIDE VIEW




BOTTOM VIEW




A–A CROSS SECTION

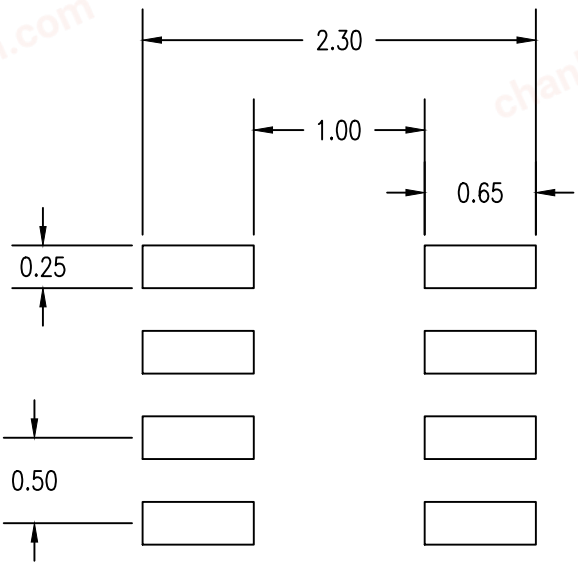
NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| | | |
| Oct 23, 2018 | Rev 00 | Initial Release |

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(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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www.renesas.com/contact/

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