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# MicroClock Programmable Clock Generator

5L1503
Datasheet

## Description

The 5L1503 is a series of small form factor programmable clock generators intended for low-power, consumer, battery powered applications, wearable and smart devices.

The device is a 1 PLL + DCO architecture design with an external fundamental crystal or clock input. The device allows up to 3 unique frequency outputs. The 5L1503 has built-in unique features such as Proactive Power Saving (PPS) and an extreme low power DCO to support system date/time keeping clock at 32.768kHz. Dynamic Frequency Control (DFC) supports dynamically changing between four different PLL frequencies via external requests with controlled frequency changes, reducing frequency overshoot and undershoot (ORT). The 5L1503S device can also support a spread clock output for EMI reduction. For a description of terms and their functions, see Glossary of Features.

An internal OTP memory allows the user to store up to four independent configurations that can be loaded on power-up without programming.

The 5L1503 supports three LVCMOS type outputs with VDDO1.8V, as well as various amplitude clocks. A low-power 32.768kHz clock is supported with only less than 1µA current consumption for system RTC reference clock needs.

| 5L1503 Base Number | Description | VCO Range (MHz) |
|---|---|---|
| 5L1503 | Standard, External Crystal | 50 – 130 |
| 5L1503L | Ultra Low-power, External Crystal | 50 – 130 |
| 5L1503S | Spread Clock, External Crystal | 500 –1100 |

## Typical Applications

- SmartDevice
- Handheld
- Wearable applications
- Portable Consumer applications

## Features

- Proactive Power Saving (PPS) features save power during the end device power-down mode
- Dynamic Frequency Control (DFC) feature allows programming up to 4 difference frequencies that switch dynamically
- Multiple output clock amplitude (1V, 1.1V, 1.2V and 1.8V) to support low swing clock requirement
- Dedicated 32kHz output with 6 clock amplitude options (5L1503L)
- Configurable through OTP programming
- Spread spectrum clock support (5L1503S)
- 1.8V operating supply voltage
- 2 × 2 mm 10-VFQFPN package

## Output Features

- 3 LVCMOS outputs, 1MHz–100MHz or 32.768kHz
- Low-power 32.768kHz clock supported

## Key Specifications

- Output cycle-cycle jitter: 50ps (typ)
- Low power-on fully active mode: 2mA (typ)
- Low-power 32.768kHz < 1.0µA (5L1503L)

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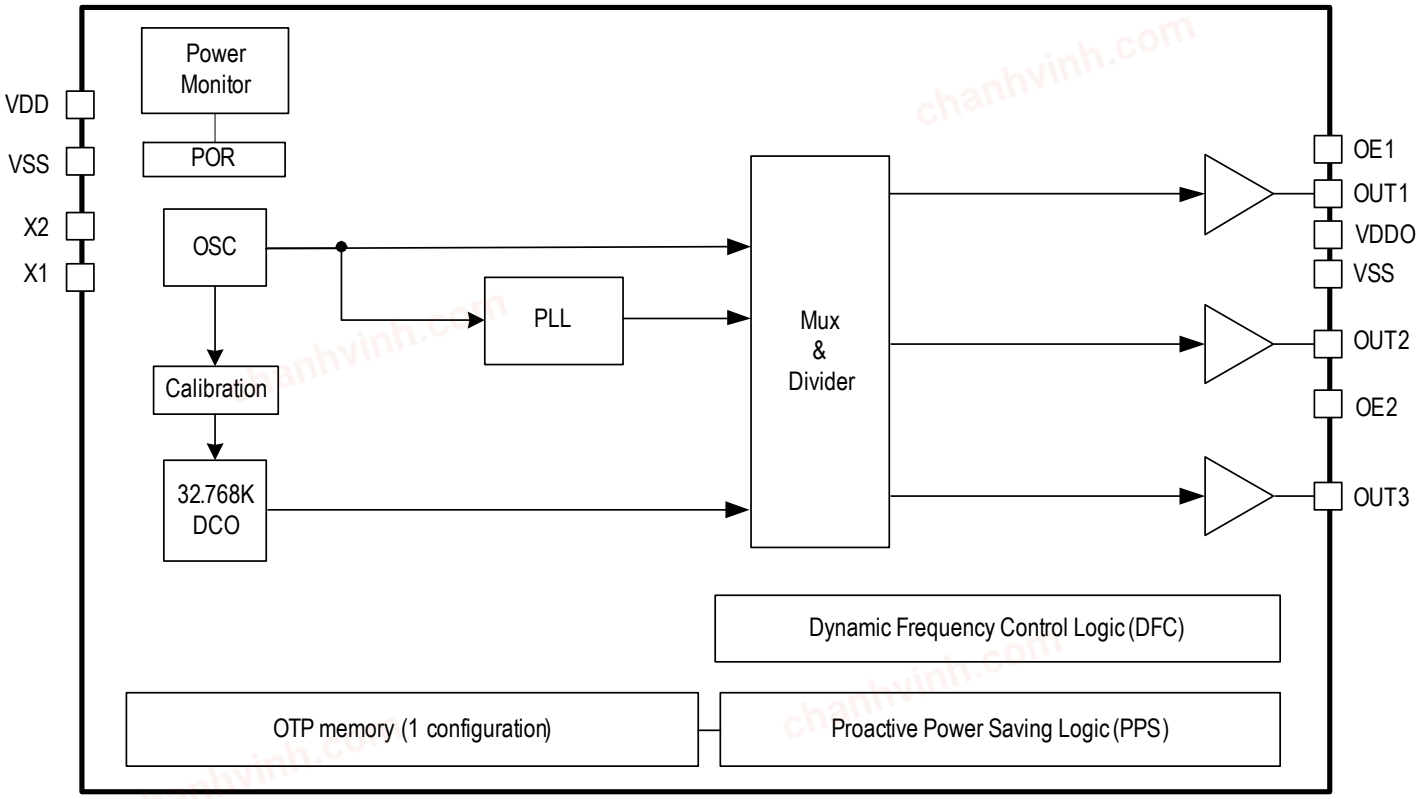
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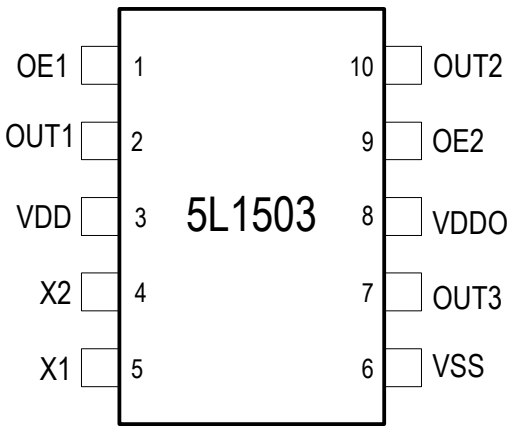


## Block Diagram




## Pin Assignments

Figure 1. Pin Assignments for 2.0 × 2.0 mm 10-VFQFPN Package



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# Pin Descriptions

Table 1. Pin Descriptions

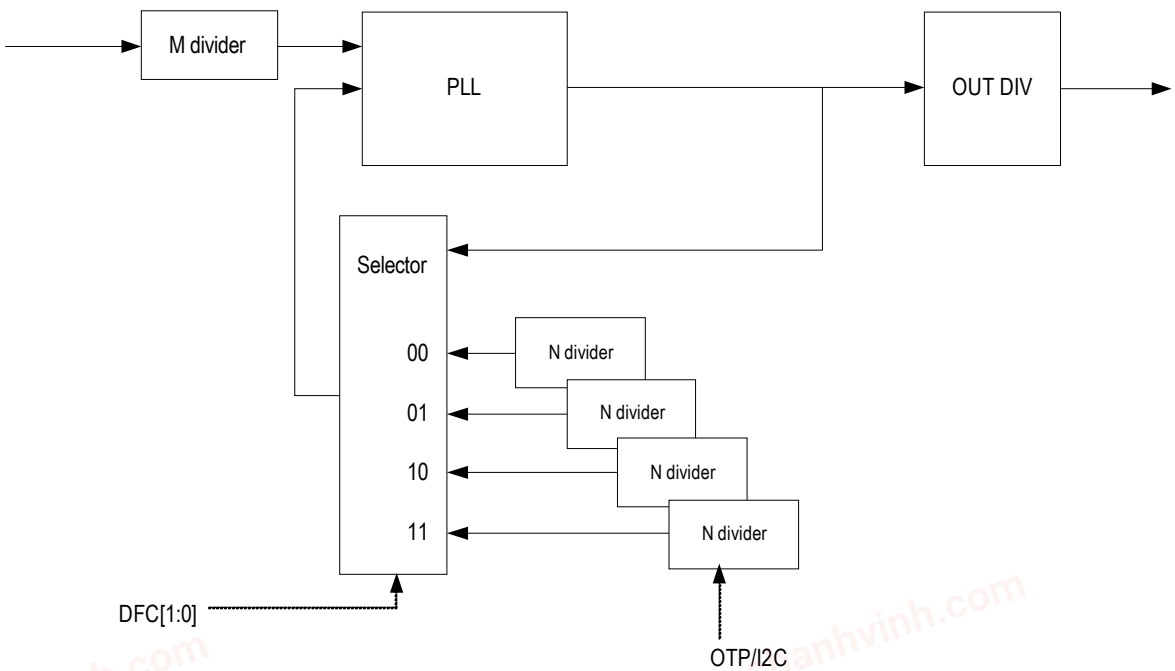
| Number | Name | Type | Description |
|---|---|---|---|
| 1 | OE1 | Input | OUT1 Output Enable Pin. The pin can be configured to other functions (DFC and PPS) refer to OE Pin Function table. |
| 2 | OUT1 | Output | Programmable LVCMOS clock output (32.768kHz only on 5L1503L). |
| 3 | VDD | Power | 1.8V power supply for core, PLL and 32kHZ DCO. |
| 4 | X2 | Output | Crystal oscillator interface output. |
| 5 | X1/CLKIN | Input | Crystal oscillator interface input or single-ended LVCMOS clock input. |
| 6 | VSS | GND | Connect to ground. |
| 7 | OUT3 | Output | Programmable LVCMOS clock output. |
| 8 | VDDO | Power | 1.8V power supply for I/O. |
| 9 | OE2 | Input | OUT2 output enable pin. The pin can be configured to other functions (DFC, PPS). |
| 10 | OUT2 | Output | Programmable LVCMOS clock output. |

# Device Feature and Function

## DFC – Dynamic Frequency Control

- OTP programmable–4 different feedback fractional dividers (4 VCO frequencies) that apply to PLL.
- ORT (overshoot reduction) function will be applied automatically during the VCO frequency change.
- Smooth frequency incremental or decremental from current VCO to targeted VCO based on DFC hardware pins selection.

Figure 2. DFC Function Block Diagram



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Table 2. DFC Function Priority

| Mode | DFC_EN B17[0] | SCL_HW_Mode_sel B18[5] | OE1_fun_sel B16[6:5] | OE2_fun_sel B16[3:2] | Config | DFC1 | DFC0 | Notes |
|---|---|---|---|---|---|---|---|---|
| x | 0 | x | x | x | x | x | x | DFC disable. |
| HW | 1 | 1 | 11 | 11 | OTP | OE2 | OE1 | Select via pins. |
| HW | 1 | 1 | 11 | 01 | OE2 | — | OE1 | Select via single pin. |

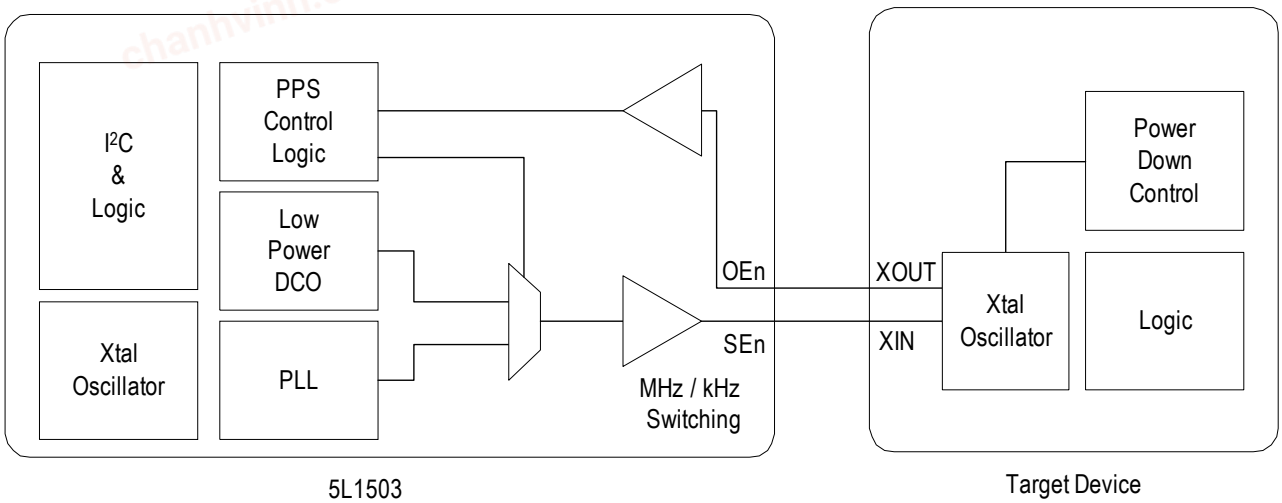
## DFC Function Programming

- Register B0b1:0 – select DFC00–DFC11 configuration.
- Byte5–8 are the registers for PLL VCO setting. Based on B0b1:0 configuration selection, the data write to B5–8 will be stored in selected configuration OTP memory.
- Refer to DFC Function Priority table. Select proper control pin(s) to activate DFC function.

## PPS – Proactive Power Saving Function

PPS (Proactive Power Saving) is an IDT patented unique design for the clock generator that proactively detects end device power down state and then switches output clocks between normal operation clock frequency and low power mode 32kHz clock that only consumes < 1.5µA current. The system could save power when the device goes into power down or sleep mode. The PPS function diagram is shown as below.

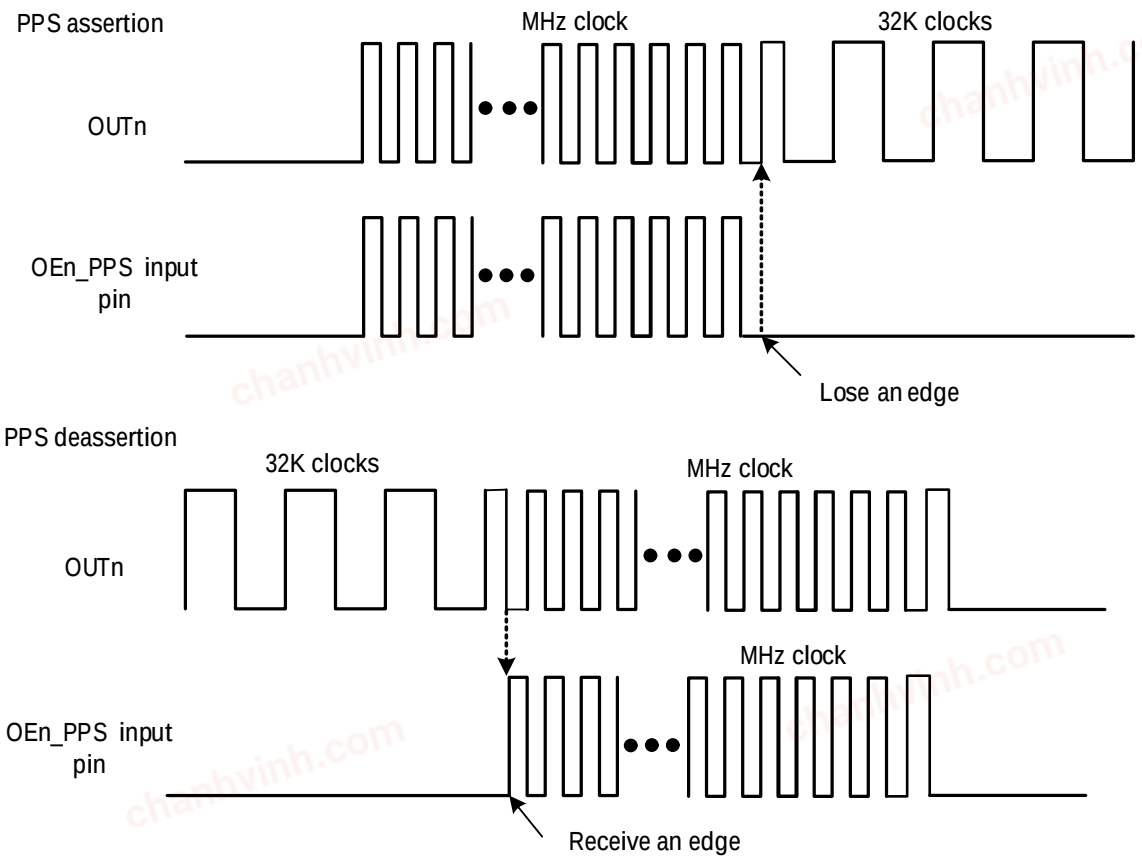
Figure 3. PPS Function Block Diagram



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Figure 4. PPS Assertion/Deassertion Timing Chart




## PPS Function Programming

- Refer to the OE Pin Function table to have proper PPS function selected for OE pin(s). Note that the register default is set to Output Enable (OE) function for OE pins.
- Have proper setup to Byte 16 for OE1–OE2 function selection. For PPS function, select 10 to control register bits.

## Output Divider Selection

Table 3. Output Divider Selection

| Output Divider bits<4:3> | Output Divider bits<2:0> | | | | | |
|---|---|---|---|---|---|---|
| | 000 | 001 | 010 | 011 | 100 | 101 |
| 00 | 1 | 3 | 5 | 7 | 9 | 11 |
| 01 | 2 | 6 | 10 | 14 | 18 | 22 |
| 10 | 4 | 12 | 20 | 28 | 36 | 44 |
| 11 | 8 | 24 | 40 | 56 | 72 | 88 |

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## Device Output Support

### 5L1503

| Outputs | Frequency | Amplitude | VCO Range | Spread Spectrum |
|---|---|---|---|---|
| OUT1 | 32kHz or up to 100MHz LVCMOS | 1.8V | 50MHz – 130MHz | N/A |
| OUT2 | | 1V, 1.1V, 1.2V, 1.8V | | |
| OUT3 | | | | |

### 5L1503L

| Outputs | Frequency | Amplitude | VCO Range | Spread Spectrum |
|---|---|---|---|---|
| OUT1 | 32kHz | 0.8V, 0.9V, 1V, 1.1V, 1.2V, 1.8V | 50MHz – 130MHz | N/A |
| OUT2 | 32kHz or up to 100MHz LVCMOS | 1V, 1.1V,1.2V,1.8V | | |
| OUT3 | | | | |

### 5L1503S

| Outputs | Frequency | Amplitude | VCO Range | Spread Spectrum |
|---|---|---|---|---|
| OUT1 | 32kHz or up to 100MHz LVCMOS | 1.8V | 500MHz – 1100MHz | Available |
| OUT2 | | 1V, 1.1V, 1.2V, 1.8V | | |
| OUT3 | | | | |

## OE Pin Function

OE pins in the 5L1503 have multiple functions. The OE pins can be configured as output enable control (OE) or chip power-down control (PD#) or Proactive Power Saving function (PPS). Furthermore, the OE pins can be configured as single or Dynamic Frequency Control (DFC).

Table 4. OE Pin Function

| Function | OE1 | | OE2 | |
|---|---|---|---|---|
| | B16<6:5> | Function | B16<3:2> | Function |
| SE Output Enable/Disable | 00 | OUT1 (Default) | 00 | OUT2 (Default) |
| Global Power Down (PD#) | 01 | PD# | 01 | Config_SEL |
| Proactive Power Saving Input | 10 | OUT1_PPS | 10 | OUT2_PPS |
| DFC Control | 11 | DFC0 | 11 | DFC1 |

Note: Config_SEL and DFC Control require the device to be in H/W mode with no I2C access.

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Table 5. OE Pin Function Summary

| Pin | Function |
|---|---|
| OE1: OUT1 | OE1 only control OUT1 enable/disable, other outputs are not affected by this pin status. |
| OE2: OUT2 | OE2 only control OUT2 enable/disable, other outputs are not affected by this pin status. |
| OE1: PD# | OE1 control chip global power down (PD#) except 32.768kHz on OE1 (when 32K is enabled), When the PD# pin is active low, the chip goes to lowest power down mode and all outputs are disabled except 32kHz output, and only keeps 32k/Xtal calibration. |
| OE1: OUT1_PPS | Config OE1 as OUT1_PPS (Proactive Power Saving) function pin. |
| OE2: OUT2_PPS | Config OE2 as OUT2_PPS (Proactive Power Saving) function pin. |
| OE1:DFC0 | Config OE1 as DFC0 control pin 0. |
| OE2:DFC1 | Config OE2 as DFC1 control pin 1. |

Table 6. PD# Priority

| PD# | I2C_OE_EN_bit | OUT1/2/3, OUTx_PPS | Output | Notes |
|---|---|---|---|---|
| 0 | x | x | stop | 32kHz free run |
| 1 | 0 | x | stop | |
| 1 | 1 | 0 | stop | |
| 1 | 1 | 1 | running | |

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# Spread Spectrum

## Spread Spectrum

The 5L1503 supports spread spectrum clocks from PLL with digital spread spectrum.

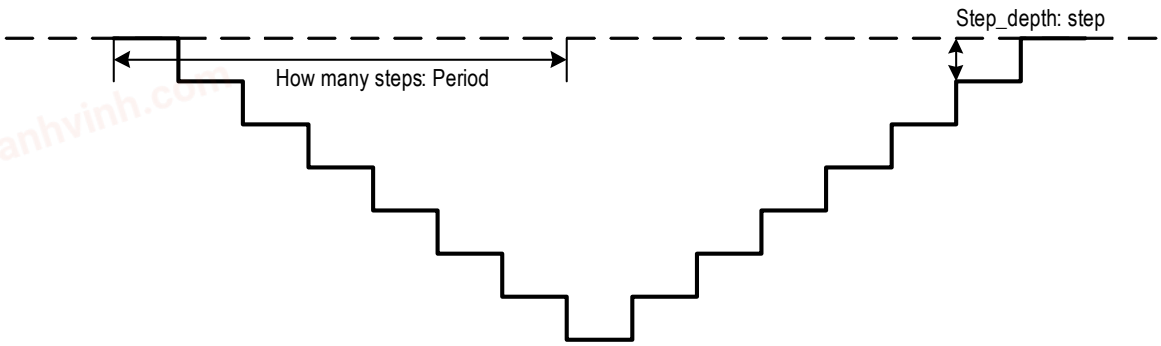
### Digital Spread Spectrum

Figure 5. Digital Spread Spectrum

$$N = \frac{Fvco}{2 * Fout}$$

$$period = \frac{Fpfd}{2 * Fss}$$

$$step = \frac{N * SSamount}{period}$$




Down spread or spread off

N = Fvco/Fpfd
N: include integer and fraction
Fvco: VCOs frequency
Fpfd: PLLs pfd frequency
Fss: spread modulation rate
SSamount: spread percentage

N will decrease to make the center frequency lower than spread off.

Example: 0.5% down spread at 32kHz modulation rate.

## Reference Input and Selection

The 5L1503 accepts an 8MHz–40MHz crystal input or 1MHz–100MHz LVCMOS (to X1) input. See the Crystal Oscillator Reference Circuit for details.

### Crystal Input (X1/X2)

The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 54MHz maximum.

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate as 0 PPM. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal.

In order to get an accurate oscillation frequency, the matching the oscillator load capacitance with the crystal load capacitance is required.

To set the oscillator load capacitance, 5L1503 has built-in two programmable tuning capacitors inside the chip, one at XIN and one at XOUT. They can not be adjusted independently, The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL_CAP[3:0] register.

Adjustment of the crystal tuning capacitors allows for maximum flexibility to accommodate crystals from various manufacturers. The approximate range of tuning capacitor values available are in accordance with the following table.

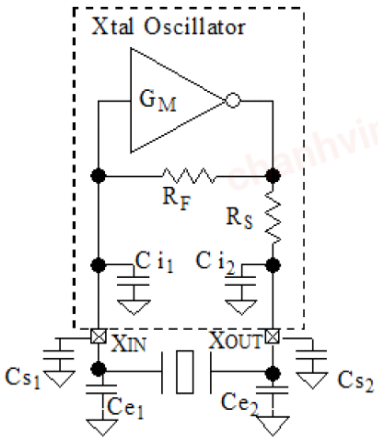
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Table 7. Programmable Tuning Capacitors

| Parameter | Bits | Range | Minimum (pF) | Maximum (pF) |
|---|---|---|---|---|
| XTAL [3:0] | 4 × 2 | +1 / +2 / +4 / +8 pF | 0 | 15 |

Figure 6. Crystal Oscillator Reference Circuit




XTAL[4:0] = (XTAL CL - 7pF) × 2 (Eq.1)

Equation 1 and the Programmable Tuning Capacitors table show that the parallel tuning capacitance can be set between 4.5pF to 12.5pF with a resolution of 0.25 pF.

For a crystal $C_L$= 8pF, where $C_L$ is the parallel capacity specified by the crystal vendor that sets the crystal frequency to the nominal value. Under the assumptions that the stray capacity between the crystal leads on the circuit board is zero and that no external tuning caps are placed on the crystal leads, then the internal parallel tuning capacity is equal to the load capacity presented to the crystal by the device.

The internal load capacitors are true parallel-plate capacitors for ultra-linear performance. Parallel-plate capacitors were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. External non-linear crystal load capacitors should not be used for applications that are sensitive to absolute frequency requirements.

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## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5L1503. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 8. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Supply Voltage: $V_{DD}$, $V_{DDO}$ | -0.5V – 2.2V |
| Inputs; DFC, OE1, OE2, SCL | -0.5V to $V_{DD}/V_{DDO}$ |
| Outputs: LVCMOS | -0.5V to $V_{DD}/V_{DDO}$ + 0.5V |
| Outputs: SDA | 10mA |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |
| ESD Human Body Model | 2000V |
| Junction Temperature | 125°C |

## Thermal Characteristics

Table 9. Thermal Characteristics

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $\theta_{Jb}$ | Theta $J_B$. Junction to board | 23.6 | °C/W |
| $\theta_{JC}$ | Theta $J_C$. Junction to case | 185.3 | °C/W |
| | Moisture Sensitivity Rating (per J-STD-020) | MSL1 | — |

## Recommended Operating Conditions

Table 10. Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 1.71 | — | 1.89 | V |
| $V_{DDO}$ | Power Supply Voltage | 1.71 | — | 1.89 | V |
| $T_A$ | Ambient Operating Temperature | -40 | — | 85 | °C |
| $C_{LOAD_OUT}$ | Maximum Load Capacitance (1.8V LVCMOS only) | — | 2 | — | pF |
| $t_{PU}$ | Power-up Time for all $V_{DD}$s to reach Minimum Specified Voltage (power ramps must be monotonic) | 0.05 | — | 3 | ms |

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## Crystal Characteristics

Table 11. Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | — | Fundamental | | | |
| Frequency | — | 8 | — | 40 | MHz |
| Frequency Tolerance [1] | — | — | — | ±20 | ppm |
| Equivalent Series Resistance (ESR) | — | — | 10 | 80 | Ω |
| Shunt Capacitance | — | — | 2 | 7 | pF |
| Load Capacitance ($C_L$) | — | 6 | 8 | 10 | pF |
| Maximum Crystal Drive Level | — | — | — | 100 | µW |

[1] Frequency tolerance includes initial frequency, over temperature range and aging data.

[2] High Drive only when crystal frequency is higher than 30MHz.

## DC Electrical Characteristics

Table 12. DC Electrical Characteristics – Current

$V_{DD}$ = $V_{DDO}$ = 1.8V ±5%, $V_{SS}$ = 0V, $T_A$ = -40°C to +85°C.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| Idd | Core Supply Current (5L1503/5L1503L) | $V_{DD}$ = $V_{DDO}$ = 1.8V, Xtal = 54MHz, DCO = OFF, no output; PLL default. | — | — | 2.0 | mA |
| | Core Supply Current (5L1503S) | $V_{DD}$ = $V_{DDO}$ = 1.8V, Xtal = 54MHz, DCO = OFF, no output; PLL default. | — | — | 9.5 | mA |
| Idd_PLL | PLL Supply Current (5L1503/5L1503L) | $V_{DD}$ = $V_{DDO}$ = 1.8V, Xtal = 54MHz, no output; PLL= default | — | — | 1.0 | mA |
| | PLL Supply Current (5L1503S) | $V_{DD}$ = $V_{DDO}$ = 1.8V, Xtal = 54MHz, no output; PLL= default | — | — | 9.0 | mA |
| Iddox | Output Buffer Supply Current (5L1503/5L1503L) | LVCMOS, OUT1 = 8MHz, $V_{DD}$ = $V_{DDO}$ = 1.8V. | — | — | 0.5 | mA |
| | | LVCMOS, OUT1 = 100MHz, $V_{DD}$ = $V_{DDO}$ = 1.8V. | — | — | 2 | mA |
| | Output Buffer Supply Current (5L1503S) | LVCMOS, OUT1 = 8MHz, $V_{DD}$ = $V_{DDO}$ = 1.8V. | — | — | 0.5 | mA |
| | | LVCMOS, OUT1 = 100MHz, $V_{DD}$ = $V_{DDO}$ = 1.8V. | — | — | 2 | mA |
| Iddpd | Power Down Current (5L1503/5L1503L) | PD asserted with $V_{DD}$ and $V_{DDO}$ ON, I2C enable, 32.768kHz clock running. | — | — | 310 | µA |
| | Power Down Current (5L1503S) | PD asserted with $V_{DD}$ and $V_{DDO}$ ON, I2C enable, 32.768kHz clock running. | — | — | 320 | µA |
| Iddupd | Ultra Power Down Current (5L1503/5L1503L) | PD asserted with $V_{DD}$ and $V_{DDO}$ ON, I2C disable, 32.768kHz clock running. | — | — | 7 | µA |
| | Ultra Power Down Current (5L1503S) | PD asserted with $V_{DD}$ and $V_{DDO}$ ON, I2C disable, 32.768kHz clock running. | — | — | 9.5 | µA |

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Table 12. DC Electrical Characteristics – Current (Cont.)

$V_{DD}$ = $V_{DDO}$ = 1.8V ±5%, $V_{SS}$ = 0V, $T_A$ = -40°C to +85°C.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| Iddsuspend | Power Suspend Current (5L1503) | $V_{DDD}$ = 1.8V, $V_{DDO}$ = GND, OUT1 = 32.768kHz running in DCO mode, no output loads, I2C and OE pins open. | — | — | 1.4 | µA |
| | Power Suspend Current (5L1503L) | $V_{DDD}$ = 1.8V, $V_{DDO}$ = GND, OUT1 = 32.768kHz running in DCO mode, no output loads, I2C and OE pins open. | — | — | 1 | µA |
| | Power Suspend Current (5L1503S) | $V_{DDD}$ = 1.8V, $V_{DDO}$ = GND, OUT1 = 32.768kHz running in DCO mode, no output loads, I2C and OE pins open. | — | — | 1.4 | µA |

Table 13. DC Electrical Characteristics – Input and Output Voltage

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -8mA. | 0.7 × $V_{DDO}$ | — | $V_{DDO}$ | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8mA. | — | — | 0.25 × $V_{DDO}$ | V |
| $I_{OZDD}$ | Output Leakage Current | Tri-state outputs, $V_{DDO}$ = 1.89V. | — | — | 80 | µA |
| $V_{IH}$ | Input High Voltage | Single-ended inputs – OE. | 0.65 × $V_{DDO}$ | — | $V_{DDO}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | Single-ended inputs – OE. | GND - 0.3 | — | 0.35 × $V_{DDO}$ | V |

# AC Electrical Characteristics

Table 14. AC Timing Electrical Characteristics

$V_{DDSE}$= 1.8V ±5%, $T_A$ = -40°C to +85°C. Spread spectrum = OFF.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Xtal Frequency Range | Input frequency limit (XIN)[1]. | 8 | — | 40 | MHz |
| | Clock In | Input frequency limit (Clock In). | 1 | — | 100 | MHz |
| $f_{OUT}$ | Output Frequency | Single-ended clock output limit (LVCMOS). | 1 | — | 100 | MHz |
| $f_{VCO1}$ | VCO Frequency Range of PLL | VCO operating frequency range (5L1503). | 50 | — | 130 | MHz |
| $f_{VCO2}$ | VCO Frequency Range of PLL | VCO operating frequency range (5L1503L). | 50 | — | 130 | MHz |
| $f_{VCO3}$ | VCO Frequency Range of PLL | VCO operating frequency range (5L1503S). | 500 | — | 1100 | MHz |
| $f_{PFD1}$ | PFD Frequency Range of PLL1 | PFD operating frequency range (5L1503 and 5L1503L). | 0 | — | 13 | MHz |
| $f_{PFD1}$ | PFD Frequency Range of PLL1 | PFD operating frequency range(5L1503S). | 0.8 | — | 100 | MHz |
| $f_{BW1}$ | Loop Bandwidth for PLL1 | Input frequency = TBD. | 0.001 | — | 1 | MHz |
| $F_{32K_ACC1}$ | 32K Stability | Average accuracy after 24 hours[2]. | — | — | 42 | ppm |
| $F_{32K_ACC2}$ | 32K Stability | Average accuracy after 3 days[2]. | — | — | 36 | ppm |

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Table 14. AC Timing Electrical Characteristics (Cont.)

$V_{DDSE}$= 1.8V ±5%, $T_A$ = -40°C to +85°C. Spread spectrum = OFF.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $F_{32K_ACC3}$ | 32K Stability | Average accuracy after 7 days[2]. | — | — | 32 | ppm |
| | Minimum Input Amplitude | For a 40/60% SE input duty cycle. | 800 | — | $V_{DD}$ | mV |
| t2 | Input Duty Cycle | Duty cycle. | 30 | — | 70 | % |
| t3 | Output Duty Cycle | Measured at $V_{DD}$/2, all outputs with a crystal or a 50% input duty cycle clock. | 45 | — | 55 | % |
| t4[3] | Rise/Fall Slew Rate | 1.8V LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$ (output load = 2pF). | — | 2.0 | — | V/ns |
| t4[3] | Rise/Fall Slew Rate | 1.2V LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$ (output load = 2pF). | — | 1.1 | — | V/ns |
| t4[3] | Rise/Fall Slew Rate | 1.1V LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$ (output load = 2pF). | — | 1.0 | — | V/ns |
| t4[3] | Rise/Fall Slew Rate | 1.0V LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$ (output load = 2pF). | — | 1.0 | — | V/ns |
| t4 | Rise/Fall Slew | OUT1 1.8V 32kHz LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$, Byte20<2:0> = x0 (5X1503L). | — | 27.4 | — | V/µs |
| t4 | Rise/Fall Slew | OUT1 0.8V 32kHz LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$, Byte20<2:0> = x1 (5X1503L). | — | 2.3 | — | V/µs |
| t4 | Rise/Fall Slew | OUT1 0.9V 32kHz LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$, Byte20<2:0> = x2 (5X1503L). | — | 3.9 | — | V/µs |
| t4 | Rise/Fall Slew | OUT1 1.0V 32kHz LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$, Byte20<2:0> = x3 (5X1503L). | — | 5.4 | — | V/µs |
| t4 | Rise/Fall Slew | OUT1 1.1V 32kHz LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$, Byte20<2:0> = x4 (5X1503L). | — | 6.7 | — | V/µs |
| t4 | Rise/Fall Slew | OUT1 1.2V 32kHz LVCMOS clock rise and fall time, 20% to 80% of $V_{DDO}$/$V_{DD}$, Byte20<2:0> = x5 (5X1503L). | — | 8.5 | — | V/µs |
| t6[4] | Clock Jitter | Cycle-to-cycle jitter, 1.8V LVCMOS output clock.<br>OUT1 = 32.768kHz (1.8V LVCMOS)<br>OUT2 = 72MHz<br>OUT3 = 26MHz | — | 50 | — | ps |

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Table 14. AC Timing Electrical Characteristics (Cont.)

$V_{DDSE}$= 1.8V ±5%, $T_A$ = -40°C to +85°C. Spread spectrum = OFF.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| t6[4] | Clock Jitter | Cycle-to-cycle jitter, 1.2V LVCMOS output clock.<br>SOUT1 = 32.768kHz (1.8V LVCMOS)<br>OUT2 = 72MHz<br>OUT3 = 26MHz | — | 50 | — | ps |
| t6[4] | Clock Jitter | Cycle-to-cycle jitter, 1.1V LVCMOS output clock.<br>OUT1 = 32.768kHz (1.8V LVCMOS)<br>OUT2 = 72MHz<br>OUT3 = 26MHz | — | 50 | — | ps |
| t6[4] | Clock Jitter | Cycle-to-cycle jitter, 1.0V LVCMOS output clock.<br>OUT1 = 32.768kHz (1.8V LVCMOS)<br>OUT2 = 72MHz<br>OUT3 = 26MHz | — | 50 | — | ps |
| t7 | Output Skew | Skew between the same frequencies, with outputs using the same driver format. | — | | 300 | ps |
| t8[5] | Lock Time | PLL lock time from power-up. | — | | 5 | ms |
| t9 | Lock Time | 32.768kHz clock low power power-up time. | — | 10 | 20 | ms |
| t9[6] | Lock Time | PLL lock time from shutdown mode. | — | 0.5 | 1 | ms |

[1] High Drive only when Crystal Frequency is higher than 30MHz.

[2] The data is measured on constant temperature.

[3] The slew rate is set by Byte19<3:2> and Byte19<1:0>.

[4] Jitter performance depend on output configuration.

[5] Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.

[6] Actual PLL lock time depends on the loop configuration.

## I²C Bus DC Characteristics

Table 15. I²C Bus DC Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | — | 0.7 × $V_{DDO}$ | — | — | V |
| $V_{IL}$ | Input Low Level | — | — | — | 0.3 × $V_{DDO}$ | V |
| $V_{HYS}$ | Hysteresis of Inputs | — | 0.05 × $V_{DDO}$ | — | — | V |
| $I_{IN}$ | Input Leakage Current | — | — | 1 | 10 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 3mA. | — | — | 0.4 | V |

Note: I2C bus is 3.3V tolerant.

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Table 16. $I^2C$ Bus AC Characteristics

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $F_{SCLK}$ | Serial Clock Frequency (SCL) | 0 | — | 400 | kHz |
| $t_{BUF}$ | Bus Free Time between STOP and START | 1.3 | — | — | µs |
| $t_{SU:START}$ | Setup Time, START | 0.6 | — | — | µs |
| $t_{HD:START}$ | Hold Time, START | 0.6 | — | — | µs |
| $t_{SU:DATA}$ | Setup Time, Data Input (SDA) | 100 | — | — | ns |
| $t_{HD:DATA}$ | Hold Time, Data Input (SDA) [1] | 0 | — | — | µs |
| $t_{OVD}$ | Output Data Valid from Clock | — | — | 0.9 | µs |
| $C_B$ | Capacitive Load for Each Bus Line | — | — | 400 | pF |
| $t_R$ | Rise Time, Data and Clock (SDA, SCL) | $20 + 0.1 \times C_B$ | — | 300 | ns |
| $t_F$ | Fall Time, Data and Clock (SDA, SCL) | $20 + 0.1 \times C_B$ | — | 300 | ns |
| $t_{HIGH}$ | High Time, Clock (SCL) | 0.6 | — | — | µs |
| $t_{LOW}$ | Low Time, Clock (SCL) | 1.3 | — | — | µs |
| $t_{SU:STOP}$ | Setup Time, STOP | 0.6 | — | — | µs |

[1] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

## Spread Spectrum Generation Specifications

Table 17. Spread Spectrum Generation Specifications (5L1503S only)

| Symbol | Parameter | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | Output frequency range. | 1 | — | 100 | MHz |
| $f_{MOD}$ | Mod Frequency | Modulation frequency. | 30 – 60 | | | kHz |
| $f_{SPREAD}$ | Spread Value | Amount of spread value (programmable)–down spread. | 0.15% – 2.0% | | | % $f_{OUT}$ |

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# General I2C Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

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Byte 0: General Control

| Byte 00h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OTP_Burned | OTP memory programming indication | R/W | OTP memory non-programmed | OTP memory programmed | 0 |
| Bit 6 | OTP TRIM | OTP memory programming indication | R/W | OTP TRIM bits non-programmed | OTP TRIM bits programmed | 0 |
| Bit 5 | I2C_addr[1] | I2C address select bit 1 | R/W | 00: D0 / 01: D2<br>10: D4 / 11: D6 | | 0 |
| Bit 4 | I2C_addr[0] | I2C address select bit 0 | R/W | | | 0 |
| Bit 3 | OTP TRIM Protect | OTP TRIM bits memory protection | R/W | read/write | write locked | 0 |
| Bit 2 | OTP Configure Select 2 | OTP Config Select Bit | R/W | Config 0 | Config 1 | 0 |
| Bit 1 | OTP Configure Select <1> | DFC Config Select Bit 1 | R/W | 00: DFC Config 0<br>01: DFC Config 1<br>10: DFC Config 2<br>11: DFC Config 3 | | 0 |
| Bit 0 | OTP Configure Select <0> | DFC Config Select Bit 0 | R/W | | | 0 |

Byte 1: Dash Code ID (optional)

| Byte 01h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | XTAL_DIV2 | XTAL Divider | R/W | Div /2 | Bypass | 0 |
| Bit 6 | DashCode ID[6] | Dash code ID | R/W | — | — | 0 |
| Bit 5 | DashCode ID[5] | Dash code ID | R/W | — | — | 0 |
| Bit 4 | DashCode ID[4] | Dash code ID | R/W | — | — | 0 |
| Bit 3 | DashCode ID[3] | Dash code ID | R/W | — | — | 0 |
| Bit 2 | DashCode ID[2] | Dash code ID | R/W | — | — | 0 |
| Bit 1 | DashCode ID[1] | Dash code ID | R/W | — | — | 0 |
| Bit 0 | DashCode ID[0] | Dash code ID | R/W | — | — | 0 |

Byte 2: Crystal Cap Setting

| Byte 02h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | Xtal_Cap[3] | Xtal cap load trimming bits | R/W | x1 x2<br>x4 x8<br>total 15pF | | 0 |
| Bit 6 | Xtal_Cap[2] | Xtal cap load trimming bits | R/W | | | 0 |
| Bit 5 | Xtal_Cap[1] | Xtal cap load trimming bits | R/W | | | 0 |
| Bit 4 | Xtal_Cap[0] | Xtal cap load trimming bits | R/W | | | 1 |
| Bit 3 | PPS Hyst Prog | PPS Hysteresis Prog Bit1 | R/W | 00: 20mV<br>01: 40mV<br>10: 60mV<br>11: 80mV | | 0 |
| Bit 2 | PPS Hyst Prog | PPS Hysteresis Prog Bit0 | R/W | | | 0 |
| Bit 1 | PPS Vbias Prog | PPS Vbias Prog Bit 1 | R/W | — | — | 0 |
| Bit 0 | PPS Vbias Prog | PPS Vbias Prog Bit 0 | R/W | — | — | 0 |

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Byte 3: OTP Protect

| Byte 03h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OTP Configure 3 Protect | — | R/W | read/write | write locked | 0 |
| Bit 6 | OTP Configure 2 Protect | — | R/W | read/write | write locked | 0 |
| Bit 5 | OTP Configure 1 Protect | — | R/W | read/write | write locked | 0 |
| Bit 4 | OTP Configure 0 Protect | — | R/W | read/write | write locked | 0 |
| Bit 3 | PPS2 Amp Prog | PPS OE2 Amplitude Prog Bit 1 | R/W | 00: 400mV<br>01: 500mV<br>10: 600mV<br>11: 700mV | | 0 |
| Bit 2 | PPS2 Amp Prog | PPS OE2 Amplitude Prog Bit 0 | R/W | | | 0 |
| Bit 1 | PPS1 Amp Prog | PPS OE1 Amplitude Prog Bit 1 | R/W | 00: 400mV<br>01: 500mV<br>10: 600mV<br>11: 700mV | | 0 |
| Bit 0 | PPS1 Amp Prog | PPS OE1 Amplitude Prog Bit 0 | R/W | | | 0 |

Byte 4: (Apply to 5L1503S)

| Byte 04h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | UltraPowerDown | Ultra Power Down | R/W | disabled | enabled | 0 |
| Bit 6 | EN DIFF CLKIN | Enable Differential Clkin on X1/X2 | R/W | disabled | enabled | 0 |
| Bit 5 | PLL HRS EN | - | R/W | normal | enable (shift 4 bits) | 0 |
| Bit 4 | PLL EN 3rd | - | R/W | disabled | enabled | 0 |
| Bit 3 | Reserved | | R/W | — | — | 0 |
| Bit 2 | PLL_FB_INT[10] | PLL feedback integer divider 10 | R/W | — | — | 0 |
| Bit 1 | PLL_FB_INT[9] | PLL feedback integer divider 9 | R/W | — | — | 0 |
| Bit 0 | PLL_FB_INT[8] | PLL feedback integer divider 8 | R/W | — | — | 0 |

Byte 4: (Apply to 5L1503/5L1503L)

| Byte 04h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | UltraPowerDown | Ultra Power Down | R/W | disabled | enabled | 0 |
| Bit 6 | EN DIFF CLKIN | Enable Differential Clkin on X1/X2 | R/W | disabled | enabled | 0 |
| Bit 5 | PLL HRS EN | — | R/W | normal | enable (shift 4 bits) | 0 |
| Bit 4 | PLL EN 3rd | — | R/W | disabled | enabled | 0 |
| Bit 3 | SEL_PREDIV | Divide by 4 | R/W | disabled | enabled | 0 |
| Bit 2 | PLL_FB_INT[10] | PLL feedback integer divider 10 | R/W | — | — | 0 |
| Bit 1 | PLL_FB_INT[9] | PLL feedback integer divider 9 | R/W | — | — | 0 |
| Bit 0 | PLL_FB_INT[8] | PLL feedback integer divider 8 | R/W | — | — | 0 |

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Byte 5: PLL Integer Feedback Divider (Apply to 5L1503S)

| Byte 05h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_FB_INT_DIV[7] | PLL feedback integer divider 7 | R/W | — | — | 0 |
| Bit 6 | PLL_FB_INT_DIV[6] | PLL feedback integer divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL_FB_INT_DIV[5] | PLL feedback integer divider 5 | R/W | — | — | 1 |
| Bit 4 | PLL_FB_INT_DIV[4] | PLL feedback integer divider 4 | R/W | — | — | 0 |
| Bit 3 | PLL_FB_INT_DIV[3] | PLL feedback integer divider 3 | R/W | — | — | 1 |
| Bit 2 | PLL_FB_INT_DIV[2] | PLL feedback integer divider 2 | R/W | — | — | 0 |
| Bit 1 | PLL_FB_INT_DIV[1] | PLL feedback integer divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL_FB_INT_DIV[0] | PLL feedback integer divider 0 | R/W | — | — | 0 |

Byte 5: PLL Integer Feedback Divider (Apply to 5L1503/5L1503L)

| Byte 05h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_FB_INT_DIV[7] | PLL feedback integer divider 7 | R/W | — | — | 0 |
| Bit 6 | PLL_FB_INT_DIV[6] | PLL feedback integer divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL_FB_INT_DIV[5] | PLL feedback integer divider 5 | R/W | — | — | 1 |
| Bit 4 | PLL_FB_INT_DIV[4] | PLL feedback integer divider 4 | R/W | — | — | 1 |
| Bit 3 | PLL_FB_INT_DIV[3] | PLL feedback integer divider 3 | R/W | — | — | 0 |
| Bit 2 | PLL_FB_INT_DIV[2] | PLL feedback integer divider 2 | R/W | — | — | 0 |
| Bit 1 | PLL_FB_INT_DIV[1] | PLL feedback integer divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL_FB_INT_DIV[0] | PLL feedback integer divider 0 | R/W | — | — | 0 |

Byte 6: PLL Fractional Feedback Divider

| Byte 06h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_FB_FRC_DIV[15] | PLL feedback fractional divider 15 | R/W | — | — | 0 |
| Bit 6 | PLL_FB_FRC_DIV[14] | PLL feedback fractional divider 14 | R/W | — | — | 0 |
| Bit 5 | PLL_FB_FRC_DIV[13] | PLL feedback fractional divider 13 | R/W | — | — | 0 |
| Bit 4 | PLL_FB_FRC_DIV[12] | PLL feedback fractional divider 12 | R/W | — | — | 0 |
| Bit 3 | PLL_FB_FRC_DIV[11] | PLL feedback fractional divider 11 | R/W | — | — | 0 |
| Bit 2 | PLL_FB_FRC_DIV[10] | PLL feedback fractional divider 10 | R/W | — | — | 0 |
| Bit 1 | PLL_FB_FRC_DIV[9] | PLL feedback fractional divider 9 | R/W | — | — | 0 |
| Bit 0 | PLL_FB_FRC_DIV[8] | PLL feedback fractional divider 8 | R/W | — | — | 0 |

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Byte 7: Fractional Feedback Divider

| Byte 07h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_FB_FRC_DIV[7] | PLL feedback fractional divider 7 | R/W | — | — | 0 |
| Bit 6 | PLL_FB_FRC_DIV[6] | PLL feedback fractional divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL_FB_FRC_DIV[5] | PLL feedback fractional divider 5 | R/W | — | — | 0 |
| Bit 4 | PLL_FB_FRC_DIV[4] | PLL feedback fractional divider 4 | R/W | — | — | 0 |
| Bit 3 | PLL_FB_FRC_DIV[3] | PLL feedback fractional divider 3 | R/W | — | — | 0 |
| Bit 2 | PLL_FB_FRC_DIV[2] | PLL feedback fractional divider 2 | R/W | — | — | 0 |
| Bit 1 | PLL_FB_FRC_DIV[1] | PLL feedback fractional divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL_FB_FRC_DIV[0] | PLL feedback fractional divider 0 | R/W | — | — | 0 |

Byte 8: PLL Spread Spectrum Control

| Byte 08h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_STEP[15] | PLL spread step size control bit 15 | R/W | — | — | 0 |
| Bit 6 | PLL_STEP[14] | PLL spread step size control bit 14 | R/W | — | — | 0 |
| Bit 5 | PLL_STEP[13] | PLL spread step size control bit 13 | R/W | — | — | 0 |
| Bit 4 | PLL_STEP[12] | PLL spread step size control bit 12 | R/W | — | — | 0 |
| Bit 3 | PLL_STEP[11] | PLL spread step size control bit 11 | R/W | — | — | 0 |
| Bit 2 | PLL_STEP[10] | PLL spread step size control bit 10 | R/W | — | — | 0 |
| Bit 1 | PLL_STEP[9] | PLL spread step size control bit 9 | R/W | — | — | 0 |
| Bit 0 | PLL_STEP[8] | PLL spread step size control bit 8 | R/W | — | — | 0 |

Byte 9: PLL Spread Spectrum Control

| Byte 09h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_STEP[7] | PLL spread step size control bit 7 | R/W | — | — | 0 |
| Bit 6 | PLL_STEP[6] | PLL spread step size control bit 6 | R/W | — | — | 0 |
| Bit 5 | PLL_STEP[5] | PLL spread step size control bit 5 | R/W | — | — | 0 |
| Bit 4 | PLL_STEP[4] | PLL spread step size control bit 4 | R/W | — | — | 0 |
| Bit 3 | PLL_STEP[3] | PLL spread step size control bit 3 | R/W | — | — | 0 |
| Bit 2 | PLL_STEP[2] | PLL spread step size control bit 2 | R/W | — | — | 0 |
| Bit 1 | PLL_STEP[1] | PLL spread step size control bit 1 | R/W | — | — | 0 |
| Bit 0 | PLL_STEP[0] | PLL spread step size control bit 0 | R/W | — | — | 0 |

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Byte 10: PLL Period Control

| Byte 0Ah | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_PERIOD[7] | PLL period control bit 7 | R/W | — | — | 0 |
| Bit 6 | PLL_PERIOD[6] | PLL period control bit 6 | R/W | — | — | 0 |
| Bit 5 | PLL_PERIOD[5] | PLL period control bit 5 | R/W | — | — | 0 |
| Bit 4 | PLL_PERIOD[4] | PLL period control bit 4 | R/W | — | — | 0 |
| Bit 3 | PLL_PERIOD[3] | PLL period control bit 3 | R/W | — | — | 0 |
| Bit 2 | PLL_PERIOD[2] | PLL period control bit 2 | R/W | — | — | 0 |
| Bit 1 | PLL_PERIOD[1] | PLL period control bit 1 | R/W | — | — | 0 |
| Bit 0 | PLL_PERIOD[0] | PLL period control bit 0 | R/W | — | — | 0 |

Byte 11: PLL M Divider Setting (Apply to 5L1503S)

| Byte 0Bh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_MDIV1 | PLL reference divider 1 | R/W | disable M DIV1 | bypadd divider (/1) | 1 |
| Bit 6 | PLL_MDIV2 | PLL reference divider 2 | R/W | disable M DIV2 | bypadd divider (/2) | 0 |
| Bit 5 | PLL_MDIV[5] | PLL reference divider control bit 5 | R/W | 3–63, default is 26 | | 0 |
| Bit 4 | PLL_MDIV[4] | PLL reference divider control bit 4 | R/W | | | 1 |
| Bit 3 | PLL_MDIV[3] | PLL reference divider control bit 3 | R/W | | | 1 |
| Bit 2 | PLL_MDIV[2] | PLL reference divider control bit 2 | R/W | | | 0 |
| Bit 1 | PLL_MDIV[1] | PLL reference divider control bit 1 | R/W | | | 1 |
| Bit 0 | PLL_MDIV[0] | PLL reference divider control bit 0 | R/W | | | 0 |

Byte 11: PLL M Divider Setting (Apply to 5L1503/5L1503L)

| Byte 0Bh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_MDIV1 | PLL reference divider 1 | R/W | disable M DIV1 | bypadd divider (/1) | 0 |
| Bit 6 | PLL_MDIV2 | PLL reference divider 2 | R/W | disable M DIV2 | bypadd divider (/2) | 0 |
| Bit 5 | PLL_MDIV[5] | PLL reference divider control bit 5 | R/W | 3–63, default is 26 | | 0 |
| Bit 4 | PLL_MDIV[4] | PLL reference divider control bit 4 | R/W | | | 1 |
| Bit 3 | PLL_MDIV[3] | PLL reference divider control bit 3 | R/W | | | 1 |
| Bit 2 | PLL_MDIV[2] | PLL reference divider control bit 2 | R/W | | | 0 |
| Bit 1 | PLL_MDIV[1] | PLL reference divider control bit 1 | R/W | | | 1 |
| Bit 0 | PLL_MDIV[0] | PLL reference divider control bit 0 | R/W | | | 0 |

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Byte 12: PLL Loop R Setting (Apply to 5L1503S)

| Byte 0Ch | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_MDIV_Doubler | PLL reference divider - doubler | R/W | disable | enable | 0 |
| Bit 6 | PLL IREF | PLL CP reference current | R/W | 1X | 2X | 1 |
| Bit 5 | PLL_SSEN | PLL spread spectrum enable | R/W | disable | enable | 0 |
| Bit 4 | PLL_R100K | PLL Loop filter resister 100kOhm | R/W | bypass | plus 100Kohm | 0 |
| Bit 3 | PLL_R50K | PLL Loop filter resister 50kOhm | R/W | bypass | plus 50Kohm | 0 |
| Bit 2 | PLL_R25K | PLL Loop filter resister 25kOhm | R/W | bypass | plus 25Kohm | 0 |
| Bit 1 | PLL_R12.5K | PLL Loop filter resister 12.5kOhm | R/W | bypass | plus 12.5Kohm | 0 |
| Bit 0 | PLL_R1K | PLL Loop filter resister 1kOhm | R/W | bypass | only 1Kohm applied | 1 |

Byte 12: PLL Loop R Setting (Apply to 5L1503/5L1503L)

| Byte 0Ch | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_MDIV_Doubler | PLL reference divider - doubler | R/W | disable | enable | 0 |
| Bit 6 | PLL IREF | PLL CP reference current | R/W | 1X | 2X | 0 |
| Bit 5 | PLL_SSEN | PLL spread spectrum enable | R/W | disable | enable | 0 |
| Bit 4 | PLL_R100K | PLL Loop filter resister 100kOhm | R/W | bypass | plus 100kOhm | 0 |
| Bit 3 | PLL_R75K | PLL Loop filter resister 75kOhm | R/W | bypass | plus 75kOhm | 0 |
| Bit 2 | PLL_R50K | PLL Loop filter resister 50kOhm | R/W | bypass | plus 50kOhm | 0 |
| Bit 1 | PLL_R25K | PLL Loop filter resister 25kOhm | R/W | bypass | plus 25kOhm | 1 |
| Bit 0 | PLL_R12.5K | PLL Loop filter resister 12.5kOhm | R/W | bypass | plus 12.5kOhm | 1 |

Byte 13: PLL Charge Pump Control (Apply to 5L1503S)

| Byte 0Dh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_CP_31X | PLL charge pump control | R/W | — | x31 | 1 |
| Bit 6 | PLL_CP_16X | PLL charge pump control | R/W | — | x16 | 0 |
| Bit 5 | PLL_CP_8X | PLL charge pump control | R/W | — | x8 | 1 |
| Bit 4 | PLL_CP_4X | PLL charge pump control | R/W | — | x4 | 1 |
| Bit 3 | PLL_CP_2X | PLL charge pump control | R/W | — | x2 | 1 |
| Bit 2 | PLL_CP_1X | PLL charge pump control | R/W | — | x1 | 0 |
| Bit 1 | PLL_CP_/24 | PLL charge pump control | R/W | — | /24 | 0 |
| Bit 0 | PLL_CP_/3 | PLL charge pump control | R/W | — | /3 | 1 |

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Byte 13: PLL Charge Pump Control (Apply to 5L1503/5L1503L)

| Byte 0Dh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL_CP_31X | PLL charge pump control | R/W | — | x31 | 0 |
| Bit 6 | PLL_CP_16X | PLL charge pump control | R/W | — | x16 | 0 |
| Bit 5 | PLL_CP_8X | PLL charge pump control | R/W | — | x8 | 0 |
| Bit 4 | PLL_CP_4X | PLL charge pump control | R/W | — | x4 | 1 |
| Bit 3 | PLL_CP_2X | PLL charge pump control | R/W | — | x2 | 0 |
| Bit 2 | PLL_CP_1X | PLL charge pump control | R/W | — | x1 | 1 |
| Bit 1 | PLL_CP_/24 | PLL charge pump control | R/W | — | /24 | 1 |
| Bit 0 | PLL_CP_/3 | PLL charge pump control | R/W | — | /3 | 0 |

Byte 14: Output Divider1 Control (Apply to 5L1503S)

| Byte 0Eh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUTDIV1[4] | Output divider1 control bit 4 | R/W | DIV1[3:2] = 1, 3, 5, 7, 9, 11; DIV1[1:0] = 1, 2, 4, 8; Default Divider = 00001 = 3 | | 0 |
| Bit 6 | OUTDIV1[3] | Output divider1 control bit 3 | R/W | | | 1 |
| Bit 5 | OUTDIV1[2] | Output divider1 control bit 2 | R/W | | | 0 |
| Bit 4 | OUTDIV1[1] | Output divider1 control bit 1 | R/W | | | 1 |
| Bit 3 | OUTDIV1[0] | Output divider1 control bit 0 | R/W | | | 0 |
| Bit 2 | OUTDIV2 Source Select | OUTDIV2 Source Select | R/W | From REF | OUTDIV2_Source | 0 |
| Bit 1 | OUTDIV1 Source Select | OUTDIV1 Source Select | R/W | From REF | From PLL | 1 |
| Bit 0 | OUTDIV1 Seed | OUTDIV1 Seed | R/W | disabled | enable seed to OUTDIV2 | 0 |

Byte 14: Output Divider1 Control (Apply to 5L1503/5L1503L)

| Byte 0Eh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUTDIV1[4] | Output divider1 control bit 4 | R/W | DIV1[3:2]=1,3,5,7,9,11; DIV1[1:0]=1,2,4,8; Default Divider = 00001=3 | | 0 |
| Bit 6 | OUTDIV1[3] | Output divider1 control bit 3 | R/W | | | 0 |
| Bit 5 | OUTDIV1[2] | Output divider1 control bit 2 | R/W | | | 0 |
| Bit 4 | OUTDIV1[1] | Output divider1 control bit 1 | R/W | | | 0 |
| Bit 3 | OUTDIV1[0] | Output divider1 control bit 0 | R/W | | | 1 |
| Bit 2 | OUTDIV2 Source Select | OUTDIV2 Source Select | R/W | From REF | OUTDIV2_Source | 0 |
| Bit 1 | OUTDIV1 Source Select | OUTDIV1 Source Select | R/W | From REF | From PLL | 1 |
| Bit 0 | OUTDIV1 Seed | OUTDIV1 Seed | R/W | disabled | enable seed to OUTDIV2 | 0 |

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Byte 15: Output Divider 2 Control

| Byte 0Fh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUTDIV2[4] | Output divider2 control bit 4 | R/W | DIV1[3:2]=1,3,5,7,9,11; DIV1[1:0]=1,2,4,8; Default Divider=00001=3 | | 0 |
| Bit 6 | OUTDIV2[3] | Output divider2 control bit 3 | R/W | | | 0 |
| Bit 5 | OUTDIV2[2] | Output divider2 control bit 2 | R/W | | | 0 |
| Bit 4 | OUTDIV2[1] | Output divider2 control bit 1 | R/W | | | 0 |
| Bit 3 | OUTDIV2[0] | Output divider2 control bit 0 | R/W | | | 1 |
| Bit 2 | OUT3_OUT_TRI | OUT3 State Select | R/W | normal | Tristate | 0 |
| Bit 1 | OUT2_OUT_TRI | OUT2 State Select | R/W | normal | Tristate | 0 |
| Bit 0 | OUT1_OUT_TRI | OUT1 State Select | R/W | normal | Tristate | 0 |

Byte 16: PLL Operation Control Register

| Byte 10h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUT1_EN | OUT1 output enable control | R/W | disable | enable | 1 |
| Bit 6 | OE1_fun_sel[1] | OE1 pin function selection bit 1 | R/W | 11: DFC0 10: OUT1_PPS 01: PD# 00: OUT1 OE | | 0 |
| Bit 5 | OE1_fun_sel[0] | OE1 pin function selection bit 0 | R/W | | | 0 |
| Bit 4 | OUT2_EN | OUT2 output enable control | R/W | disable | enable | 1 |
| Bit 3 | OE2_fun_sel[1] | OE2 pin function selection bit 1 | R/W | 11: DFC1 10: OUT2_PPS 01: Config_SEL 00: OUT2 OE | | 0 |
| Bit 2 | OE2_fun_sel[0] | OE2 pin function selection bit 0 | R/W | | | 0 |
| Bit 1 | OUT2 Freerun | OUT2 Freerun enable control | R/W | Freerun | normal | 1 |
| Bit 0 | OUT1 Freerun | OUT1 Freerun enable control | R/W | Freerun | normal | 0 |

Byte 17: OE and DFC Control

| Byte 11h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUT1 CLKSEL 1 | OUT1 output clock selection | R/W | 00: CLK32K, 01: OUTDIV2 10: NA, 11: OUTDIV1 | | 0 |
| Bit 6 | OUT1 CLKSEL 0 | OUT1 output clock selection | R/W | | | 0 |
| Bit 5 | OUT2 CLKSEL 1 | OUT2 output clock selection | R/W | 00: CLK32K, 01: OUTDIV2 10: NA, 11: OUTDIV1 | | 1 |
| Bit 4 | OUT2 CLKSEL 0 | OUT2 output clock selection | R/W | | | 1 |
| Bit 3 | OUT3 CLKSEL 1 | OUT3 output clock selection | R/W | 00: CLK32K, 01: OUTDIV2 10: REF, 11: OUTDIV1 | | 1 |
| Bit 2 | OUT3 CLKSEL 0 | OUT3 output clock selection | R/W | | | 0 |
| Bit 1 | OUT3_EN | OUT3 output enable control | R/W | disable | enable | 1 |
| Bit 0 | DFC_EN | DFC function control | R/W | disable | enable | 0 |

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Byte 18: Control Register

| Byte 12h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL PDB | PLL Powerdown enable control | R/W | Powerdown | Not powerdown | 1 |
| Bit 6 | PLL LOCKBYPASS | PLL Lock Bypass enable control | R/W | Bypass | Not Bypass | 1 |
| Bit 5 | Reserved | | R/W | — | — | 0 |
| Bit 4 | PPS PDB EN | PPS PDB enable control | R/W | disable | enable | 0 |
| Bit 3 | PPS2 Timer_sel<1> | PPS2 Timer select bit 1 | R/W | 00: 100µs 01: 200µs<br>10: 400µs 11: 800µs | | 0 |
| Bit 2 | PPS2 Timer_sel<0> | PPS2 Timer select bit 0 | R/W | | | 0 |
| Bit 1 | PPS1 Timer_sel<1> | PPS1 Timer select bit 1 | R/W | 00: 100µs 01: 200µs<br>10: 400µs 11: 800µs | | 0 |
| Bit 0 | PPS1 Timer_sel<0> | PPS1 Timer select bit 0 | R/W | | | 0 |

Byte 19: Control Register

| Byte 13h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUT1 CLK Invert | OUT1 CLK Invert control | R/W | Non-Invert | Invert | 0 |
| Bit 6 | OUT2 CLK Invert | OUT2 CLK Invert control | R/W | Non-Invert | Invert | 0 |
| Bit 5 | OUT3 CLK Invert | OUT3 CLK Invert control | R/W | Non-Invert | Invert | 0 |
| Bit 4 | OUT3 Freerun | OUT3 Freerun enable control | R/W | Freerun | normal | 1 |
| Bit 3 | OUT2 Amp OUT 1 | OUT2 Amplitude Select control | R/W | 00: 1.8V 01: 1.0V<br>10: 1.1V 11: 1.0V | | 0 |
| Bit 2 | OUT2 Amp OUT 0 | OUT2 Amplitude Select control | R/W | | | 0 |
| Bit 1 | OUT3 Amp OUT 1 | OUT3 Amplitude Select control | R/W | 00: 1.8V 01: 1.0V<br>10: 1.1V 11: 1.0V | | 0 |
| Bit 0 | OUT3 Amp OUT 0 | OUT3 Amplitude Select control | R/W | | | 0 |

Byte 20: OUT1 and DIV4 Control (Apply to 5L1503/5L1503S)

| Byte 14h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | I2C_PDB | chip power down control bit | R/W | power down | normal | 1 |
| Bit 6 | Ref_free_run | Reference clock output (OUT2/OUT3) | R/W | stop | freerun | 0 |
| Bit 5 | free_run_output_config | OUT clocks free run control | R/W | OUT2 free run | OUT2/3 free run | 0 |
| Bit 4 | PDB Invert | PDB polarity control bit | R/W | Non-Invert | Invert | 0 |
| Bit 3 | BYP_AC | Bypass AC cap in X1 (5L1503 only) | R/W | normal | Bypass | 0 |
| Bit 2 | Reserved | | R/W | — | — | 0 |
| Bit 1 | Reserved | | R/W | — | — | 1 |
| Bit 0 | Reserved | | R/W | — | — | 1 |

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Byte 20: OUT1 and DIV4 Control (Apply to 5L1503L)

| Byte 14h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | I2C_PDB | chip power down control bit | R/W | power down | normal | 1 |
| Bit 6 | Ref_free_run | Reference clock output (OUT2/OUT3) | R/W | stop | freerun | 0 |
| Bit 5 | free_run_output_config | OUT clocks free run control | R/W | OUT2 free run | OUT2/3 free run | 0 |
| Bit 4 | PDB Invert | PDB polarity control bit | R/W | Non-Invert | Invert | 0 |
| Bit 3 | BYP_AC | Bypass AC cap in X1 | R/W | normal | Bypass | 0 |
| Bit 2 | CLK32K Low Drive Amp Select<2:0> | CLK32K Low Drive Amplitude Select<2:0> | R/W | 000: 1.8V 001: 0.8V 010: 0.9V 011: 1.0V 100: 1.1V 101:1.2V | | 0 |
| Bit 1 | | | R/W | | | 1 |
| Bit 0 | | | R/W | | | 1 |

# Glossary of Features

Table 18. Glossary of Features

| Term | Function Description | Apply to |
|---|---|---|
| DFC | Dynamic Frequency Control from selected PLL to support two VCO frequencies–two different output frequencies by assigning H/W pin state changes (H-L or L-H). Needs to have frequency change glitch-free function in order to not crash application system. | All |
| ORT | Overshoot Reduction Technology–when the PLL performs VCO frequency changes by DFC, or manually programming, the VCO changes frequencies smoothly to target frequency without overshoot or undershoot. | All |
| OE | Output Enable function. High active. Each output can be controlled by assigned OE pin and the dedicated OE pin can be OTP programmable as Global Power Down function (PD#) or Output enable (OE) or proactive power saving function (PPS). | All |
| PCT | Programmable Calibration Time, for 32K DCO, the programmable calibration time will help power saving or output accuracy adjustments. | All |
| Glitch-free | The output clock should not have short pulses that will kill the application system, the output frequency switch (based on DFC) should has glitch-free function. | All |
| SS | Spread Spectrum Clock | 5L1503S |
| PPS | Proactive Power Saving. Utilizes OE pin as monitor pin for end device X2 clock status. See PPS – Proactive Power Saving Function description for details. | All |

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## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

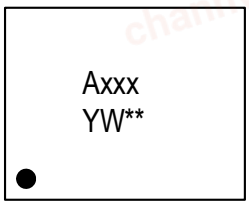
www.idt.com/document/psc/10-vfqfpn-package-outline-drawing-20-x-20-x-055-mm-body-04mm-pitch-nvg10p1

## Ordering Information

| Orderable Part Number | Package | Shipping Packaging | Temperature |
|---|---|---|---|
| 5L1503-xxxNVGI | 2.0 × 2.0 × 0.55 mm 10-VFQFPN | Tray | -40° to +85°C |
| 5L1503-xxxNVGI8 | 2.0 × 2.0 × 0.55 mm 10-VFQFPN | Reel | -40° to +85°C |
| 5L1503L-xxxNVGI | 2.0 × 2.0 × 0.55 mm 10-VFQFPN | Tray | -40° to +85°C |
| 5L1503L-xxxNVGI8 | 2.0 × 2.0 × 0.55 mm 10-VFQFPN | Reel | -40° to +85°C |
| 5L1503S-xxxNVGI | 2.0 × 2.0 × 0.55 mm 10-VFQFPN | Tray | -40° to +85°C |
| 5L1503S-xxxNVGI8 | 2.0 × 2.0 × 0.55 mm 10-VFQFPN | Reel | -40° to +85°C |

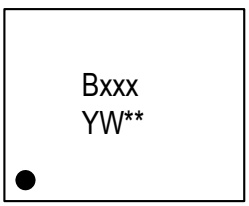
## Marking Diagrams

5L1503

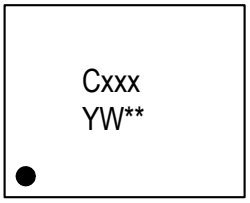



- Line 1 is the truncated part number and indicates the following:
  - “A” denotes 5L1503; “xxx” denotes dash code.
  - “B” denotes 5L1503L; “xxx” denotes dash code.
  - “C” denotes 5L1503S; “xxx” denotes dash code.
- Line 2 indicates the following:
  - “YW” is the last digit of the year and work week the part was assembled.
  - “**” denotes sequential lot number.

5L1503L




5L1503S



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# Revision History

| Revision Date | Description of Change |
|---|---|
| December 13, 2019 | Updated pinout diagram; swapped names for pins 9 and 10. |
| October 17, 2019 | Updated orderable part numbers. |
| June 19, 2019 | Initial release. |

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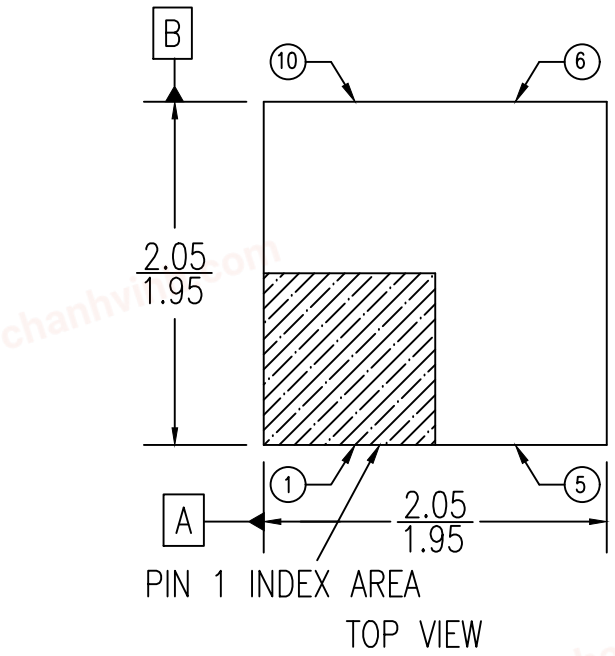
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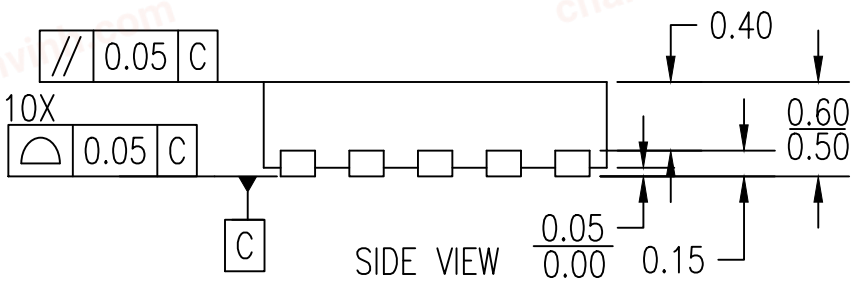
# 10-VFQFPN, Package Outline Drawing

2.0 x 2.0 x 0.55 mm Body, 0.4mm Pitch

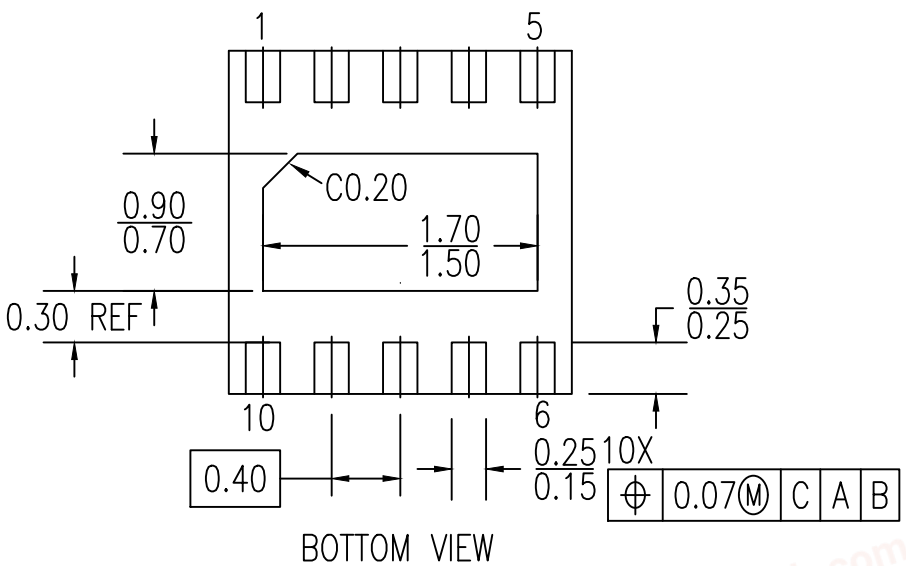





TOP VIEW




SIDE VIEW



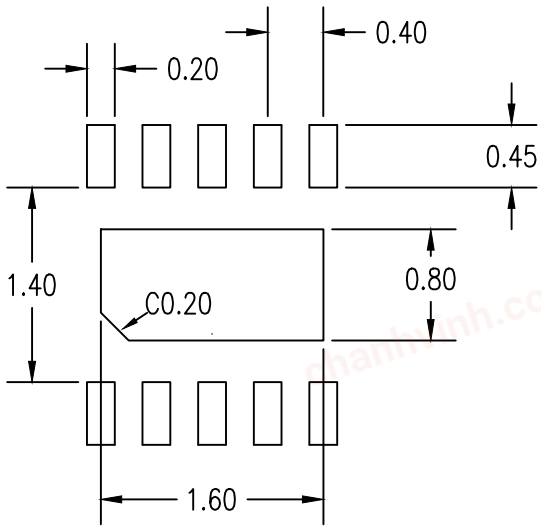

BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| June 13, 2018 | Rev 01 | Change QFN to VFQFPN |
| Dec 20, 2017 | Rev 00 | Initial Release |

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