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LOW SKEW 2 INPUT MUX AND 1 TO 8 CLOCK BUFFER ICS552-02

Description

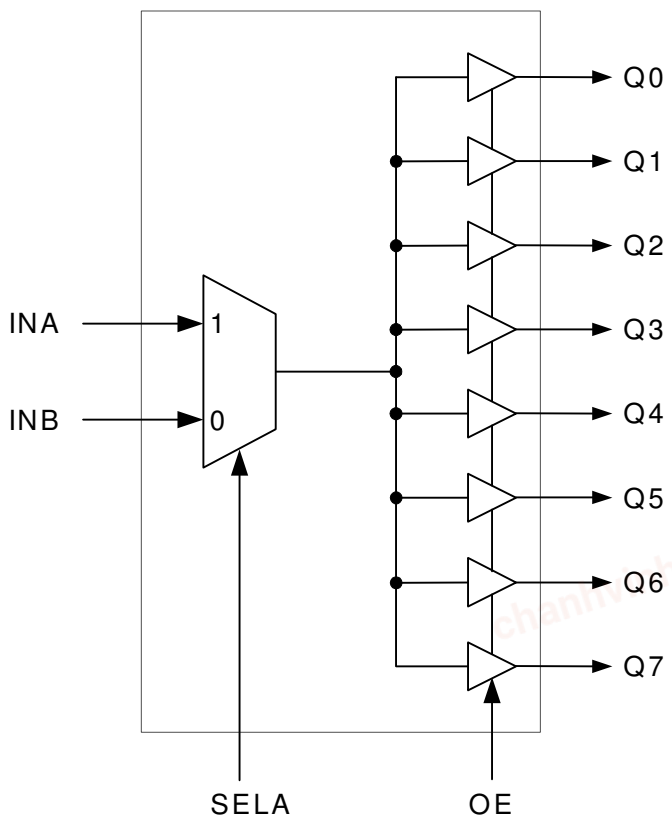
The ICS552-02 is a low skew, single-input to eight-output clock buffer. The device offers a dual input with pin select for switching between two clock sources. It is part of IDT's ClockBlocks™ family. See the ICS553 for a 1 to 4 low skew buffer. For more than 8 outputs see the MK74CBxxx Buffalo™ series of clock drivers.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

Features

- Extremely low skew outputs (50ps maximum)
- Packaged in 16 pin TSSOP
- Pb (lead) free package
- Low power CMOS technology
- Operating Voltages of 2.5 V to 5 V
- Output Enable pin tri-states outputs
- 5 V tolerant input clocks
- Input/Output clock frequency up to 200 MHz
- Input clock multiplexer simplifies clock selection
- Industrial temperature

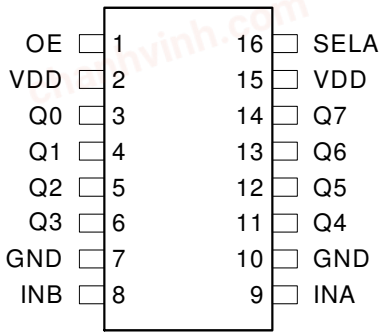
Block Diagram



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Pin Assignment



16 Pin TSSOP

Input Source Select

SELA	Input
0	INB
1	INA

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	OE	Input	Output Enable. Tri-states outputs when low. Internal pull-up resistor.
2	VDD	Power	Connect to +2.5V, +3.3V or +5.0V. Must be the same as pin 15.
3	Q0	Output	Clock Output 0
4	Q1	Output	Clock Output 1
5	Q2	Output	Clock Output 2
6	Q3	Output	Clock Output 3
7	GND	Power	Connect to ground.
8	INB	Input	Clock Input B. 5V tolerant input.
9	INA	Input	Clock Input A. 5V tolerant input.
10	GND	Power	Connect to ground.
11	Q4	Output	Clock Output 4
12	Q5	Output	Clock Output 5
13	Q6	Output	Clock Output 6
14	Q7	Output	Clock Output 7
15	VDD	Power	Connect to + 2.5V, +3.3V or +5.0V. Must be the same as pin 2.
16	SELA	Input	Selects either INA or INB. Internal pull-up resistor.

External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01 µF should be connected between VDD on pin 2 and GND on pin 7, and between VDD on pin 15 and GND on pin 10, as close to the device as possible. A 33 Ω series terminating resistor should be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skews that the ICS552-02 is capable of, careful attention must be paid to board layout. Essentially, all 8 outputs must have identical terminations, identical loads, and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15ps of skew.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS552-02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
SELA, OE, and all Outputs	-0.5 V to VDD+0.5 V
INA and INB	-0.5V to 5.5V
Ambient Operating Temperature	-40 to +85 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	175 °C
Soldering Temperature	260 °C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40	–	+85	°C
Power Supply Voltage (measured in respect to GND)	+2.375		+5.25	V

DC Electrical Characteristics

VDD=2.5 V ±5%, Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, INA, INB	V_{IH}	Note 1	VDD/2+0.5		5.5	V
Input Low Voltage, INA, INB	V_{IL}	Note 1			VDD/2-0.5	V
Input High Voltage, OE, SELA	V_{IH}		1.8		VDD	V
Input Low Voltage, OE, SELA	V_{IL}				0.7	V
Output High Voltage	V_{OH}	I_{OH} = -16 mA	2			V
Output Low Voltage	V_{OL}	I_{OL} = 16 mA			0.4	V
Operating Supply Current	IDD	No load, 135 MHz		35		mA
Short Circuit Current	I_{OS}	Each output		60		mA

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DC Electrical Characteristics (continued)

VDD=3.3 V ±5%, Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, INA, INB	V_{IH}	Note 1	VDD/2+0.7		5.5	V
Input Low Voltage, INA, INB	V_{IL}	Note 1			VDD/2-0.7	V
Input High Voltage, OE, SELA	V_{IH}		2		VDD	V
Input Low Voltage, OE, SELA	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OH} = 25 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, 135 MHz		50		mA
Short Circuit Current	I_{OS}	Each output		80		mA

VDD=5 V ±5%, Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.75		5.25	V
Input High Voltage, INA, INB	V_{IH}	Note 1	VDD/2+1		5.5	V
Input Low Voltage, INA, INB	V_{IL}	Note 1			VDD/2-1	V
Input High Voltage, OE, SELA	V_{IH}		2		VDD	V
Input Low Voltage, OE, SELA	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -35 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 35 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, 135 MHz		85		mA
Short Circuit Current	I_{OS}	Each output		100		mA

Note: 1. Nominal switching threshold is VDD/2

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AC Electrical Characteristics

VDD = 2.5V ±5%, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		1.0	1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		1.0	1.5	ns
Propagation Delay	Note 1			3.5		ns
Output to output skew	Note 2	Rising edges at VDD/2		0	50	ps
Input A to Input B skew	Note 3			0	50	ps

VDD = 3.3V ±5%, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		0.6	1.0	ns
Propagation Delay	Note 1		2.0	3.0	5.5	ns
Output to output skew	Note 2	Rising edges at VDD/2		0	50	ps
Input A to Input B skew	Note 3			0	50	ps
Part to Part Skew					3.5	ns

VDD = 5.0V ±5%, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		0.3	0.7	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		0.3	0.7	ns
Propagation Delay	Note 1			2.8		ns
Output to output skew	Note 2	Rising edges at VDD/2		0	50	ps
Input A to Input B skew	Note 3			0	50	ps

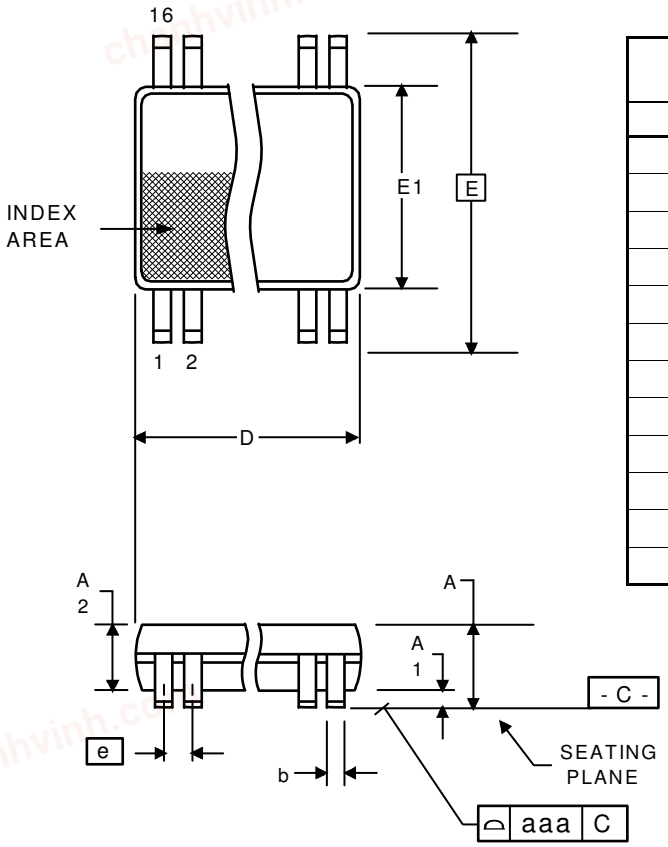
Notes: 1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.
3. Propagation delay matching through the part.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

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Package Outline and Package Dimensions (16 pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
552G-02ILN	552G02IN	Tubes	16-pin TSSOP	-40 to +85 °C
552G-02ILNT	552G02IN	Tape and Reel	16-pin TSSOP	-40 to +85 °C

"LN" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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