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To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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2SJ517

Silicon P Channel MOS FET

REJ03G0874-0400
(Previous: ADE-208-575B)
Rev.4.00
Sep 07, 2005

Description

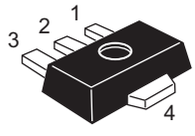
High speed power switching

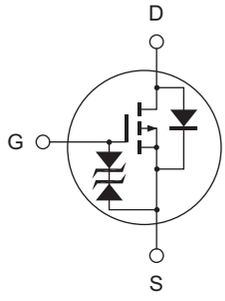
Features

- Low on-resistance
  $R_{DS\ (on)}$ = 0.18 Ω typ. (at V_{GS} = –4 V, I_D = –1 A)
- Low drive current
- High speed switching
- 2.5 V gate drive devices.

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK®)





1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is “YY”.

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Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	–2	A
Drain peak current	$I_{D\ (pulse)}$ Note 1	–4	A
Body to drain diode reverse drain current	I_{DR}	–2	A
Channel dissipation	Pch Note 2	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 100 µs, duty cycle ≤ 10%
2. When using the aluminium ceramic board (12.5 × 20 × 0.7 mm)

Electrical Characteristics

(Ta = 25°C)

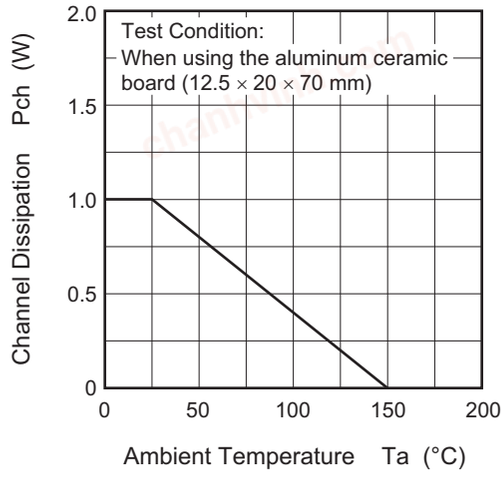
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)\ DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)\ GSS}$	±10	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –20 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±8 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS\ (off)}$	–0.5	—	–1.5	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS\ (on)}$	—	0.18	0.24	Ω	I_D = –1 A, V_{GS} = –4 V Note 3
	$R_{DS\ (on)}$	—	0.27	0.43	Ω	I_D = –1 A, V_{GS} = –2.5 V Note 3
Forward transfer admittance	$\|y_{fs}\|$	1.8	3.0	—	S	I_D = –1 A, V_{DS} = –10 V Note 3
Input capacitance	Ciss	—	320	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	190	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	90	—	pF	f = 1 MHz
Turn-on delay time	$t_{d\ (on)}$	—	14	—	ns	V_{GS} = –4 V
Rise time	t_r	—	75	—	ns	I_D = –1 A
Turn-off delay time	$t_{d\ (off)}$	—	90	—	ns	R_L = 10 Ω
Fall time	t_f	—	90	—	ns	
Body to drain diode forward voltage	V_{DF}	—	–0.95	—	V	I_F = –2 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	70	—	ns	I_F = –2 A, V_{GS} = 0 di_F/dt = 50 A/µs

Note: 3. Pulse test

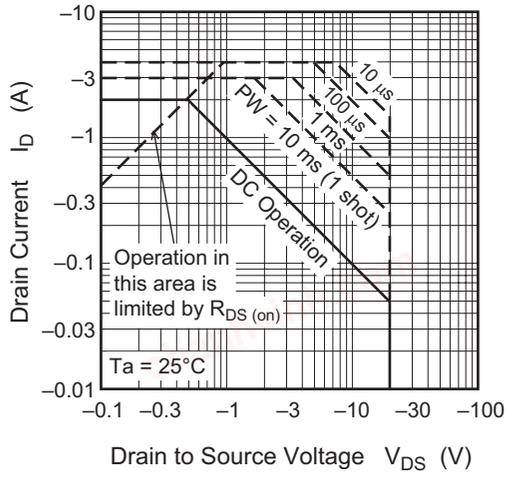
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Main Characteristics

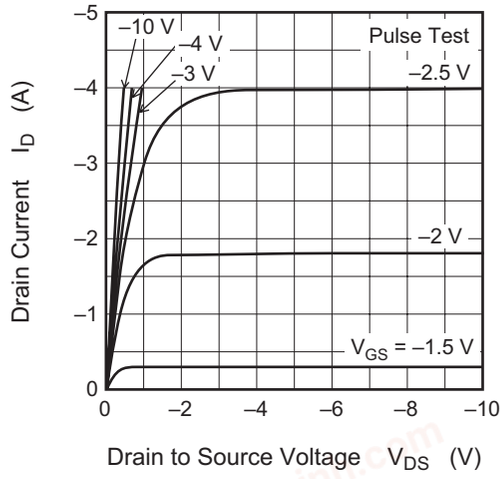
Power vs. Temperature Derating



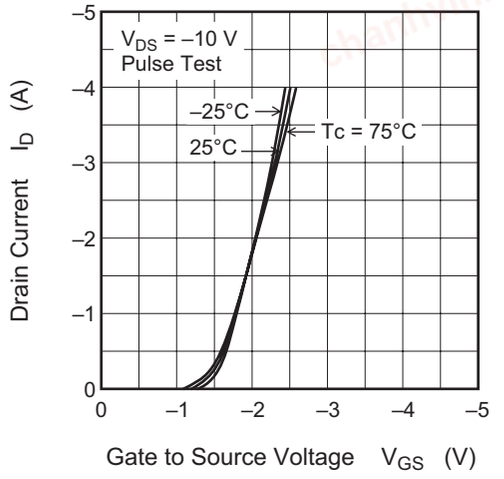
Maximum Safe Operation Area



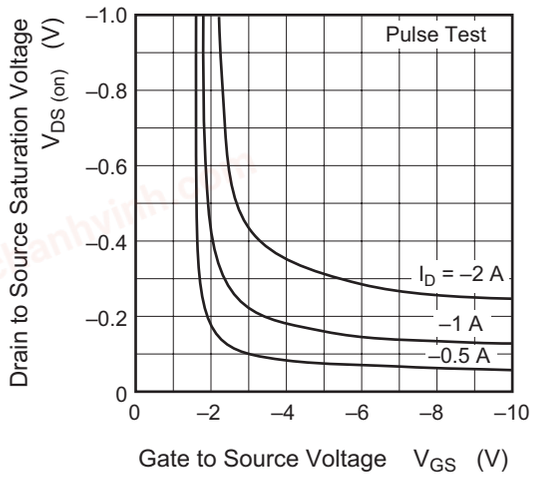
Typical Output Characteristics



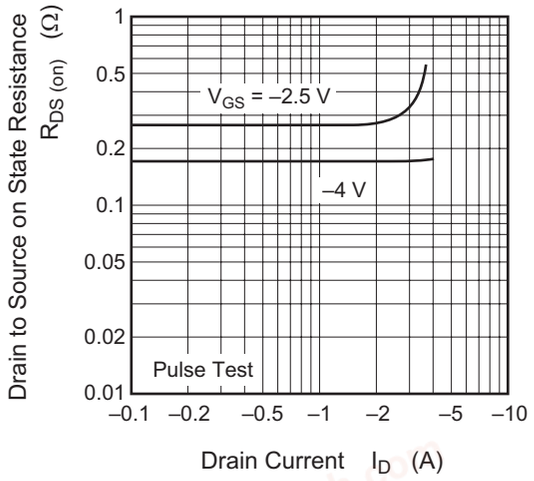
Typical Transfer Characteristics



Drain to Source Saturation Voltage vs. Gate to Source Voltage



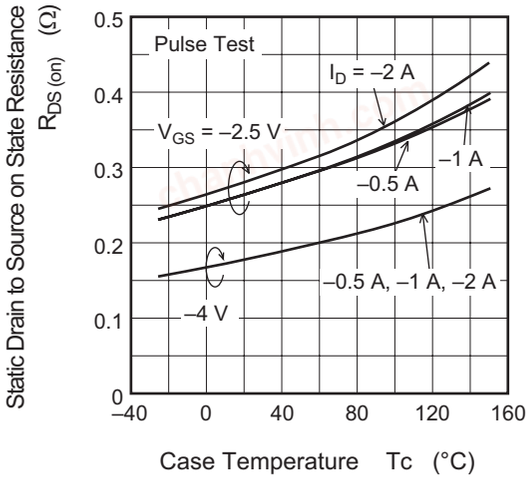
Static Drain to Source on State Resistance vs. Drain Current



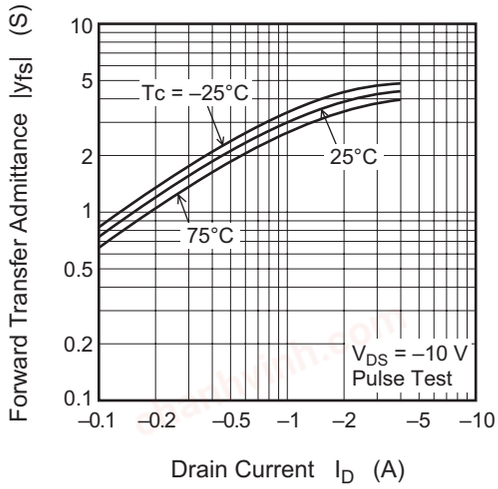
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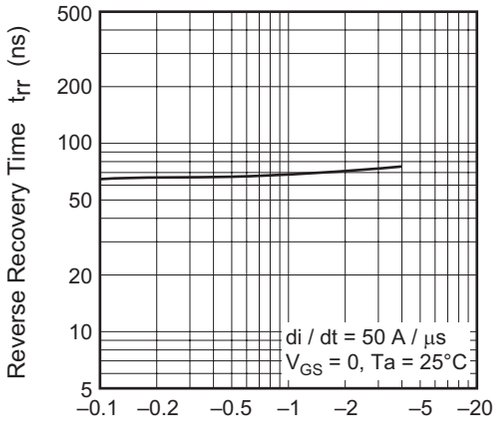
Static Drain to Source on State Resistance vs. Temperature



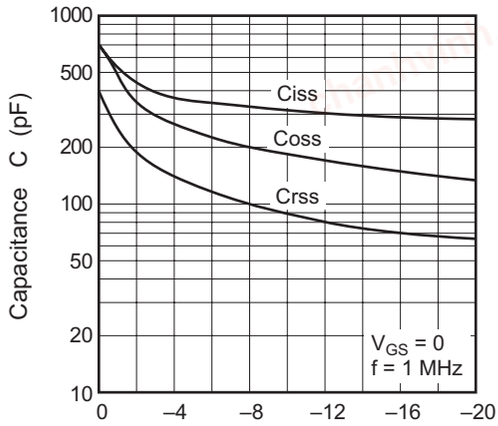
Forward Transfer Admittance vs. Drain Current



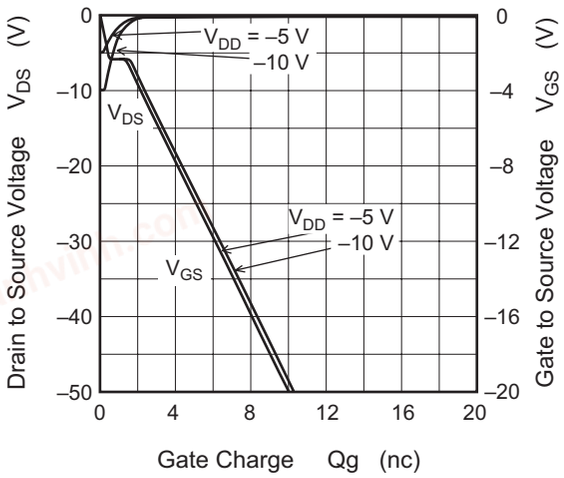
Body-Drain Diode Reverse Recovery Time



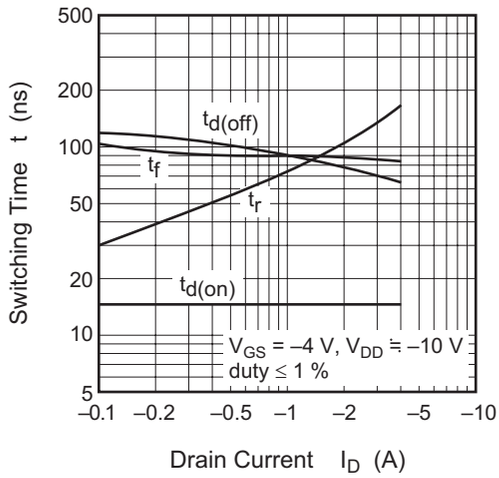
Typical Capacitance vs. Drain to Source Voltage



Dynamic Input Characteristics



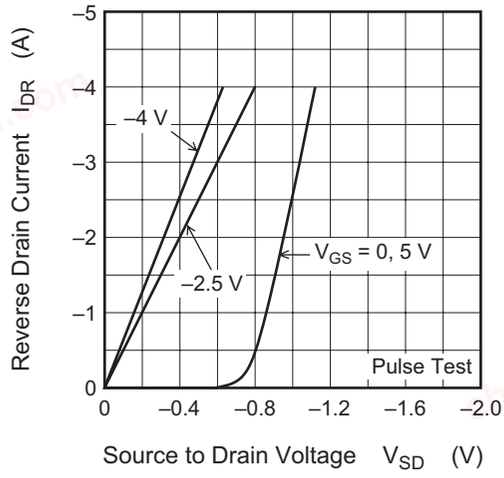
Switching Characteristics



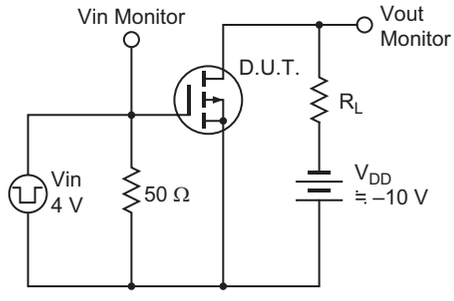
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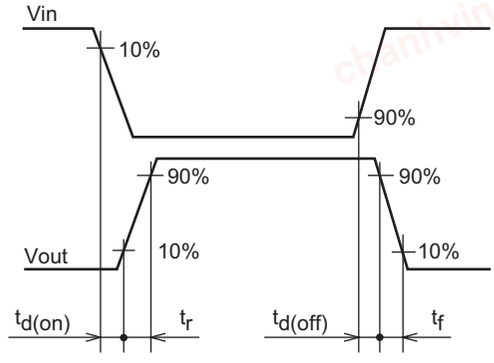
Reverse Drain Current vs.
Source to Drain Voltage



Switching Time Test Circuit



Waveform



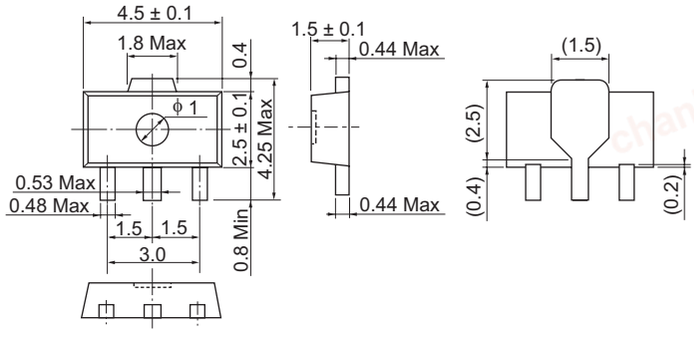
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Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
SC-62	PLZZ0004CA-A	UPAK / UPAKV	0.050g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
2SJ517YYTL-E	1000 pcs	Taping
2SJ517YYTR-E	1000 pcs	Taping

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Renesas Technology Singapore Pte. Ltd.
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Renesas Technology Korea Co., Ltd.
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Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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