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TOP252-262
TOPSwitch-HX Family

Enhanced EcoSmart, Integrated Off-Line Switcher with Advanced Feature Set and Extended Power Range

Product Highlights

Lower System Cost, Higher Design Flexibility

- Multi-mode operation maximizes efficiency at all loads
- New eSIP-7F and eSIP-7C packages
  - Low thermal impedance junction-to-case (2 °C per watt)
  - Low height is ideal for adapters where space is limited
  - Simple mounting using a clip to aid low cost manufacturing
  - Horizontal eSIP-7F package ideal for ultra low height adapter and monitor applications
  - Extended package creepage distance from DRAIN pin to adjacent pin and to heat sink
- No heat sink required up to 35 W using P, G and M packages with universal input voltage and up to 48 W at 230 VAC
- Output overvoltage protection (OVP) is user programmable for latching/non-latching shutdown with fast AC reset
  - Allows both primary and secondary sensing
- Line undervoltage (UV) detection prevents turn-off glitches
- Line overvoltage (OV) shutdown extends line surge limit
- Accurate programmable current limit
- Optimized line feed-forward for line ripple rejection
- 132 kHz frequency (254Y-258Y and all E/L packages) reduces transformer and power supply size
  - Half frequency option for video applications
- Frequency jittering reduces EMI filter cost

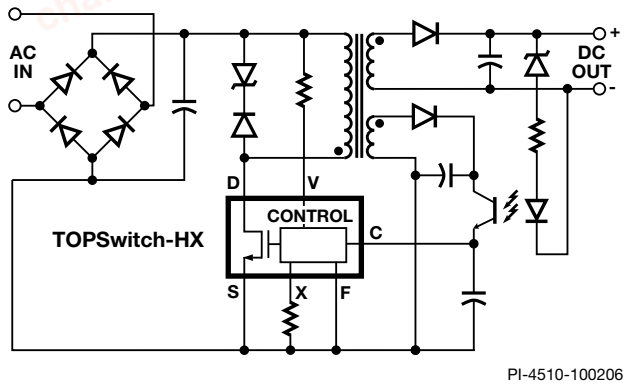


Figure 1. Typical Flyback Application.

- Heat sink is connected to SOURCE for low EMI
- Improved auto-restart delivers <3% of maximum power in short circuit and open loop fault conditions
- Accurate hysteretic thermal shutdown function automatically recovers without requiring a reset
- Fully integrated soft-start for minimum start-up stress
- Extended creepage between DRAIN and all other pins improves field reliability

Output Power Table

Product[5]	230 VAC ±15%[4]			85-265 VAC		
	Adapter[1]	Open Frame[2]	Peak[3]	Adapter[1]	Open Frame[2]	Peak[3]
TOP252PN/GN	9 W	15 W	21 W	6 W	10 W	13 W
TOP252MN			21 W			13 W
TOP253PN/GN	15 W	25 W	38 W	9 W	15 W	25 W
TOP253MN			43 W			29 W
TOP254PN/GN	16 W	28 W	47 W	11 W	20 W	30 W
TOP254MN			62 W			40 W
TOP255PN/GN	19 W	30 W	54 W	13 W	22 W	35 W
TOP255MN			81 W			52 W
TOP256PN/GN	21 W	34 W	63 W	15 W	26 W	40 W
TOP256MN			98 W			64 W
TOP257PN/GN	25 W	41 W	70 W	19 W	30 W	45 W
TOP257MN			119 W			78 W
TOP258PN/GN	29 W	48 W	77 W	22 W	35 W	50 W
TOP258MN			140 W			92 W

Product[5]	230 VAC ±15%		85-265 VAC	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
TOP252EN/EG	10 W	21 W	6 W	13 W
TOP253EN/EG	21 W	43 W	13 W	29 W
TOP254EN/YN/EG	30 W	62 W	20 W	43 W
TOP255EN/YN/EG	40 W	81 W	26 W	57 W
TOP255LN	40 W	81 W	26 W	57 W
TOP256EN/YN/EG	60 W	119 W	40 W	86 W
TOP256LN	60 W	88 W	40 W	64 W
TOP257EN/YN/EG	85 W	157 W	55 W	119 W
TOP257LN	85 W	105 W	55 W	78 W
TOP258EN/YN/EG	105 W	195 W	70 W	148 W
TOP258LN	105 W	122 W	70 W	92 W
TOP259EN/YN/EG	128 W	238 W	80 W	171 W
TOP259LN	128 W	162 W	80 W	120 W
TOP260EN/YN/EG	147 W	275 W	93 W	200 W
TOP260LN	147 W	190 W	93 W	140 W
TOP261EN/YN/EG	177 W	333 W	118 W	254 W
TOP261LN	177 W	244 W	118 W	177 W
TOP262EN[6]	177 W	333 W	118 W	254 W
TOP262LN[6]	177 W	244 W	118 W	177 W

Table 1. Output Power Table. (for notes see page 2).

This Product is Covered by Patents and/or Pending Patent Applications.

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EcoSmart™– Energy Efficient

- Energy efficient over entire load range
- No-load consumption
  - Less than 200 mW at 230 VAC
- Standby power for 1 W input
  - >600 mW output at 110 VAC input
  - >500 mW output at 265 VAC input

Description

TOPSwitch™-HX cost effectively incorporates a 700 V power MOSFET, high voltage switched current source, PWM control, oscillator, thermal shutdown circuit, fault protection and other control circuitry onto a monolithic device.

Notes for Table 1:

1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at +50 °C ambient. Use of an external heat sink will increase power capability.
2. Minimum continuous power in an open frame design at +50 °C ambient.
3. Peak power capability in any design at +50 °C ambient.
4. 230 VAC or 110/115 VAC with doubler.
5. Packages: P: DIP-8C, G: SMD-8C, M: SDIP-10C, Y: TO-220-7C, E: eSIP-7C, L: eSIP-7F. See part ordering information.
6. TOP261 and TOP262 have the same current limit set point. In some applications TOP262 may run cooler than TOP261 due to a lower $R_{DS(ON)}$ for the larger device.

Y Package Option for TOP259-261

In order to improve noise-immunity on large TOPSwitch-HX Y package parts, the F pin has been removed (TOP259-261YN are fixed at 66 kHz switching frequency) and replaced with a SIGNAL GROUND (G) pin. This pin acts as a low noise path for the C pin capacitor and the X pin resistor. It is only required for the TOP259-261YN package parts.

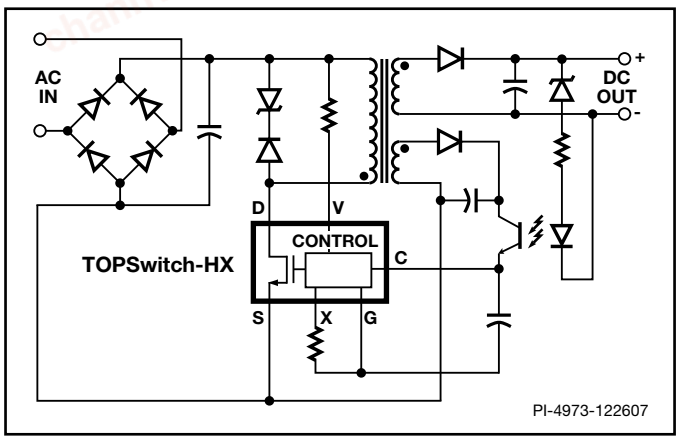


Figure 2. Typical Flyback Application TOP259YN, TOP260YN and TOP261YN.

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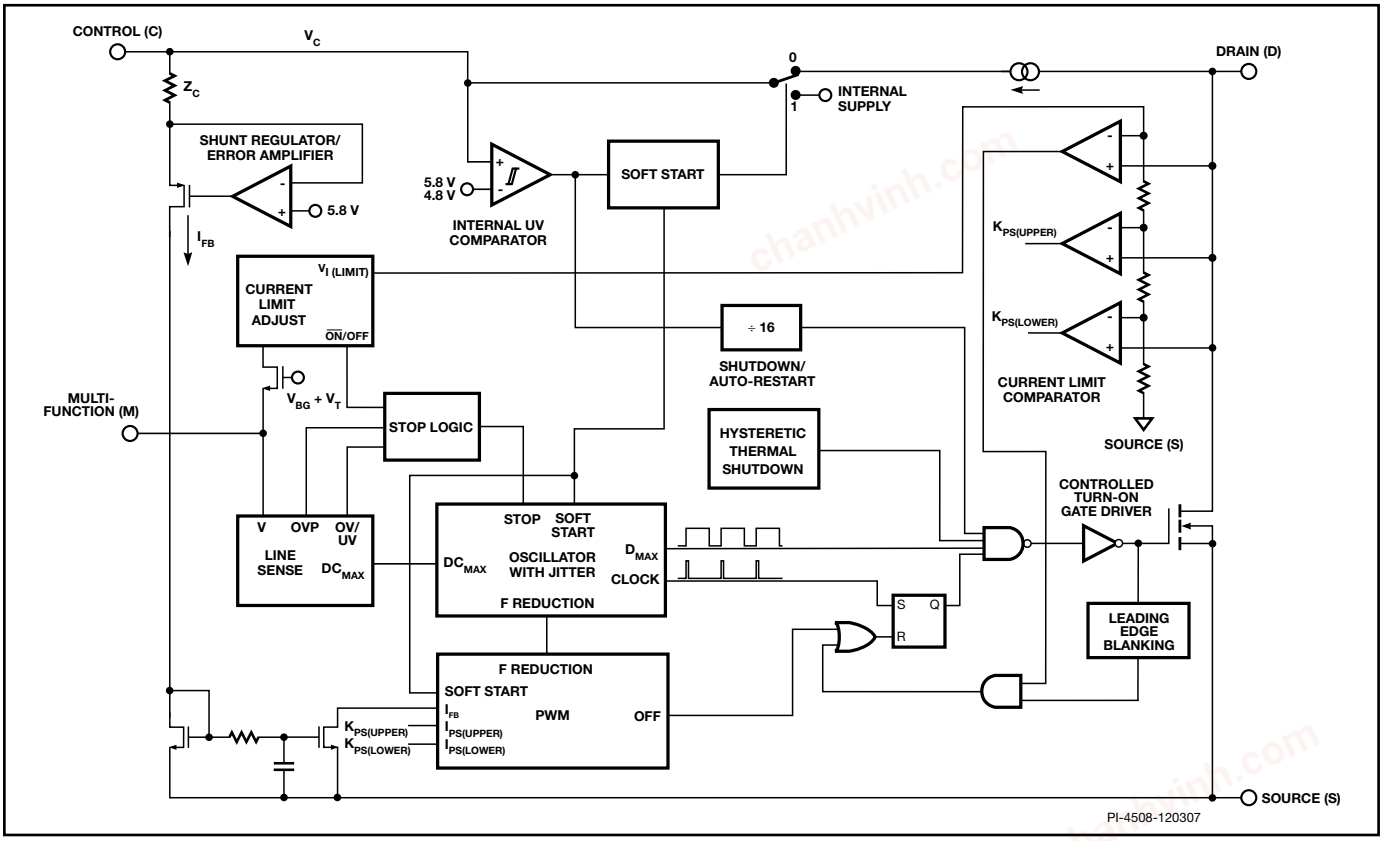


Figure 3a. Functional Block Diagram (P and G Packages).

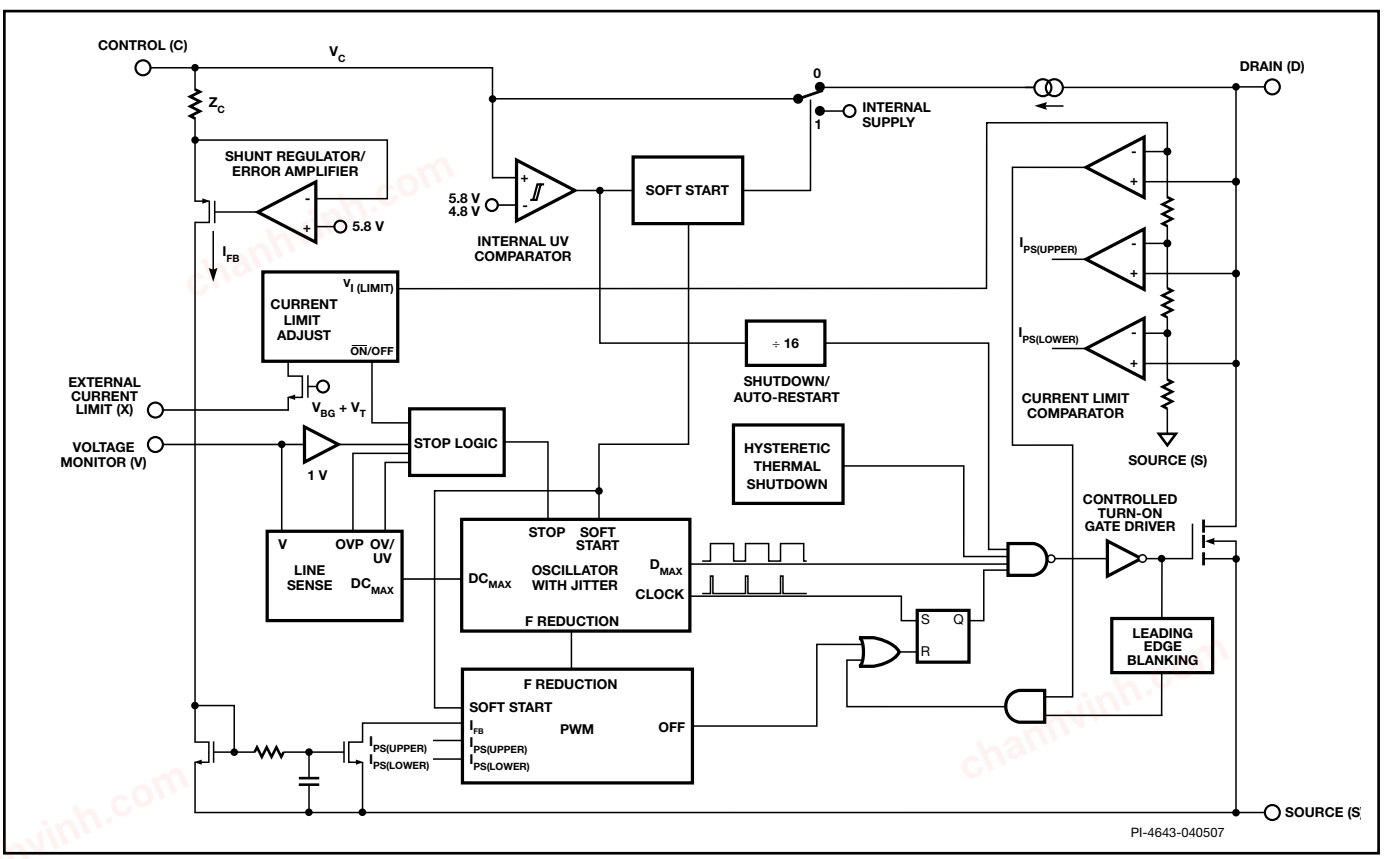


Figure 3b. Functional Block Diagram (M Package).

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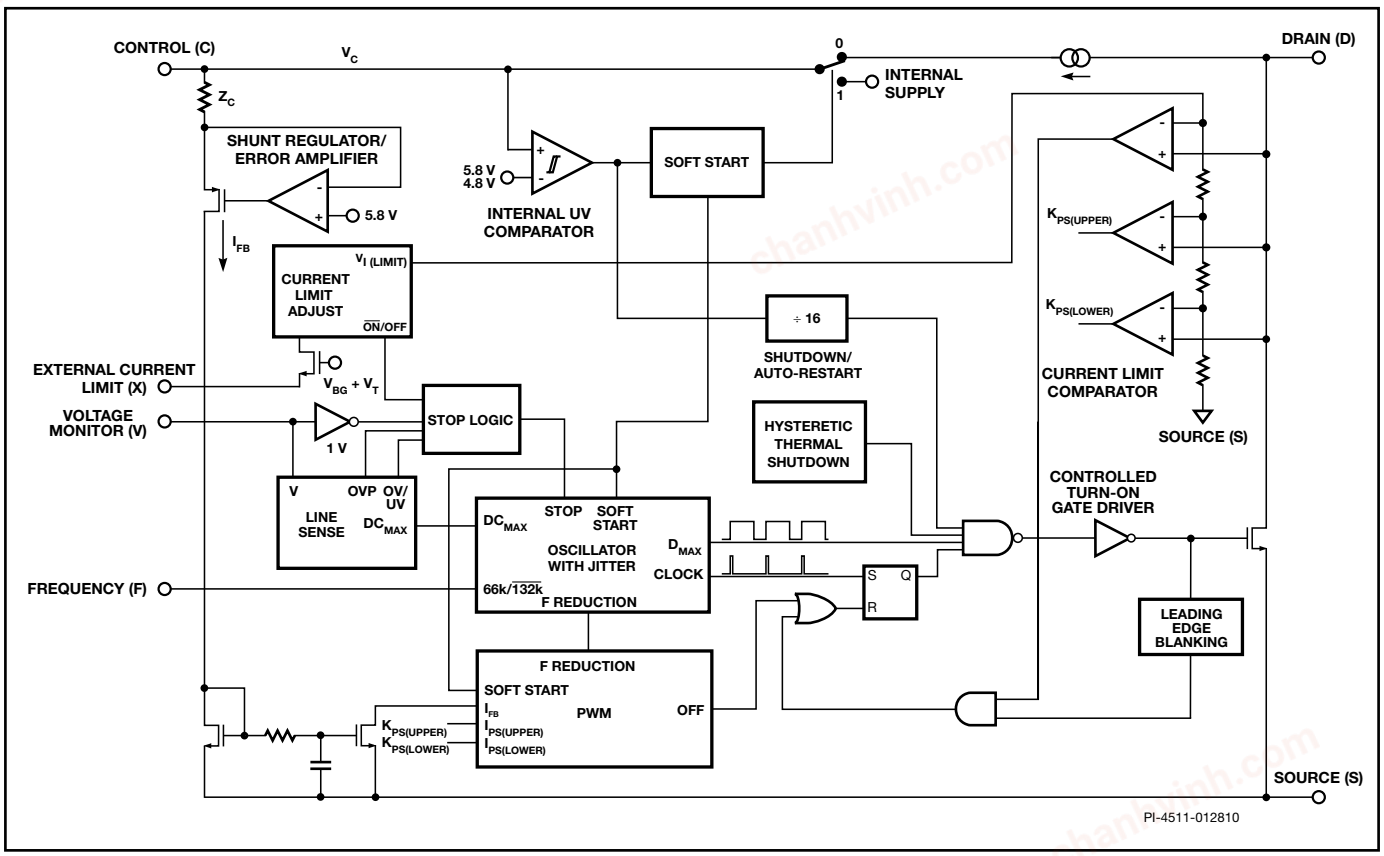


Figure 3c. Functional Block Diagram (TOP254-258 YN Package and all eSIP Packages).

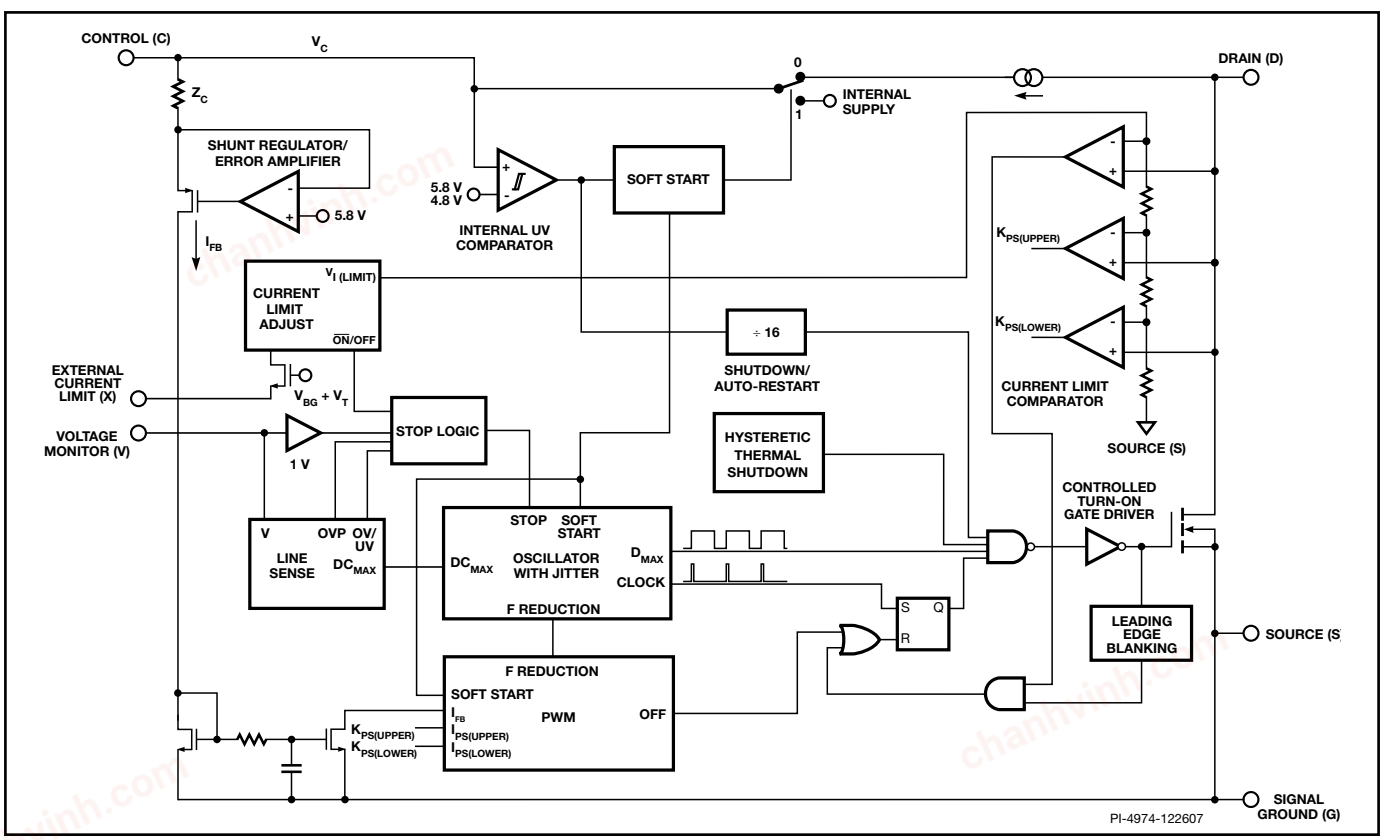


Figure 3d. Functional Block Diagram TOP259YN, TOP260YN, TOP261YN.

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Pin Functional Description

DRAIN (D) Pin:
High-voltage power MOSFET DRAIN pin. The internal start-up bias current is drawn from this pin through a switched high-voltage current source. Internal current limit sense point for drain current.

CONTROL (C) Pin:
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. It is also used as the connection point for the supply bypass and auto-restart/ compensation capacitor.

EXTERNAL CURRENT LIMIT (X) Pin (Y, M, E and L package):
Input pin for external current limit adjustment and remote ON/OFF. A connection to SOURCE pin disables all functions on this pin.

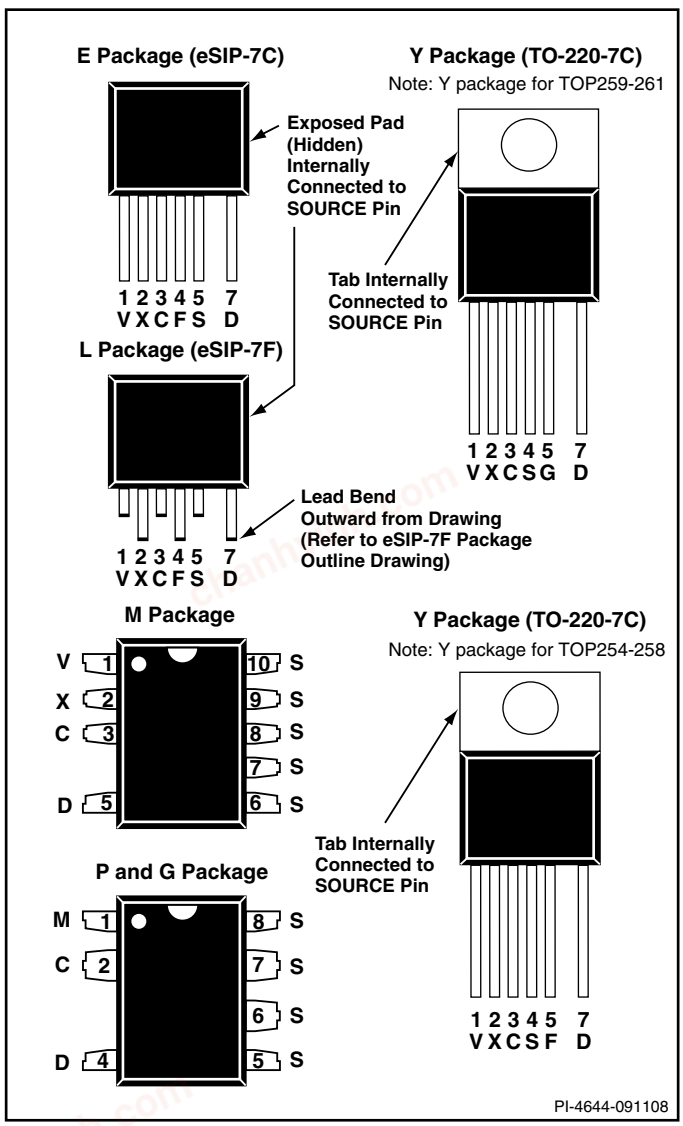


Figure 4. Pin Configuration (Top View).

VOLTAGE MONITOR (V) Pin (Y & M package only):
Input for OV, UV, line feed forward with DC_{MAX} reduction, output overvoltage protection (OVP), remote ON/OFF and device reset. A connection to the SOURCE pin disables all functions on this pin.

MULTI-FUNCTION (M) Pin (P & G packages only):
This pin combines the functions of the VOLTAGE MONITOR (V) and EXTERNAL CURRENT LIMIT (X) pins of the Y package into one pin. Input pin for OV, UV, line feed forward with DC_{MAX}

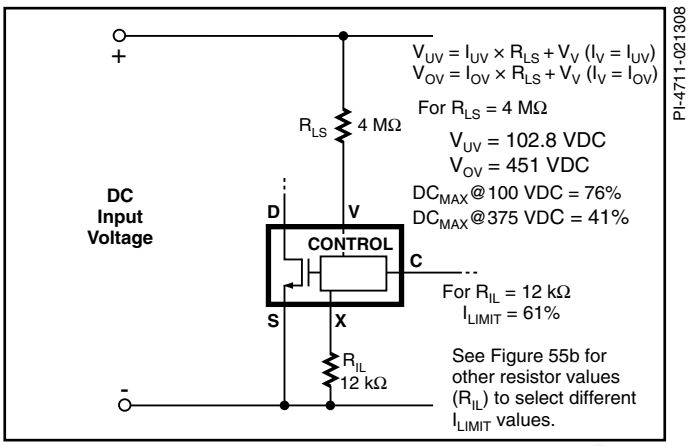


Figure 5. TOP254-258 Y and All M/E/L Package Line Sense and Externally Set Current Limit.

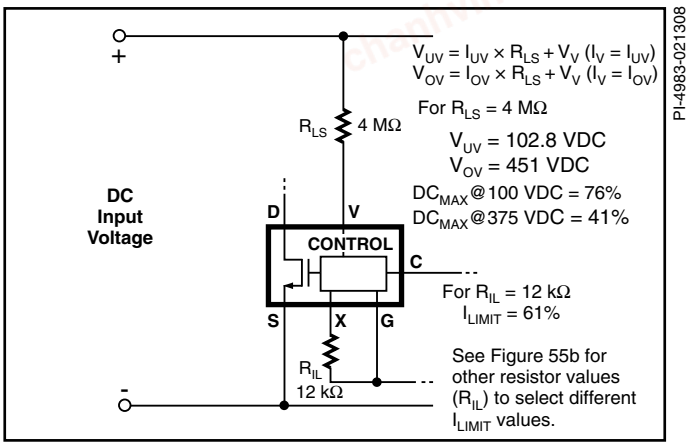


Figure 6. TOP259-261 Y Package Line Sense and External Current Limit.

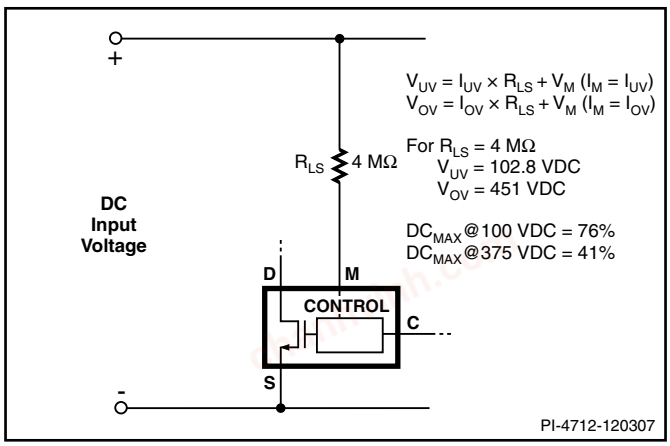


Figure 7. P/G Package Line Sense.

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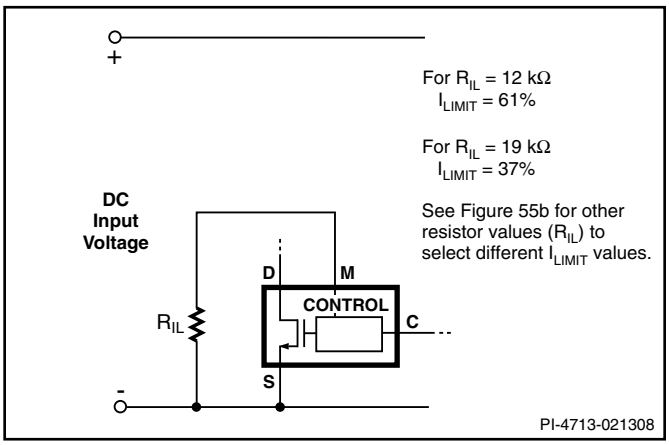


Figure 8. P/G Package Externally Set Current Limit.

reduction, output overvoltage protection (OVP), external current limit adjustment, remote ON/OFF and device reset. A connection to SOURCE pin disables all functions on this pin and makes TOPSwitch-HX operate in simple three terminal mode (like TOPSwitch-II).

FREQUENCY (F) Pin (TOP254-258Y, and all E and L packages):
Input pin for selecting switching frequency 132 kHz if connected to SOURCE pin and 66 kHz if connected to CONTROL pin. The switching frequency is internally set for fixed 66 kHz operation in the P, G, M package and TOP259YN, TOP260YN and TOP261YN.

SIGNAL GROUND (G) Pin (TOP259YN, TOP260YN & TOP261YN only):
Return for C pin capacitor and X pin resistor.

SOURCE (S) Pin:
Output MOSFET source connection for high voltage power return. Primary side control circuit common and reference point.

TOPSwitch-HX Family Functional Description

Like TOPSwitch-GX, TOPSwitch-HX is an integrated switched mode power supply chip that converts a current at the control input to a duty cycle at the open drain output of a high voltage power MOSFET. During normal operation the duty cycle of the power MOSFET decreases linearly with increasing CONTROL pin current as shown in Figure 9.

In addition to the three terminal TOPSwitch features, such as the high voltage start-up, the cycle-by-cycle current limiting, loop compensation circuitry, auto-restart and thermal shutdown, the TOPSwitch-HX incorporates many additional functions that reduce system cost, increase power supply performance and design flexibility. A patented high voltage CMOS technology allows both the high-voltage power MOSFET and all the low voltage control circuitry to be cost effectively integrated onto a single monolithic chip.

Three terminals, FREQUENCY, VOLTAGE-MONITOR, and EXTERNAL CURRENT LIMIT (available in Y and E/L packages),

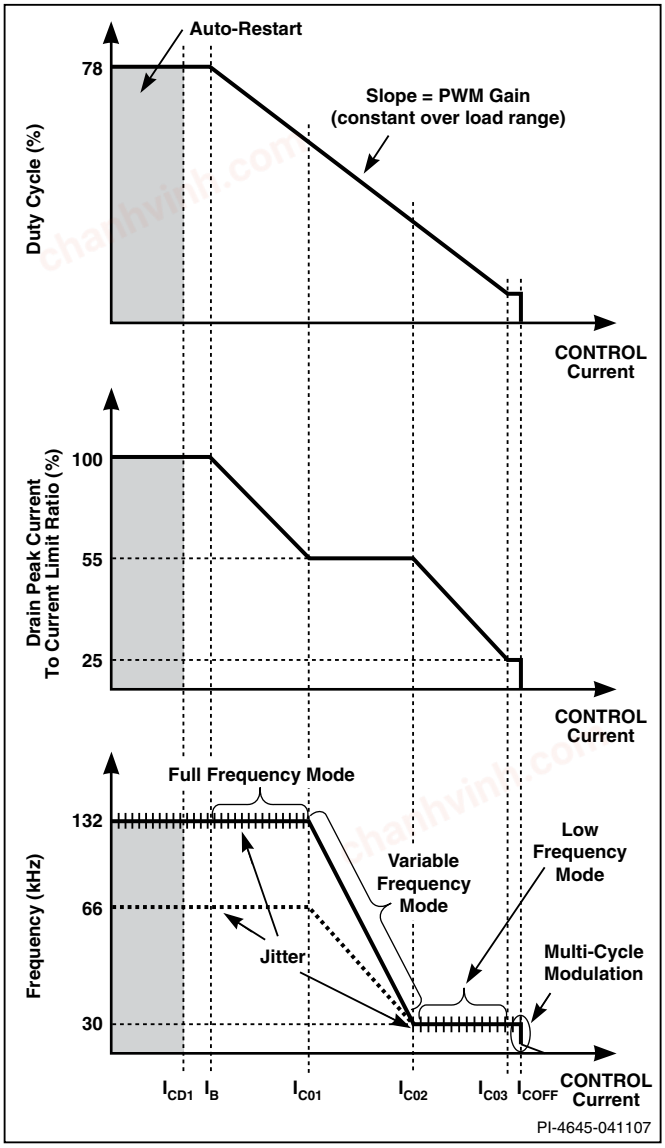


Figure 9. Control Pin Characteristics (Multi-Mode Operation).

two terminals, VOLTAGE-MONITOR and EXTERNAL CURRENT LIMIT (available in M package) or one terminal MULTI-FUNCTION (available in P and G package) have been used to implement some of the new functions. These terminals can be connected to the SOURCE pin to operate the TOPSwitch-HX in a TOPSwitch-like three terminal mode. However, even in this three terminal mode, the TOPSwitch-HX offers many transparent features that do not require any external components:

1. A fully integrated 17 ms soft-start significantly reduces or eliminates output overshoot in most applications by sweeping both current limit and frequency from low to high to limit the peak currents and voltages during start-up.
2. A maximum duty cycle (DC_{MAX}) of 78% allows smaller input storage capacitor, lower input voltage requirement and/or higher power capability.
3. Multi-mode operation optimizes and improves the power supply efficiency over the entire load range while maintaining good cross regulation in multi-output supplies.

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4. Switching frequency of 132 kHz reduces the transformer size with no noticeable impact on EMI.
5. Frequency jittering reduces EMI in the full frequency mode at high load condition.
6. Hysteretic over-temperature shutdown ensures automatic recovery from thermal fault. Large hysteresis prevents circuit board overheating.
7. Packages with omitted pins and lead forming provide large drain creepage distance.
8. Reduction of the auto-restart duty cycle and frequency to improve the protection of the power supply and load during open loop fault, short circuit, or loss of regulation.
9. Tighter tolerances on I^2f power coefficient, current limit reduction, PWM gain and thermal shutdown threshold.

The VOLTAGE-MONITOR (V) pin is usually used for line sensing by connecting a 4 MΩ resistor from this pin to the rectified DC high voltage bus to implement line overvoltage (OV), under-voltage (UV) and dual-slope line feed-forward with DC_{MAX} reduction. In this mode, the value of the resistor determines the OV/UV thresholds and the DC_{MAX} is reduced linearly with a dual slope to improve line ripple rejection. In addition, it also provides another threshold to implement the latched and hysteretic output overvoltage protection (OVP). The pin can also be used as a remote ON/OFF using the I_{UV} threshold.

The EXTERNAL CURRENT LIMIT (X) pin can be used to reduce the current limit externally to a value close to the operating peak current, by connecting the pin to SOURCE through a resistor. This pin can also be used as a remote ON/OFF input.

For the P and G package the VOLTAGE-MONITOR and EXTERNAL CURRENT LIMIT pin functions are combined on one MULTI-FUNCTION (M) pin. However, some of the functions become mutually exclusive.

The FREQUENCY (F) pin in the TOP254-258 Y and E/L packages set the switching frequency in the full frequency PWM mode to the default value of 132 kHz when connected to SOURCE pin. A half frequency option of 66 kHz can be chosen by connecting this pin to the CONTROL pin instead. Leaving this pin open is not recommended. In the P, G and M packages and the TOP259-261 Y packages, the frequency is set internally at 66 kHz in the full frequency PWM mode.

CONTROL (C) Pin Operation

The CONTROL pin is a low impedance node that is capable of receiving a combined supply and feedback current. During normal operation, a shunt regulator is used to separate the feedback signal from the supply current. CONTROL pin voltage V_C is the supply voltage for the control circuitry including the MOSFET gate driver. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the instantaneous gate drive current. The total amount of capacitance connected to this pin also sets the auto-restart timing as well as control loop compensation. When rectified DC high voltage is applied to the DRAIN pin during start-up, the MOSFET is initially off, and the CONTROL pin capacitor is charged through a switched high voltage current source connected internally between the DRAIN and CONTROL pins. When the CONTROL pin voltage V_C reaches approximately 5.8 V, the control circuitry is activated and the soft-start begins. The soft-start circuit gradually increases the drain peak current and switching frequency from a low starting value to the maximum drain peak current at the full frequency over approximately 17 ms. If no external feedback/supply current is fed into the CONTROL pin by the end of the soft-start, the high voltage current source is turned off and the CONTROL pin will start discharging in response to the supply current drawn by the control circuitry. If the power supply is designed properly, and no fault condition such as open loop or shorted output exists, the feedback loop will close, providing external CONTROL pin current, before the CONTROL pin voltage has had a chance to discharge to the lower threshold voltage of approximately 4.8 V (internal supply undervoltage lockout threshold). When the externally fed current charges the CONTROL pin to the shunt regulator voltage of 5.8 V, current in excess of the consumption of the chip is shunted to SOURCE through an NMOS current mirror as shown in Figure 3. The output current of that NMOS current mirror controls the duty cycle of the power MOSFET to provide closed loop regulation. The shunt regulator has a finite low output impedance Z_C that sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance Z_C of the CONTROL pin together with the external CONTROL pin capacitance sets the dominant pole for the control loop.

When a fault condition such as an open loop or shorted output prevents the flow of an external current into the CONTROL pin, the capacitor on the CONTROL pin discharges towards 4.8 V. At 4.8 V, auto-restart is activated, which turns the output MOSFET off and puts the control circuitry in a low current standby mode. The high-voltage current source turns on and charges the external capacitance again. A hysteretic internal supply undervoltage comparator keeps V_C within a window of typically 4.8 V to 5.8 V by turning the high-voltage current source on and off as shown in Figure 11. The auto-restart circuit has a divide-by-sixteen counter, which prevents the output MOSFET from turning on again until sixteen discharge/charge cycles have elapsed. This is accomplished by enabling the output MOSFET only when the divide-by-sixteen counter reaches the full count (S15). The counter effectively limits TOPSwitch-HX power dissipation by reducing the auto-restart duty cycle to typically 2%. Auto-restart mode continues until output voltage regulation is again achieved through closure of the feedback loop.

Oscillator and Switching Frequency

The internal oscillator linearly charges and discharges an internal capacitance between two voltage levels to create a triangular waveform for the timing of the pulse width modulator. This oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle.

The nominal full switching frequency of 132 kHz was chosen to minimize transformer size while keeping the fundamental EMI frequency below 150 kHz. The FREQUENCY pin (available only in TOP254-258 Y and E, L packages), when shorted to the CONTROL pin, lowers the full switching frequency to 66 kHz

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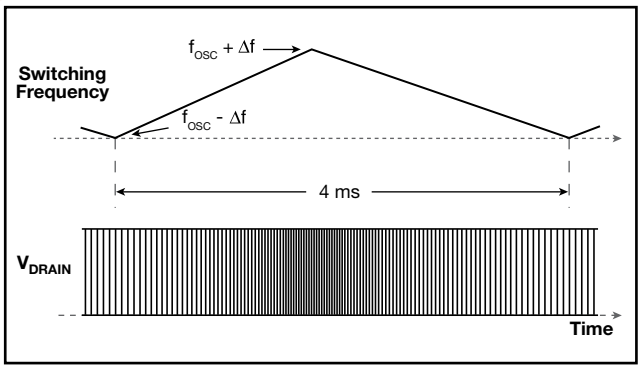


Figure 10. Switching Frequency Jitter (Idealized V_{DRAIN} Waveforms).

(half frequency), which may be preferable in some cases such as noise sensitive video applications or a high efficiency standby mode. Otherwise, the FREQUENCY pin should be connected to the SOURCE pin for the default 132 kHz. In the M, P and G packages and the TOP259-261 Y package option, the full frequency PWM mode is set at 66 kHz, for higher efficiency and increased output power in all applications.

To further reduce the EMI level, the switching frequency in the full frequency PWM mode is jittered (frequency modulated) by approximately ±2.5 kHz for 66 kHz operation or ±5 kHz for 132 kHz operation at a 250 Hz (typical) rate as shown in Figure 10. The jitter is turned off gradually as the system is entering the variable frequency mode with a fixed peak drain current.

Pulse Width Modulator

The pulse width modulator implements multi-mode control by driving the output MOSFET with a duty cycle inversely proportional to the current into the CONTROL pin that is in excess of the internal supply current of the chip (see Figure 9). The feedback error signal, in the form of the excess current, is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise in the chip supply current generated by the MOSFET gate driver.

To optimize power supply efficiency, four different control modes are implemented. At maximum load, the modulator operates in full frequency PWM mode; as load decreases, the modulator automatically transitions, first to variable frequency PWM mode, then to low frequency PWM mode. At light load, the control operation switches from PWM control to multi-cycle-modulation control, and the modulator operates in multi-cycle-modulation mode. Although different modes operate differently to make transitions between modes smooth, the simple relationship between duty cycle and excess CONTROL pin current shown in Figure 9 is maintained through all three PWM modes. Please see the following sections for the details of the operation of each mode and the transitions between modes.

Full Frequency PWM mode: The PWM modulator enters full frequency PWM mode when the CONTROL pin current (I_C) reaches I_B. In this mode, the average switching frequency is kept constant at f_{OSC} (66 kHz for P, G and M packages and TOP259-261 Y, pin selectable 132 kHz or 66 kHz for Y and E/L packages). Duty cycle is reduced from DC_{MAX} through the reduction of the on-time when I_C is increased beyond I_B. This operation is identical to the PWM control of all other TOPSwitch families. TOPSwitch-HX only operates in this mode if the cycle-by-cycle peak drain current stays above $k_{PS(UPPER)}$*I_{LIMIT}(set), where $k_{PS(UPPER)}$ is 55% (typical) and I_{LIMIT}(set) is the current limit externally set via the X or M pin.

Variable Frequency PWM mode: When peak drain current is lowered to $k_{PS(UPPER)}$* I_{LIMIT}(set) as a result of power supply load reduction, the PWM modulator initiates the transition to variable frequency PWM mode, and gradually turns off frequency jitter. In this mode, peak drain current is held constant at $k_{PS(UPPER)}$* I_{LIMIT}(set) while switching frequency drops from the initial full frequency of f_{OSC} (132 kHz or 66 kHz) towards the minimum frequency of $f_{MCM(MIN)}$ (30 kHz typical). Duty cycle reduction is accomplished by extending the off-time.

Low Frequency PWM mode: When switching frequency reaches $f_{MCM(MIN)}$ (30 kHz typical), the PWM modulator starts to transition to low frequency mode. In this mode, switching frequency is held constant at $f_{MCM(MIN)}$ and duty cycle is reduced, similar to the full frequency PWM mode, through the reduction of the on-time. Peak drain current decreases from the initial value of $k_{PS(UPPER)}$* I_{LIMIT}(set) towards the minimum value of $k_{PS(LOWER)}$*I_{LIMIT}(set), where $k_{PS(LOWER)}$ is 25% (typical) and I_{LIMIT}(set) is the current limit externally set via the X or M pin.

Multi-Cycle-Modulation mode: When peak drain current is lowered to $k_{PS(LOWER)}$*I_{LIMIT}(set), the modulator transitions to multi-cycle-modulation mode. In this mode, at each turn-on, the modulator enables output switching for a period of $T_{MCM(MIN)}$ at the switching frequency of $f_{MCM(MIN)}$ (4 or 5 consecutive pulses at 30 kHz) with the peak drain current of $k_{PS(LOWER)}$*I_{LIMIT}(set), and stays off until the CONTROL pin current falls below $I_{C(OFF)}$. This mode of operation not only keeps peak drain current low but also minimizes harmonic frequencies between 6 kHz and 30 kHz. By avoiding transformer resonant frequency this way, all potential transformer audible noises are greatly suppressed.

Maximum Duty Cycle

The maximum duty cycle, DC_{MAX}, is set at a default maximum value of 78% (typical). However, by connecting the VOLTAGE-MONITOR or MULTI-FUNCTION pin (depending on the package) to the rectified DC high voltage bus through a resistor with appropriate value (4 MΩ typical), the maximum duty cycle can be made to decrease from 78% to 40% (typical) when input line voltage increases from 88 V to 380 V, with dual gain slopes.

Error Amplifier

The shunt regulator can also perform the function of an error amplifier in primary side feedback applications. The shunt regulator voltage is accurately derived from a temperature-compensated bandgap reference. The CONTROL pin dynamic impedance Z_C sets the gain of the error amplifier. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and becomes the feedback current I_{fb} for the pulse width modulator.

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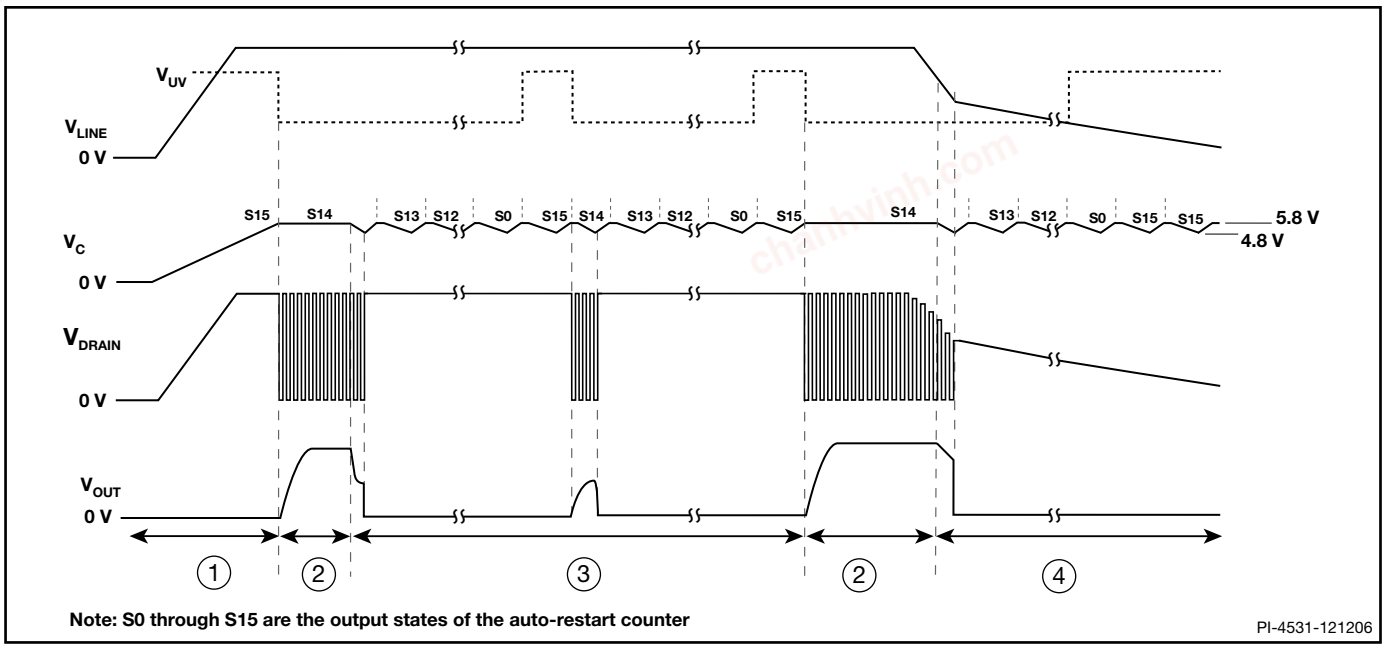


Figure 11. Typical Waveforms for (1) Power Up (2) Normal Operation (3) Auto-Restart (4) Power Down.

On-Chip Current Limit with External Programmability

The cycle-by-cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET on-state drain to source voltage $V_{DS(ON)}$ with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize the variation of the current limit due to temperature related changes in $R_{DS(ON)}$ of the output MOSFET. The default current limit of TOPSwitch-HX is preset internally. However, with a resistor connected between EXTERNAL CURRENT LIMIT (X) pin (Y, E/L and M packages) or MULTI-FUNCTION (M) pin (P and G package) and SOURCE pin (for TOP259-261 Y, the X pin is connected to the SIGNAL GROUND (G) pin), current limit can be programmed externally to a lower level between 30% and 100% of the default current limit. By setting current limit low, a larger TOPSwitch-HX than necessary for the power required can be used to take advantage of the lower $R_{DS(ON)}$ for higher efficiency/smaller heat sinking requirements. TOPSwitch-HX current limit reduction initial tolerance through the X pin (or M pin) has been improved significantly compare with previous TOPSwitch-GX. With a second resistor connected between the EXTERNAL CURRENT LIMIT (X) pin (Y, E/L and M packages) or MULTI-FUNCTION (M) pin (P and G package) and the rectified DC high voltage bus, the current limit is reduced with increasing line voltage, allowing a true power limiting operation against line variation to be implemented. When using an RCD clamp, this power limiting technique reduces maximum clamp voltage at high line. This allows for higher reflected voltage designs as well as reducing clamp dissipation.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that, if a power supply is designed properly, current spikes caused by primary-side capacitances and secondary-side rectifier reverse recovery time should not cause premature termination of the switching pulse.

The current limit is lower for a short period after the leading edge blanking time. This is due to dynamic characteristics of the MOSFET. During startup and fault conditions the controller prevents excessive drain currents by reducing the switching frequency.

Line Undervoltage Detection (UV)

At power up, UV keeps TOPSwitch-HX off until the input line voltage reaches the undervoltage threshold. At power down, UV prevents auto-restart attempts after the output goes out of regulation. This eliminates power down glitches caused by slow discharge of the large input storage capacitor present in applications such as standby supplies. A single resistor connected from the VOLTAGE-MONITOR pin (Y, E/L and M packages) or MULTI-FUNCTION pin (P and G packages) to the rectified DC high voltage bus sets UV threshold during power up. Once the power supply is successfully turned on, the UV threshold is lowered to 44% of the initial UV threshold to allow extended input voltage operating range (UV low threshold). If the UV low threshold is reached during operation without the power supply losing regulation, the device will turn off and stay off until UV (high threshold) has been reached again. If the power supply loses regulation before reaching the UV low threshold, the device will enter auto-restart. At the end of each auto-restart cycle (S15), the UV comparator is enabled. If the UV high threshold is not exceeded, the MOSFET will be disabled during the next cycle (see Figure 11). The UV feature can be disabled independent of the OV feature.

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Line Overvoltage Shutdown (OV)

The same resistor used for UV also sets an overvoltage threshold, which, once exceeded, will force TOPSwitch-HX to stop switching instantaneously (after completion of the current switching cycle). If this condition lasts for at least 100 µs, the TOPSwitch-HX output will be forced into off state. Unlike with TOPSwitch-GX, however, when the line voltage is back to normal with a small amount of hysteresis provided on the OV threshold to prevent noise triggering, the state machine sets to S13 and forces TOPSwitch-HX to go through the entire auto-restart sequence before attempting to switch again. The ratio of OV and UV thresholds is preset at 4.5, as can be seen in Figure 12. When the MOSFET is off, the rectified DC high voltage surge capability is increased to the voltage rating of the MOSFET (700 V), due to the absence of the reflected voltage and leakage spikes on the drain. The OV feature can be disabled independent of the UV feature.

In order to reduce the no-load input power of TOPSwitch-HX designs, the V-pin (or M-pin for P Package) operates at very low currents. This requires careful layout considerations when designing the PCB to avoid noise coupling. Traces and components connected to the V-pin should not be adjacent to any traces carrying switching currents. These include the drain, clamp network, bias winding return or power traces from other converters. If the line sensing features are used, then the sense resistors must be placed within 10 mm of the V-pin to minimize the V-pin node area. The DC bus should then be routed to the line sense resistors. Note that external capacitance must not be connected to the V-pin as this may cause misoperation of the V pin related functions.

Hysteretic or Latching Output Overvoltage Protection (OVP)

The detection of the hysteretic or latching output overvoltage protection (OVP) is through the trigger of the line overvoltage threshold. The V-pin or M-pin voltage will drop by 0.5 V, and the controller measures the external attached impedance immediately after this voltage drops. If I_V or I_M exceeds $I_{OV(LS)}$ (336 µA typical) longer than 100 µs, TOPSwitch-HX will latch into a permanent off state for the latching OVP. It only can be reset if V_V or V_M goes below 1 V or V_C goes below the power-up-reset threshold ($V_{C(RESET)}$) and then back to normal.

If I_V or I_M does not exceed $I_{OV(LS)}$ or exceeds no longer than 100 µs, TOPSwitch-HX will initiate the line overvoltage and the hysteretic OVP. Their behavior will be identical to the line overvoltage shutdown (OV) that has been described in detail in the previous section.

Voltage Monitor and External Current Limit Pin Table*

Figure Number	16	17	18	19	20	21	22	23	24	25	26	27	28
Three Terminal Operation	✓												
Line Undervoltage		✓	✓	✓	✓						✓	✓	
Line Overvoltage		✓	✓	✓		✓					✓	✓	
Line Feed-Forward (DC_{MAX})		✓	✓	✓							✓	✓	
Output Overvoltage Protection			✓	✓									
Overload Power Limiting								✓					
External Current Limit							✓	✓		✓	✓	✓	
Remote ON/OFF									✓	✓	✓		
Device Reset													✓

*This table is only a partial list of many VOLTAGE MONITOR and EXTERNAL CURRENT LIMIT Pin Configurations that are possible.

Table 2. VOLTAGE MONITOR (V) Pin and EXTERNAL CURRENT LIMIT (X) Pin Configuration Options.

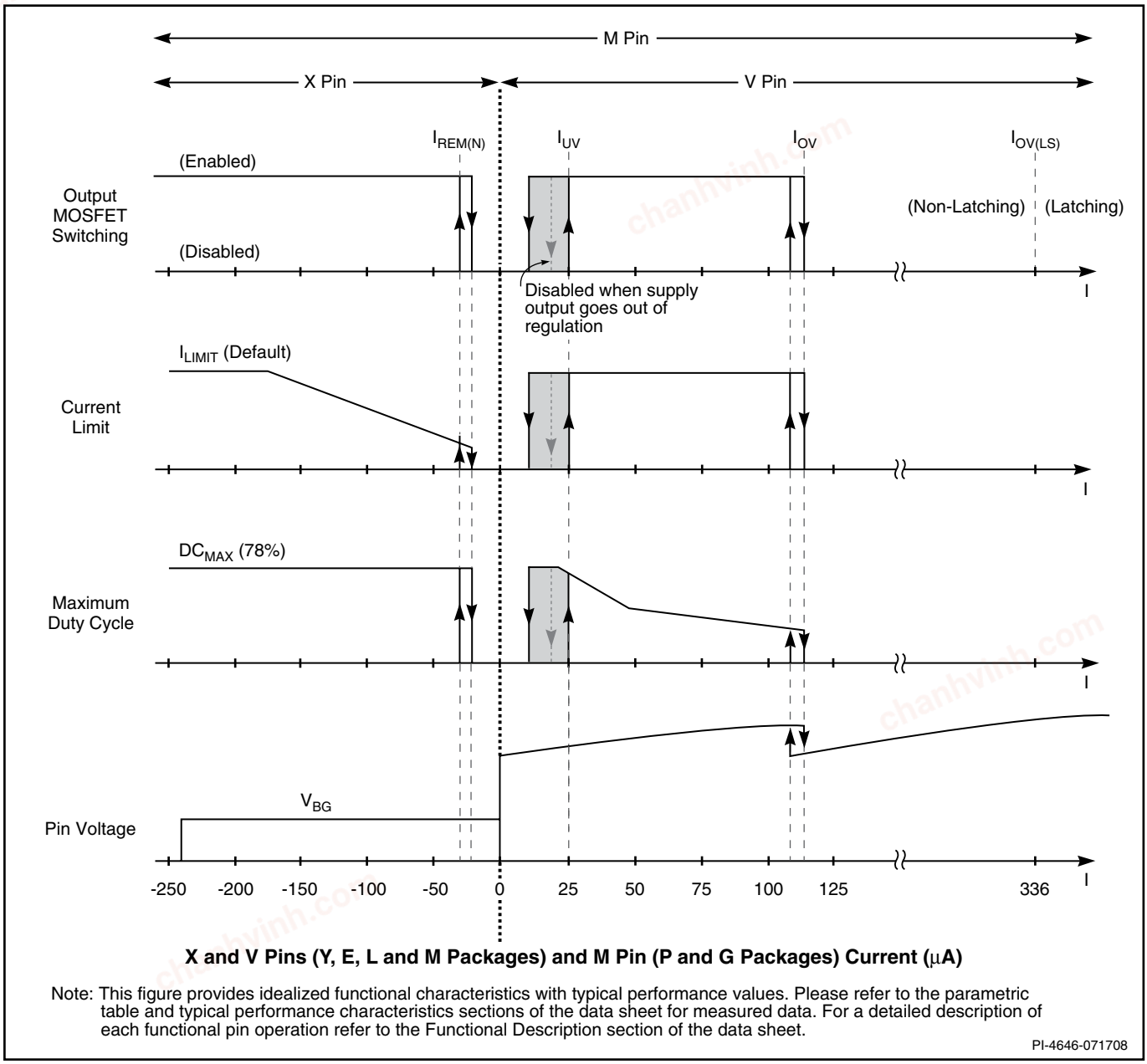
Multi-Function Pin Table*

Figure Number	29	30	31	32	33	34	35	36	37	38	39	40
Three Terminal Operation	✓											
Line Undervoltage		✓	✓	✓	✓							
Line Overvoltage		✓	✓	✓		✓						
Line Feed-Forward (DC_{MAX})		✓	✓	✓								
Output Overvoltage Protection			✓	✓								
Overload Power Limiting								✓				
External Current Limit							✓	✓		✓	✓	
Remote ON/OFF									✓	✓	✓	
Device Reset												✓

*This table is only a partial list of many MULTI-FUNCTIONAL Pin Configurations that are possible.

Table 3. MULTI-FUNCTION (M) Pin Configuration Options.

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X and V Pins (Y, E, L and M Packages) and M Pin (P and G Packages) Current (µA)

Note: This figure provides idealized functional characteristics with typical performance values. Please refer to the parametric table and typical performance characteristics sections of the data sheet for measured data. For a detailed description of each functional pin operation refer to the Functional Description section of the data sheet.

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Figure 12. MULTI-FUNCTION (P and G package). VOLTAGE MONITOR and EXTERNAL CURRENT LIMIT (Y, E/L and M package) Pin Characteristics.

The circuit examples shown in Figures 41, 42 and 43 show a simple method for implementing the primary sensed over-voltage protection.

During a fault condition resulting from loss of feedback, output voltage will rapidly rise above the nominal voltage. The increase in output voltage will also result in an increase in the voltage at the output of the bias winding. A voltage at the output of the bias winding that exceeds of the sum of the voltage rating of the Zener diode connected from the bias winding output to the V-pin (or M-pin) and V-pin (or M-pin) voltage, will cause a current in excess of I_V or I_M to be injected into the V-pin (or M-pin), which will trigger the OVP feature.

The primary sensed OVP protection circuit shown in Figures 41, 42 and 43 is triggered by a significant rise in output voltage (and therefore bias winding voltage). If the power supply is operating under heavy load or low input line conditions when an open loop occurs, the output voltage may not rise significantly. Under these conditions, a latching shutdown will not occur until load or line conditions change. Nevertheless, the operation provides the desired protection by preventing significant rise in the output voltage when the line or load conditions do change. Primary side OVP protection with the TOPSwitch-HX in a typical application will prevent a nominal 12 V output from rising above approximately 20 V under open loop conditions. If greater accuracy is required, a secondary sensed OVP circuit is recommended.

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Line Feed-Forward with DC_{MAX} Reduction

The same resistor used for UV and OV also implements line voltage feed-forward, which minimizes output line ripple and reduces power supply output sensitivity to line transients. Note that for the same CONTROL pin current, higher line voltage results in smaller operating duty cycle. As an added feature, the maximum duty cycle DC_{MAX} is also reduced from 78% (typical) at a voltage slightly lower than the UV threshold to 36% (typical) at the OV threshold. DC_{MAX} of 36% at high line was chosen to ensure that the power capability of the TOPSwitch-HX is not restricted by this feature under normal operation. TOPSwitch-HX provides a better fit to the ideal feed-forward by using two reduction slopes: -1% per μA for all bus voltage less than 195 V (typical for 4 MΩ line impedance) and -0.25% per μA for all bus voltage more than 195 V. This dual slope line feed-forward improves the line ripple rejection significantly compared with the TOPSwitch-GX.

Remote ON/OFF

TOPSwitch-HX can be turned on or off by controlling the current into the VOLTAGE-MONITOR pin or out from the EXTERNAL CURRENT LIMIT pin (Y, E/L and M packages) and into or out from the MULTI-FUNCTION pin (P and G package, see Figure 12). In addition, the VOLTAGE-MONITOR pin has a 1 V threshold comparator connected at its input. This voltage threshold can also be used to perform remote ON/OFF control.

When a signal is received at the VOLTAGE-MONITOR pin or the EXTERNAL CURRENT LIMIT pin (Y, E/L and M packages) or the MULTI-FUNCTION pin (P and G package) to disable the output through any of the pin functions such as OV, UV and remote ON/OFF, TOPSwitch-HX always completes its current switching cycle before the output is forced off.

As seen above, the remote ON/OFF feature can also be used as a standby or power switch to turn off the TOPSwitch-HX and keep it in a very low power consumption state for indefinitely long periods. If the TOPSwitch-HX is held in remote off state for long enough time to allow the CONTROL pin to discharge to the internal supply undervoltage threshold of 4.8 V (approximately 32 ms for a 47 μF CONTROL pin capacitance), the CONTROL pin goes into the hysteretic mode of regulation. In this mode, the CONTROL pin goes through alternate charge and discharge cycles between 4.8 V and 5.8 V (see CONTROL pin operation section above) and runs entirely off the high voltage DC input, but with very low power consumption (160 mW typical at 230 VAC with M or X pins open). When the TOPSwitch-HX is remotely turned on after entering this mode, it will initiate a normal start-up sequence with soft-start the next time the CONTROL pin reaches 5.8 V. In the worst case, the delay from remote on to start-up can be equal to the full discharge/charge cycle time of the CONTROL pin, which is approximately 125 ms for a 47 μF CONTROL pin capacitor. This reduced consumption remote off mode can eliminate expensive and unreliable in-line mechanical switches. It also allows for microprocessor controlled turn-on and turn-off sequences that may be required in certain applications such as inkjet and laser printers.

Soft-Start

The 17 ms soft-start sweeps the peak drain current and switching frequency linearly from minimum to maximum value by operating through the low frequency PWM mode and the variable frequency mode before entering the full frequency mode. In addition to start-up, soft-start is also activated at each restart attempt during auto-restart and when restarting after being in hysteretic regulation of CONTROL pin voltage (V_C), due to remote OFF or thermal shutdown conditions. This effectively minimizes current and voltage stresses on the output MOSFET, the clamp circuit and the output rectifier during start-up. This feature also helps minimize output overshoot and prevents saturation of the transformer during start-up.

Shutdown/Auto-Restart

To minimize TOPSwitch-HX power dissipation under fault conditions, the shutdown/auto-restart circuit turns the power supply on and off at an auto-restart duty cycle of typically 2% if an out of regulation condition persists. Loss of regulation interrupts the external current into the CONTROL pin. V_C regulation changes from shunt mode to the hysteretic auto-restart mode as described in CONTROL pin operation section. When the fault condition is removed, the power supply output becomes regulated, V_C regulation returns to shunt mode, and normal operation of the power supply resumes.

Hysteretic Over-Temperature Protection

Temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (142 °C typical). When the junction temperature cools to below the lower hysteretic temperature point, normal operation resumes, thus providing automatic recovery. A large hysteresis of 75 °C (typical) is provided to prevent overheating of the PC board due to a continuous fault condition. V_C is regulated in hysteretic mode, and a 4.8 V to 5.8 V (typical) triangular waveform is present on the CONTROL pin while in thermal shutdown.

Bandgap Reference

All critical TOPSwitch-HX internal voltages are derived from a temperature-compensated bandgap reference. This voltage reference is used to generate all other internal current references, which are trimmed to accurately set the switching frequency, MOSFET gate drive current, current limit, and the line OV/UV/OVP thresholds. TOPSwitch-HX has improved circuitry to maintain all of the above critical parameters within very tight absolute and temperature tolerances.

High-Voltage Bias Current Source

This high-voltage current source biases TOPSwitch-HX from the DRAIN pin and charges the CONTROL pin external capacitance during start-up or hysteretic operation. Hysteretic operation occurs during auto-restart, remote OFF and over-temperature shutdown. In this mode of operation, the current source is switched on and off, with an effective duty cycle of approximately 35%. This duty cycle is determined by the ratio of CONTROL pin charge (I_C) and discharge currents (I_{CD1} and I_{CD2}). This current source is turned off during normal operation when the output MOSFET is switching. The effect of the current source switching will be seen on the DRAIN voltage waveform as small disturbances and is normal.

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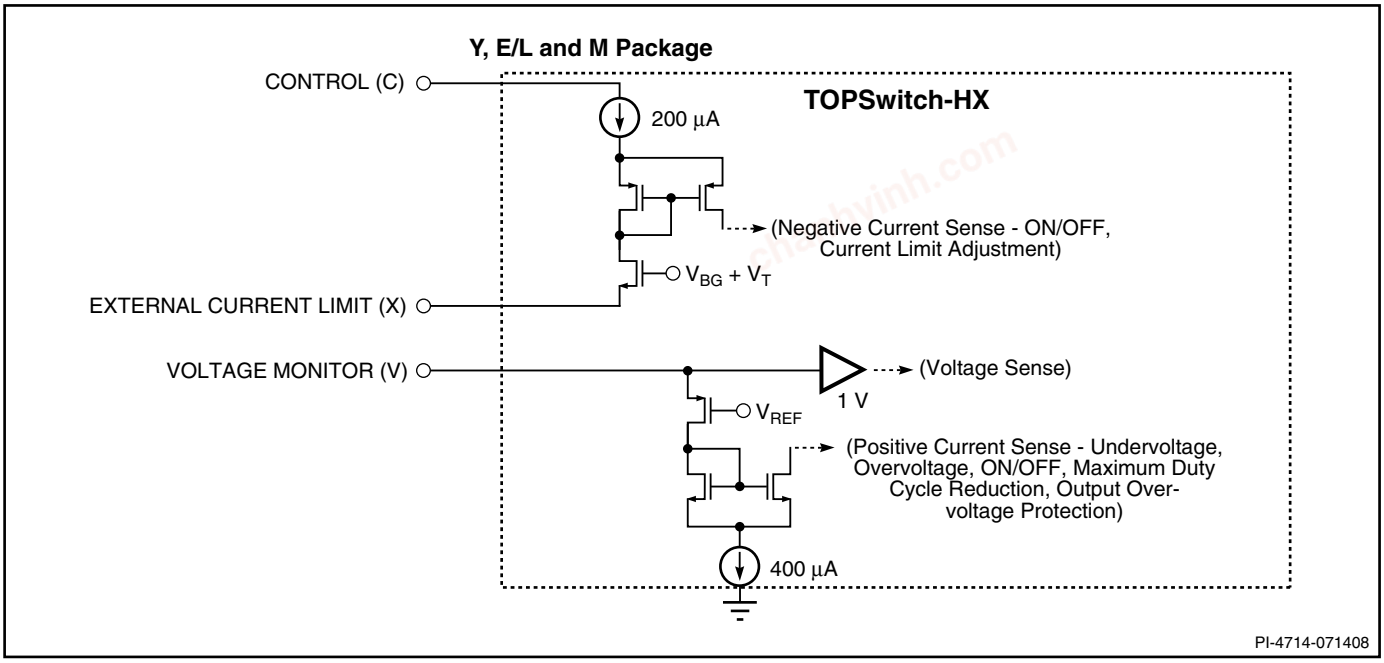


Figure 13a. VOLTAGE MONITOR (V) and EXTERNAL CURRENT LIMIT (X) Pin Input Simplified Schematic.

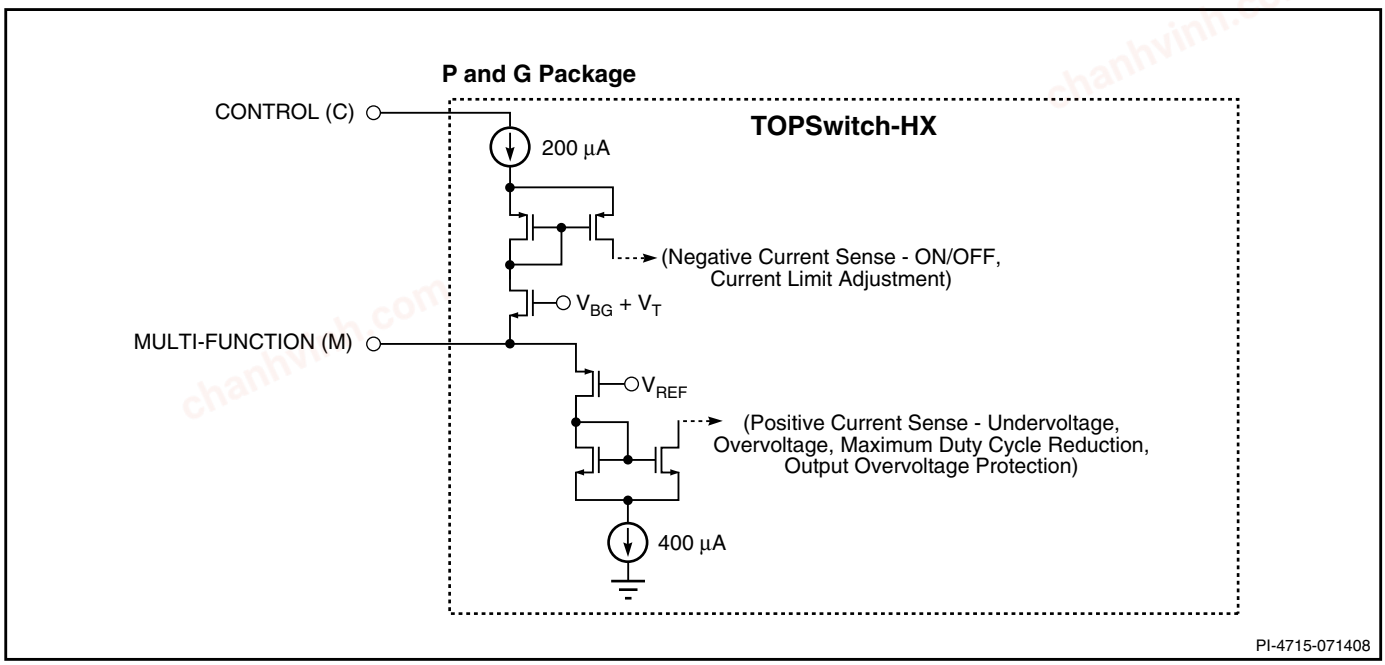


Figure 13b. MULTI-FUNCTION (M) Pin Input Simplified Schematic.

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Typical Uses of FREQUENCY (F) Pin

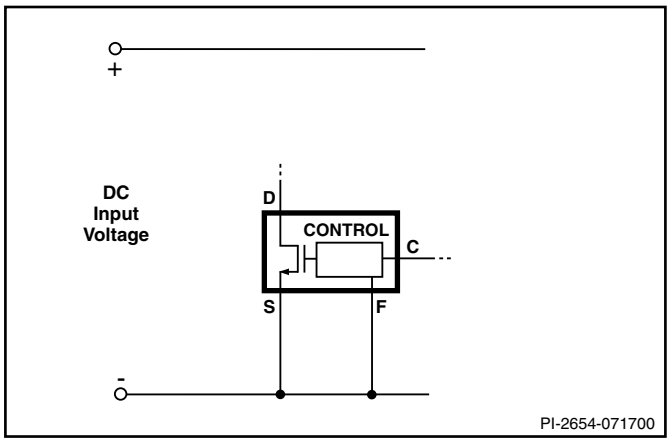


Figure 14. Full Frequency Operation (132 kHz).

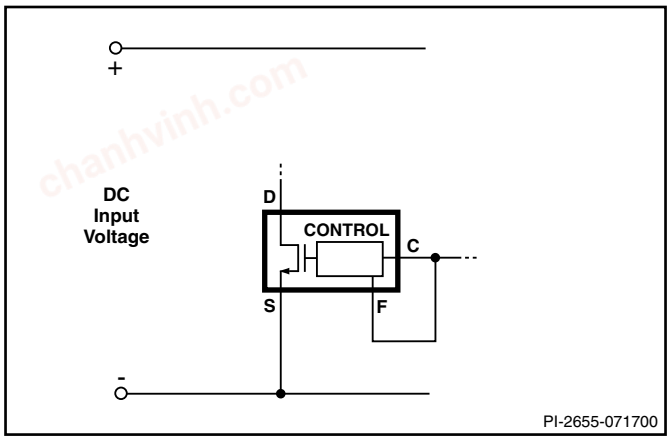


Figure 15. Half Frequency Operation (66 kHz).

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Typical Uses of VOLTAGE MONITOR (V) and EXTERNAL CURRENT LIMIT (X) Pins

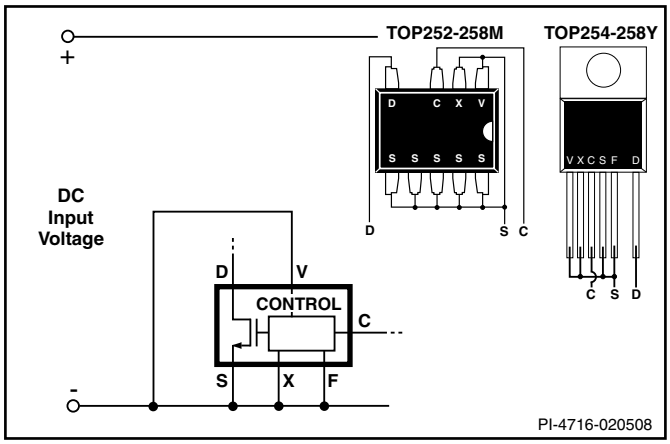


Figure 16a. Three Terminal Operation (VOLTAGE MONITOR and EXTERNAL CURRENT LIMIT Features Disabled. FREQUENCY Pin Tied to SOURCE or CONTROL Pin) for TOP254-258 Y Packages.

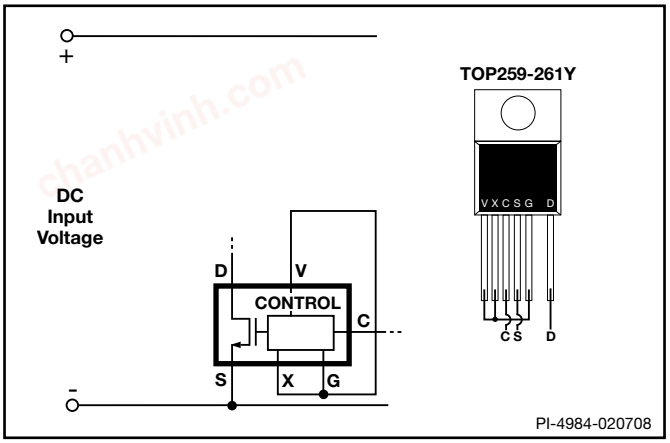


Figure 16b. Three Terminal Operation (VOLTAGE MONITOR and EXTERNAL CURRENT LIMIT Features Disabled for TOP259-261 Y Packages.

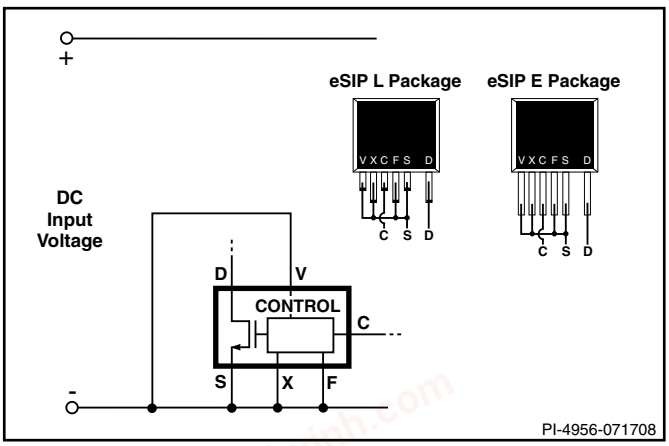


Figure 16c. Three Terminal Operation (VOLTAGE MONITOR and EXTERNAL CURRENT LIMIT Features Disabled. FREQUENCY Pin Tied to SOURCE or CONTROL Pin) for TOP252-262 L and E Packages.

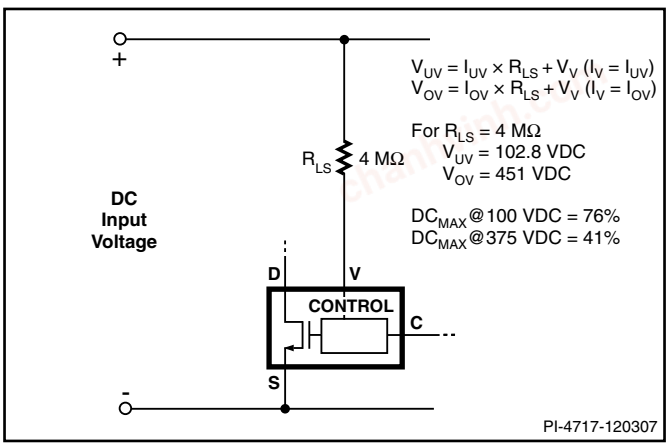


Figure 17. Line-Sensing for Undervoltage, Overvoltage and Line Feed-Forward.

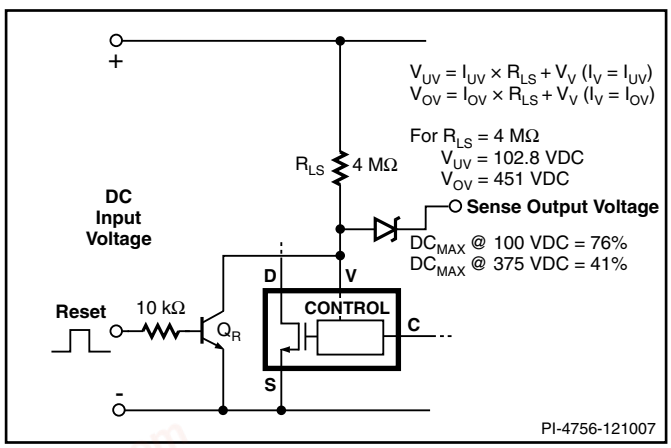


Figure 18. Line-Sensing for Undervoltage, Overvoltage, Line Feed-Forward and Latched Output Overvoltage Protection.

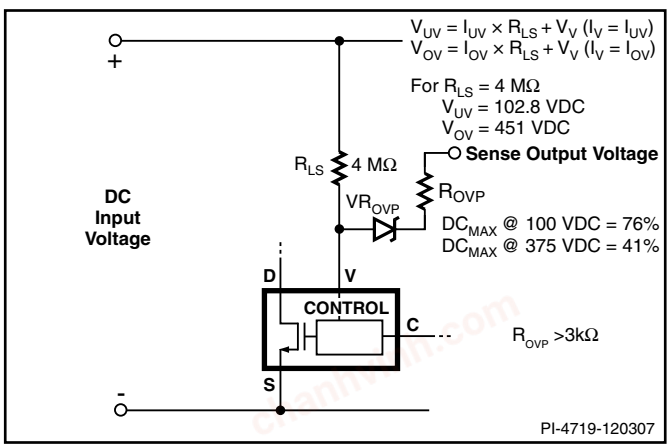


Figure 19. Line-Sensing for Undervoltage, Overvoltage, Line Feed-Forward and Hysteretic Output Overvoltage Protection.

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Typical Uses of VOLTAGE MONITOR (V) and EXTERNAL CURRENT LIMIT (X) Pins (cont.)

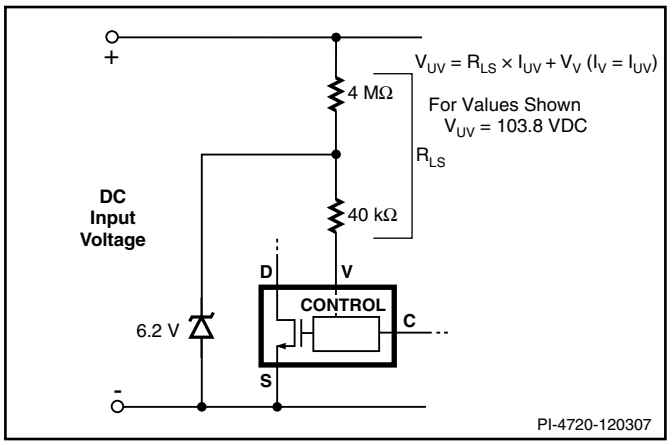


Figure 20. Line Sensing for Undervoltage Only (Overvoltage Disabled).

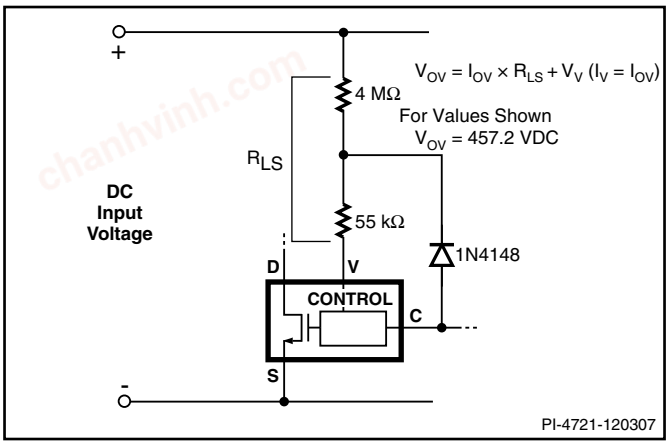


Figure 21. Line-Sensing for Overvoltage Only (Undervoltage Disabled). Maximum Duty Cycle Reduced at Low Line and Further Reduction with Increasing Line Voltage.

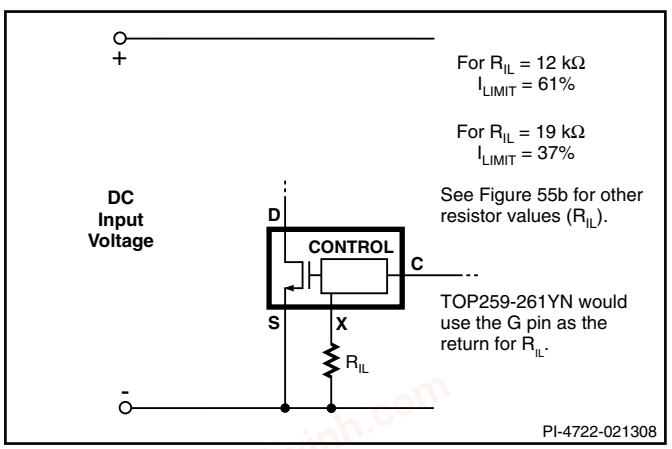


Figure 22. External Set Current Limit.

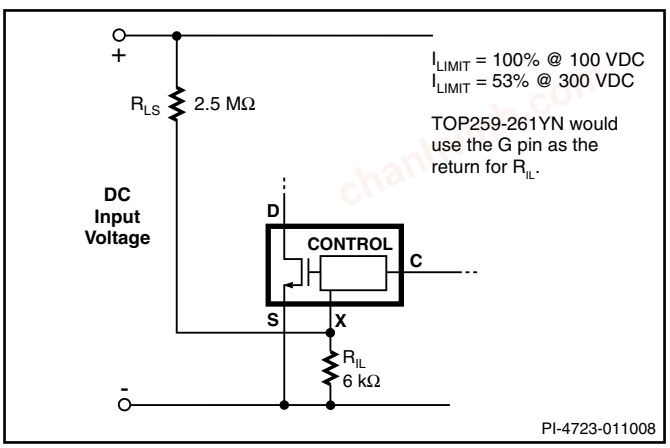


Figure 23. Current Limit Reduction with Line Voltage.

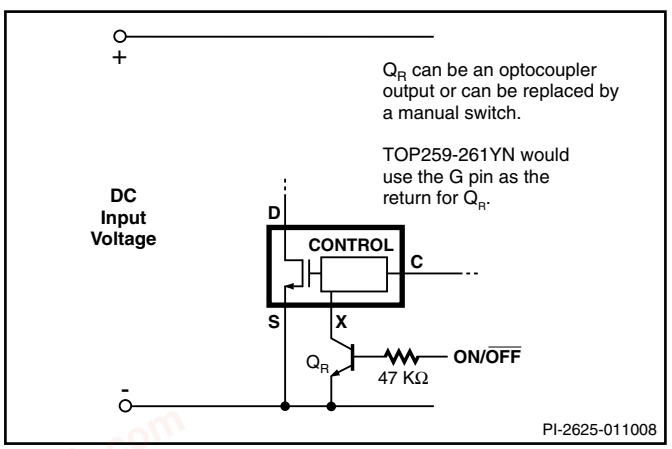


Figure 24. Active-on (Fail Safe) Remote ON/OFF.

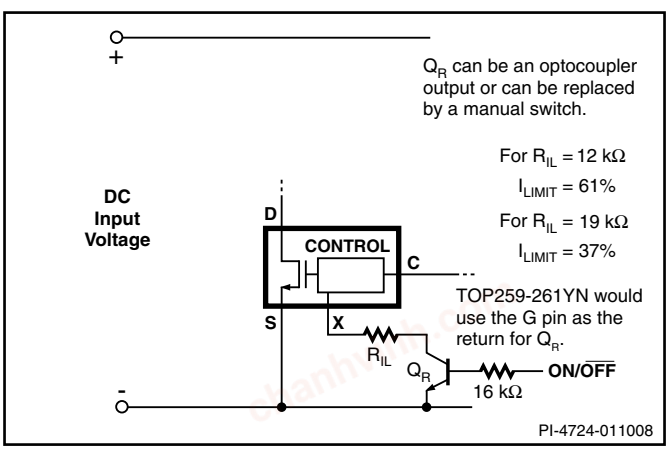


Figure 25. Active-on Remote ON/OFF with Externally Set Current Limit.

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Typical Uses of VOLTAGE MONITOR (V) and EXTERNAL CURRENT LIMIT (X) Pins (cont.)

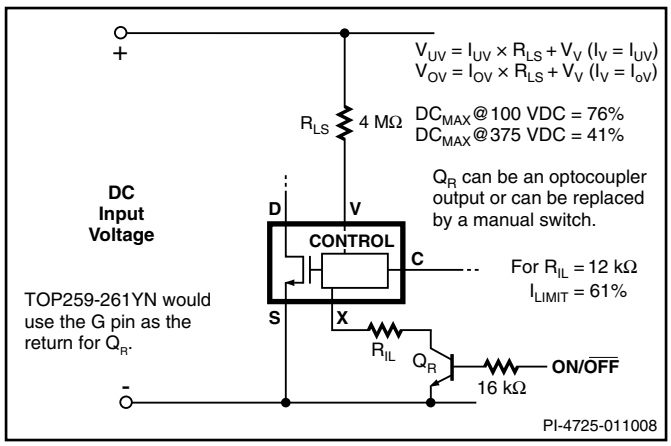


Figure 26. Active-on Remote ON/OFF with Line-Sense and External Current Limit.

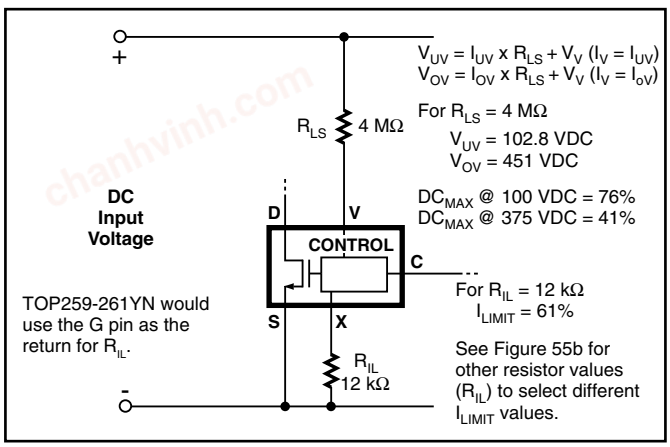


Figure 27. Line Sensing and Externally Set Current Limit.

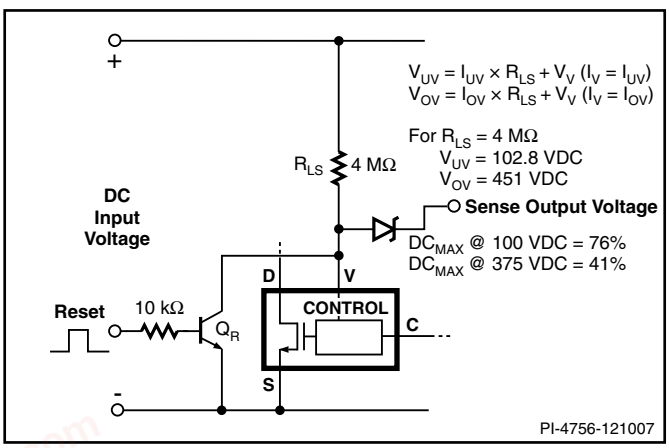


Figure 28. Line-Sensing for Undervoltage, Overvoltage, Line Feed-Forward and Latched Output Overvoltage Protection with Device Reset.

Typical Uses of MULTI-FUNCTION (M) Pin

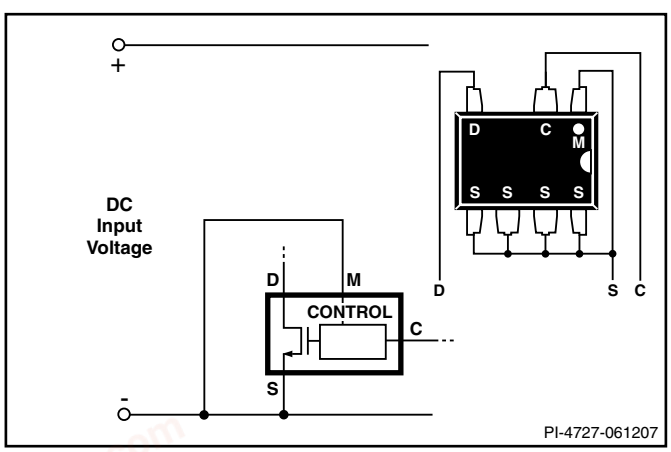


Figure 29. Three Terminal Operation (MULTI-FUNCTION Features Disabled).

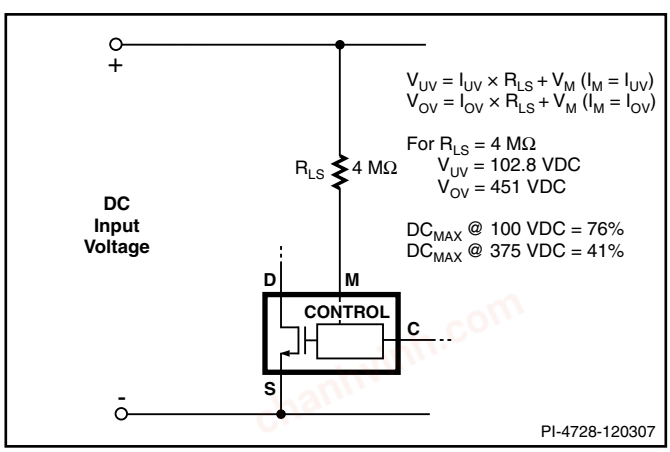


Figure 30. Line Sensing for Undervoltage, Overvoltage and Line Feed-Forward.

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Typical Uses of MULTI-FUNCTION (M) Pin (cont.)

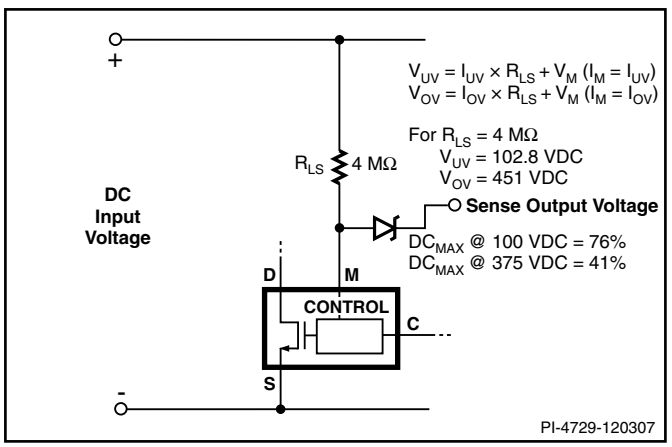


Figure 31. Line Sensing for Undervoltage, Overvoltage, Line Feed-Forward and Latched Output Overvoltage Protection.

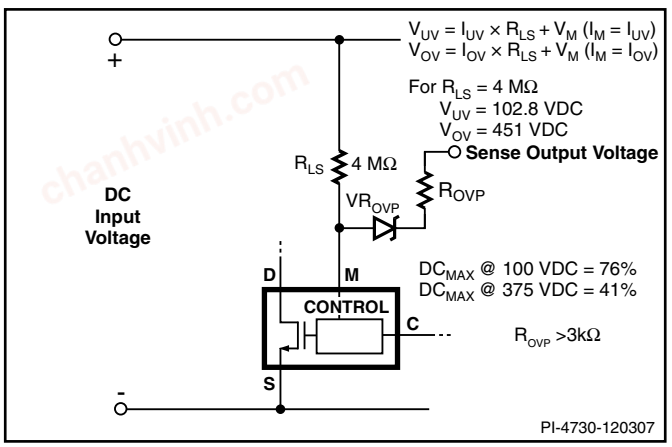


Figure 32. Line Sensing for Undervoltage, Overvoltage, Line Feed-Forward and Hysteretic Output Overvoltage Protection.

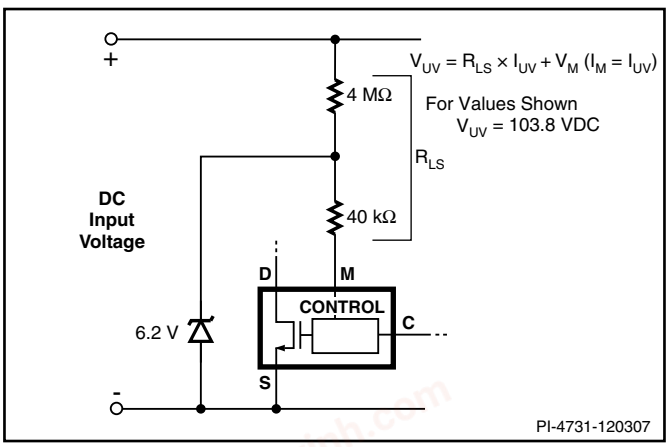


Figure 33. Line Sensing for Undervoltage Only (Overvoltage Disabled).

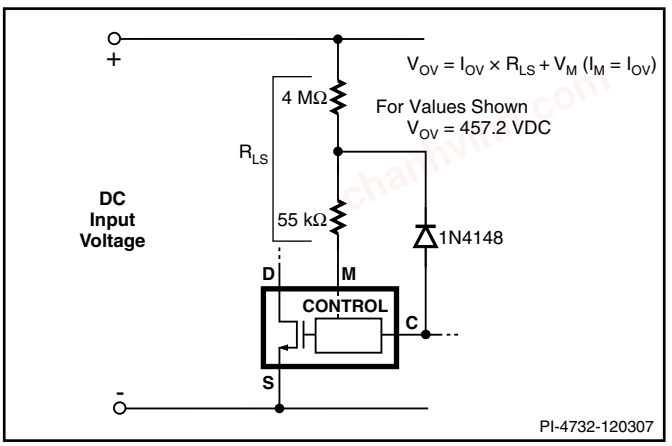


Figure 34. Line Sensing for Overvoltage Only (Undervoltage Disabled). Maximum Duty Cycle Reduced at Low Line and Further Reduction with Increasing Line Voltage.

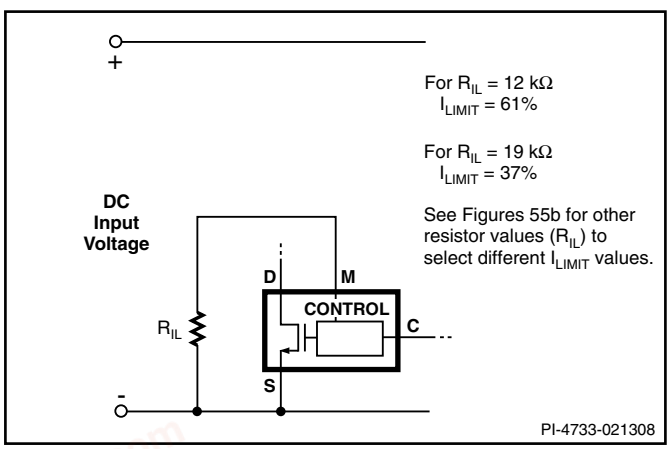


Figure 35. Externally Set Current Limit (Not Normally Required – See M Pin Operation Description).

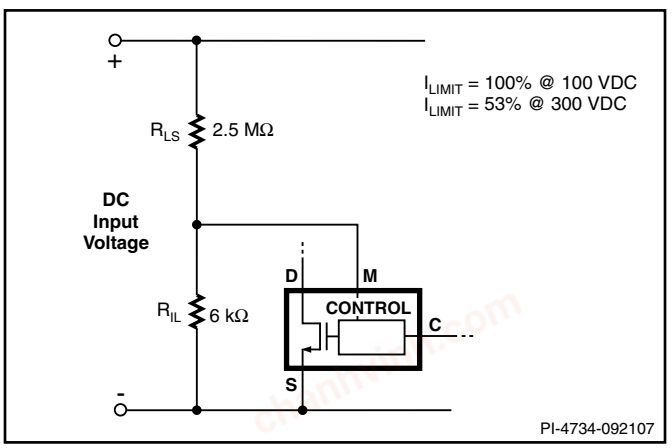


Figure 36. Current Limit Reduction with Line Voltage (Not Normally Required – See M Pin Operation Description).

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Typical Uses of MULTI-FUNCTION (M) Pin (cont.)

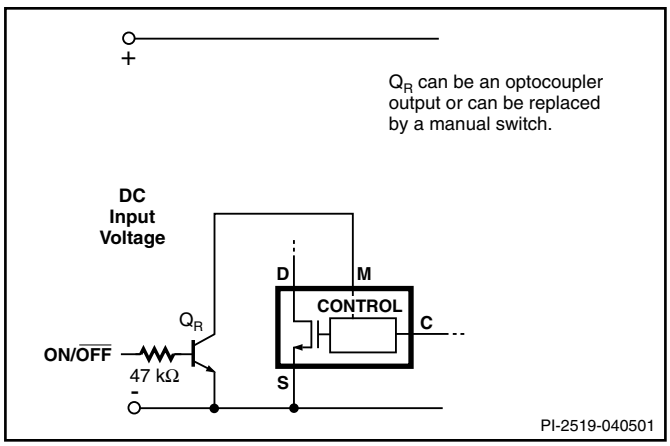


Figure 37. Active-on (Fail Safe) Remote ON/OFF.

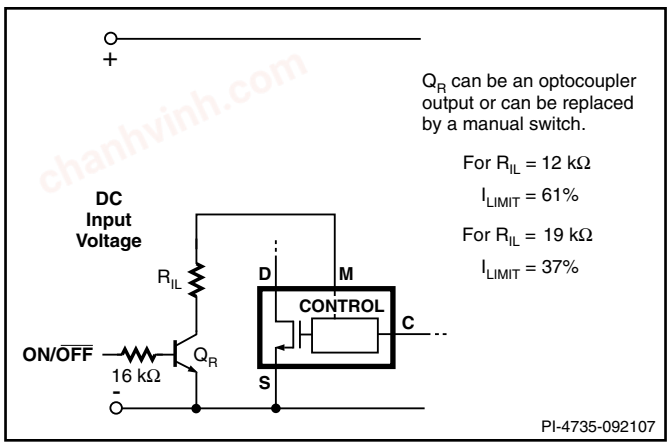


Figure 38. Active-on Remote ON/OFF with Externally Set Current Limit (see M Pin Operation Description).

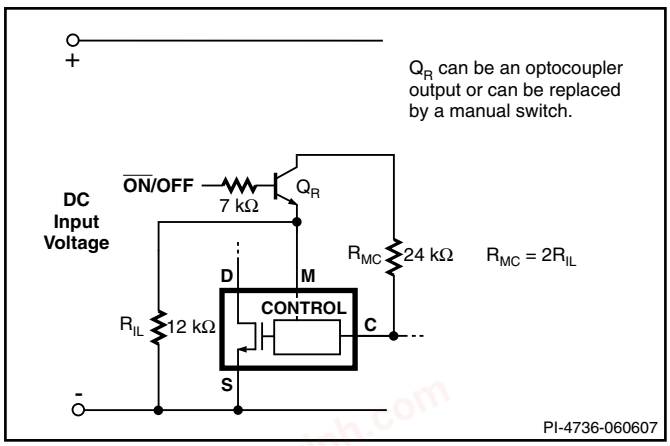


Figure 39. Active-off Remote ON/OFF with Externally Set Current Limit (see M Pin Operation Description).

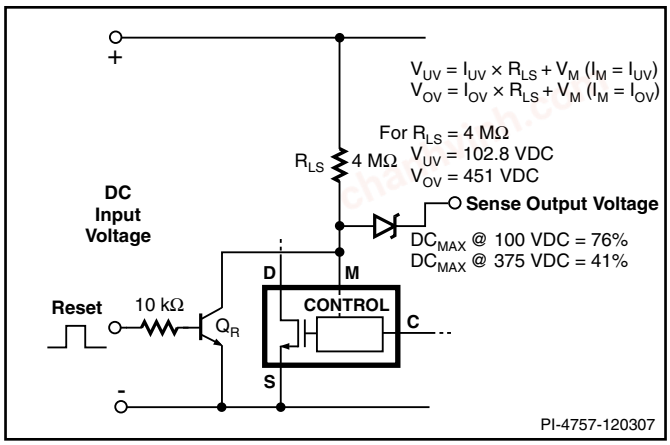


Figure 40. Line-Sensing for Undervoltage, Overvoltage, Line Feed-Forward and Latched Output Overvoltage Protection with Device Reset.

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Application Examples

A High Efficiency, 35 W, Dual Output - Universal Input Power Supply

The circuit in Figure 41 takes advantage of several of the TOPSwitch-HX features to reduce system cost and power supply size and to improve efficiency. This design delivers 35 W total continuous output power from a 90 VAC to 265 VAC input at an ambient of 50 ºC in an open frame configuration. A nominal efficiency of 84% at full load is achieved using TOP258P. With a DIP-8 package, this design provides 35 W continuous output power using only the copper area on the circuit board underneath the part as a heat sink. The different operating modes of the TOPSwitch-HX provide significant improvement in the no-load, standby, and light load performance of the power supply as compared to the previous generations of the TOPSwitch.

Resistors R3 and R4 provide line sensing, setting line UV at 100 VDC and line OV at 450 VDC.

Diode D5, together with resistors R6, R7, capacitor C6 and TVS VR1, forms a clamp network that limits the drain voltage of the TOPSwitch after the integrated MOSFET turns off. TVS VR1 provides a defined maximum clamp voltage and typically only conducts during fault conditions such as overload. This allows the RCD clamp (R6, R7, C6 and D5) to be sized for normal operation, thereby maximizing efficiency at light load. Should the feedback circuit fail, the output of the power supply may exceed regulation limits. This increased voltage at output will also result in an increased voltage at the output of the bias winding. Zener VR2 will break down and current will flow into the “M” pin of the TOPSwitch initiating a hysteretic overvoltage protection with automatic restart attempts. Resistor R5 will limit the current into the M pin to < 336 µA, thus setting hysteretic OVP. If latching OVP is desired, the value of R5 can be reduced to 20 Ω.

The output voltage is controlled using the amplifier TL431. Diode D9, capacitor C20 and resistor R16 form the soft finish circuit. At startup, capacitor C20 is discharged. As the output voltage starts rising, current flows through the optocoupler diode inside U2A, resistor R13 and diode D9 to charge capacitor C20. This provides feedback to the circuit on the primary side. The current in the optocoupler diode U2A gradually decreases as the capacitor C20 becomes charged and the control amplifier IC U3 becomes operational. This ensures that the output voltage increases gradually and settles to the final value without any overshoot. Resistor R16 ensures that the capacitor C20 is maintained charged at all times after startup, which effectively isolates C20 from the feedback circuit after startup. Capacitor C20 discharges through R16 when the supply shuts down.

Resistors R20, R21 and R18 form a voltage divider network. The output of this divider network is primarily dependent on the divider circuit formed using R20 and R21 and will vary to some extent for changes in voltage at the 15 V output due to the connection of resistor R18 to the output of the divider network. Resistor R19 and Zener VR3 improve cross regulation in case only the 5 V output is loaded, which results in the 12 V output operating at the higher end of the specification.

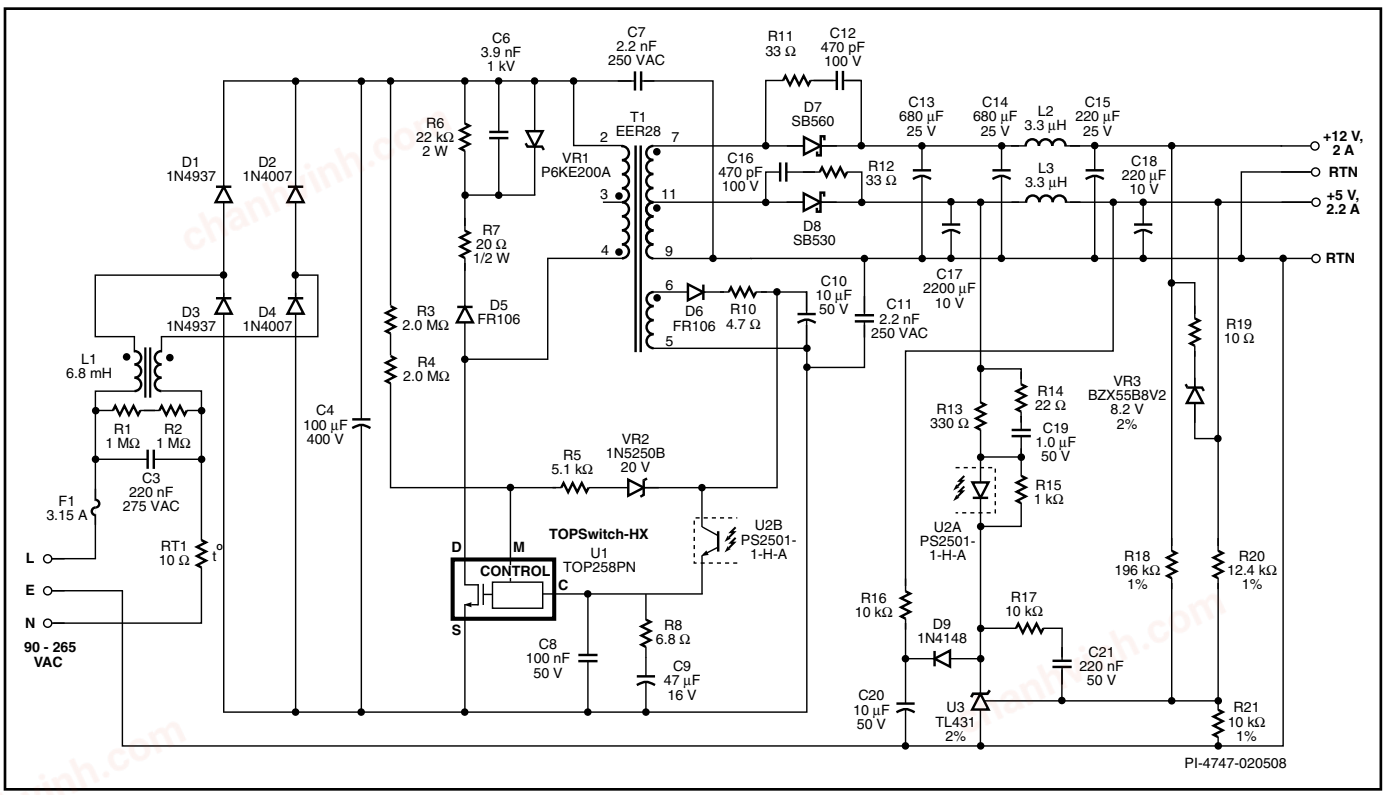


Figure 41. 35 W Dual Output Power Supply using TOP258PN.

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A High Efficiency, 150 W, 250 – 380 VDC Input Power Supply

The circuit shown in Figure 42 delivers 150 W (19 V @ 7.7 A) at 84% efficiency using a TOP258Y from a 250 VDC to 380 VDC input. A DC input is shown, as typically at this power level a power factor correction stage would precede this supply, providing the DC input. Capacitor C1 provides local decoupling, necessary when the supply is remote from the main PFC output capacitor.

The flyback topology is still usable at this power level due to the high output voltage, keeping the secondary peak currents low enough so that the output diode and capacitors are reasonably sized. In this example, the TOP258YN is at the upper limit of its power capability.

Resistors R3, R6 and R7 provide output power limiting, maintaining relatively constant overload power with input voltage. Line sensing is implemented by connecting a 4 MΩ resistor from the V pin to the DC rail. Resistors R4 and R5 together form the 4 MΩ line sense resistor. If the DC input rail rises above 450 VDC, then TOPSwitch-HX will stop switching until the voltage returns to normal, preventing device damage.

Due to the high primary current, a low leakage inductance transformer is essential. Therefore, a sandwich winding with a copper foil secondary was used. Even with this technique, the leakage inductance energy is beyond the power capability of a simple Zener clamp. Therefore, R1, R2 and C3 are added in parallel to VR1 and VR3, two series TVS diodes being used to reduce dissipation. During normal operation, very little power is dissipated by VR1 and VR3, the leakage energy instead being dissipated by R1 and R2. However, VR1 and VR3 are essential to limit the peak drain voltage during start-up and/or overload conditions to below the 700 V rating of the TOPSwitch-HX MOSFET. The schematic shows an additional turn-off snubber circuit consisting of R20, R21, R22, D5 and C18. This reduces turn-off losses in the TOPSwitch-HX.

The secondary is rectified and smoothed by D2, D3 and C5, C6, C7 and C8. Two windings are used and rectified with separate diodes D2 and D3 to limit diode dissipation. Four capacitors are used to ensure their maximum ripple current specification is not exceeded. Inductor L1 and capacitors C15 and C16 provide switching noise filtering.

Output voltage is controlled using a TL431 reference IC and R15, R16 and R17 to form a potential divider to sense the output voltage. Resistor R12 and R24 together limit the optocoupler LED current and set overall control loop DC gain. Control loop compensation is achieved using components C12, C13, C20 and R13. Diode D6, resistor R23 and capacitor C19 form a soft finish network. This feeds current into the control pin prior to output regulation, preventing output voltage overshoot and ensuring startup under low line, full load conditions.

Sufficient heat sinking is required to keep the TOPSwitch-HX device below 110 °C when operating under full load, low line and maximum ambient temperature. Airflow may also be required if a large heat sink area is not acceptable.

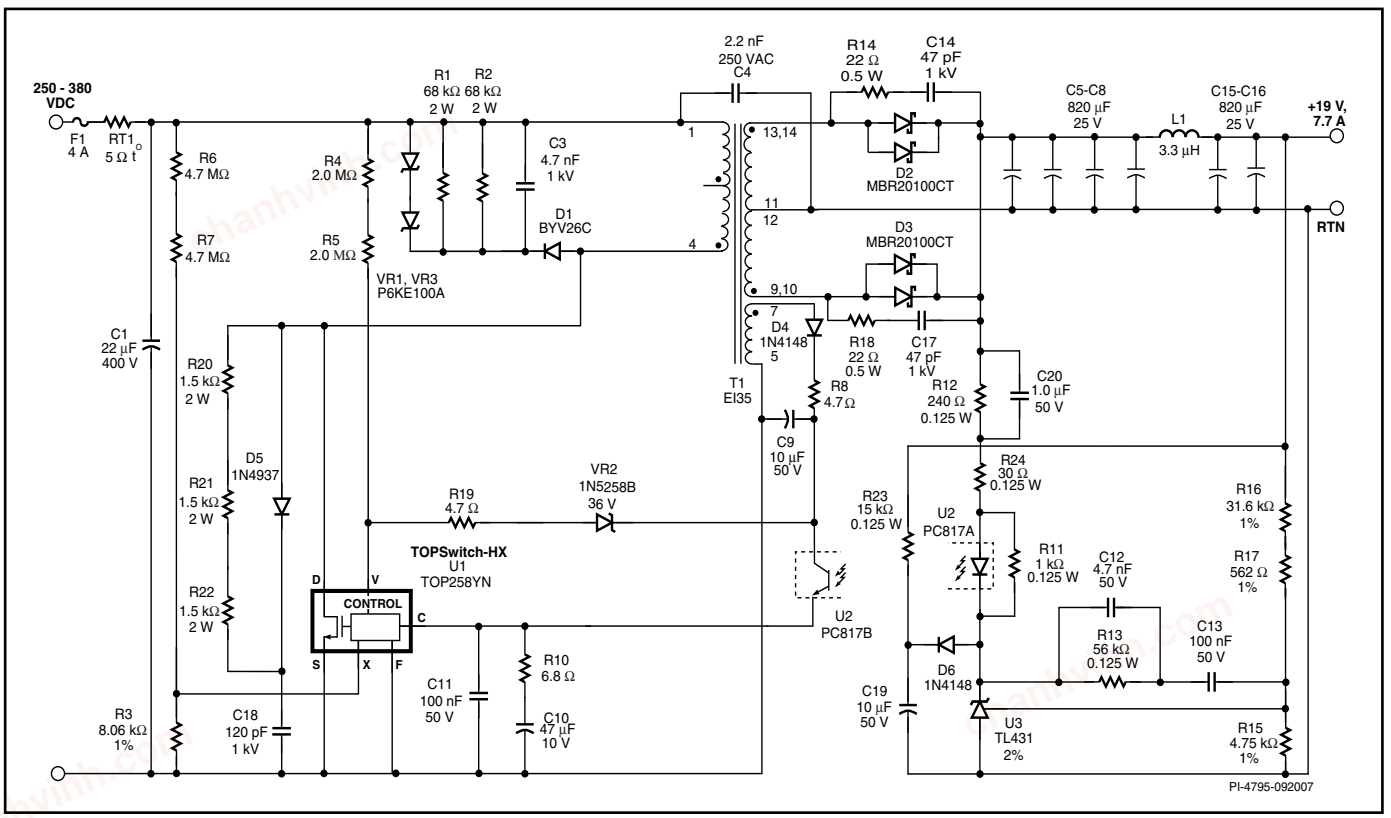


Figure 42. 150 W, 19 V Power Supply using TOP258YN.

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A High Efficiency, 20 W continuous – 80 W Peak, Universal Input Power Supply

The circuit shown in Figure 43 takes advantage of several of TOPSwitch-HX features to reduce system cost and power supply size and to improve power supply efficiency while delivering significant peak power for a short duration. This design delivers continuous 20 W and peak 80 W at 32 V from an 90 VAC to 264 VAC input. A nominal efficiency of 82% at full load is achieved using TOP258MN. The M-package part has an optimized current limit to enable design of power supplies capable of delivering high power for a short duration.

Resistor R12 sets the current limit of the part. Resistors R11 and R14 provide line feed forward information that reduces the current limit with increasing DC bus voltage, thereby maintaining a constant overload power level with increasing line voltage. Resistors R1 and R2 implement the line undervoltage and overvoltage function and also provide feed forward compensation for reducing line frequency ripple at the output. The overvoltage feature inhibits TOPSwitch-HX switching during a line surge extending the high voltage withstand to 700 V without device damage.

The snubber circuit comprising of VR7, R17, R25, C5 and D2 limits the maximum drain voltage and dissipates energy stored in the leakage inductance of transformer T1. This clamp configuration maximizes energy efficiency by preventing C5 from discharging below the value of VR7 during the lower frequency operating modes of TOPSwitch-HX. Resistor R25 damps high frequency ringing for reduced EMI.

A combined output overvoltage and over power protection circuit is provided via the latching shutdown feature of TOPSwitch-HX and R20, C9, R22 and VR5. Should the bias winding output voltage across C13 rise due to output overload or an open loop fault (opto coupler failure), then VR5 conducts triggering the latching shutdown. To prevent false triggering due to short duration overload, a delay is provided by R20, R22 and C9.

To reset the supply following a latching shutdown, the V pin must fall below the reset threshold. To prevent the long reset delay associated with the input capacitor discharging, a fast AC reset circuit is used. The AC input is rectified and filtered by D13 and C30. While the AC supply is present, Q3 is on and Q1 is off, allowing normal device operation. However when AC is removed, Q1 pulls down the V pin and resets the latch. The supply will then return to normal operation when AC is again applied.

Transistor Q2 provides an additional lower UV threshold to the level programmed via R1, R2 and the V pin. At low input AC voltage, Q2 turns off, allowing the X pin to float and thereby disabling switching.

A simple feedback circuit automatically regulates the output voltage. Zener VR3 sets the output voltage together with the voltage drop across series resistor R8, which sets the DC gain of the circuit. Resistors R10 and C28 provide a phase boost to improve loop bandwidth.

Diodes D6 and D7 are low-loss Schottky rectifiers, and capacitor C20 is the output filter capacitor. Inductor L3 is a common mode choke to limit radiated EMI when long output cables are used and the output return is connected to safety earth ground. Example applications where this occurs include PC peripherals, such as inkjet printers.

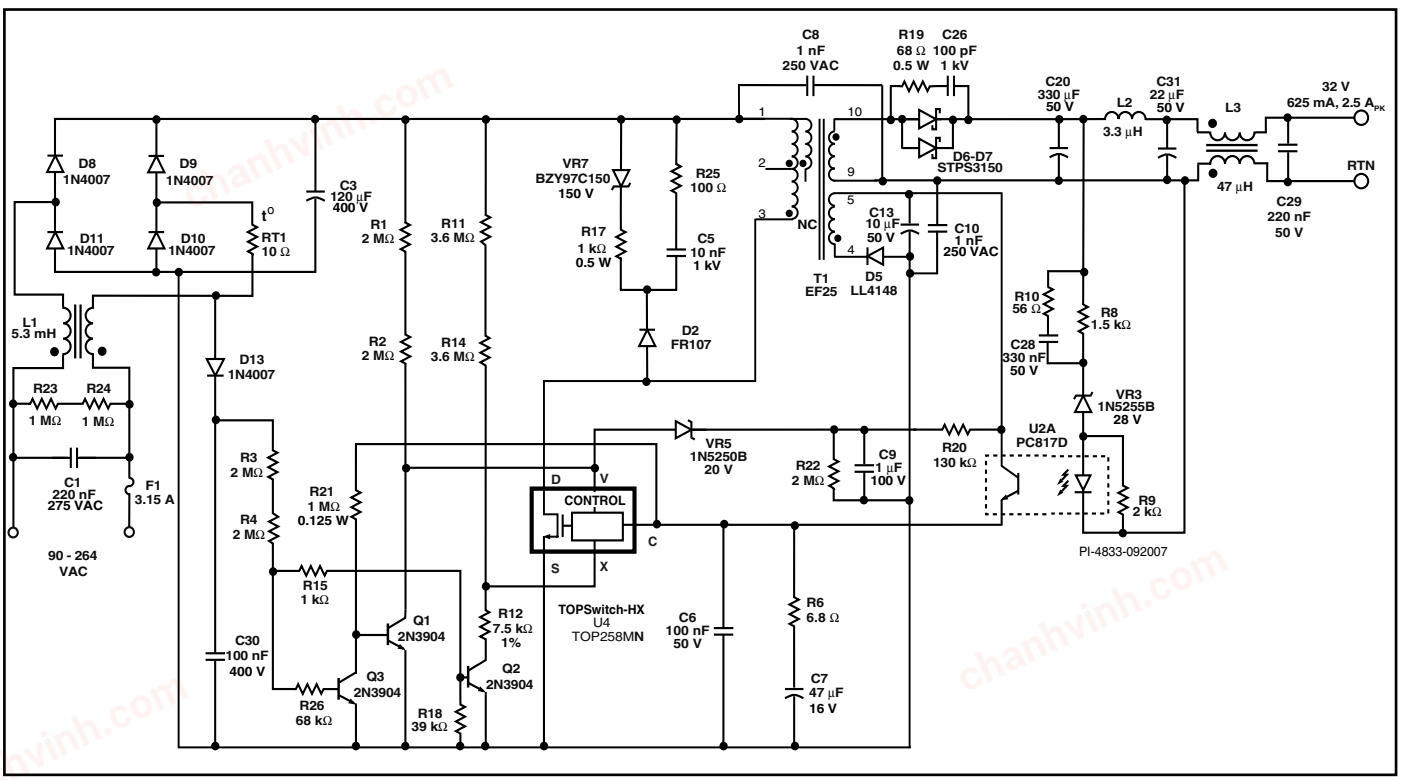


Figure 43. 20 W Continuous, 80 W Peak, Universal Input Power Supply using TOP258MN.

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A High Efficiency, 65 W, Universal Input Power Supply
The circuit shown in Figure 44 delivers 65 W (19 V @ 3.42 A) at 88% efficiency using a TOP260EN operating over an input voltage range of 90 VAC to 265 VAC.

Capacitors C1 and C6 and inductors L1 and L2 provide common mode and differential mode EMI filtering. Capacitor C2 is the bulk filter capacitor that ensures low ripple DC input to the flyback converter stage. Capacitor C4 provides decoupling for switching currents reducing differential mode EMI.

In this example, the TOP260EN is used at reduced current limit to improve efficiency.

Resistors R5, R6 and R7 provide power limiting, maintaining relatively constant overload power with input voltage. Line sensing is implemented by connecting a 4 MΩ impedance from the V pin to the DC rail. Resistors R3 and R4 together form the 4 MΩ line sense resistor. If the DC input rail rises above 450 VDC, then TOPSwitch-HX will stop switching until the voltage returns to normal, preventing device damage.

This circuit features a high efficiency clamp network consisting of diode D1, zener VR1, capacitor C5 together with resistors R8 and R9. The snubber clamp is used to dissipate the energy of the leakage reactance of the transformer. At light load levels, very little power is dissipated by VR1 improving efficiency as compared to a conventional RCD clamp network.

The secondary output from the transformer is rectified by diode D2 and filtered by capacitors C13 and C14. Ferrite Bead L3 and capacitors C15 form a second stage filter and effectively reduce the switching noise to the output.

Output voltage is controlled using a LM431 reference IC. Resistor R19 and R20 form a potential divider to sense the output voltage. Resistor R16 limits the optocoupler LED current and sets the overall control loop DC gain. Control loop compensation is achieved using C18 and R21. The components connected to the control pin on the primary side C8, C9 and R15 set the low frequency pole and zero to further shape the control loop response. Capacitor C17 provides a soft finish during startup. Optocoupler U2 is used for isolation of the feedback signal.

Diode D4 and capacitor C10 form the bias winding rectifier and filter. Should the feedback loop break due to a defective component, a rising bias winding voltage will cause the Zener VR2 to break down and trigger the over voltage protection which will inhibit switching.

An optional secondary side over voltage protection feature which offers higher precision (as compared to sensing via the bias winding) is implemented using VR3, R18 and U3. Excess voltage at the output will cause current to flow through the optocoupler U3 LED which in turn will inject current in the V-pin through resistor R13, thereby triggering the over voltage protection feature.

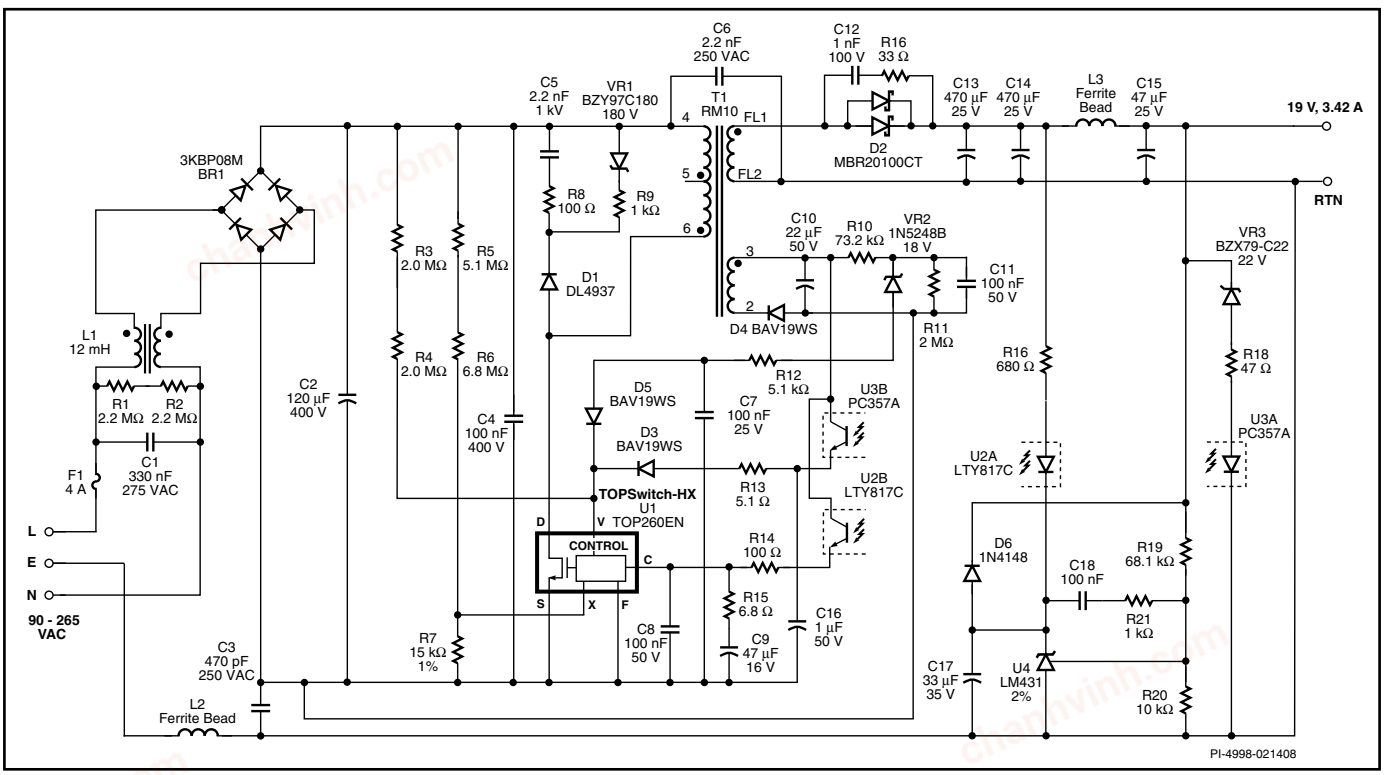


Figure 44. 65 W, 19 V Power Supply Using TOP260EN.

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Key Application Considerations

TOPSwitch-HX vs. TOPSwitch-GX

Table 4 compares the features and performance differences between TOPSwitch-HX and TOPSwitch-GX. Many of the new features eliminate the need for additional discrete components. Other features increase the robustness of design, allowing cost savings in the transformer and other power components.

TOPSwitch-HX vs. TOPSwitch-GX

Function	TOPSwitch-GX	TOPSwitch-HX	TOPSwitch-HX Advantages
EcoSmart	Linear frequency reduction to 30 kHz (@ 132 kHz) for duty cycles < 10%	Multi-mode operation with linear frequency reduction to 30 kHz (@ 132 kHz) and multi-cycle modulation (virtually no audible noise)	• Improved efficiency over load (e.g. at 25% load point) • Improved standby efficiency • Improved no-load consumption
Output Overvoltage Protection (OVP)	Not available	User programmable primary or secondary hysteretic or latching OVP	• Protects power supply output during open loop fault • Maximum design flexibility
Line Feed-Forward with Duty Cycle Reduction	Linear reduction	Dual slope reduction with lower, more accurate onset point	• Improved line ripple rejection • Smaller DC bus capacitor
Switching Frequency DIP-8 Package	132 kHz	66 kHz	• Increased output power for given MOSFET size due to higher efficiency
Lowest MOSFET On Resistance in DIP-8 Package	3.0 Ω (TOP246P)	1.8 Ω (TOP258P)	• Increased output power in designs without external heat sink
I^2f Trimming	Not available	-10% / +20%	• Increased output power for given core size • Reduced over-load power
Auto-restart Duty Cycle	5.6%	2%	• Reduced delivered average output power during open loop faults
Frequency Jitter	±4 kHz @ 132 kHz ±2 kHz @ 66 kHz	±5 kHz @ 132 kHz ±2.5 kHz @ 66 kHz	• Reduced EMI filter cost
Thermal Shutdown	130 °C to 150 °C	135 °C to 150 °C	• Increased design margin
External Current Limit	30%-100% of I_{LIMIT}	30%-100% of I_{LIMIT}, additional trim at 0.7 × I_{LIMIT}	• Reduced tolerances when current limit is set externally
Line UV Detection Threshold	50 µA (2 MΩ sense impedance)	25 µA (4 MΩ sense impedance)	• Reduced dissipation for lower no-load consumption
Soft-Start	10 ms duty cycle and current limit ramp	17 ms sweep through multi-mode characteristic	• Reduced peak current and voltage component stress at startup • Smooth output voltage rise

Table 4. Comparison Between TOPSwitch-GX and TOPSwitch-HX.

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TOPSwitch-HX Design Considerations

Power Table

The data sheet power table (Table 1) represents the maximum practical continuous output power based on the following conditions:

1. 12 V output.
2. Schottky or high efficiency output diode.
3. 135 V reflected voltage (V_{OR}) and efficiency estimates.
4. A 100 VDC minimum for 85-265 VAC and 250 VDC minimum for 230 VAC.
5. Sufficient heat sinking to keep device temperature ≤100 °C.
6. Power levels shown in the power table for the M/P package device assume 6.45 cm^2 of 610 g/m^2 copper heat sink area in an enclosed adapter, or 19.4 cm^2 in an open frame.

The provided peak power depends on the current limit for the respective device.

TOPSwitch-HX Selection

Selecting the optimum TOPSwitch-HX depends upon required maximum output power, efficiency, heat sinking constraints, system requirements and cost goals. With the option to externally reduce current limit, an Y, E/L or M package TOPSwitch-HX may be used for lower power applications where higher efficiency is needed or minimal heat sinking is available.

Input Capacitor

The input capacitor must be chosen to provide the minimum DC voltage required for the TOPSwitch-HX converter to maintain regulation at the lowest specified input voltage and maximum output power. Since TOPSwitch-HX has a high DC_{MAX} limit and an optimized dual slope line feed forward for ripple rejection, it is possible to use a smaller input capacitor. For TOPSwitch-HX, a capacitance of 2 µF per watt is possible for universal input with an appropriately designed transformer.

Primary Clamp and Output Reflected Voltage V_{OR}

A primary clamp is necessary to limit the peak TOPSwitch-HX drain to source voltage. A Zener clamp requires few parts and takes up little board space. For good efficiency, the clamp Zener should be selected to be at least 1.5 times the output reflected voltage V_{OR}, as this keeps the leakage spike conduction time short. When using a Zener clamp in a universal input application, a V_{OR} of less than 135 V is recommended to allow for the absolute tolerances and temperature variations of the Zener. This will ensure efficient operation of the clamp circuit and will also keep the maximum drain voltage below the rated breakdown voltage of the TOPSwitch-HX MOSFET. A high V_{OR} is required to take full advantage of the wider DC_{MAX} of TOPSwitch-HX. An RCD clamp provides tighter clamp voltage tolerance than a Zener clamp and allows a VOR as high as 150 V. RCD clamp dissipation can be minimized by reducing the external current limit as a function of input line voltage (see Figures 23 and 36). The RCD clamp is more cost effective than the Zener clamp but requires more careful design (see Quick Design Checklist).

Output Diode

The output diode is selected for peak inverse voltage, output current, and thermal conditions in the application (including heat sinking, air circulation, etc.). The higher DC_{MAX} of TOPSwitch-HX, along with an appropriate transformer turns ratio, can allow the use of a 80 V Schottky diode for higher efficiency on output voltages as high as 15 V (see Figure 41).

Bias Winding Capacitor

Due to the low frequency operation at no-load, a 10 µF bias winding capacitor is recommended.

Soft-Start

Generally, a power supply experiences maximum stress at start-up before the feedback loop achieves regulation. For a period of 17 ms, the on-chip soft-start linearly increases the drain peak current and switching frequency from their low starting values to their respective maximum values. This causes the output voltage to rise in an orderly manner, allowing time for the feedback loop to take control of the duty cycle. This reduces the stress on the TOPSwitch-HX MOSFET, clamp circuit and output diode(s), and helps prevent transformer saturation during start-up. Also, soft-start limits the amount of output voltage overshoot and, in many applications, eliminates the need for a soft-finish capacitor.

EMI

The frequency jitter feature modulates the switching frequency over a narrow band as a means to reduce conducted EMI peaks associated with the harmonics of the fundamental switching frequency. This is particularly beneficial for average detection mode. As can be seen in Figure 45, the benefits of jitter increase with the order of the switching harmonic due to an increase in frequency deviation. Devices in the P, G or M package and TOP259-261YN operate at a nominal switching frequency of 66 kHz. The FREQUENCY pin of devices in the TOP254-258 Y and E packages offer a switching frequency option of 132 kHz or 66 kHz. In applications that require heavy snubber on the drain node for reducing high frequency radiated noise (for example, video noise sensitive applications such as VCRs, DVDs, monitors, TVs, etc.), operating at 66 kHz will reduce snubber loss, resulting in better efficiency. Also, in applications where transformer size is not a concern, use of the 66 kHz option will provide lower EMI and higher efficiency. Note that the second harmonic of 66 kHz is still below 150 kHz, above which the conducted EMI specifications get much tighter. For 10 W or below, it is possible to use a simple inductor in place of a more costly AC input common mode choke to meet worldwide conducted EMI limits.

Transformer Design

It is recommended that the transformer be designed for maximum operating flux density of 3000 Gauss and a peak flux density of 4200 Gauss at maximum current limit. The turns ratio should be chosen for a reflected voltage (V_{OR}) no greater than 135 V when using a Zener clamp or 150 V (max) when using an RCD clamp with current limit reduction with line voltage (overload protection). For designs where operating current is significantly lower than the default current limit, it is recommended to use an externally set current limit close to the operating peak current to reduce peak flux density and peak power (see Figures 22 and 35). In most applications, the tighter current limit tolerance, higher switching frequency and soft-start features of TOPSwitch-HX contribute to a smaller transformer when compared to TOPSwitch-GX.

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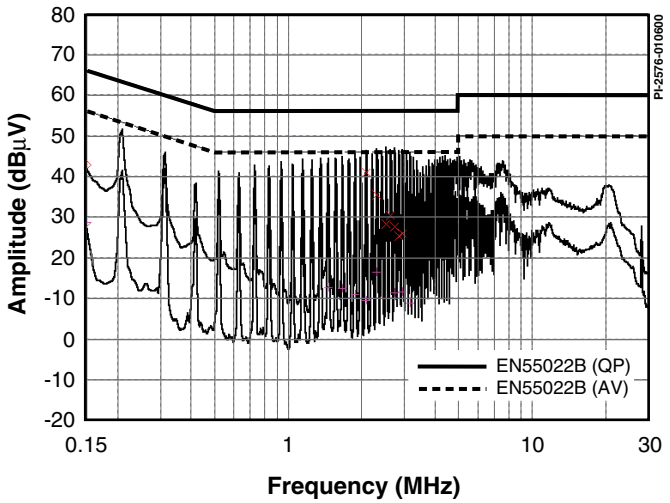


Figure 45a. Fixed Frequency Operation Without Jitter.

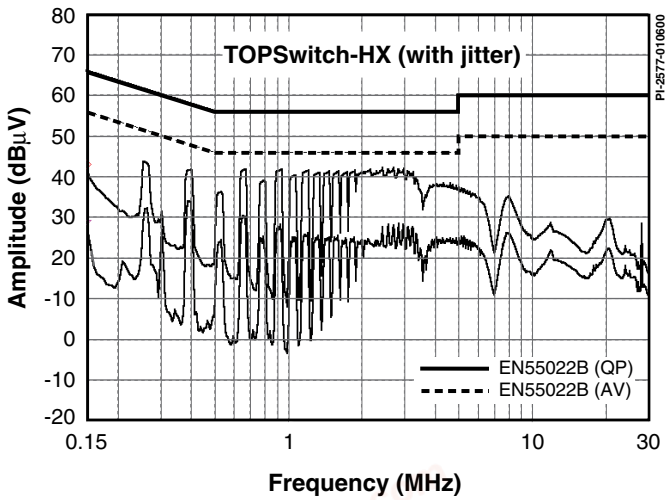


Figure 45b. TOPSwitch-HX Full Range EMI Scan (132 kHz With Jitter) With Identical Circuitry and Conditions.

Standby Consumption

Frequency reduction can significantly reduce power loss at light or no load, especially when a Zener clamp is used. For very low secondary power consumption, use a TL431 regulator for feedback control. A typical TOPSwitch-HX circuit automatically enters MCM mode at no load and the low frequency mode at light load, which results in extremely low losses under no-load or standby conditions.

High Power Designs

The TOPSwitch-HX family contains parts that can deliver up to 333 W. High power designs need special considerations. Guidance for high power designs can be found in the Design Guide for TOPSwitch-HX (AN-43).

TOPSwitch-HX Layout Considerations

The TOPSwitch-HX has multiple pins and may operate at high power levels. The following guidelines should be carefully followed.

Primary Side Connections

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the TOPSwitch-HX SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor. The CONTROL pin bypass capacitor should be located as close as possible to the SOURCE and CONTROL pins, and its SOURCE connection trace should not be shared by the main MOSFET switching currents. All SOURCE pin referenced components connected to the MULTI-FUNCTION (M-pin), VOLTAGE MONITOR (V-pin) or EXTERNAL CURRENT LIMIT (X-pin) pins should also be located closely between their respective pin and SOURCE. Once again, the SOURCE connection trace of these components should not be shared by the main MOSFET switching currents. It is very critical that SOURCE pin switching currents are returned to the input capacitor negative terminal through a separate trace that is not shared by the components connected to CONTROL, MULTI-FUNCTION, VOLTAGE MONITOR or EXTERNAL CURRENT LIMIT pins. This is because the SOURCE pin is also the controller ground reference pin. Any traces to the M, V, X or C pins should be kept as short as possible and away from the DRAIN trace to prevent noise coupling. VOLTAGE MONITOR resistors (R1 and R2 in Figures 46, 47, 48, R3 and R4 in Figure 49, and R14 in Figure 50) should be located close to the M or V pin to minimize the trace length on the M or V pin side. Resistors connected to the M, V or X pin should be connected as close to the bulk cap positive terminal as possible while routing these connections away from the power switching circuitry. In addition to the 47 µF CONTROL pin capacitor, a high frequency bypass capacitor in parallel may be used for better noise immunity. The feedback optocoupler output should also be located close to the CONTROL and SOURCE pins of TOPSwitch-HX and away from the drain and clamp component traces.

Y Capacitor

The Y capacitor should be connected close to the secondary output return pin(s) and the positive primary DC input pin of the transformer.

Heat Sinking

The tab of the Y package (TO-220C) and E package (eSIP-7C) and L package (eSIP-7F) are internally electrically tied to the SOURCE pin. To avoid circulating currents, a heat sink attached to the tab should not be electrically tied to any primary ground/source nodes on the PC board. When using a P (DIP-8), G (SMD-8) or M (DIP-10) package, a copper area underneath the package connected to the SOURCE pins will act as an effective heat sink. On double sided boards, topside and bottom side areas connected with vias can be used to increase the effective heat sinking area. In addition, sufficient copper area should be provided at the anode and cathode leads of the output diode(s) for heat sinking. In Figures 46 to 50 a narrow trace is shown between the output rectifier and output filter capacitor. This trace acts as a thermal relief between the rectifier and filter capacitor to prevent excessive heating of the capacitor.

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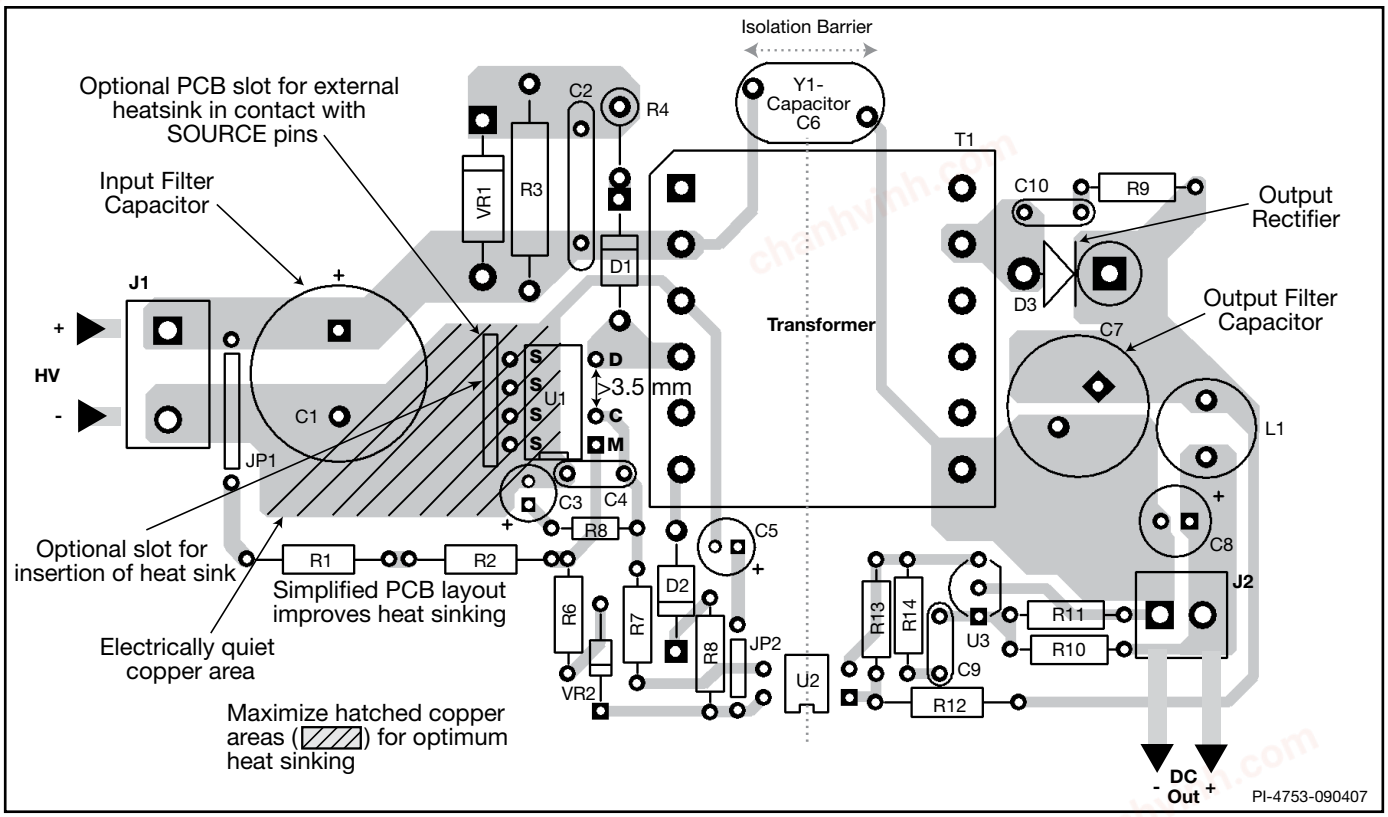


Figure 46. Layout Considerations for TOPSwitch-HX Using P Package.

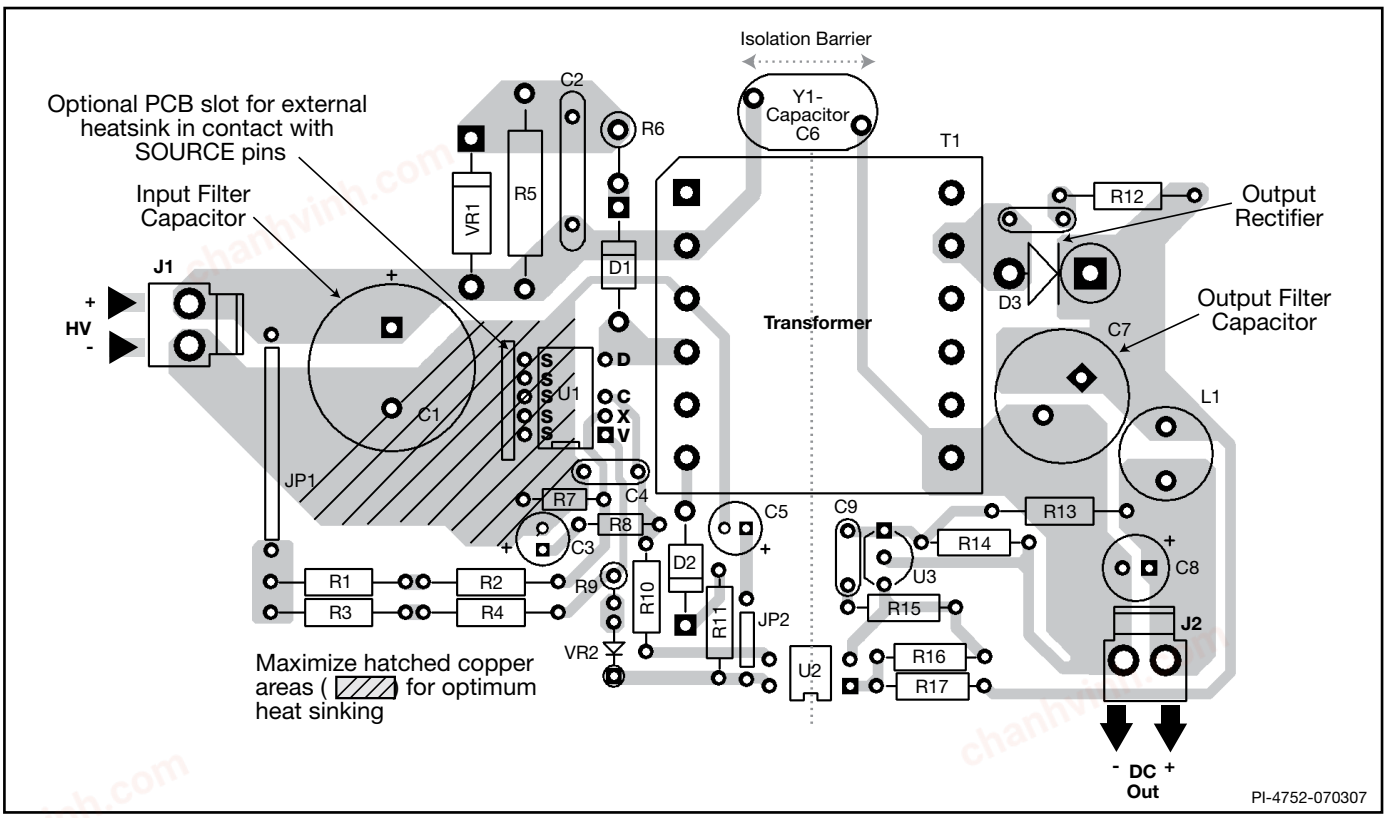


Figure 47. Layout Considerations for TOPSwitch-HX Using M Package.

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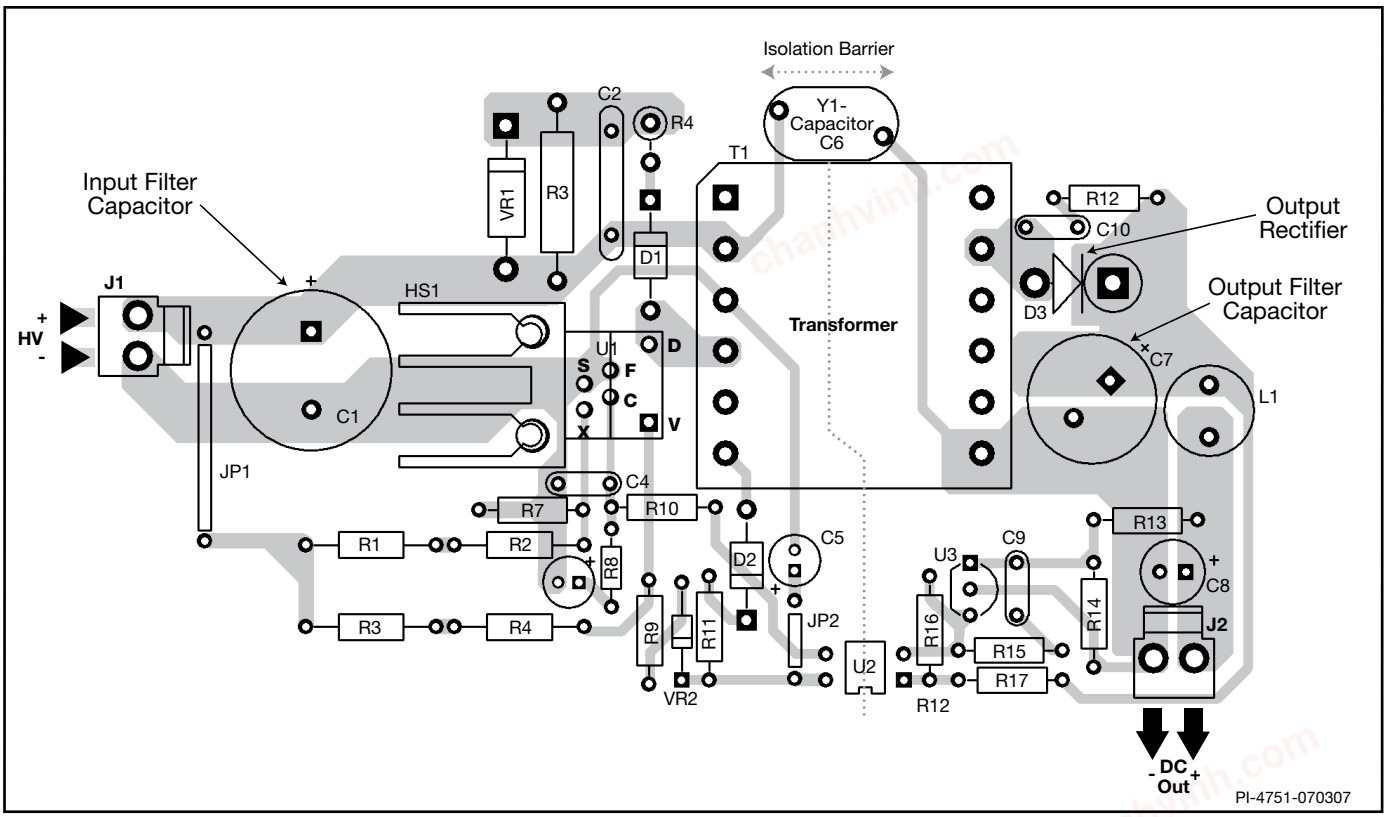


Figure 48. Layout Considerations for TOPSwitch-HX Using TOP254-258 Y Package.

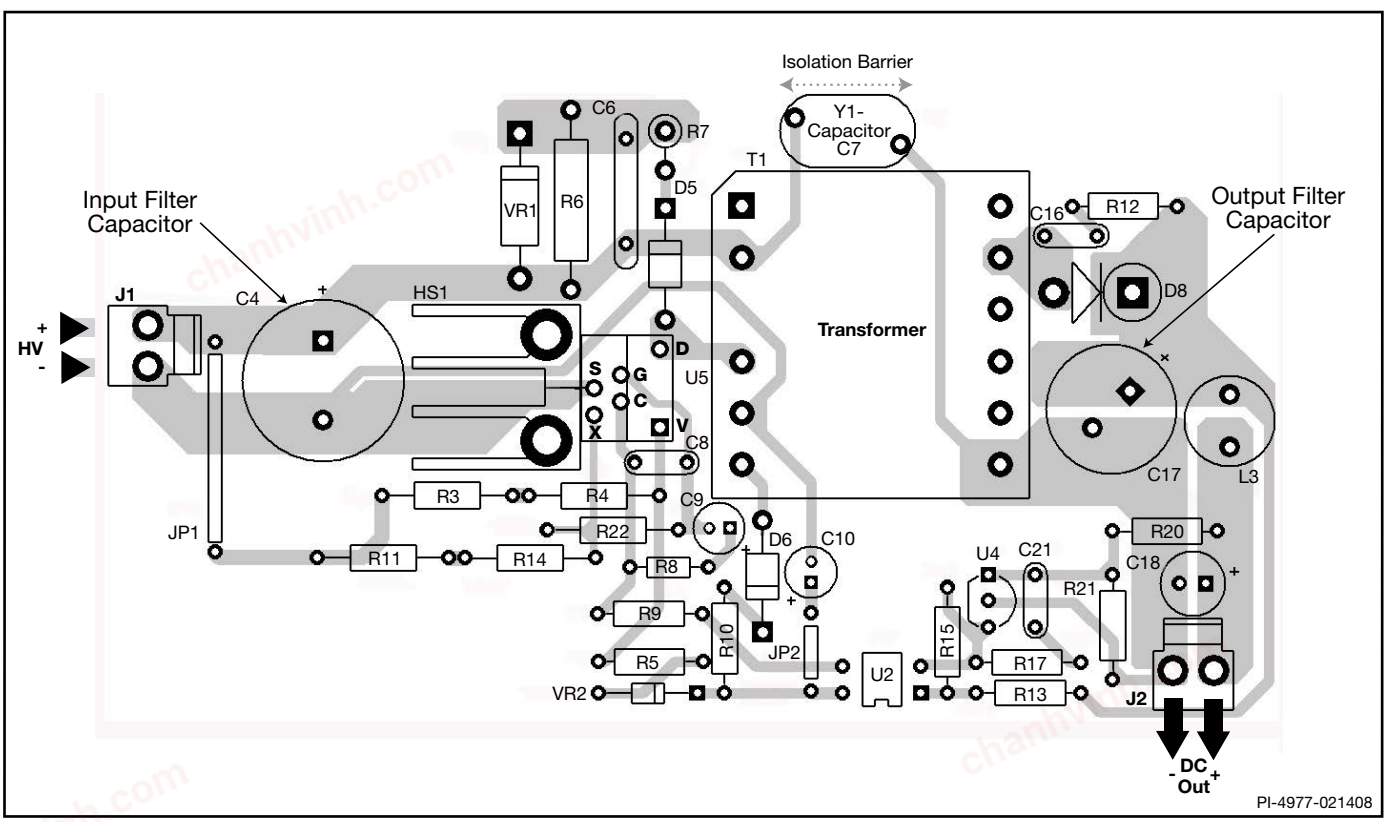


Figure 49. Layout Considerations for TOPSwitch-HX Using TOP259-261 Y Package.

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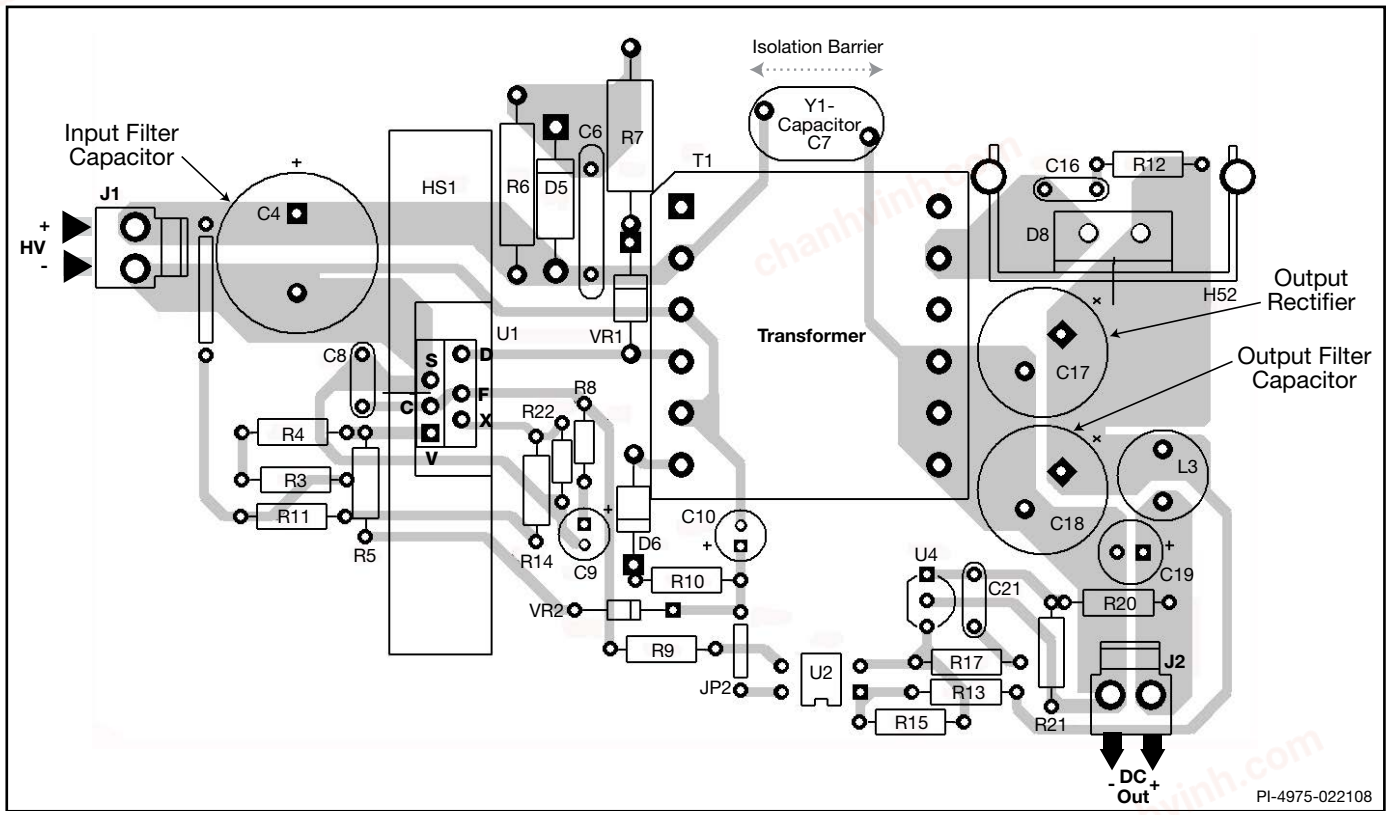


Figure 50a. Layout Considerations for TOPSwitch-HX Using E Package and Operating at 66 kHz.

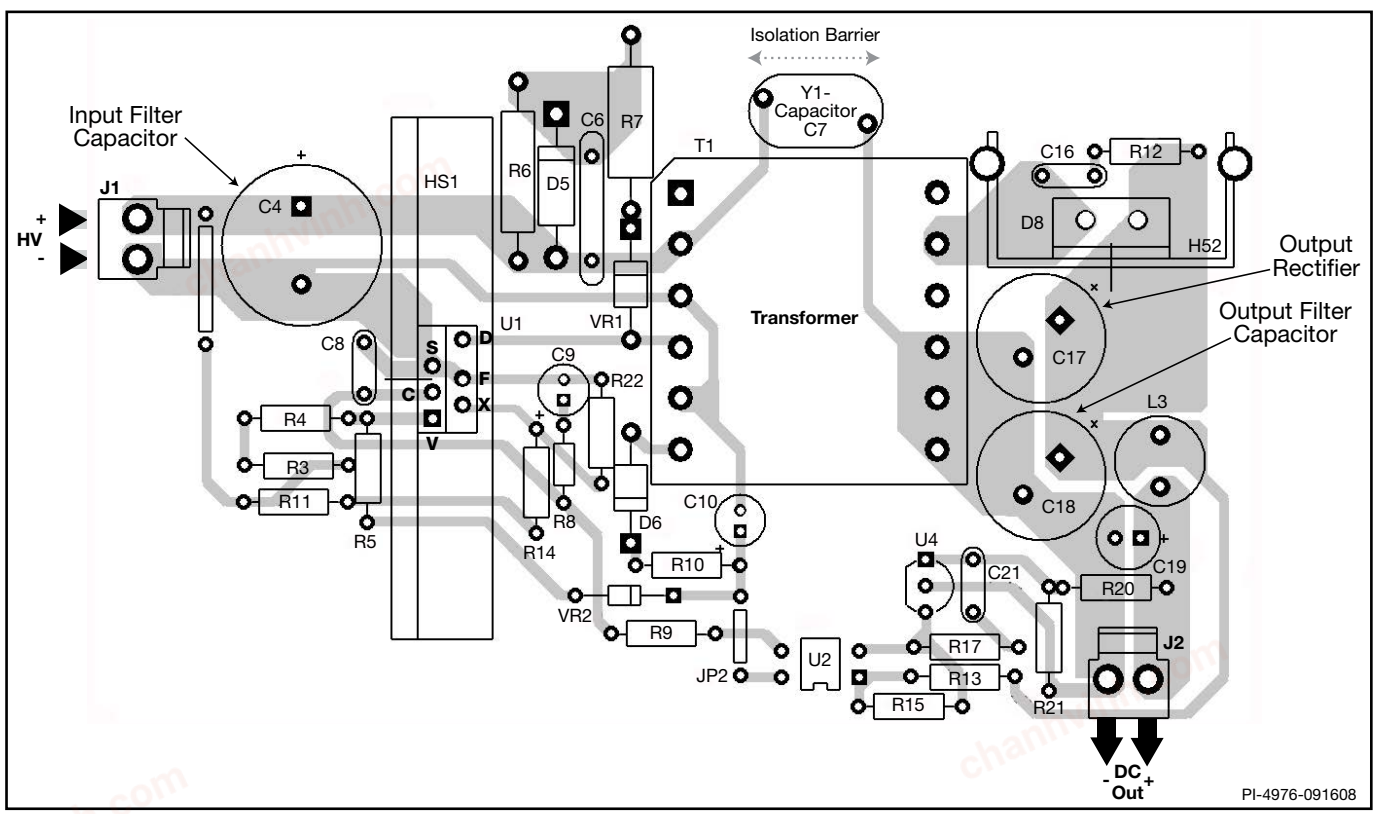


Figure 50b. Layout Considerations for TOPSwitch-HX Using E Package and Operating at 132 kHz.

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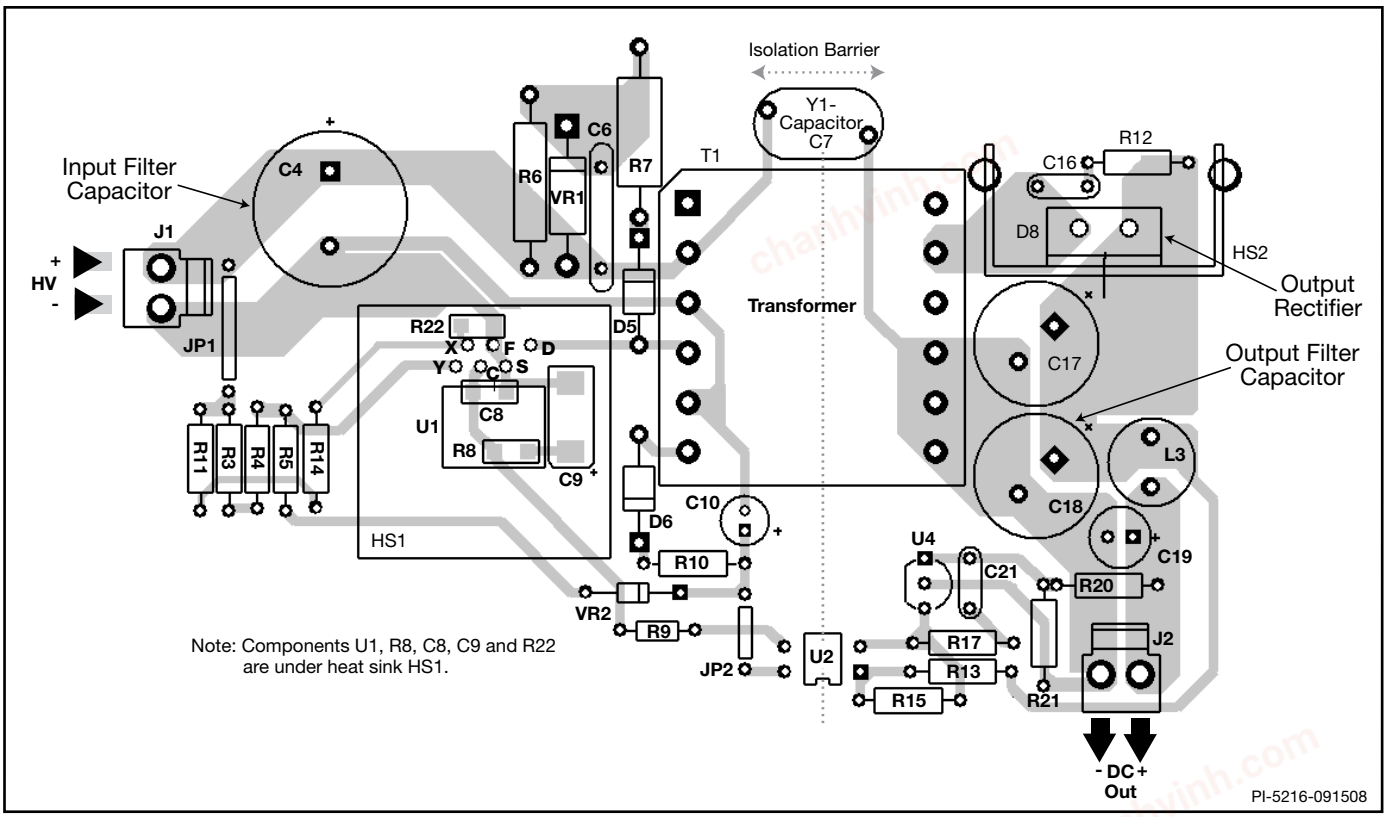


Figure 50c. Layout Considerations for TOPSwitch-HX Using L Package and Operating at 132 kHz.

Quick Design Checklist

In order to reduce the no-load input power of TOPSwitch-HX designs, the V-pin (or M-pin for P Package) operates at very low current. This requires careful layout considerations when designing the PCB to avoid noise coupling. Traces and components connected to the V-pin should not be adjacent to any traces carrying switching currents. These include the drain, clamp network, bias winding return or power traces from other converters. If the line sensing features are used, then the sense resistors must be placed within 10 mm of the V-pin to minimize the V pin node area. The DC bus should then be routed to the line sense resistors. Note that external capacitance must not be connected to the V-pin as this may cause misoperation of the V pin related functions.

As with any power supply design, all TOPSwitch-HX designs should be verified on the bench to make sure that components specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak V_{DS} does not exceed 675 V at highest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level just before the power supply goes into auto-restart (loss of regulation).
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. TOPSwitch-HX has a leading edge blanking time of 220 ns to prevent premature termination of the ON-cycle. Verify that the leading edge current spike is below the allowed current limit envelope (see Figure 53) for the drain current waveform at the end of the 220 ns blanking period.
3. Thermal check – At maximum output power, both minimum and maximum voltage and ambient temperature; verify that temperature specifications are not exceeded for TOPSwitch-HX, transformer, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation of the $R_{DS(ON)}$ of TOPSwitch-HX, as specified in the data sheet. The margin required can either be calculated from the values in the parameter table or it can be accounted for by connecting an external resistance in series with the DRAIN pin and attached to the same heat sink, having a resistance value that is equal to the difference between the measured $R_{DS(ON)}$ of the device under test and the worst case maximum specification.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations website: www.power.com

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Absolute Maximum Ratings[2]

DRAIN Peak Voltage ..... -0.3 V to 700 V
DRAIN Peak Current: TOP252 ..... 0.68 A
DRAIN Peak Current: TOP253 ..... 1.37 A
DRAIN Peak Current: TOP254 ..... 2.08 A
DRAIN Peak Current: TOP255 ..... 2.72 A
DRAIN Peak Current: TOP256 ..... 4.08 A
DRAIN Peak Current: TOP257 ..... 5.44 A
DRAIN Peak Current: TOP258 ..... 6.88 A
DRAIN Peak Current: TOP259 ..... 7.73 A
DRAIN Peak Current: TOP260 ..... 9.00 A
DRAIN Peak Current: TOP261 ..... 11.10 A
DRAIN Peak Current: TOP262 ..... 11.10 A
CONTROL Voltage ..... -0.3 V to 9 V
CONTROL Current ..... 100 mA
VOLTAGE MONITOR Pin Voltage ..... -0.3 V to 9 V
CURRENT LIMIT Pin Voltage ..... -0.3 V to 4.5 V
MULTI-FUNCTION Pin Voltage ..... -0.3 V to 9 V
FREQUENCY Pin Voltage ..... -0.3 V to 9 V
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature ..... -40 °C to 150 °C
Lead Temperature[1] ..... 260 °C

Notes:
1. 1/16 in. from case for 5 seconds.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

Thermal Resistance

Thermal Resistance: Y Package:
(θ_{JA}) ..... 80 °C/W[1]
(θ_{JC}) ..... 2 °C/W[2]
P, G and M Packages:
(θ_{JA}) ..... 70 °C/W[3]; 60 °C/W[4]
(θ_{JC}) ..... 11 °C/W[5]
E/L Package:
(θ_{JA}) ..... 105 °C/W[1]
(θ_{JC}) ..... 2 °C/W[2]

Notes:
1. Free standing with no heat sink.
2. Measured at the back surface of tab.
3. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
4. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.
5. Measured on the SOURCE pin close to plastic interface.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 54 (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Switching Frequency in Full Frequency Mode (average)	f_{OSC}	T_J = 25 °C	FREQUENCY Pin Connected to SOURCE TOP254-258Y TOP255-262L TOP252-262E	119	132	145	kHz
			FREQUENCY Pin Connected to CONTROL TOP254-258Y TOP255-262L TOP252-262E	59.4	66	72.6	
			TOP252-258P/G/M TOP259-261Y	59.4	66	72.6	
Frequency Jitter Deviation	Δf		132 kHz Operation		±5		kHz
			66 kHz Operation		±2.5		
Frequency Jitter Modulation Rate	f_M				250		Hz
Maximum Duty Cycle	DC_{MAX}	$I_C = I_{CD1}$	$I_V \le I_{V(DC)}$ or $I_M \le I_{M(DC)}$ or V_V, V_M = 0 V	75	78	83	%
			I_V or I_M = 95 µA	30			
Soft-Start Time	t_{SOFT}	T_J = 25 °C			17		ms
PWM Gain	DC_{reg}	T_J = 25 °C	TOP252-255	-31	-25	-20	%/mA
			TOP256-258	-27	-22	-17	
			TOP259-262	-25	-20	-15	
PWM Gain Temperature Drift		See Note A			-0.01		%/mA/°C
External Bias Current	I_B	66 kHz Operation	TOP252-255	0.9	1.5	2.1	mA
			TOP256-258	1.0	1.6	2.2	
			TOP259-262	1.1	1.7	2.4	

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
External Bias Current	I_B	132 kHz Operation	TOP252-255	1.0	1.6	2.2	mA
			TOP256-258	1.3	1.9	2.5	
			TOP259-262	1.6	2.2	2.9	
CONTROL Current at 0% Duty Cycle	$I_{C(OFF)}$	66 kHz Operation	TOP252-255		4.4	5.8	mA
			TOP256-258		4.7	6.1	
			TOP259-262		5.1	6.5	
		132 kHz Operation	TOP252-255		4.6	6.0	
			TOP256-258		5.1	6.5	
			TOP259-262		6.0	7.4	
Dynamic Impedance	Z_C	I_C = 4 mA; T_J = 25 °C, See Figure 52		10	18	22	Ω
Dynamic Impedance Temperature Drift					0.18		%/°C
CONTROL Pin Internal Filter Pole					7		kHz
Upper Peak Current to Set Current Limit Ratio	$k_{PS(UPPER)}$	T_J = 25 °C See Note B		50	55	60	%
Lower Peak Current to Set Current Limit Ratio	$k_{PS(LOWER)}$	T_J = 25 °C See Note B			25		%
Multi-Cycle-Modulation Switching Frequency	$f_{MCM(MIN)}$	T_J = 25 °C			30		kHz
Minimum Multi-Cycle-Modulation On Period	$T_{MCM(MIN)}$	T_J = 25 °C			135		µs
Shutdown/Auto-Restart							
Control Pin Charging Current	$I_{C(CH)}$	T_J = 25 °C	V_C = 0 V	-5.0	-3.5	-1.0	mA
			V_C = 5 V	-3.0	-1.8	-0.6	
Charging Current Temperature Drift		See Note A			0.5		%/°C
Auto-Restart Upper Threshold Voltage	$V_{C(AR)U}$				5.8		V
Auto-Restart Lower Threshold Voltage	$V_{C(AR)L}$			4.5	4.8	5.1	V
Multi-Function (M), Voltage Monitor (V) and External Current Limit (X) Inputs							
Auto-Restart Hysteresis Voltage	$V_{C(AR)hyst}$			0.8	1.0		V
Auto-Restart Duty Cycle	$DC_{(AR)}$				2	4	%
Auto-Restart Frequency	$f_{(AR)}$				0.5		Hz
Line Undervoltage Threshold Current and Hysteresis (M or V Pin)	I_{UV}	T_J = 25 °C	Threshold	22	25	27	µA
			Hysteresis		14		µA
Line Overvoltage Threshold Current and Hysteresis (M or V Pin)	I_{OV}	T_J = 25 °C	Threshold	107	112	117	µA
			Hysteresis		4		µA

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Multi-Function (M), Voltage Monitor (V) and External Current Limit (X) Inputs							
Output Overvoltage Latching Shutdown Threshold Current	$I_{OV(LS)}$	T_J = 25 °C		269	336	403	µA
V or M Pin Reset Voltage	$V_{V(TH)}$ or $V_{M(TH)}$	T_J = 25 °C		0.8	1.0	1.6	V
Remote ON/OFF Negative Threshold Current and Hysteresis (M or X Pin)	$I_{REM (N)}$	T_J = 25 °C	Threshold	-35	-27	-20	µA
			Hysteresis		5		
V or M Pin Short Circuit Current	$I_{V(SC)}$ or $I_{M(SC)}$	T_J = 25 °C	V_V, V_M = V_C	300	400	500	µA
X or M Pin Short Circuit Current	$I_{X(SC)}$ or $I_{M(SC)}$	V_X, V_M = 0 V	Normal Mode	-260	-200	-140	µA
			Auto-Restart Mode	-95	-75	-55	
V or M Pin Voltage (Positive Current)	V_V or V_M		I_V or I_M = I_{UV}	2.10	2.8	3.20	V
		I_V or I_M = I_{OV}	TOP252-TOP257	2.79	3.0	3.21	
			TOP258-TOP262	2.83	3.0	3.25	
V or M Pin Voltage Hysteresis (Positive Current)	$V_{V(hyst)}$ or $V_{M(hyst)}$		I_V or I_M = I_{OV}	0.2	0.5		V
X or M Pin Voltage (Negative Current)	V_X or V_M		I_X or I_M = -50 µA	1.23	1.30	1.37	V
			I_X or I_M = -150 µA	1.15	1.22	1.29	
Maximum Duty Cycle Reduction Onset Threshold Current	$I_{V(DC)}$ or $I_{M(DC)}$	$I_C \geq I_B$, T_J = 25 °C		18.9	22.0	24.2	µA
Maximum Duty Cycle Reduction Slope		T_J = 25 °C	$I_{V(DC)} < I_V$ <48 µA or $I_{M(DC)} < I_M$ <48 µA		-1.0		%/µA
			I_V or I_M ≥48 µA		-0.25		
Remote OFF DRAIN Supply Current	$I_{D(RMT)}$	V_{DRAIN} = 150 V	X, V or M Pin Floating		0.6	1.0	mA
			V or M Pin Shorted to CONTROL		1.0	1.6	
Remote ON Delay	$t_{R(ON)}$	From Remote ON to Drain Turn-On See Note B	66 kHz		3.0		µs
			132 kHz		1.5		
Remote OFF Setup Time	$t_{R(OFF)}$	Minimum Time Before Drain Turn-On to Disable Cycle See Note B	66 kHz		3.0		µs
			132 kHz		1.5		
Frequency Input							
FREQUENCY Pin Threshold Voltage	V_F	See Note B			2.9		V
FREQUENCY Pin Input Current	I_F	T_J = 25 °C	V_F = V_C	10	55	90	µA

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Self Protection Current Limit (See Note C)	I_{LIMIT}	TOP252PN/GN/MN T_J = 25 °C	di/dt = 45 mA/µs	0.400	0.43	0.460	A
		TOP252EN T_J = 25 °C	di/dt = 90 mA/µs	0.400	0.43	0.460	
		TOP253PN/GN T_J = 25 °C	di/dt = 80 mA/µs	0.697	0.75	0.803	
		TOP253MN T_J = 25 °C	di/dt = 90 mA/µs	0.790	0.85	0.910	
		TOP253EN T_J = 25 °C	di/dt = 180 mA/µs	0.790	0.85	0.910	
		TOP254PN/GN T_J = 25 °C	di/dt = 105 mA/µs	0.93	1.00	1.07	
		TOP254MN T_J = 25 °C	di/dt = 135 mA/µs	1.209	1.30	1.391	
		TOP254YN/EN T_J = 25 °C	di/dt = 270 mA/µs	1.209	1.30	1.391	
		TOP255PN/GN T_J = 25 °C	di/dt = 120 mA/µs	1.069	1.15	1.231	
		TOP255MN T_J = 25 °C	di/dt = 175 mA/µs	1.581	1.70	1.819	
		TOP255LN T_J = 25 °C	di/dt = 350 mA/µs	1.581	1.70	1.819	
		TOP255YN/EN T_J = 25 °C	di/dt = 350 mA/µs	1.581	1.70	1.819	
		TOP256PN/GN T_J = 25 °C	di/dt = 140 mA/µs	1.255	1.35	1.445	
		TOP256MN T_J = 25 °C	di/dt = 220 mA/µs	1.953	2.10	2.247	
		TOP256LN T_J = 25 °C	di/dt = 435 mA/µs	1.953	2.10	2.247	
		TOP256YN/EN T_J = 25 °C	di/dt = 530 mA/µs	2.371	2.55	2.729	
		TOP257PN/GN T_J = 25 °C	di/dt = 155 mA/µs	1.395	1.50	1.605	
		TOP257MN T_J = 25 °C	di/dt = 265 mA/µs	2.371	2.55	2.729	
		TOP257LN T_J = 25 °C	di/dt = 530 mA/µs	2.371	2.55	2.729	
		TOP257YN/EN T_J = 25 °C	di/dt = 705 mA/µs	3.162	3.40	3.638	
		TOP258PN/GN T_J = 25 °C	di/dt = 170 mA/µs	1.534	1.65	1.766	
		TOP258MN T_J = 25 °C	di/dt = 310 mA/µs	2.790	3.00	3.210	
		TOP258LN T_J = 25 °C	di/dt = 620 mA/µs	2.790	3.00	3.210	

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Self Protection Current Limit (See Note C)	I_{LIMIT}	TOP258YN/EN T_J = 25 °C	di/dt = 890 mA/µs	3.999	4.30	4.601	A
		TOP259LN T_J = 25 °C	di/dt = 720 mA/µs	3.236	3.48	3.724	
		TOP259YN/EN T_J = 25 °C	di/dt = 1065 mA/µs	4.790	5.15	5.511	
		TOP260LN T_J = 25 °C	di/dt = 870 mA/µs	3.906	4.20	4.494	
		TOP260YN/EN T_J = 25 °C	di/dt = 1240 mA/µs	5.580	6.00	6.420	
		TOP261LN T_J = 25 °C	di/dt = 1065 mA/µs	4.808	5.17	5.532	
		TOP261YN/EN T_J = 25 °C	di/dt = 1530 mA/µs	6.882	7.40	7.918	
		TOP262LN T_J = 25 °C	di/dt = 1065 mA/µs	4.808	5.17	5.532	
		TOP262EN T_J = 25 °C	di/dt = 1530 mA/µs	6.882	7.40	7.918	
Initial Current Limit	I_{INIT}	See Note B		0.70 × $I_{LIMIT(MIN)}$			A
Power Coefficient	P_{COEFF}	T_J = 25 °C, See Note D	I_X or I_M ≤ - 165 µA	0.9 × I^2f	I^2f	1.2 × I^2f	A^2kHz
			I_X or I_M ≤ - 117 µA	0.9 × I^2f	I^2f	1.2 × I^2f	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C, See Figure 53			220		ns
Current Limit Delay	$t_{IL(D)}$				100		ns
Thermal Shutdown Temperature				135	142	150	°C
Thermal Shutdown Hysteresis					75		°C
Power-Up Reset Threshold Voltage	$V_{C(RESET)}$	Figure 54 (S1 Open Condition)		1.75	3.0	4.25	V
Output							
ON-State Resistance	$R_{DS(ON)}$	TOP252 I_D = 50 mA	T_J = 25 °C		19.1	22.00	Ω
			T_J = 100 °C		28.8	33.40	
		TOP253 I_D = 100 mA	T_J = 25 °C		8.8	10.10	
			T_J = 100 °C		13.1	15.20	
		TOP254 I_D = 150 mA	T_J = 25 °C		5.4	6.25	
			T_J = 100 °C		8.35	9.70	
		TOP255 I_D = 200 mA	T_J = 25 °C		4.1	4.70	
			T_J = 100 °C		6.3	7.30	
		TOP256 I_D = 300 mA	T_J = 25 °C		2.8	3.20	
			T_J = 100 °C		4.1	4.75	
		TOP257 I_D = 400 mA	T_J = 25 °C		2.0	2.30	
			T_J = 100 °C		3.1	3.60	
		TOP258 I_D = 500 mA	T_J = 25 °C		1.7	1.95	
			T_J = 100 °C		2.5	2.90	

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)			Min	Typ	Max	Units
Output (cont.)								
ON-State Resistance	$R_{DS(ON)}$	TOP259 I_D = 600 mA	T_J = 25 °C			1.45	1.70	Ω
			T_J = 100 °C			2.25	2.60	
		TOP260 I_D = 700 mA	T_J = 25 °C			1.20	1.40	
			T_J = 100 °C			1.80	2.10	
		TOP261 I_D = 800 mA	T_J = 25 °C			1.05	1.20	
			T_J = 100 °C			1.55	1.80	
		TOP262 I_D = 900 mA	T_J = 25 °C			0.90	1.05	
			T_J = 100 °C			1.35	1.55	
DRAIN Supply Voltage		T_J ≤ 85 °C, See Note E			18			V
					36			
OFF-State Drain Leakage Current	I_{DSS}	V_V, V_M = Floating, I_C = 4 mA, V_{DS} = 560 V, T_J = 125 °C					470	µA
Breakdown Voltage	BV_{DSS}	V_V, V_M = Floating, I_C = 4 mA, T_J = 25 °C See Note F			700			V
Rise Time	t_R	Measured in a Typical Flyback Converter Application				100		ns
Fall Time	t_F					50		ns
Supply Voltage Characteristics								
Control Supply/ Discharge Current	I_{CD1}	Output MOSFET Enabled V_X, V_V, V_M = 0 V	66 kHz Operation	TOP252-255	0.6	1.2	2.0	mA
				TOP256-258	0.9	1.4	2.3	
				TOP259-262	1.1	1.6	2.5	
			132 kHz Operation	TOP252-255	0.8	1.3	2.2	
				TOP256-258	1.1	1.6	2.5	
				TOP259-262	1.5	2.2	2.9	
	I_{CD2}	Output MOSFET Disabled V_X, V_V, V_M = 0 V			0.3	0.6	1.3	

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. Guaranteed by characterization. Not tested in production.

C. For externally adjusted current limit values, please refer to Figures 55a and 55b (Current Limit vs. External Current Limit Resistance) in the Typical Performance Characteristics section. The tolerance specified is only valid at full current limit.

D. I^2f calculation is based on typical values of I_{LIMIT} and f_{OSC}, i.e. $I_{LIMIT(TYP)}{}^2 \times f_{OSC}$, where f_{OSC} = 66 kHz or 132 kHz depending on package / F pin connection. See f_{OSC} specification for detail.

E. The TOPSwitch-HX will start up at 18 V_{DC} drain voltage. The capacitance of electrolytic capacitors drops significantly at temperatures below 0 °C. For reliable start up at 18 V in sub zero temperatures, designers must ensure that circuit capacitors meet recommended capacitance values.

F. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

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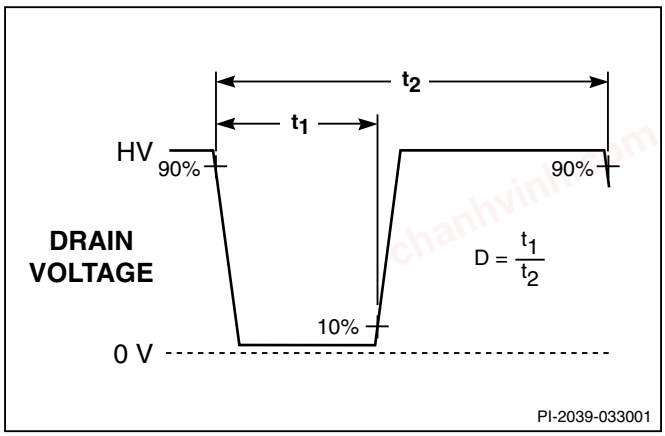


Figure 51. Duty Cycle Measurement.

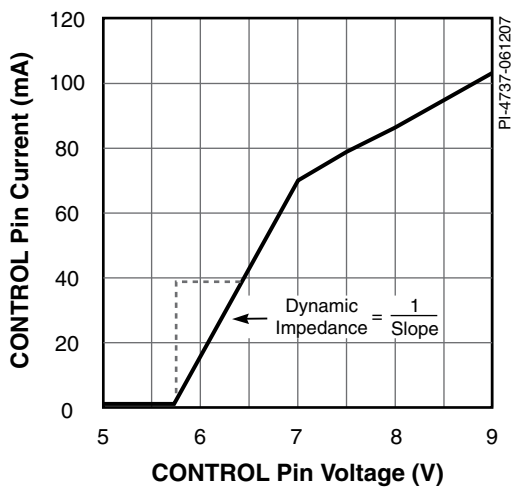


Figure 52. CONTROL Pin I-V Characteristic.

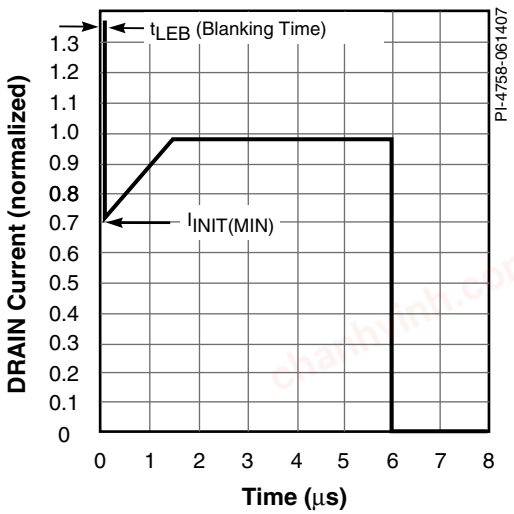
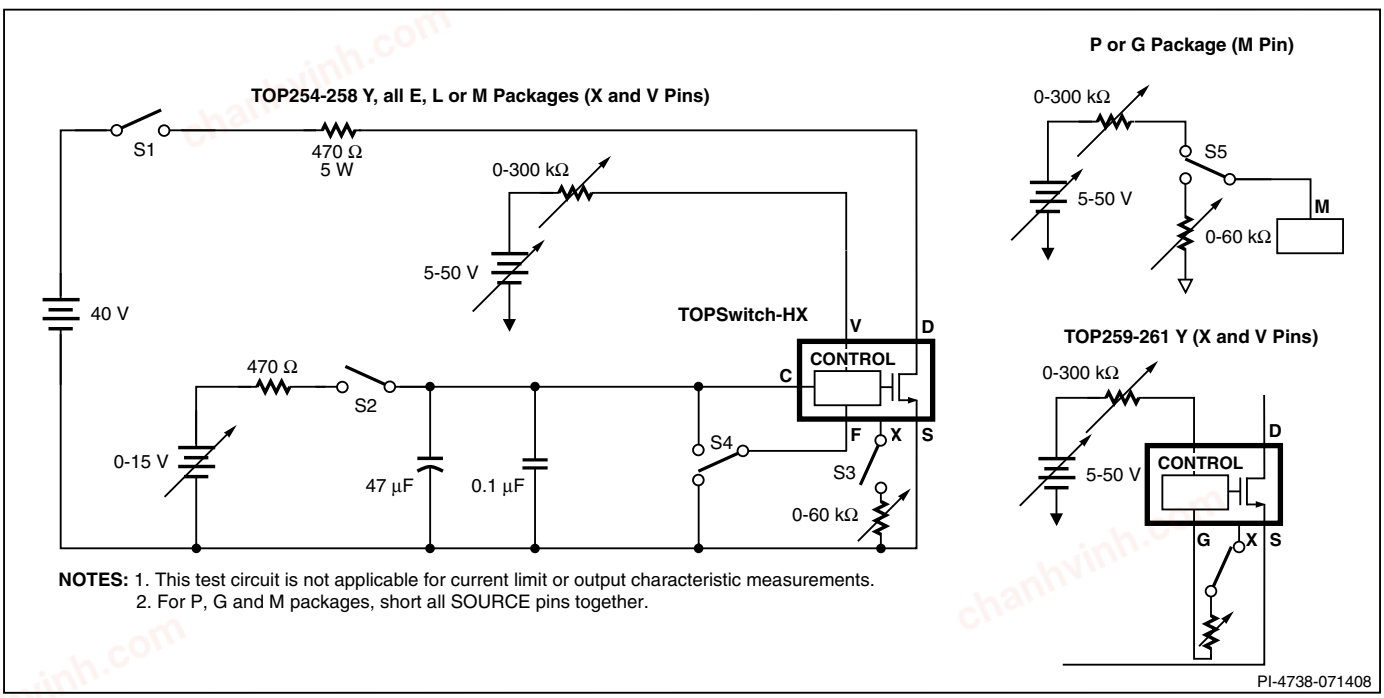


Figure 53. Drain Current Operating Envelope.



NOTES: 1. This test circuit is not applicable for current limit or output characteristic measurements.
2. For P, G and M packages, short all SOURCE pins together.

Figure 54. TOPSwitch-HX General Test Circuit.

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Typical Performance Characteristics

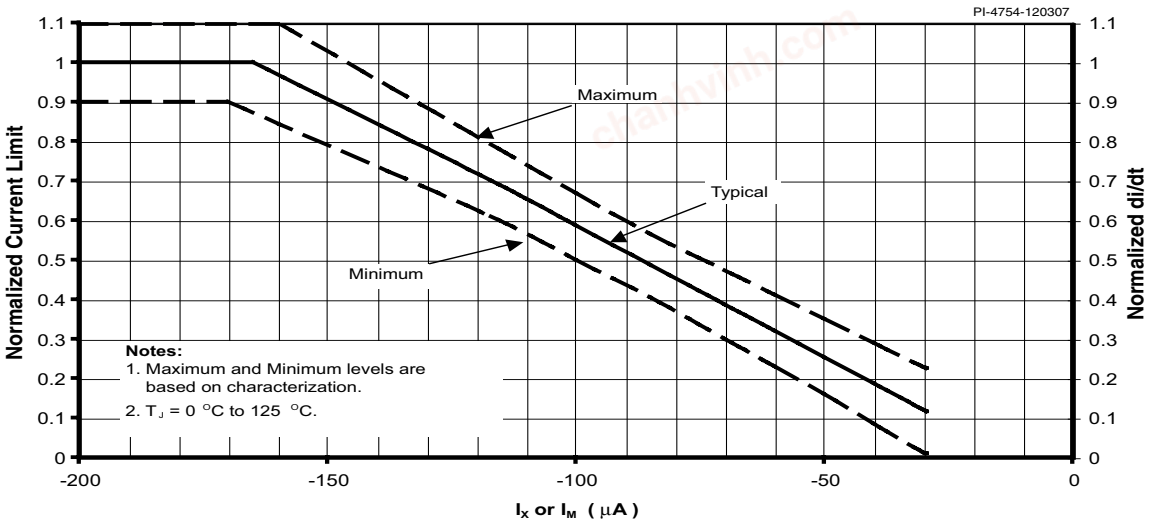


Figure 55a. Normalized Current Limit vs. X or M Pin Current.

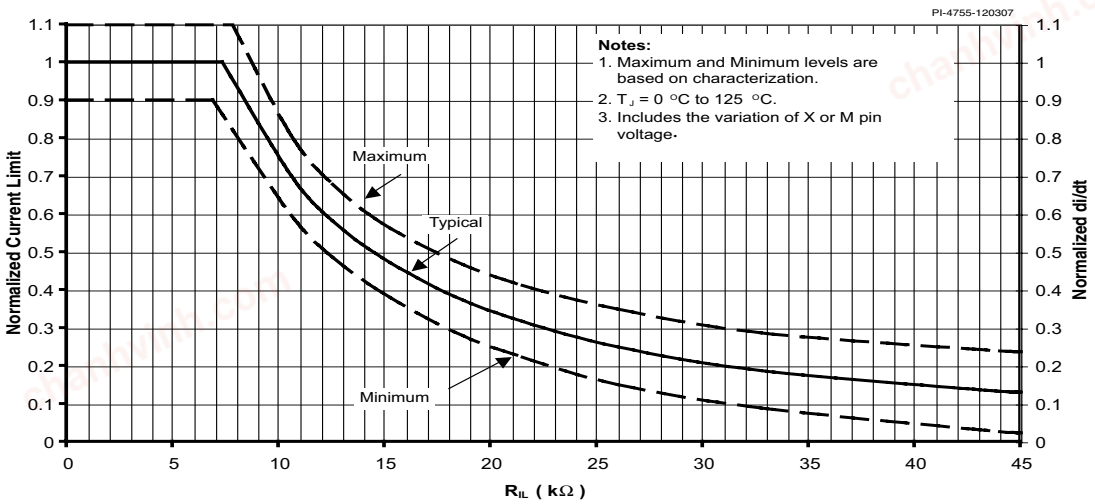


Figure 55b. Normalized Current Limit vs. External Current Limit Resistance.

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Typical Performance Characteristics (cont.)

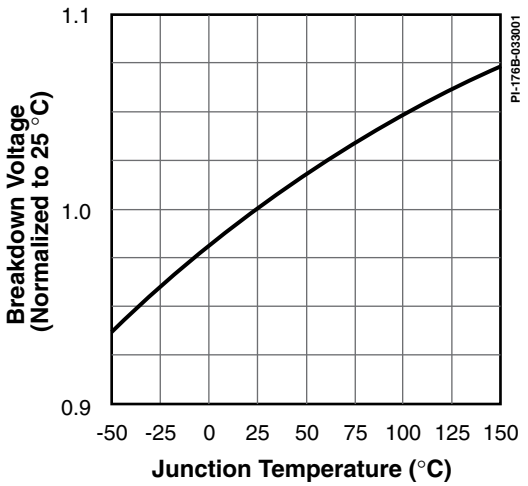


Figure 56. Breakdown Voltage vs. Temperature.

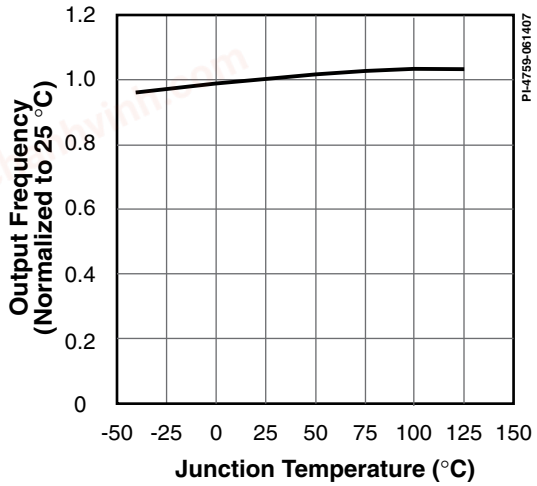


Figure 57. Frequency vs. Temperature.

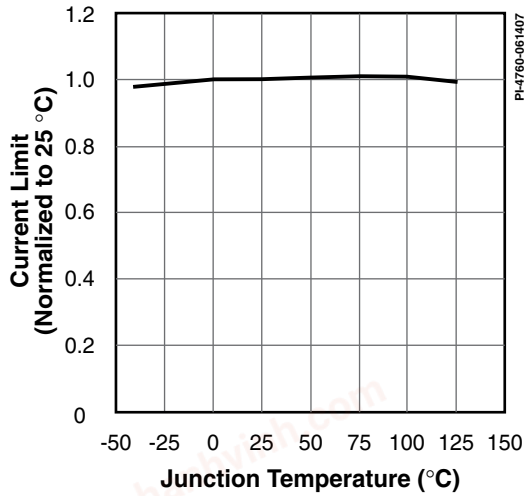


Figure 58. Internal Current Limit vs. Temperature.

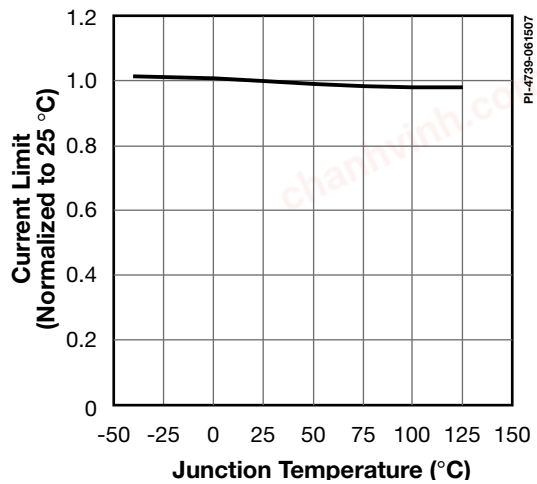


Figure 59. External Current Limit vs. Temperature with R_{IL} = 10.5 kΩ.

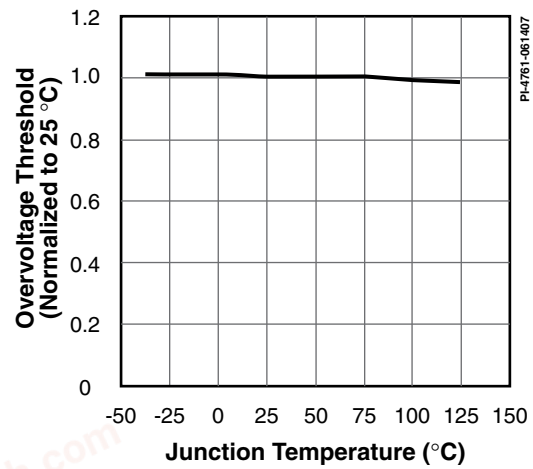


Figure 60. Overvoltage Threshold vs. Temperature.

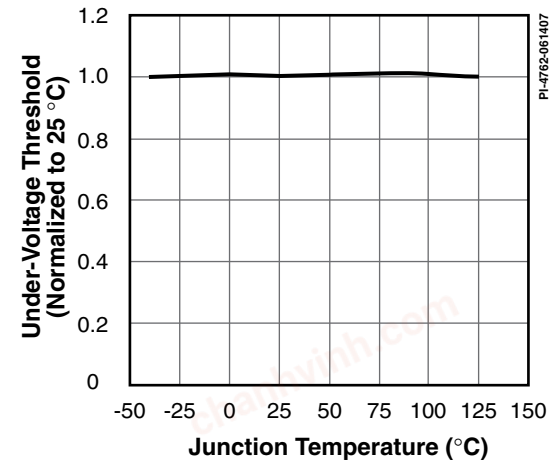


Figure 61. Undervoltage Threshold vs. Temperature.

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Typical Performance Characteristics (cont.)

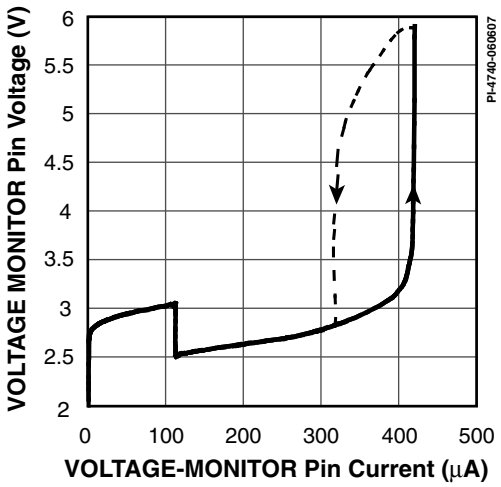


Figure 62a. VOLTAGE-MONITOR Pin vs. Current.

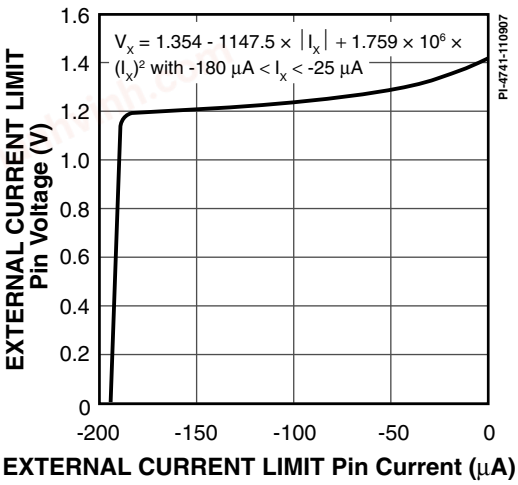


Figure 62b. EXTERNAL CURRENT LIMIT Pin Voltage vs. Current.

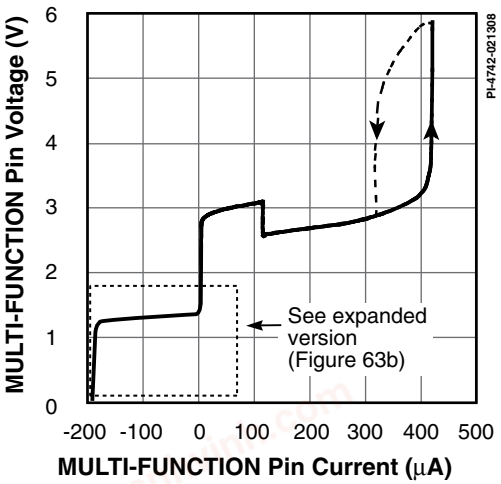


Figure 63a. MULTI-FUNCTION Pin Voltage vs. Current.

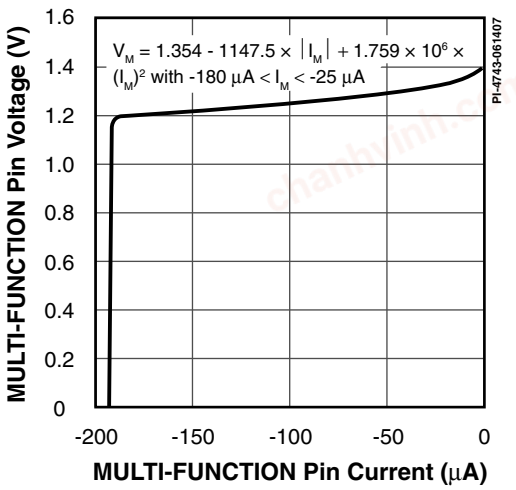


Figure 63b. MULTI-FUNCTION Pin Voltage vs. Current (Expanded).

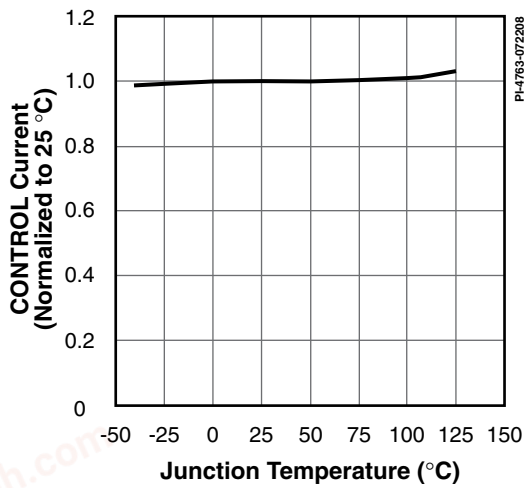


Figure 64. Control Current Out at 0% Duty Cycle vs. Temperature.

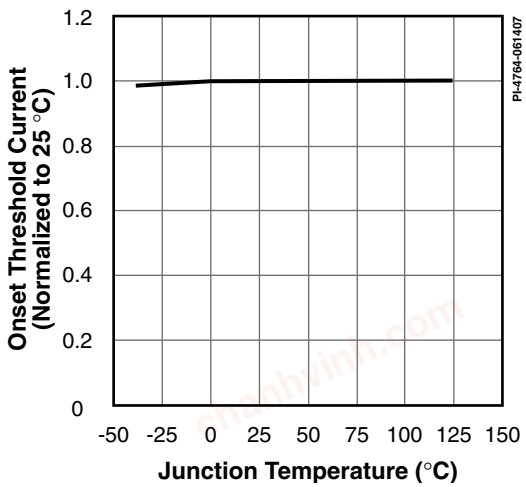


Figure 65. Maximum Duty Cycle Reduction Onset Threshold Current vs. Temperature.

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Typical Performance Characteristics (cont.)

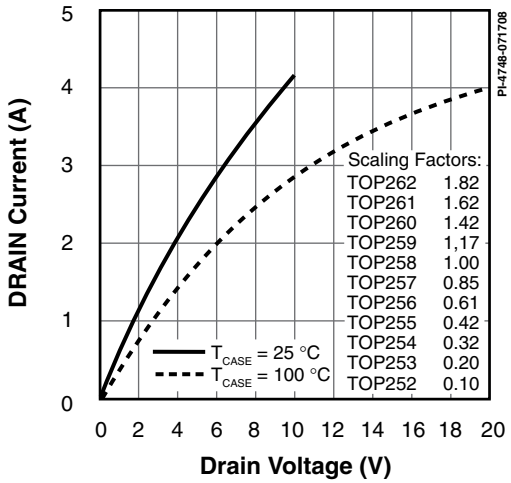


Figure 66. Output Characteristics.

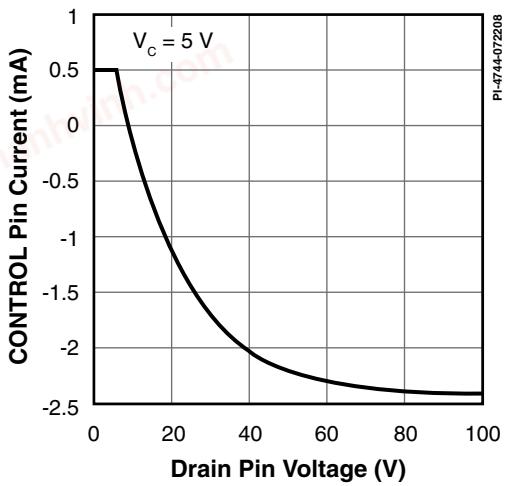


Figure 67. I_C vs. DRAIN Voltage.

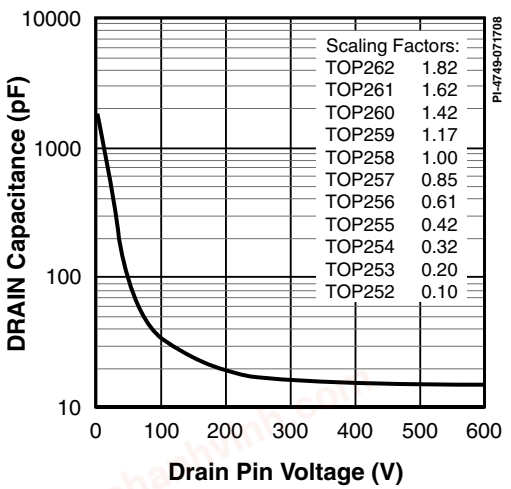


Figure 68. C_{OSS} vs. DRAIN Voltage.

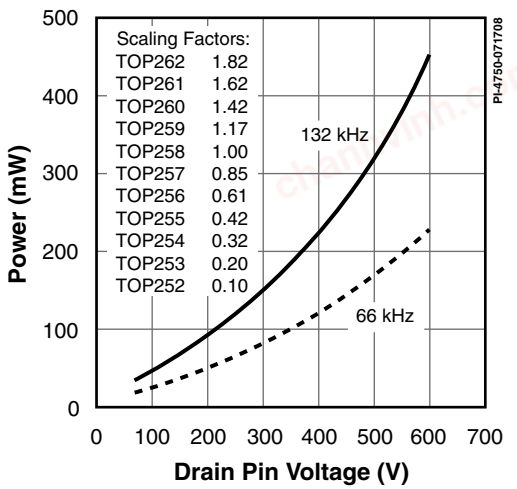


Figure 69. DRAIN Capacitance Power.

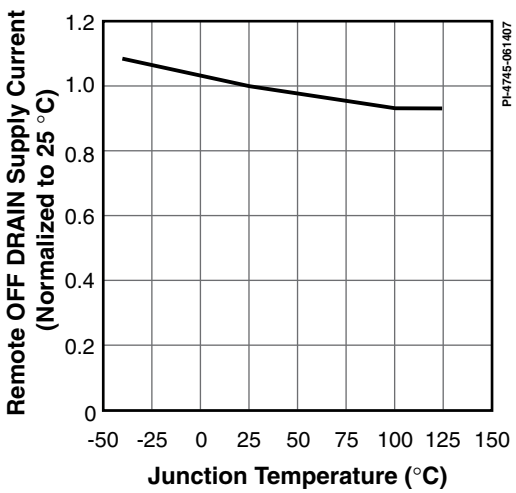
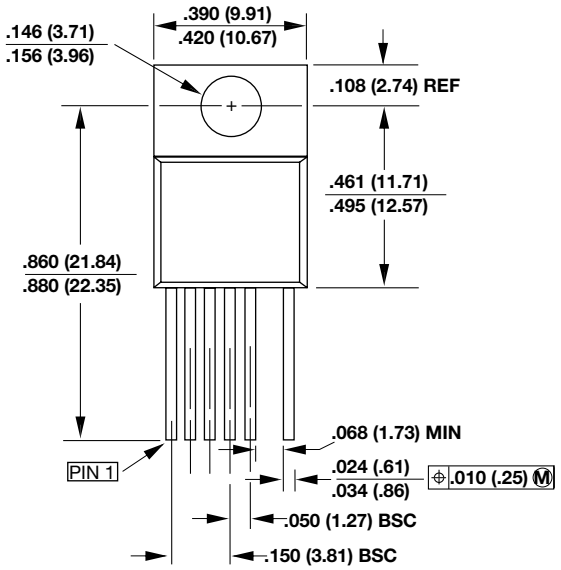
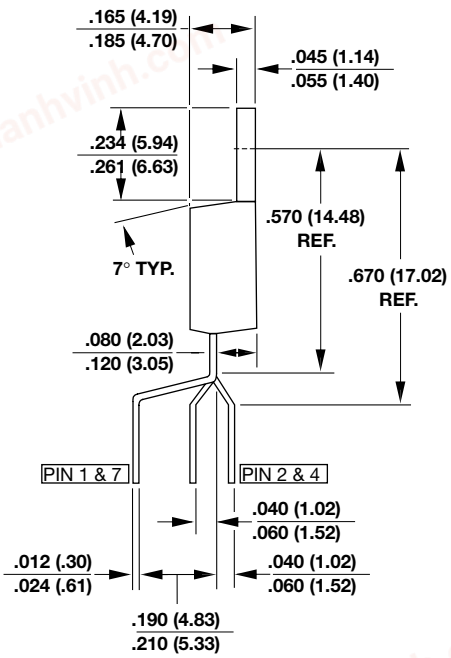


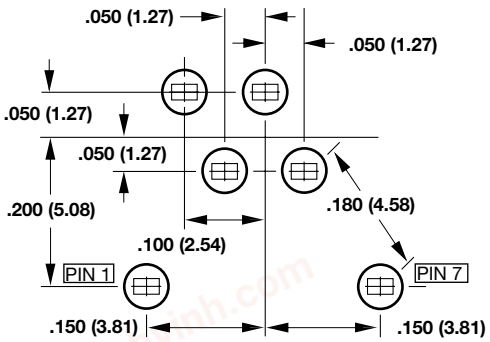
Figure 70. Remote OFF DRAIN Supply Current vs. Temperature.

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TO-220-7C (Y Package)







Y07C MOUNTING HOLE PATTERN

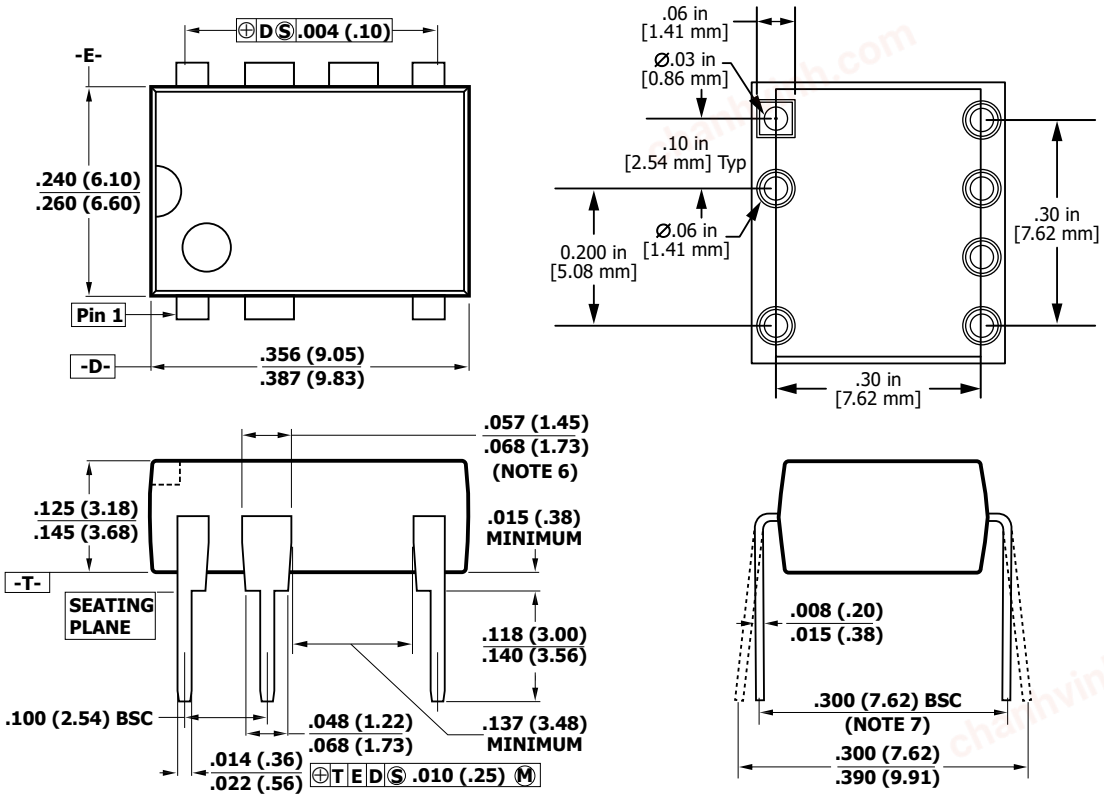
Notes:

1. Controlling dimensions are inches. Millimeter dimensions are shown in parentheses.
2. Pin numbers start with Pin 1, and continue from left to right when viewed from the front.
3. Dimensions do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15 mm) on any side.
4. Minimum metal to metal spacing at the package body for omitted pin locations is .068 in. (1.73 mm).
5. Position of terminals to be measured at a location .25 (6.35) below the package body.
6. All terminals are solder plated.

PI-2644-040110

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PDIP-8C (P Package)



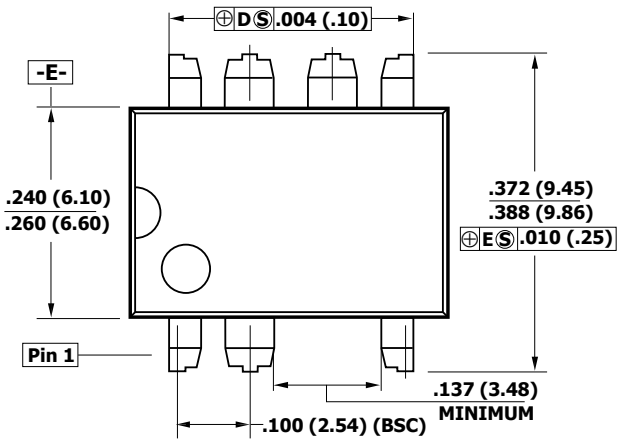
Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clock-wise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.

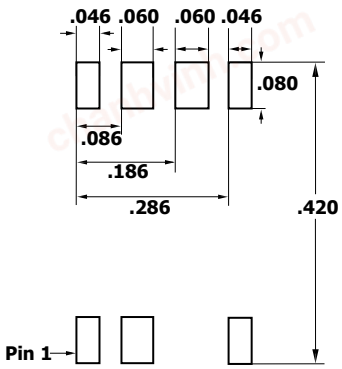
P08C

PI-3933b-092920

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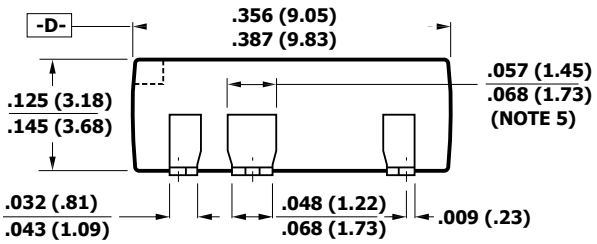
SMD-8C (G Package)

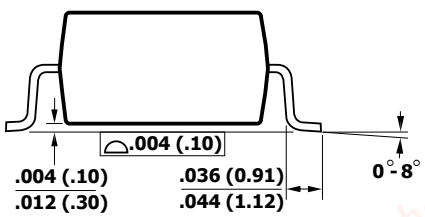




Solder Pad Dimensions

Notes:
1. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
2. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
3. Pin locations start with Pin 1, and continue counter-clock-wise to Pin 8 when viewed from the top. Pin 3 is omitted.
4. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
5. Lead width measured at package body.
6. D and E are referenced datums on the package body.

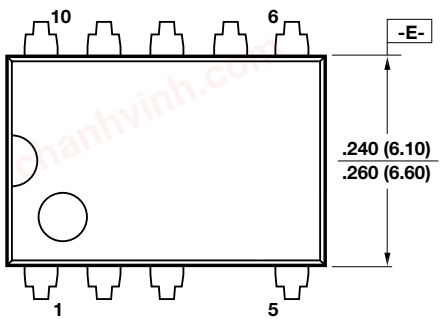




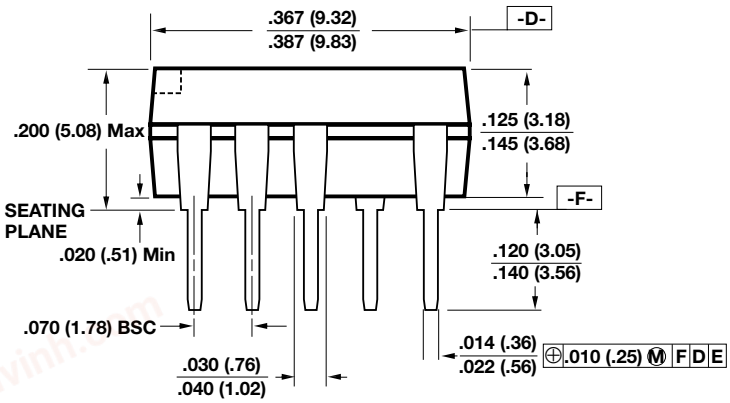
G08C

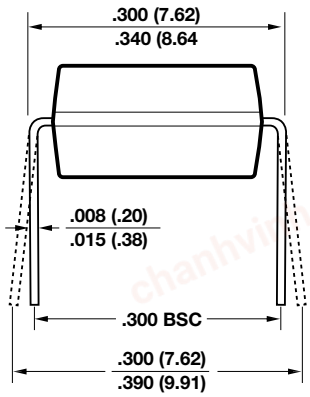
PI-4015b-072320

SDIP-10C (M Package)



Notes:
1. Package dimensions conform to JEDEC specification MS-019.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums.
5. Dimensioning and tolerancing conform to ASME Y14.5M-1994.



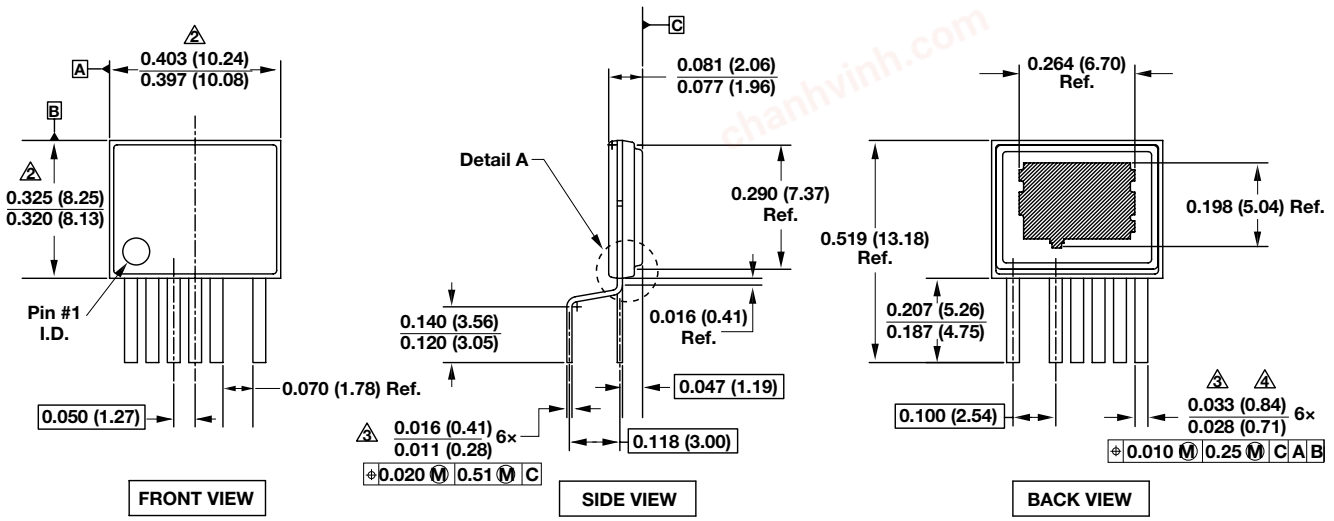


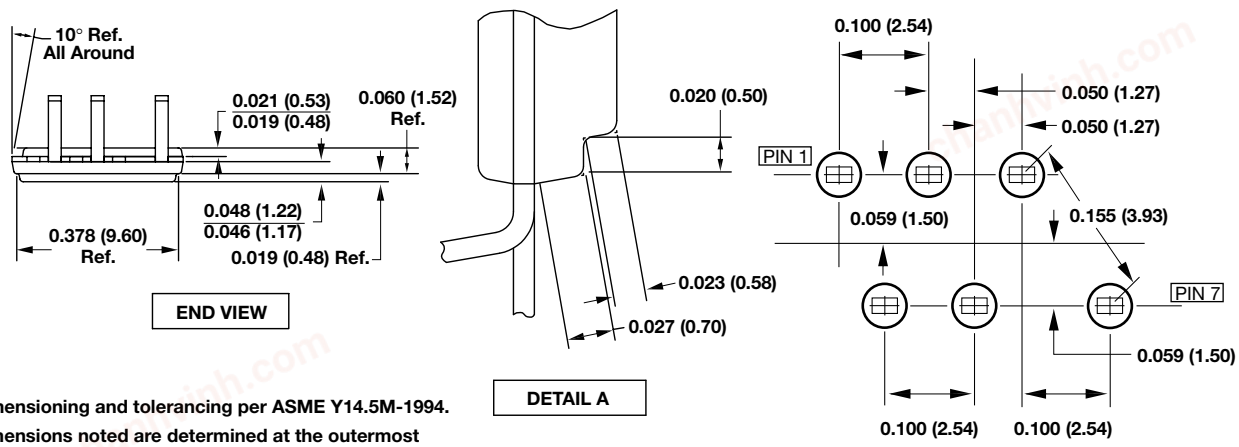
P10C

PI-4648-101507

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eSIP-7C (E Package)





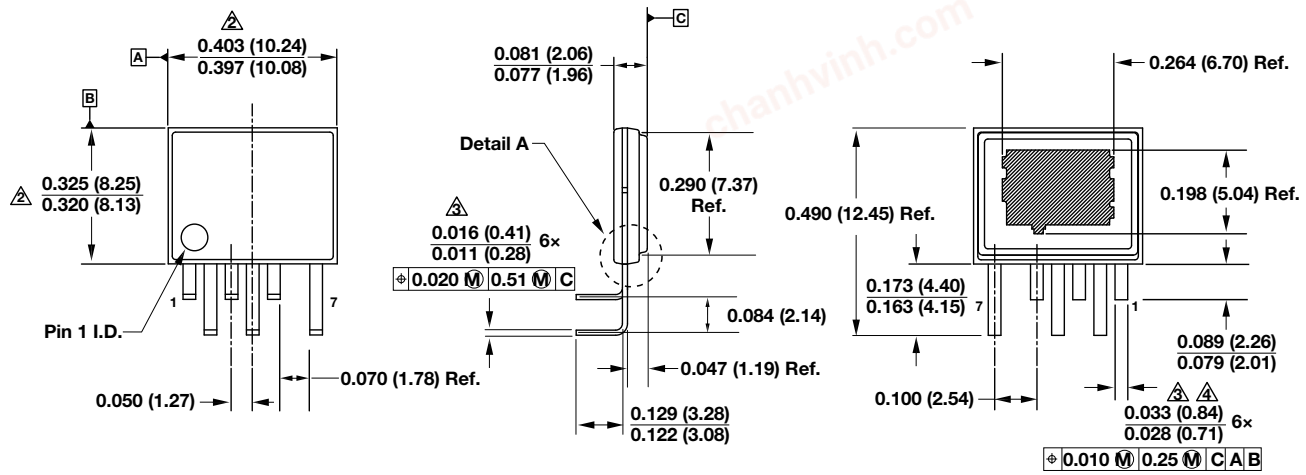
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-4917-061510

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eSIP-7F (L Package)



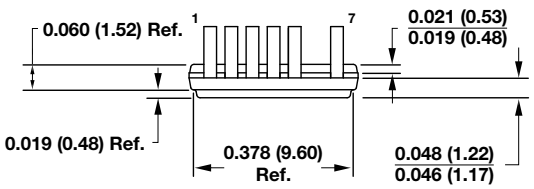
BOTTOM VIEW

Exposed pad hidden

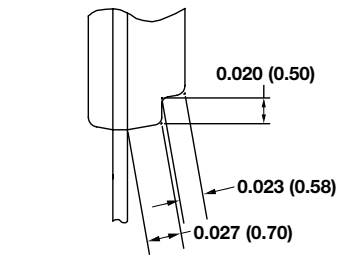
SIDE VIEW

TOP VIEW

Exposed pad up



END VIEW



DETAIL A (Not drawn to scale)

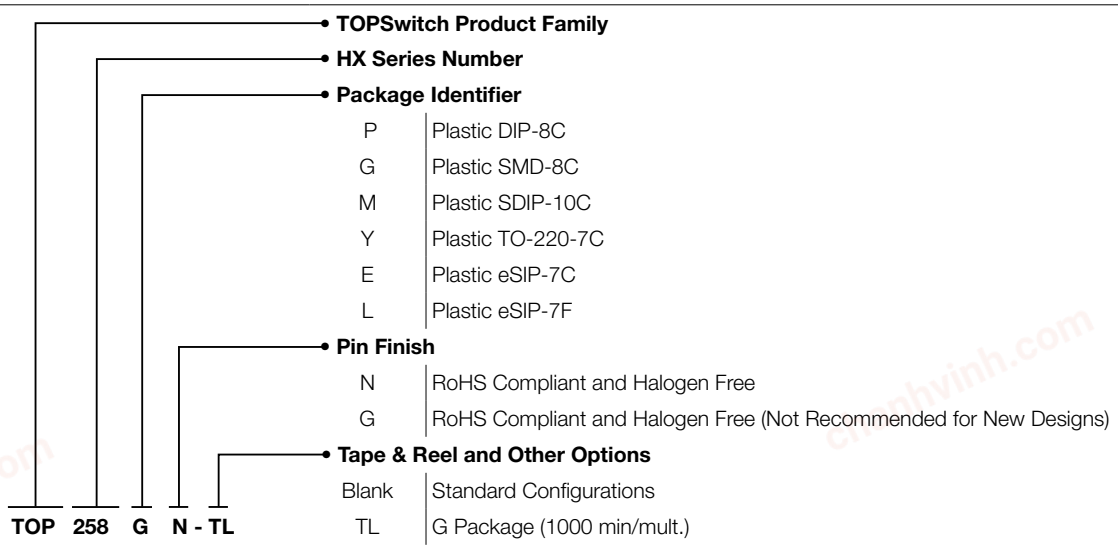
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-5204-061510

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Part Ordering Information



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Revision	Notes	Date
B	Data sheet release.	02/08
C	Added L package and TOP262.	07/08
D	Changed eSIP-7E to eSIP-7F. Added detail to PI-4917 and PI-5204.	08/08
E	Released TOP255-259LN and TOP262EN parts.	10/08
F	Added note for TOP256E halogen free part availability.	01/09
G	Added note for TOP258P and TOP259E halogen free part availability. Updated E & L bend package drawings. Minor text changes to page 27.	01/10
H	Added EG parts. Removed Note 7 from Table 1 on page 2.	06/13
I	Updated with new Brand Style.	05/15
J	Updated PDIP-8C (P Package) and SMD-8C (G Package) per PCN-16232.	08/16
K	Updated part numbers in fOSC parameters.	06/19
L	Updated package drawings PDIP-8C and SMD-8C.	10/20
M	Updated Lead Finish description in Part Ordering Information table.	12/21

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