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MIN1072M
MinE-CAP

Bulk Capacitor Miniaturization and Inrush Management IC for Very High Power Density AC/DC Converters

Product Highlights

- Up to 50% volume reduction of input bulk capacitors (E-CAPs)
- Eliminates inrush NTC
- Significantly reduces i^2t stress on the input bridge rectifier and fuse
- Partners with the InnoSwitch™ IC family for lowest component count ultra-compact AC/DC converters

Advanced Protection / Safety Features

- Integrated temperature sensing and hysteretic thermal shutdown
- Input surge protection
- Pin open/short-circuit and E-CAP UV/OV fault reporting

Applications

- High power density universal input AC-DC converters
- Applications with very wide input range (90 – 350+ VAC)

Description

The MinE-CAP™ IC dramatically shrinks the size of input bulk capacitors without compromising output ripple, operating efficiency or requiring redesign of the transformer. When compared to traditional techniques such as very high switching frequency operation, MinE-CAP achieves the same or greater overall power supply size reduction whilst avoiding the challenges of complex EMI filtering and the increased transformer/clamp dissipation associated with very high frequency designs.

MinE-CAP also precisely manages inrush current at AC turn-on, eliminating the need for dissipative NTCs or large slow-blow fuses.

Figure 1 illustrates, the circuit configuration when using MinE-CAP. The input E-CAPs are arranged with a small high-voltage capacitor (C_{HV} typically 400 V) in parallel with a low-voltage capacitor (C_{LV} typically 160 V) connected in series with the MinE-CAP IC. The physical size of the input capacitors is minimized because a high percentage of the input capacitance is 160 V rated rather than 400 V as would normally be used in conventional universal input converters.

MinE-CAP can also be used in applications requiring extended wide-range input (90 VAC to 350+VAC), again with a high percentage of the input capacitance 160 V rated along with either stacked 400 V or 500-600 V rated capacitors of much smaller value than would normally be required.

During steady state-operation MinE-CAP introduces C_{LV} into the circuit at low AC line voltage when maximum input capacitance is required. To achieve this, MinE-CAP monitors the input rail and voltage across C_{LV} to dynamically engage and disengage this capacitor during every AC line cycle as required to ensure that the power supply operates smoothly across the entire specified input voltage range.

The selection chart of Figure 2 illustrates the recommended range of C_{HV} and C_{LV} values to achieve the required total input capacitance for a given output power.

C_{LV} is an electrolytic capacitor while C_{HV} can be selected as an electrolytic or ceramic. Ceramic capacitors in the range of 1 to 5 µF 400 V (depending on power level) have very low esr and typically offer the most space saving when the power supply is designed to accommodate ceramic capacitor characteristics (see Applications Considerations section). 400 V electrolytic capacitors are lower cost and when selected according to Figure 2 also provide up to 50% size reduction compared to traditional designs. A variety of standard input

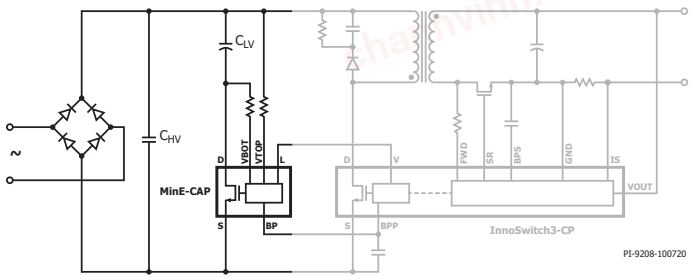


Figure 1. Typical Application Schematic.

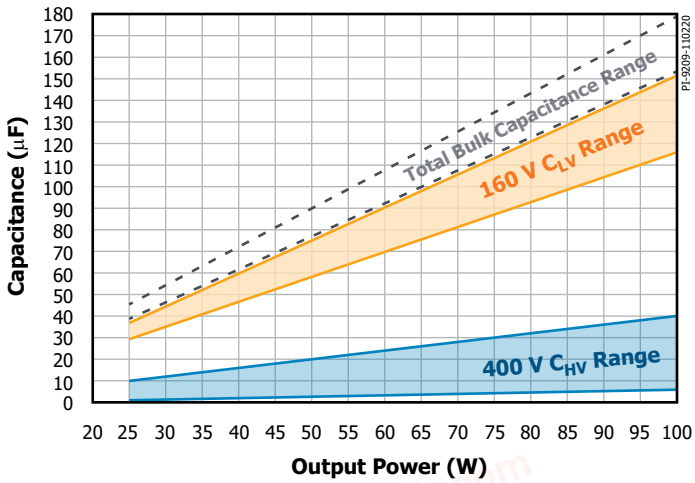


Figure 2. Typical Component Value Ranges for Optimal Space Saving and Converter Operation.

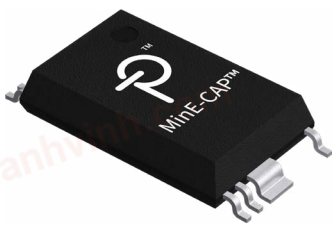


Figure 3. MIN1072M MinSOP-16A Package.

EMI filter configurations can be adopted depending on the form factor of a particular application. The MinE-CAP IC is designed to partner directly with the InnoSwitch family of power supply ICs with a minimum of external components. The existing InnoSwitch V pin resistor is connected to the MinE-CAP VTOP pin while a resistor connected to the VBOT pin enables C_{LV} voltage monitoring. Input voltage and fault information is transmitted from the MinE-CAP LINE (L) pin to the InnoSwitch V pin with no additional components. The MinE-CAP IC also derives its bias supply directly from the InnoSwitch BPP pin.

This Product is Covered by Patents and/or Pending Patent Applications.

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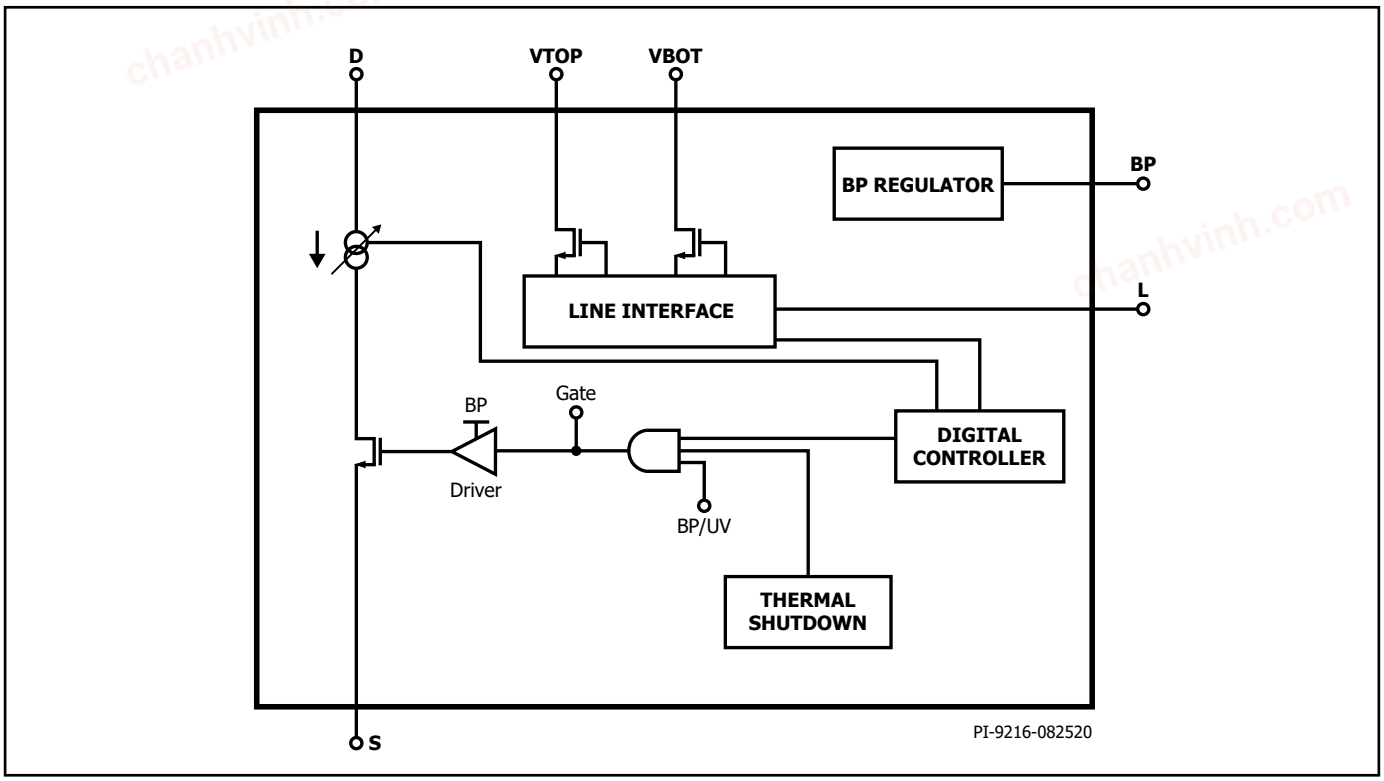


Figure 4. MinE-CAP IC Block Diagram.

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Pin Functional Description

VBOT Pin (Pin 1)
A high-voltage pin connected to the drain of the MinE-CAP IC. A high-voltage switch is closed when the MinE-CAP IC is operated in trickle-charge mode. A 1 MΩ resistor is tied between this pin and the negative end of the LV capacitor.

No Connect (NC) Pin (Pin 2)
Leave open. Should not be connected to any other pins or traces.

SIGNAL GROUND (SG) Pins (Pins 3, 6)
This pin is signal ground for the digital controller. Must be externally connected to S pin.

BYPASS (BP) Pin (Pin 4)
It is the connection point for an external bypass capacitor for the IC supply. Must be supplied by the BPP pin of the InnoSwitch IC or other external supply.

LINE (L) Pin (Pin 5)
This pin connects to the V pin of the InnoSwitch IC and is used to provide bulk capacitor voltage, start-up and fault information to the InnoSwitch IC.

NO CONNECT (NC) Pin (Pin 7)
Leave open. Should not be connected to any other pins or traces.

VTOP Pin (Pin 8)
A high-voltage pin connected to the DC side of the input bridge rectifier for monitoring bulk voltage information. A high-voltage switch is opened when the InnoSwitch IC is not sensing line information to reduce power consumption. R_{TOP} resistor connected between positive end of the LV capacitor and VTOP pin must be selected as per design line OV/UV requirements. In systems using InnoSwitch, this R_{TOP} resistor corresponds to the resistor used on V pin of the InnoSwitch.

GND Pin (Pin 9 - 10)
These pins must be connected to the SOURCE pin.

SOURCE (S) Pin (Pin 11)
This pin is the power switch source connection.

DRAIN (D) Pin (Pin 16)
This pin is the power switch drain connection.

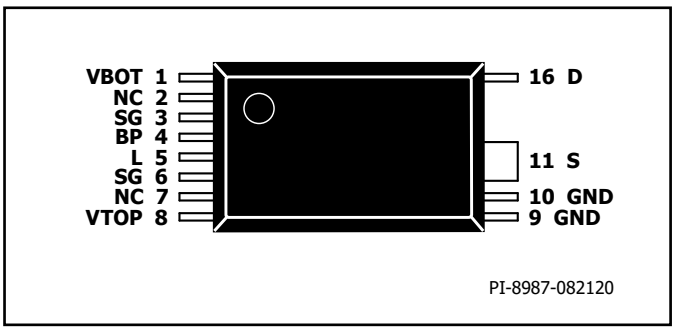


Figure 5. Pin Configuration.

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MinE-CAP Functional Description

The MinE-CAP IC comprises a digital controller and high-voltage power switch which connected in series with a low-voltage (160 V) bulk electrolytic capacitor in a power converter. The MinE-CAP IC connects this low-voltage capacitor into the power supply at low input line voltage conditions and disconnects it at high input line voltages. A high-voltage (400 V) capacitor is connected in parallel to support power delivery in high line conditions. The effective input capacitance is equivalent the sum of C_{LV} and C_{HV} at low input line to maintain the same minimum DC voltage to the DC/DC converter stage. At high input line condition the switch is disabled to ensure the voltage across C_{LV} does not exceeded the rated voltage of the capacitor. The MinE-CAP IC also includes a control signal transmitted from the MinE-CAP LINE pin to control the start-up and fault shutdown of an InnoSwitch IC via its V pin. Figure 4 illustrates the high level block diagram.

Start-Up

Inrush Management

Upon application of AC input, the MinE-CAP controller is in the off-state and the power switch is open. The C_{LV} is not engaged in the circuit and only C_{HV} is charged by the AC input. C_{HV} is significantly smaller than C_{LV} and the inrush stress on the bridge rectifier and fuse is therefore greatly reduced. The MinE-CAP IC then performs controlled charging of C_{LV} as described in the next section. This controlled charging of the C_{LV} allows MinE-CAP designs to eliminate the inrush NTC, improving the overall system design by removing a thermal hotspot and increases conversion efficiency.

Power-Up

The MinE-CAP Bypass is derived externally through direct connection with the InnoSwitch BPP pin. Note that during this time, the InnoSwitch IC is disabled from delivering power since the current received by the InnoSwitch V pin is $I_{INJECT(UV)}$ which is below brown-in threshold of InnoSwitch (further details on V pin operation available in InnoSwitch data sheets).

Active Charging

Once the BYPASS (BP) pin reaches regulation the MinE-CAP controller waits for the bulk voltage to be above the MinE-CAP brown-in threshold (I_{UV+}) measured on the VTOP pin. After brown-in, the controller enters a wait state for 20 ms to ensure power supply input voltage levels have stabilized. After that time, the MinE-CAP IC samples the bulk DC voltage to determine which of two possible C_{LV} charge up schemes to adopt as described below.

In low-line start-up conditions (V_{IN} < 150 VAC), the MinE-CAP IC performs precisely controlled active charging of C_{LV}. At low-line start-up condition, it is important to pre-charge C_{LV} to support full power capability prior to enabling the InnoSwitch. The MinE-CAP IC controls the internal high-voltage switch as a current source and uses a precise constant current, pulse charging of C_{LV}, see Figure 6. This algorithm allows fast charging of C_{LV} and ensures PSU is able to deliver full power in less than 250 ms from initial AC line connection.

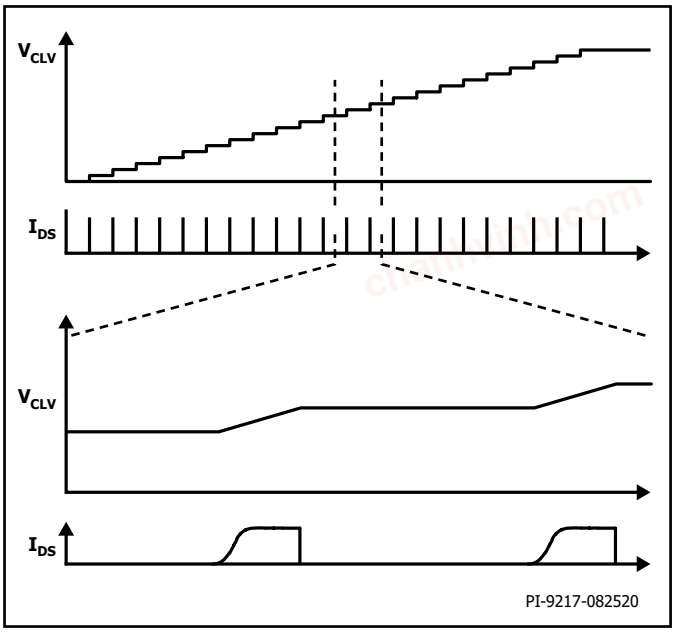


Figure 6. Charging Algorithm used for Low-Line Start-Up.

In high-line start-up condition (V_{IN} > 150 VAC), the active charging algorithm of C_{LV} described above is not employed. When selected according to Figure 2, C_{HV} alone can deliver full power converter output power at line voltages above 150 VAC. The InnoSwitch power control IC is therefore enabled immediately using the V pin output signal while C_{LV} is trickle charged at a lower rate until the steady-state C_{LV} voltage is reached. The voltage across C_{LV} is subsequently precisely monitored and recharged as required depending on input line conditions.

Steady-State

Power Switch Control Logic

The resistor connected to the VTOP pin is used to sense the line voltage. During normal operation the MinE-CAP IC is fully on while the bulk voltage remains below the user defined threshold (V_{COV+}).

$$V_{COV\pm} = I_{COV\pm} \times R_{TOP}$$

where

$$I_{COV-} = I_{COV+} - I_{COV(H)}$$

In this condition C_{LV} contributes to the output power delivery. Once the bulk voltage reaches V_{COV+}, the MinE-CAP IC is turned off to maintain C_{LV} below its rated voltage. In this state, only C_{HV} is contributing to output power delivery.

The MinE-CAP IC measures the VBOT pin voltage to determine if voltage on C_{LV} and C_{HV} are equal. Once the DC bus voltage falls below V_{COV-} and if the MinE-CAP IC determines C_{LV} and C_{HV} voltages are equal (VBOT pin voltage close to 0 V), the MinE-CAP power switch is turned on and C_{LV} is reengaged as an energy source for the power converter.

As such, the MinE-CAP IC is designed to turn on and off, engaging and disengaging C_{LV} during each AC line cycle, as may be required at intermediate AC line voltages. Figure 7 summarizes the steady-state control of the MinE-CAP power switch.

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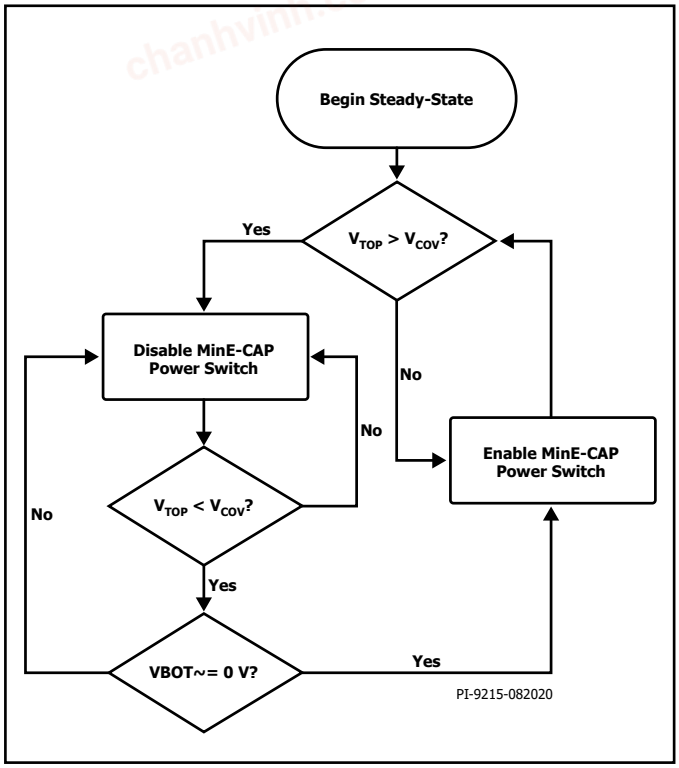


Figure 7. Steady-State MinE-CAP Power Switch Control.

Trickle Charge Regulation

During system conditions where the DC bus voltage constantly remains above V_{COV+}, e.g. during light load condition, the MinE-CAP IC uses trickle charging algorithm to ensure there is sufficient charge on C_{LV} to support power delivery if required. By measuring the differential voltage across C_{LV}, the MinE-CAP IC regulates the voltage across C_{LV} to within a predetermined range ($V_{TRKLCHRG}$). This ensures that during line dropout or load step, there is no impact on the power supply power deliver capability. The MinE-CAP IC is designed with extremely low off-state leakage current, much lower than the self-leakage current of C_{LV}, to ensure that the voltage across C_{LV} does not accumulate over time.

Brown-Out

If the bulk voltage falls below I_{UV-} for ~500 ms the controller resets and undergoes a normal start-up sequence.

Fault Handling

The MinE-CAP IC has built-in the following fault detection capabilities. Fault communication to InnoSwitch is done via the LINE pin.

Surge

The MinE-CAP IC has surge detection capability. If the power switch is on and a surge event occurs, the power switch is disabled for 130 µs. After the ~130 µs timer expires, the MinE-CAP IC returns to steady-state operation. Surge information is not communicated to the InnoSwitch IC.

Over-Temperature Protection

The MinE-CAP IC has thermal detection circuitry to maintain the MinE-CAP temperature below a safe level. In the event the MinE-CAP temperature exceeds T_{SD} the part goes into thermal shutdown and $I_{INJECT(OV)}$ is injected into the V pin of InnoSwitch IC. Once the MinE-CAP temperature falls below $T_{SD(H)}$, the MinE-CAP controller is reset and undergoes a normal start-up sequence.

Pin Open/Short Faults

The MinE-CAP IC has pin open/short detection on VBOT and DRAIN pins. In the event of a pin fault, $I_{INJECT(OV)}$ is injected into the V pin of InnoSwitch until the fault is removed. Subsequently, the MinE-CAP controller is reset and undergoes a normal start-up sequence.

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Application Example

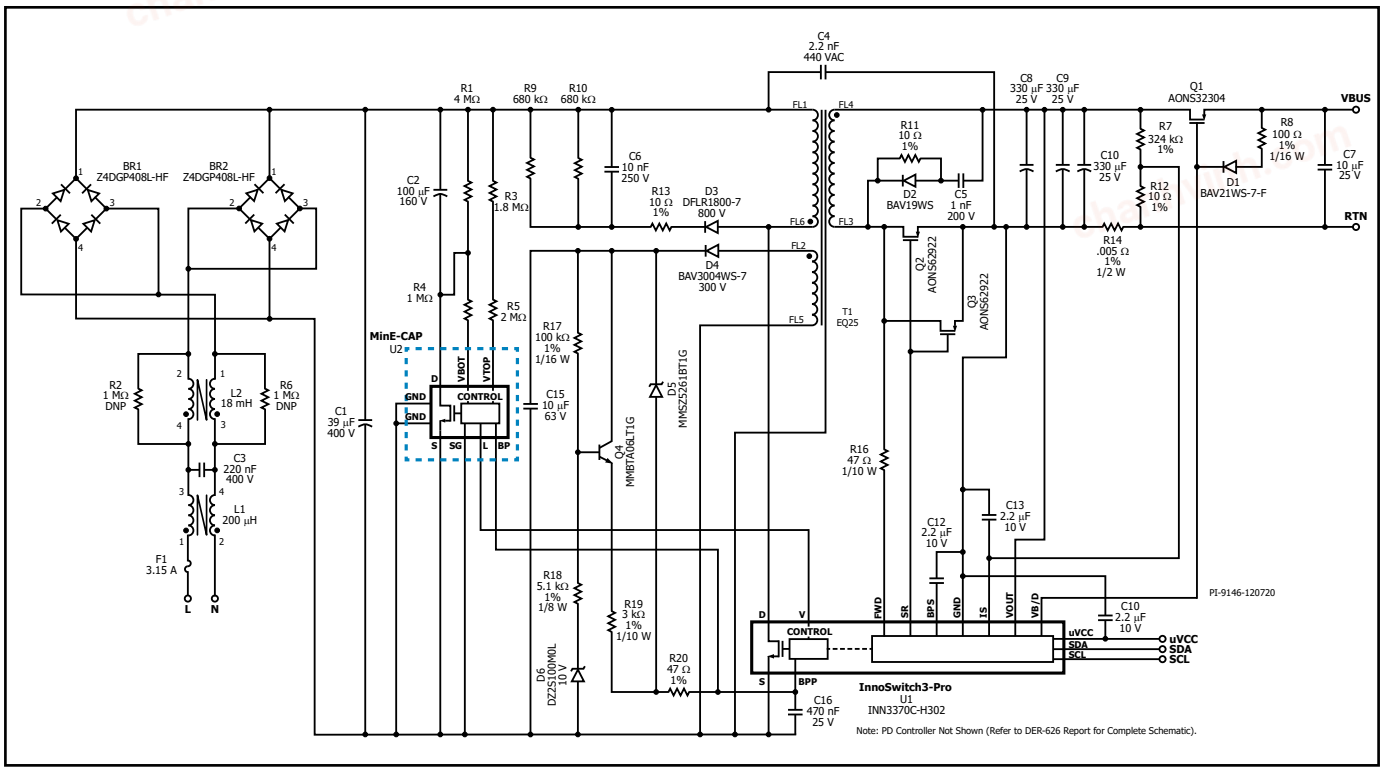


Figure 8. Schematic of DER-626, a 65 W USB PD 3.0 Adapter Design.

The circuit in Figure 8 shows a 65 W (5 V / 3 A; 9 V / 3 A; 15 / 3 A; 20 V / 3.25 A) USB PD 3.0 compliant adapter using the MinE-CAP IC to maximize power density. The MinE-CAP IC allows for the significant reduction of the physical size of the input bulk capacitors by allowing the use of a smaller (both in size and capacitance) 400 V capacitor paired with a 160 V capacitor. The MinE-CAP IC also eliminated the need for an inrush current limiting thermistor, leading to more saved space and increased efficiency. Together with the InnoSwitch3-Pro IC and low-profile planar magnetics, a form factor of L- 82 mm x W- 51 mm x H- 12 mm was realized. This corresponds to a power density of 21.22 W/in^3, with a system efficiency exceeding 90%. This design also meets DOE Level 6 and EC CoC 5 average efficiency standards.

Circuit Description

Input Rectifier and EMI Filter

Fuse F1 isolates the circuit and protects the AC line from excessive current due to component failure. Common mode chokes L1 and L2 along with capacitors C3 and C4 provide common mode and differential mode noise filtering to minimize conducted EMI emissions. The bridge rectifier formed by BR1 and BR2 rectifies the AC line voltage and provides a full-wave rectified DC voltage across the high voltage bulk capacitor, C1. Two bridge rectifiers are used to improve heat dissipation by doubling the rectifier surface area since power loss from two rectifiers is the same as that of a single device.

The MinE-CAP IC controls the rate of charge of the 160 V capacitor during start-up; thus, inrush current is mostly dependent on the value of the 400 V capacitor. Since the capacitance of the 400 V capacitor is significantly less when using a MinE-CAP IC, the use of a current limiting NTC thermistor is no longer necessary.

MinE-CAP and InnoSwitch3 Primary

When a MinE-CAP IC is used in tandem with the InnoSwitch3, the V pin of the InnoSwitch3 IC is connected directly to the LINE pin of the MinE-CAP IC. Resistors R3 and R5 provide input voltage sensing for both the the MinE-CAP IC and InnoSwitch3 ICs. The MinE-CAP IC uses R3 and R5 primarily to monitor the line voltage and maintain the voltage across the low-voltage bulk capacitor, C2 below its voltage rating when the line voltage is above 100 VAC. In contrast, the InnoSwitch3 uses the current from the LINE pin to determine line undervoltage and overvoltage conditions. During regular operation, the current from the LINE pin follows the current flowing through R3 and R5, so the InnoSwitch3 IC operates as if said resistors are connected directly to the V pin. Resistor R1 is a bleed resistor used to regulate the voltage across C3, while resistor R4 is used by the MinE-CAP IC to sample the voltage at the negative terminal of C2.

For this specific design, bypass capacitor C16 is shared by both the BPP pin of the InnoSwitch3 IC and the BYPASS pin of the MinE-CAP IC. The value of C16 is chosen based on the desired current limit of the InnoSwitch3 IC. As with any flyback design using the InnoSwitch3 IC, one end of the transformer primary is connected to the rectified DC bus while the other end is connected to the InnoSwitch3 DRAIN pin.

A low-cost RCD snubber formed by diode D3, resistors R9, R10 and R13, and capacitor C6 limits the voltage across the InnoSwitch3's Drain-Source nodes during turn-off by dissipating the energy stored in the leakage inductance of the transformer.

The InnoSwitch3 IC has an internal current source that charges capacitor C16 when AC input is first applied. Once the InnoSwitch3 IC starts switching and during normal operation, bias current is drawn from the auxiliary winding of the transformer. The output of the

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auxiliary winding is rectified using diode D4 and filtered by capacitor C15. An RC snubber can be placed across D4 to suppress voltage spikes, if necessary. Since the output voltage of the charger varies from 5 V to 20 V, the output of the auxiliary winding also varies and depending on the secondary to auxiliary turns ratio as well as the coupling coefficient between the primary and auxiliary. A linear regulator comprising resistors R17 and R18, Zener diode D6, and transistor Q4 provides a relatively stable DC voltage based on the breakdown voltage of D6 at the emitter terminal of Q4. Bias current can then be controlled using resistor R19.

Zener diode D5 offers primary sensed overvoltage protection. In case of overvoltage at the output of the converter, the auxiliary winding voltage also increases until D5 breaks down, causing excess current to flow into the BPP pin of the InnoSwitch3 IC. If the current flowing into the BPP pin exceeds the I_{SD} threshold, the InnoSwitch3 controller latches off to prevent any further increase in output voltage. Resistor R20 limits the current injected to the BPP pin during an overvoltage event.

InnoSwitch3-Pro Secondary and USB Power Delivery and Transformer design shall be in consideration of the AC-DC controller used

See InnoSwitch3-Pro data sheet for secondary-side component descriptions.

Key Application Considerations

No-Load Consumption

The MinE-CAP IC is designed to only consume around 500 µA of bias current from the BYPASS pin, which means the MinE-CAP IC only adds a few mW to the system no-load input power. For the design in Figure 8, the measured maximum no-load consumption was only 56 mW at VIN = 265 VAC. For minimal no-load consumption while ensuring proper operation of the MinE-CAP IC, follow the recommended resistor values and bias selection method outlined in the "MinE-CAP and InnoSwitch3-Pro Primary Components Selection" section of this application example.

Critical Components Selection

Input Capacitors

The value of the input capacitors can be determined based on the Capacitance vs. Output Power curve shown in Figure 2. For an output power of 65 W, the nominal capacitance for the high-voltage capacitor, C_{HV}, should be 30 µF while the low-voltage capacitor, C_{LV}, should be around 90 µF. Both capacitors are mounted with their axial lines parallel to the PCB; thus, both capacitors must have a maximum diameter of 10 mm to fit the 12 mm height requirement of the design. The remaining 2 mm clearance is for the installation of a heat spreader with insulation as well as to account for enclosure tolerances. Using the above requirements and after a few test iterations and based on component availability, the final input capacitor specifications are as follows:

1. HV Capacitor: 39 µF, 400 V_{DC}, 10 mm(D) x 37 mm(L)
2. LV Capacitor: 100 µF, 160 V_{DC}, 8 mm(D) x 42.5 mm(L)

For a more detailed and general approach to the selection of the input capacitors, check the MinE-CAP Application Note.

EMI Filter

The EMI filter in this design uses a T-Filter topology comprising a couple of common-mode chokes and a single X-capacitor, as shown in Figure 8. Both L1 and L2 use an HF60 Mn-Zn Toroid. Common mode choke L1 is 220 µH, while L2 is 18 mH. C1 is a 220 nF Class-X Film Capacitor. The common-mode chokes suppress common mode noise while the leakage inductance from both chokes combined with C1, and the input bulk capacitors form an LC-filter for differential mode noise attenuation. Common mode noise is further reduced by the Y capacitor connecting the input DC bulk voltage to the secondary ground node by shunting noise current back to the primary ground.

MinE-CAP IC and InnoSwitch3-Pro IC Primary Components Selection

The following section focuses on the selection of the MinE-CAP IC specific components as well as adjustments to the auxiliary bias circuit to accommodate the bias requirements of the InnoSwitch3-Pro IC and the MinE-CAP IC. For a comprehensive guide to InnoSwitch3-Pro component selection, see the InnoSwitch3-Pro data sheet.

The resistor V_{TOP} of the MinE-CAP IC corresponding to the series resistors R3 and R5 in the schematic in Figure 8, serves the dual purpose of allowing input line monitoring capabilities for the InnoSwitch3-Pro IC and regulating the voltage of the low-voltage input bulk capacitor, C_{LV}. The InnoSwitch3-Pro data sheet recommends a total value of 3.8 MΩ for R3 and R5 for universal line input OV/UV protection. Using this value for the R_{TOP} resistor programs the MinE-CAP IC to keep the voltage across C_{LV} to approximately 140 V, which is well within the 160 V rating of the capacitor. Use resistors with a tolerance of 1% or better for tighter regulation of the C_{LV} voltage.

The recommended value for R_{BOT} (R4 in the schematic) is 1.0 MΩ for accurate sensing of the MinE-CAP negative terminal of C_{LV}. The voltage regulation of C_{LV} is also sensitive to the value of R_{BOT}. A bleeder resistor, R1, must also be connected in parallel with C_{LV} to help regulate the voltage across the said capacitor, especially if V_{CLV} goes beyond the voltage set by R_{TOP}. Set the value of the bleeder resistor to 4.0 MΩ for optimum operation. R1 resistance values higher than recommended may cause overvoltage faults in the MinE-CAP IC. Values that are too low might prevent C_{LV} from charging to the programmed voltage, especially during trickle charging.

During normal operation, the MinE-CAP IC and InnoSwitch3-Pro IC both source their bias currents from the auxiliary winding through the linear regulator shown in Figure 8. Therefore, the selection of current limiting resistor R14 must take into account the bias requirements of both ICs ($I_{S1,\ MinE\text{-}CAP} + I_{S2,\ InnoSwitch3}$). For the circuit in Figure 8, R19 can be computed using the following equation:

$$R19 = \frac{V_{BR(D4)} - (V_{BE(Q1)} + V_{BPP(SHUNT)})}{I_{S1(MinE\text{-}CAP)} + I_{S2(INNOSWITCH)}}$$

V_{BR}, D6 = breakdown voltage of Zener D4
$V_{BE(Q1)}$ = Base-Emitter Voltage of Q1
$V_{BPP(Shunt)}$ = 5.6 V (see InnoSwitch3 data sheet)
$I_{S1(MinE\text{-}CAP)}$ = Typical MinE-CAP bas current
$I_{S2(InnoSwitch3)}$ = InnoSwitch3 bias current

Note that the computed resistance for R19 is just a starting-point value and can be adjusted to optimize performance, especially for no-load power reduction. Also, the formula given above is only valid for the regulator topology used in Figure 8.

The InnoSwitch3-Pro IC uses the bypass capacitor connected to the BPP pin (C16 in Figure 8) to set the current limit setting for the design. If the MinE-CAP IC is placed close to the InnoSwitch3 IC, both ICs could share the same bypass capacitor. However, if the MinE-CAP BYPASS pin is connected to the InnoSwitch3 BPP pin through a long trace or a via, an extra bypass capacitor should be placed as close as possible to the MinE-CAP IC and must be connected to the BYPASS and GROUND pins using very short traces. If an extra bypass capacitor is used, a 10 nF to 100 nF, 10 V X7R ceramic capacitor is recommended. Avoid using capacitance values higher than 100 nF when using standard current limits for the InnoSwitch3-Pro (see InnoSwitch3-Pro BPP capacitor tolerance limits).

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Layout Considerations

The following layout considerations are specifically for the MinE-CAP components. For placement and layout of InnoSwitch3-specific and power components, check the InnoSwitch3-Pro data sheet.

1. The MinE-CAP sense pins (VBOT and VTOP) and InnoSwitch3 IC's V pin use current in the μA range to measure line and capacitor voltages. Avoid routing lines with high dV/dt or dI/dt signals near these pins. This rule must also be observed for the LINE pin.
2. Signal lines going to the pins stated above must also be routed away from high dV/dt or dI/dt nodes or tracks.
3. All resistors associated with the MinE-CAP IC, except for the bleed resistor in parallel with C_{LV} must be placed near the MinE-CAP IC.
4. Place the MinE-CAP IC as close as possible to the InnoSwitch3-Pro IC to minimize the trace from the LINE pin to the V pin of the Innowitch IC. Placing the MinE-CAP IC next to the InnoSwitch3 IC also allows the use of a single bypass capacitor for both ICs.
5. Tie the GROUND pins to a copper plane for heat dissipation. If a large copper plane is not possible, thermal vias can also be used for boards with 2 or more copper layers. The MinE-CAP IC and InnoSwitch3-Pro IC can share the same GND plane.
6. Place both input bulk capacitors in such a way to minimize the primary switching loop. Prioritize placing the high-voltage capacitor closer to the transformer and InnoSwitch3-Pro IC since this capacitor is always part of the high-frequency switching loop.
7. Clean the board properly to prevent flux residues from interfering with the signals.

Figures 9 shows the MinE-CAP layout used for the design in Figure 8 following the recommendation stated above. In this design, the layout did not permit the RTOP to be placed right next to the VTOP pin. However, the VTOP pin trace is shielded by a ground plane beside and beneath the trace. Additionally, there are no high di/dt or dv/dt signals near the track, pin or resistor.

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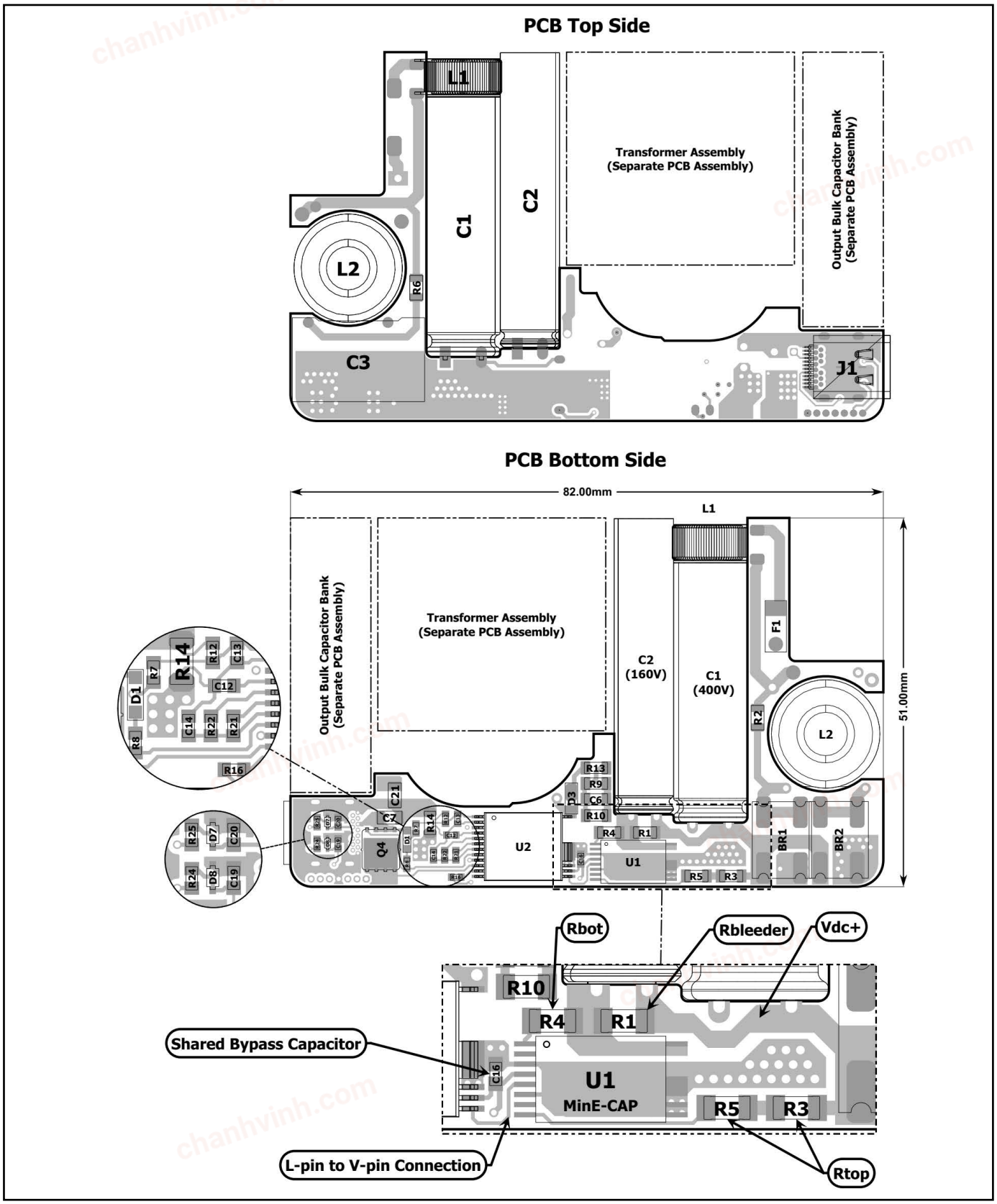


Figure 9. Layout of the Design in Figure 8 Showing the Location of Major Components.

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EMI Considerations

When the MinE-CAP disconnects the low-voltage capacitor, C_{LV} from the circuit during high-line operation, the conducted EMI may increase. For designs that utilize the EMI filter topology shown in Figure 10, removal of the low-voltage capacitor (C3) fundamentally shifts the cut-off of the low-pass filter formed by the leakage inductances of the common-mode chokes (L1 and L2), X-capacitor (C1), and the input bulk capacitors to a higher frequency. Removal of the low-voltage capacitor also increases the total input bulk capacitor ESR. These may result in an increase in differential-mode noise at high-line.

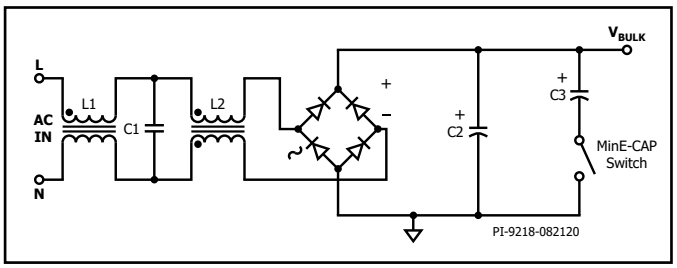


Figure 10. T-Filter EMI Filter Topology.

This effect can be remedied by either increasing the leakage inductances of the common-mode chokes or by increasing the value of C1. Such a solution may not be viable due to several restrictions, such as size or excessively high inductance requirements. The filter in Figure 11 is still a viable topology to use. However, the computation of the required values of C1, L1, and L2 must take into account the removal of C3 in the design.

An alternative approach is to use a Pi-filter to help suppress differential-mode noise. The schematic for this alternative design is shown in Figure 11.

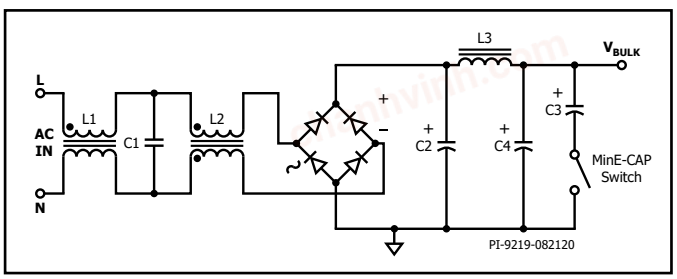


Figure 11. Typical EMI Filter with a Pi-Filter at the Rectified Side.

A dedicated differential choke enables the use of a smaller common mode choke. The 400 V capacitance is then split into two half size capacitors either side of this differential choke in a pi-filter configuration.

For the design in Figure 11, in place of the single high-voltage capacitor, two high-voltage capacitors must be chosen such that its impedance is not too high when evaluated at the maximum switching frequency of the converter. In general, the output impedance of the filter must be less than 10% of the impedance of the converter at full load. Finally, the low-voltage capacitor (C3) must be placed after the inductor, L3. This way, current from the low-voltage capacitor is not hindered by the impedance of L3 when operating at low-line.

Quick Design Checklist

Aside from the verification of the functionality of the InnoSwitch3-Pro IC, proper operation of the MinE-CAP IC must also be checked. At the minimum, the following verification tests must be performed.

1. V_{CLV} Regulation – Check that the maximum voltage across the low-voltage capacitor never exceeds the capacitor's voltage rating. Perform this test across the whole input voltage and output power range. Checking V_{CLV} regulation during brown-in and brown-out is also recommended.
2. Ensure that all resistors do not go beyond their voltage ratings. For R_{BOT} and R_{BLEED}, a single 1206 chip resistor will suffice. For R_{TOP}, the use of two 1206 chip resistors in series is recommended.
3. The MinE-CAP IC must seamlessly transition from high-line to low-line operation and vice-versa without causing the InnoSwitch3-Pro IC to enter auto-restart mode. Verify this across all loading conditions.
4. Thermal Check – Verify that the MinE-CAP IC does not cause an OTP fault when operating at maximum load throughout the whole input range. If the unit is a charger, perform the thermal check with the enclosure installed.

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Absolute Maximum Ratings(1,2)

DRAIN Pin Voltage ..... -0.3 V to 750 V[6]
DRAIN Pin Peak Current ..... 25 A
BP Pin Voltage ..... -0.3 to 6 V
BP Pin Current ..... 0 to 1 mA
VTOP Pin Voltage ..... -1.5 V to 650 V
VBOT Pin Voltage ..... -1.5 V to 650 V
LINE Pin Voltage ..... -0.3 V to 6 V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[4] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 105 °C
Lead Temperature[5] ..... 260 °C

Notes:

1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Higher peak Drain current is allowed while the Drian voltage is simultaneously less than 400 V.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Maximum drain voltage (non-repetitive pulse) ..... -0.3 V to 750 V.
   Maximum continuous drain voltage ..... -0.3 to 650 V.

Thermal Resistance

Thermal Resistance:
(θ_{JA}) ..... 83 °C/W[1], 76 °C/W[2]
(θ_{JC}) ..... 24 °C/W[3]

Notes:

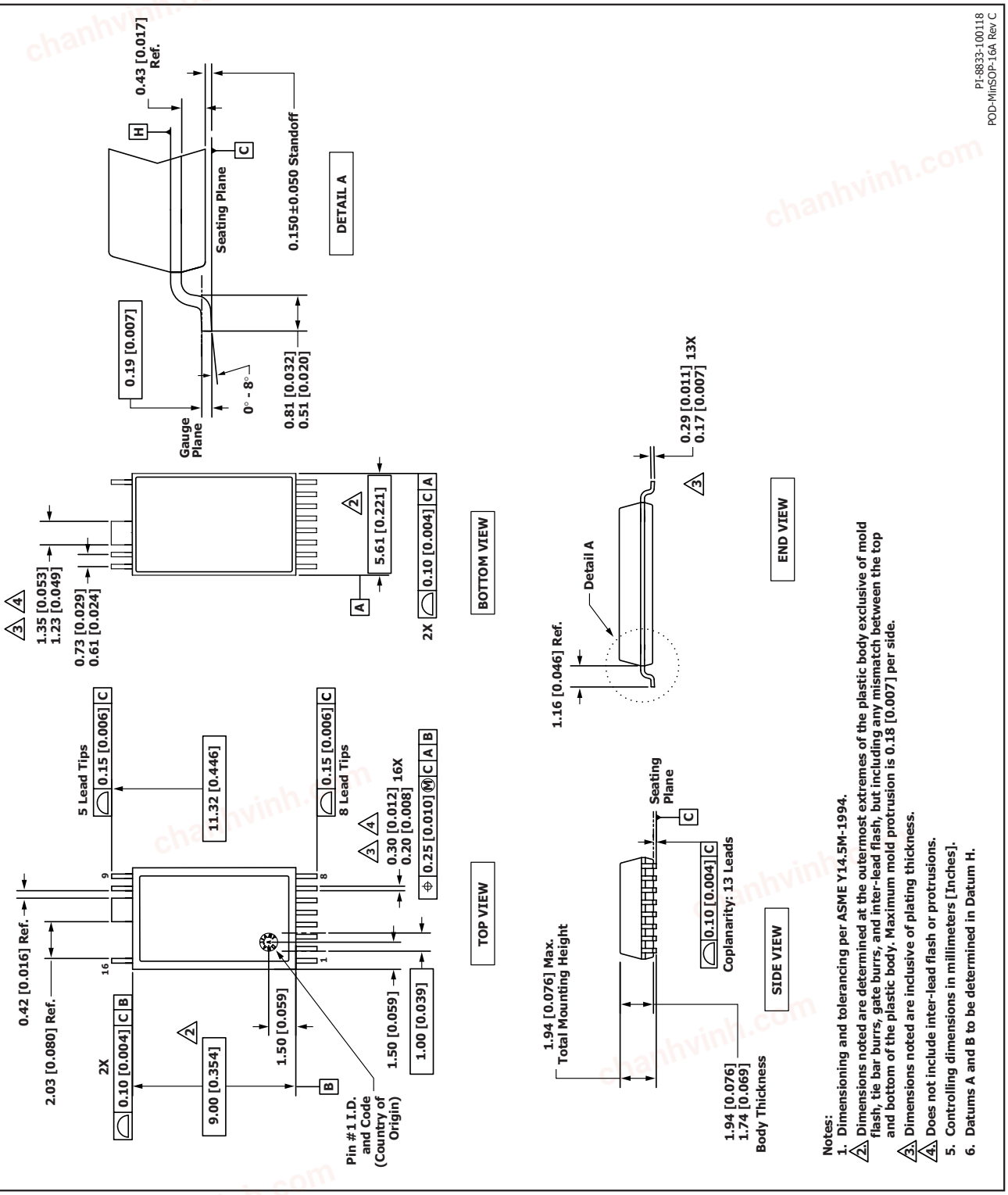
1. Solder to 0.36 sq. in (232 mm²), 2 oz. (610 g/m²) copper clad.
2. Solder to 1 sq. in (645 mm²), 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.

Parameter	Symbol	Conditions T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Analog Parameters						
BYPASS Supply Current	I_{S1}	T_J = 25 °C	300	430	475	µA
BYPASS Pin Voltage	V_{BPP}			4.45		V
BYPASS Pin Voltage Hysteresis	$V_{BPP(H)}$			0.6		V
Bypass Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C	3.45	3.75	3.90	V
Brown-In	I_{UV+}	T_J = 25 °C	17	18	19	µA
Brown-Out	I_{UV-}	T_J = 25 °C	11	12	13	µA
LV Capacitor OV Threshold	I_{COV+}	T_J = -40 °C to 100 °C	33.8	37.0	38.25	µA
	$I_{COV(H)}$	T_J = 25 °C		2.5		
Trickle Charge Regulation Voltage	$V_{TRKLCHRG}$	T_J = 25 °C Using 4M RTOP and 1M RBOT Resistors		145		V
LINE Pin Brown-Out Injection Current	$I_{INJECT(UV)}$	T_J = 25 °C	4	5	6	µA
LINE Pin OV Injection Current	$I_{INJECT(OV)}$	T_J = 25 °C	118	128		µA
Off-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP} + 0.1$ V V_{DS} = 150 V T_J = 25 °C		4.5	10	µA
	I_{DSS2}	$V_{BPP} = V_{BPP} + 0.1$ V V_{DS} = 325 V T_J = 25 °C		5	10	µA
On-State Resistance	$R_{DS(ON)}$	T_J = 25 °C		0.35	0.44	Ω
		T_J = 100 °C		0.49	0.62	Ω
Thermal Shutdown	T_{SD}	See Note A	135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A		70		°C

NOTES:
A. This parameter is derived from characterization.

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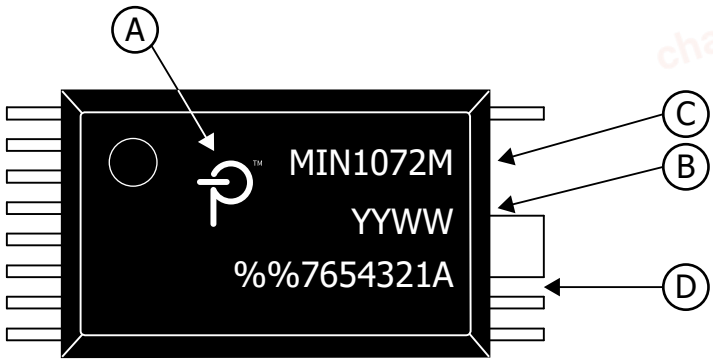
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PACKAGE MARKING

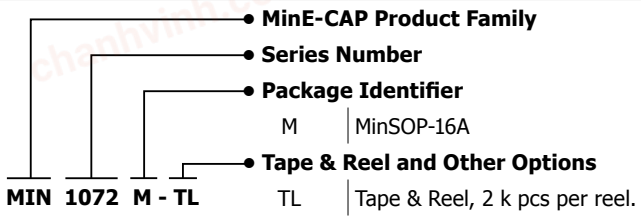
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A. Power Integrations Registered Trademark
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C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-9220-082120

Part Ordering Information



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Revision	Notes	Date
D	Code A release.	11/20
E	Updated DRAIN Pin Voltage and added Note 6 in Absolute Maximum Ratings table on page 11.	12/20

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Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan
8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com