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LinkSwitch-HP Family

power integrations

Energy Efficient, High-Power Off-Line Switcher with Accurate Primary-Side Regulation (PSR)

Product Highlights

EcoSmart™- Energy Efficient

- Multi-mode control maximizes efficiency over full load range
- No-load consumption below 30 mW at 230 VAC (LNK67xx)
- >75% efficiency with 1 W input at 230 VAC
- >50% efficiency with 0.1 W input at 230 VAC

High Design Flexibility for Low System Cost

- Dramatically simplifies power supply designs
  - Eliminates optocoupler and all secondary control circuitry
  - ±5% or better output voltage tolerance
- 132 kHz operation reduces transformer and power supply size
- Accurate programmable current limit
  - Compensation over line limits overload power
- Frequency jittering reduces EMI filter cost
- Fully integrated soft-start for minimum start-up stress
- 725 V MOSFET simplifies meeting derating requirements (LNK677x)
- 650 V MOSFET for lowest system cost (LNK676x/LNK666x)
- Fast transient response family option (LNK666x)

Extensive Protection Features

- Auto-restart limits power delivery to 3% during overload faults
  - Output short-circuit protection (SCP)
  - Output overload/over-current protection (OPP, OCP)
  - Optional extended shutdown delay time
- Output overvoltage protection (OVP), auto-restart or latching
- Line brown-in/out protection (line UV)
- Line overvoltage (OV) shutdown extends line surge withstand
- Accurate thermal shutdown (OTP), hysteretic or latching

Advanced Green Package Options

- eSIP™-7C package:
  - Vertical orientation for minimum PCB footprint
  - Simple heat sink mounting using clip or adhesive pad
- eSOP™-12B package:
  - Low profile surface mounted for ultra-slim designs
  - Heat transfer to PCB via exposed pad and SOURCE pins
  - Supports either wave or IR reflow soldering
- eDIP™-12B package:
  - Low profile through-hole mounted for ultra-slim designs
  - Heat transfer to PCB via exposed pad or optional metal heat sink
- Extended creepage to DRAIN pin
- Heat sink is connected to SOURCE for low EMI
- Halogen free and RoHS compliant

Typical Applications

- LCD Monitor and TV
- Adapter
- Appliances
- Embedded power supplies (DVD, set-top box)
- Industrial

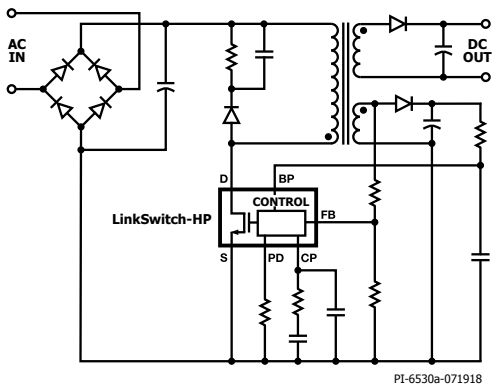
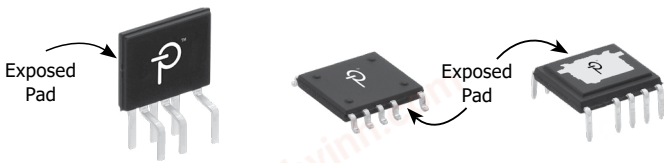


Figure 1. Typical Application Schematic.



eSIP-7C (E Package) eSOP-12B (K Package) eDIP-12B (V Package)

Figure 2. Package Options.

Product[4]	Heat Sink	230 VAC ±15%		85-265 VAC	
		Adapter	Open Frame	Adapter	Open Frame
LNK6xx3K/V	PCB-W[1]	15 W	25 W	9 W	15 W
LNK6xx3K	PCB-R[2]	21 W	35 W	12 W	21 W
LNK6xx3E	Metal	21 W	35 W	13 W	27 W
LNK6xx4K/V	PCB-W[1]	16 W	28 W	11 W	20 W
LNK6xx4K	PCB-R[2]	22 W	39 W	15 W	28 W
LNK6xx4E	Metal	30 W	47 W	20 W	36 W
LNK6xx5K/V	PCB-W[1]	19 W	30 W	13 W	22 W
LNK6xx5K	PCB-R[2]	26 W	42 W	18 W	31 W
LNK6xx5E	Metal	40 W	59[3] W	26 W	45 W
LNK6xx6K/V	PCB-W[1]	21 W	34 W	15 W	26 W
LNK6xx6K	PCB-R[2]	30 W	48 W	22 W	37 W
LNK6xx6E	Metal	60 W	88[3] W	40 W	68[3] W
LNK6xx7K/V	PCB-W[1]	25 W	41 W	19 W	30 W
LNK6xx7K	PCB-R[2]	36 W	59 W	27 W	43 W
LNK6xx7E	Metal	85[3] W	117[3] W	55 W	90[3] W
LNK6xx8K/V	PCB-W[1]	29 W	47 W	21 W	34 W
LNK6xx8K	PCB-R[2]	41 W	68 W	30 W	48 W
LNK6xx8E	Metal	98[3] W	135[3] W	63[3] W	104[3] W
LNK6xx9K/V	PCB-W[1]	33 W	54 W	25 W	39 W
LNK6xx9K	PCB-R[2]	47 W	77 W	36 W	56 W
LNK6xx9E	Metal	111[3] W	153[3] W	72[3] W	118[3] W

Table 1. Output Power Table.

Notes:
1. PCB heat sink with wave soldering.
2. PCB heat sink with IR reflow soldering (exposed pad thermally connected to PCB).
3. Maximum power specified based on proper thermal dissipation.
4. Packages: E: eSIP-7C, K: eSOP-12B, V: eDIP-12B. See Table 2 for all device options.

This Product is Covered by Patents and/or Pending Patent Applications.

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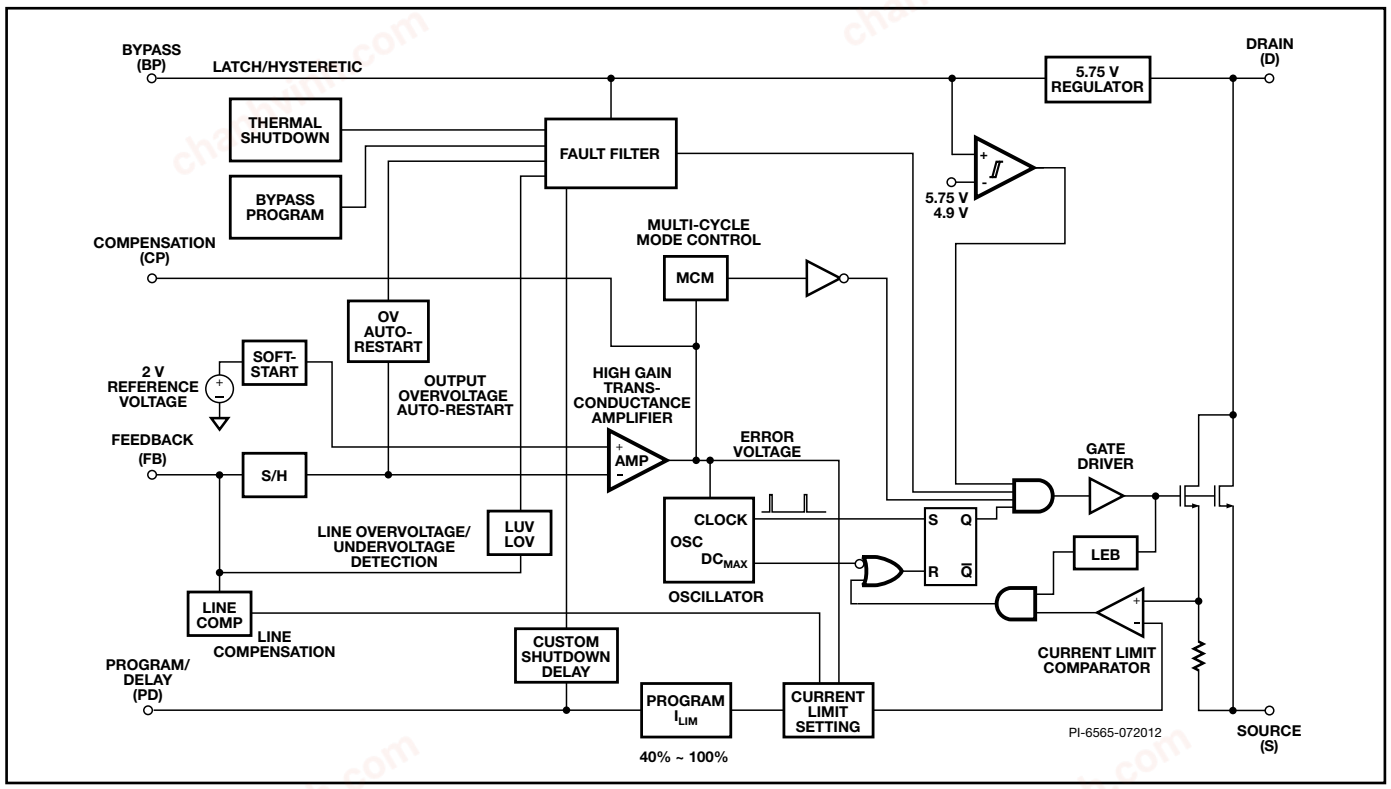


Figure 3. Block Diagram.

LNK	6	X	X	X	E/V/K
Part Number	**Series**	**$T_{MCM(OFF)}$[2], 6 = 0.5 ms 7 = 4.0 ms**	**BV_{DSS}[1], 6 = 650 V 7 = 725 V**	**Power**	**Packages**
LNK6663E/K/V	6	0.5 ms	650 V	Device Size	eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6664E/K/V		0.5 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6665E/K/V		0.5 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6666E/K/V		0.5 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6667E/K/V		0.5 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6668E/K/V		0.5 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6669E/K/V		0.5 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6763E/K/V		4.0 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6764E/K/V		4.0 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6765E/K/V		4.0 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6766E/K/V		4.0 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6767E/K/V		4.0 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6768E/K/V		4.0 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6769E/K/V		4.0 ms	650 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6773E/K/V		4.0 ms	725 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6774E/K/V		4.0 ms	725 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6775E/K/V		4.0 ms	725 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6776E/K/V		4.0 ms	725 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6777E/K/V		4.0 ms	725 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6778E/K/V		4.0 ms	725 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)
LNK6779E/K/V		4.0 ms	725 V		eSIP-7C (E), eSOP-12B (K), eDIP-12B (V)

Table 2. Device Part Numbers and Options.

Notes:

1. Minimum breakdown voltage at T_J = +25 °C.
2. $T_{MCM(OFF)}$ = 0.5 ms for fastest transient response, $T_{MCM(OFF)}$ = 4 ms for <30 mW no-load input power.

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Pin Functional Description

BYPASS (BP) Pin:
An external bypass capacitor is connected to this pin for the internally generated 5.75 V supply. Based on the connected capacitance determined at start-up, it will provide either auto-restart or latching shutdown option dependant on the fault condition. Please see Table 3.

COMPENSATION (CP) Pin:
This pin is the output of transconductance amplifier. An RC compensation network on this pin provides control loop compensation.

DRAIN (D) Pin:
This pin is the high-voltage power MOSFET drain connection. It also provides internal operating current for start-up until output is in regulation.

FEEDBACK (FB) Pin:
The FEEDBACK pin is used to sense output and input voltage by sensing the auxiliary winding voltage. During MOSFET on-time, the current out of the FEEDBACK pin is sensed to detect the line voltage. During the secondary rectifier conduction time, the feedback voltage is proportional to the output voltage via the turn's ratio between the bias and secondary windings.

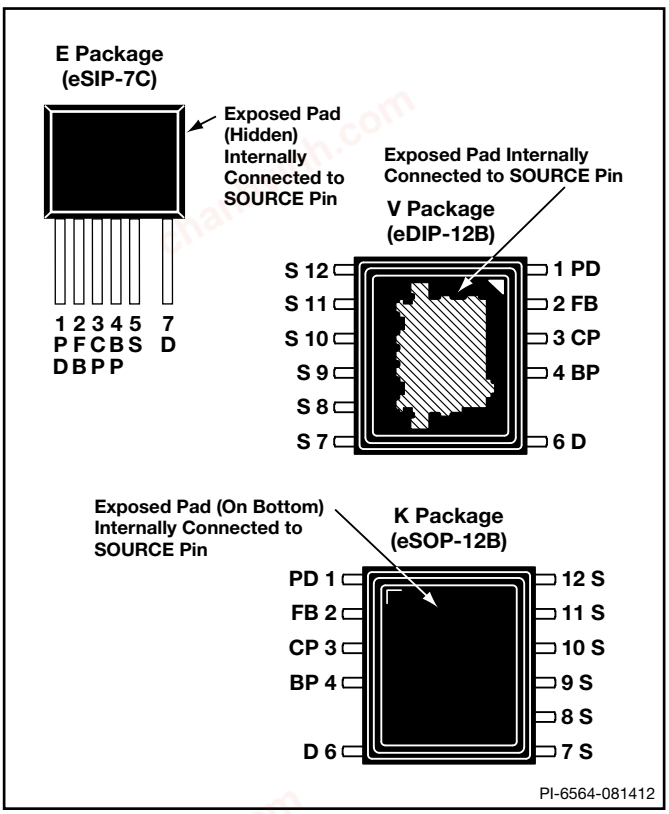


Figure 4. Pin Configuration.

PROGRAM (PD) Pin:
This MULTI-FUNCTIONAL pin sets device current limit and optional shutdown delay time extension. During start-up, the internal circuit decodes the current limit based on resistor loaded on the PROGRAM pin. Please see Table 4. It can also be used for optionally extending shutdown delay time by changing the capacitance on the pin. See Figure 6.

SOURCE (S) Pin:
This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS, FEEDBACK, PROGRAM and COMPENSATION pins.

Functional Description

A LinkSwitch™-HP device monolithically integrates a controller and high-voltage power MOSFET into one package. It has a newly developed analogue control scheme, which enables continuous conduction mode (CCM), primary side regulated (PSR) power supplies up to 90 W without the efficiency limitation of DCM or audible noise. It uses an enhanced peak current mode PWM control scheme with multi-mode operation. The multi-mode control engine uses the error amplifier output signal voltage at the COMPENSATION pin to set the operating peak current and switching frequency to maintain the output voltage in regulation as shown in Figure 5. For COMPENSATION pin voltages lower than $V_{C(MCM)}$ (typ. 1.25 V) the device enters multi-cycle modulation (MCM) with a fixed peak current of 25% of the programmed current limit. Several innovative improvements have been added to the peak current mode control to allow primary side regulated CCM operation with no instability. The device meets less than 30 mW input power with no-load at high-line (LNK67xx families).

It also offers extensive built-in features:

- External current limit selection.
- Optional programmable shutdown delay time extension.
- Optional remote On/Off.
- Optional fast AC reset.
- Primary-side sensed output overvoltage protection (OVP) .
- Lost regulation protection during output overload or short-circuit (auto-restart).
- Internal current limit over line compensation for constant overload power over line.
- High-voltage bus overvoltage sense (line OV) for extended line surge withstand.
- High-voltage bus undervoltage sense (line UV) for brown-in/out protection.
- Accurate over-temperature protection (OTP).
- Output OVP/OCP/OTP shutdown type selection (hysteretic/latching).
- Optional external latching shutdown input (current threshold)
- Cycle-by-cycle current limit control.

Regulator/Shunt Voltage Clamp
The internal 5.75 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.75 V by drawing a current from DRAIN whenever the power MOSFET is off. When the power MOSFET is on, the device operates from the energy stored in the bypass capacitor. In addition, there is a shunt regulator clamping the bypass at 6.4 V when supply current is provided by a bias winding through an external resistor. This makes the device insensitive to bias winding voltage variations.

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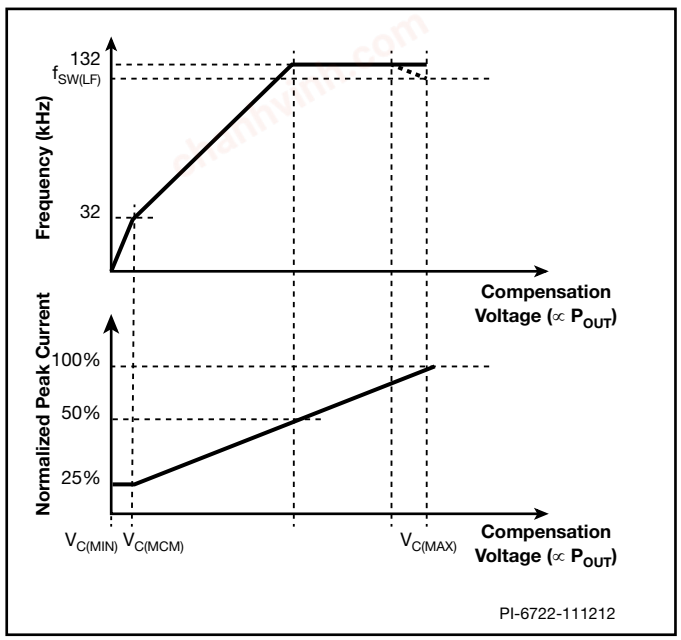


Figure 5. Compensation Pin Characteristics (Multi-Mode Operation).

Auto-Restart

In the event of an open-loop fault (no connection between the feedback winding and the feedback divider network or the FEEDBACK pin to the feedback network), the sensed current out of FEEDBACK pin will be zero during MOSFET on-time, the device enters into line brown-out protection (line UV). In the event of output short-circuit or overload condition, the device enters into auto-restart mode. Auto-restart minimizes the power dissipation under fault conditions, the device will turn on and off at duty cycle of typically 3% as long as the fault condition persists. In auto-restart switching is disabled for $t_{AR(OFF)1}$ (typ. 150 ms) when the FEEDBACK pin voltage has dropped below the auto-restart threshold $V_{FB(AR)}$ for the shutdown default delay time $t_{AR(ON)}$ (typ. 35 ms). After this period switching is enabled again with the device entering soft-start (typ. 15 ms). For the first auto-restart off-period switching is disabled for a reduced time $t_{AR(OFF)2}$ (typ. 1500 ms) to reduce the power supply restart time during line cycling. Optionally the default shutdown delay time can be extended by adding a capacitor to the PROGRAM pin.

Hysteretic Thermal Shutdown

The thermal shutdown circuitry senses the controller die temperature. The threshold is set at 142 °C with a 75 °C hysteresis (both typical). Once the device temperature rises above 142 °C, the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point the device is re-enabled. The large hysteresis maintain the average temperature below the temperature rating of low cost CEM type PCB material in most cases.

Safe Operating Area (SOA) Protection

The device features a safe operating area (SOA) protection mode which disables MOSFET switching for 4 consecutive cycles in the event the peak switching current reaches the current limit in less than time $t_{ON(SOA)}$. This prevents excessive drain currents during start-up and output short-circuit conditions by providing additional time for the primary inductance to reset. The SOA protection is disabled when the output voltage is within 7.5% of regulation voltage.

Sample and Hold (S/H)

The sample and hold block senses the output voltage at auxiliary winding during secondary rectifier on-time. The FEEDBACK pin voltage is sampled after the turn-off of the internal switch to compensate for diode conduction time differences. Sampling time increases monotonically from 1.2 µs at no or light load to 2.5 µs at full load. Sampled voltage is held until the next clock cycle. The output of S/H is fed to the error amplifier, once in regulation the sampled voltage is 2 V.

BYPASS (BP) Programming

This feature selects either hysteretic or latching OVP/OCP and OTP protection based on capacitor loading on the BYPASS pin.

The shutdown type is determined at the device power-up as shown in Table 3.

C_{BP}	0.47 mF	4.7 mF	47 mF
OVP	Latching	Auto-Restart	Latching
Lost Regulation (SC, OC)	Auto-Restart	Auto-Restart	Latching
OTP	Latching	Hysteretic	Latching

Table 3. Shutdown Type vs. Value of BYPASS Pin Capacitance.

Current Limit Setting

During power-up the cycle-by-cycle current limit is determined by measuring the resistor value connected to the PROGRAM pin by the measurement is performed by applying 1.25 V (see Figure 10). The current limit can be set between 40% to 100% in steps of 10% as shown in Table 4. After the current limit is set the PROGRAM pin voltage is reduced to ~0 in order to minimize power dissipation.

I_{PD}	R_{PD}	$I_{LIMIT(NORM)}$	I_{PD}	R_{PD}	$I_{LIMIT(NORM)}$
µA	kΩ	%	µA	kΩ	%
10	124	100	54	23.2	60
16	78.7	90	83	15.0	50
24	52.3	80	125	10.0	40
36	34.8	70			

Table 4. Current Limit Selection vs. Program Pin Resistor Value.

Programmable Shutdown Delay

The default auto-restart shutdown delay time $t_{SD(AR)}$ (typ. 35 ms) can optionally be extended by connecting a capacitor to the PROGRAM pin. Once a lost regulation fault is detected the PROGRAM pin voltage is cycled 128 times between $V_{PD(DL)}$ (typ. 0.5 V) and $V_{PD(DU)}$ (typ. 1.2 V) as shown in Figure 10. Figure 6 depicts the relationship between extended shutdown delay time, added PROGRAM pin capacitor and current limit programming resistor.

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Remote On/Off and Fast AC Reset

The PROGRAM pin can be used to turn on/off the device remotely. If the voltage on the pin is set to 1.35 V externally, the device stops switching. After releasing the PROGRAM pin the PROGRAM pin device commences switching when the voltage drops below 0.535 V.

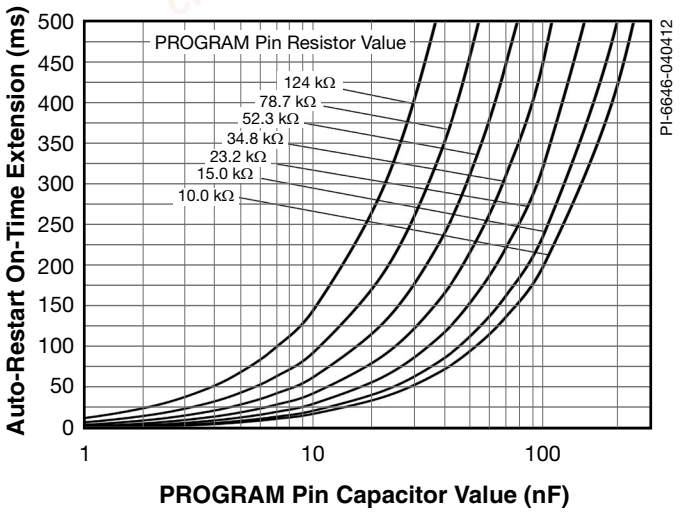


Figure 6. Optional Shutdown Time Extension Programming.

The PROGRAM pin can also be used to reset the device latch after a latching OVP or OTP event. If the voltage on the pin is set to 3.4 V externally, the device latch is reset. Once the voltage drops below 0.535 V, device will start switching.

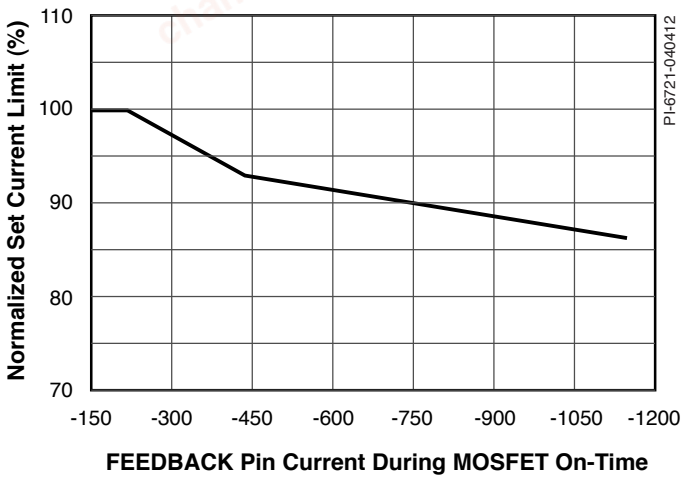


Figure 7. Current Limit Compensation Over Line.

High-Voltage Bus Sensing

LinkSwitch-HP senses indirectly the HV voltage bus V_{BUS} during the power MOSFET on-time by monitoring the current flowing out of the FEEDBACK pin. During the MOSFET on-time the voltage across the auxiliary winding is proportional to the voltage across the input winding. The current flowing through resistor R_{FB1} (see Figure 8) is therefore representing V_{BUS}. Indirect line sensing minimizes power dissipation and is used for line UV or line OV protection and current limit compensation over line.

At power-up the current out of the FEEDBACK pin has to exceed the line undervoltage turn-on threshold (brown-in) current $I_{FB(UVREF)}$ = -250 µA (typ.) before switching is enabled. During normal operation switching is disabled if the FEEDBACK pin current falls below the line undervoltage turn-off threshold (brown-out) current $I_{FB(UVOFF)}$ = -100 µA (typ.) for at least 8 consecutive switching cycles. After switching has ended, the device enters auto-restart. The applicable auto-restart off-period $t_{AR(OFF)1}$ = 150 ms (typ.).

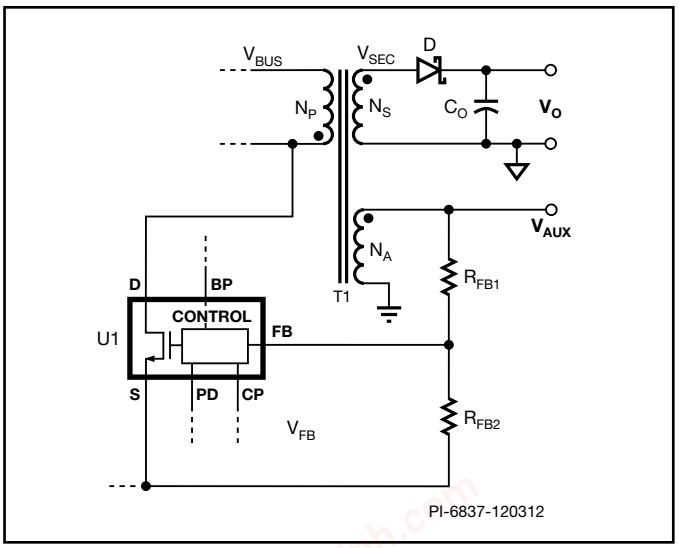


Figure 8. Indirect High-Voltage Bus Sensing.

Switching is also stopped if the FEEDBACK pin current exceeds the line overvoltage threshold current $I_{FB(OV)}$ = -1.15 mA (typ.) for at least 2 consecutive switching cycles.

Current Limit Compensation Over Line

The high-voltage bus is sensed by means of measuring the current out of the FEEDBACK pin during the MOSFET on-time. To limit available overload power over line the set current limit is compensated as shown in Figure 7. The compensation is disabled at peak currents below 50% of the set current limit, and is re-enabled at 62.5% of the set current limit.

Soft-Start

A digital soft-start is implemented to reduce component stress at power supply start-up. The internal reference voltage will ramp up to 2 V during t_{SOFT} (typ. 15 ms) at start-up. The loop will typically close (output reaches regulation) during this time to ensure smooth output voltage rise.

Fault Filter

This is the digital filter to handle all the fault conditions including line overvoltage, line undervoltage, output overvoltage, and output undervoltage, thermal shutdown as well as package level fault (pin open-circuit or pin-to-pin short-circuit).

Transconductance Amplifier

The controller uses a high gain (typ. 70 dB) transconductance amplifier to ensure exceptional output regulation.

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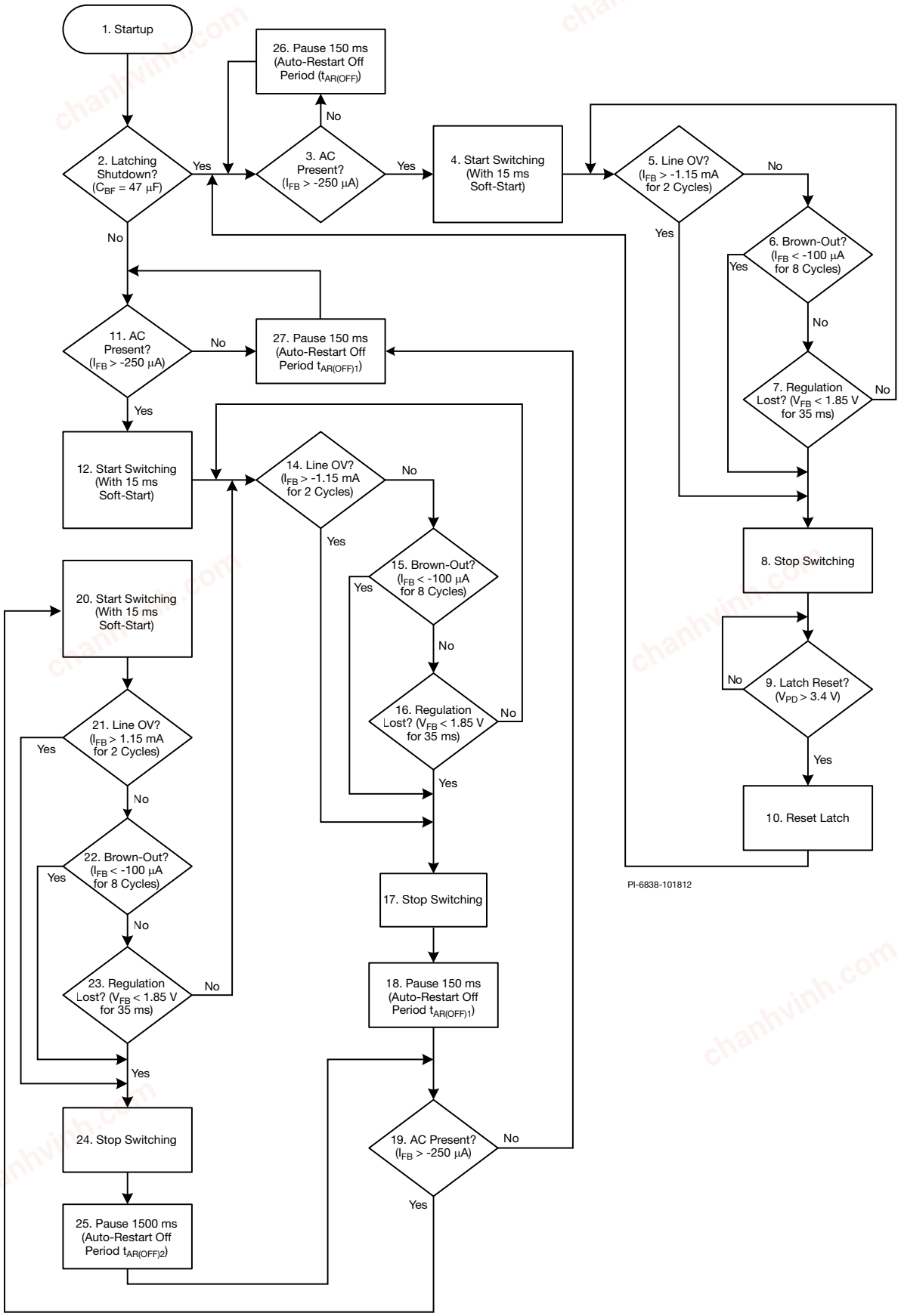


Figure 9. Line Sensing and Auto-Restart Flow Chart.

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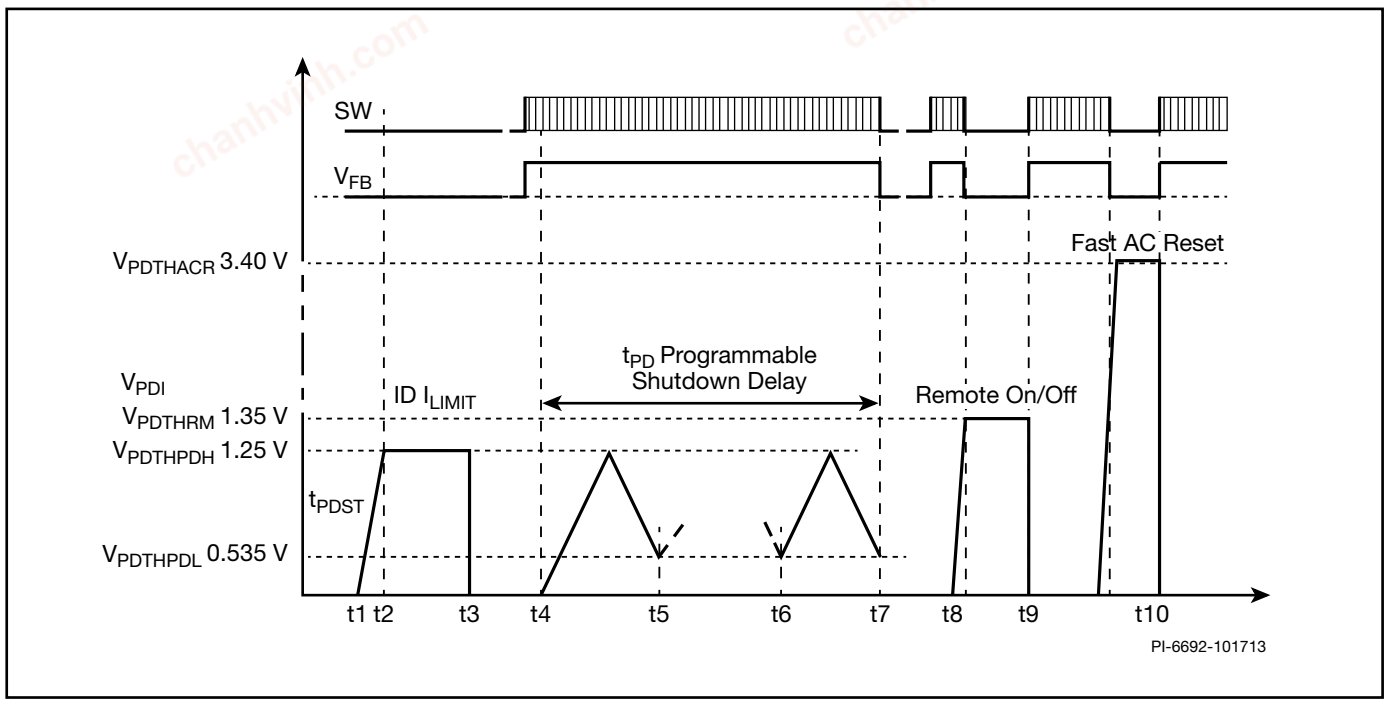


Figure 10. PROGRAM (PD) Pin Timing Diagram.

OSC
This is an adjustable frequency oscillator. Based on error voltage, the frequency will adjust from 32 kHz at light load to 132 kHz at heavy load. The oscillator employes ±5 kHz frequency jitter to reduce EMI levels.

Current Limit Comparator
This is a high-speed current limit comparator. It compares the current from the power MOSFET to the internal current reference. Once the current reaches the threshold the MOSFET on-cycle is terminated.

Multi-Cycle Modulation (MCM)
When voltage on COMPENSATION pin reaches $V_{C(MCM)}$ (about 1.25 V) the peak drain current is reduced to 25% of programmed value and the switching frequency approaches f_{MCM} = 32 kHz (typical). During MCM operation the controller intelligently maintains a relatively high output sampling rate while reducing the average switching frequency to keep the output voltage in regulation. Switching at 25% of the set current limit reduces the transformer core flux density significantly. This and the intelligent MCM operation reduce audible noise well below acceptable levels. LNK666x has a maximum MCM off-time $T_{MCM(OFF)}$ = 0.5 ms (typ.). The high minimum output sampling rate provides excellent transient load response from 0% to 50% or 100% of nominal load while offering typically below 100 mW no-load input power.

LNK67xx has a maximum MCM off-time $T_{MCM(OFF)}$ = 4 ms (typ.). The lower minimum output sampling rate enables designs below 30 mW no-load input power while providing fair transient load performance for load steps from 0% to 50% or 100% of nominal load.

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Applications Example

30 W, 12 V Universal Adapter

The circuit shown in Figure 11 is a high efficiency universal input 30 W, 12 V output adapter using the LNK6766E.

The supply uses primary winding coupled sensing for the following features: output regulation, line undervoltage lockout, input and output OVP. With primary winding sense there is no need for an external secondary referenced error amplifier such as a TL431 and optocoupler. The winding sense of bus voltage also eliminates the need for direct input voltage sensing which requires more components and is more dissipative than winding sense method.

Output regulation is ±5%, active-on efficiency is 86% and no-load input power is less than 30 mW.

The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the primary is driven by the integrated power MOSFET in U1. Diode D1, C3, R2, R3 and VR1 comprise the clamp circuit, limiting the leakage inductance turn-off voltage spike to safe value. Zener diode VR1 also helps to reduce input power consumption during no-load conditions.

Start-up of the power supply is initiated by sensing the forward negative pulse current from feedback winding through R19 into the FEEDBACK pin. This sensing is accomplished by periodically turning on the power MOSFET to sense input voltage condition with very short low frequency sampling pulses. During the forward pulse sampling time the FEEDBACK pin is held to zero volts by an internal clamp. When negative forward pulse current exceeds 250 μA, LinkSwitch-HP for two consecutive switching cycles will initiate start-up with a soft-start sequence that reduces component stress and allows the output to rise in a smooth monotonic manner. The desired input voltage for start-up is determined by the turns ratio of primary winding to feedback winding and the value of R19.

Regulation is accomplished by sampling the feedback winding during flyback period through the resistor divider R19 and R20 through FEEDBACK pin. This sampled voltage is compared to an internal error amplifier threshold of 2 V. The value of R19 is already determined by the line undervoltage function so the output regulation point is determined by setting the proper value for R20.

The loop compensation is provided by the network from COMPENSATION pin to ground. In the case above, a low frequency to mid frequency gain of 20 dB for the error amplifier is established by R7 and C7. Capacitor C8 functions essentially as a noise filter and is typically 100 pF. There is also an internal 16 kHz filter within the device. It is advised to limit R7 to no greater than 260 kΩ to avoid stability and noise sensitivity.

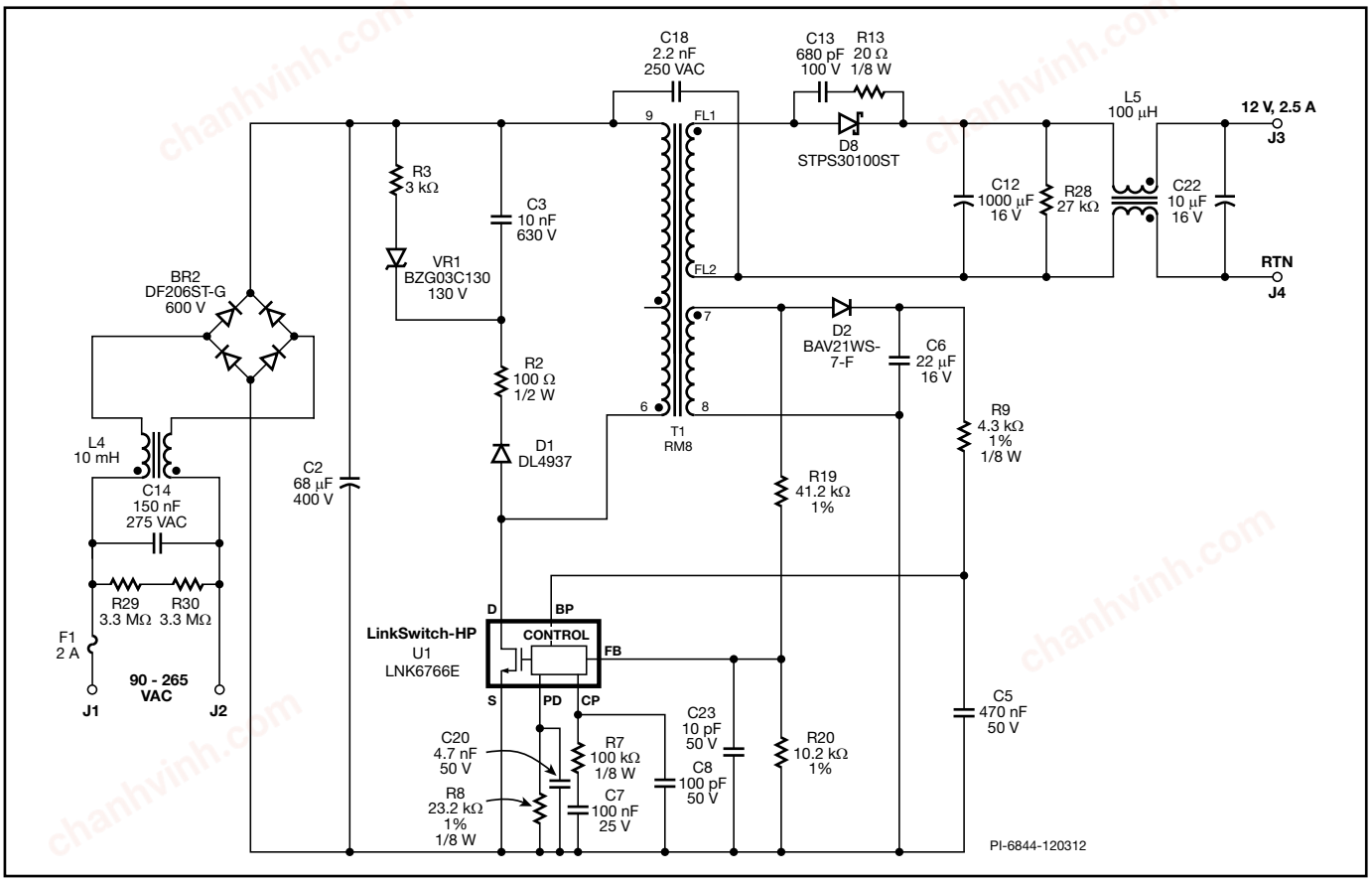


Figure 11. Schematic of a Universal Input 30 W, 12 V, 2.5 A Adapter.

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The transient load response is dependent on the loop gain and minimum switching frequency. The values of R7 and C7 shown here typically give good transient response for most designs. When the supply is at no-load, the minimum switching frequency at no-load will create a delay to respond to any step load event during the off-time. In the case above, the minimum frequency is 250 Hz so there is a potential 4 ms delay to response. If a faster response is desired from no-load initial condition there is the option to use the LNK666x which has a minimum frequency of 2 kHz. There is a trade-off in using this family as no-load input power will be slightly higher and a smaller pre-load resistor will be required.

In order to have good efficiency, regulation performance and stability, the transformer leakage inductance should be minimized. Low leakage will minimize ringing on the sense winding which can create an error in the feedback sampling. The example above uses split primary winding technique to lower leakage inductance. Leakage inductance should not be greater than 2% of nominal primary inductance and 1% is typically the desirable target value.

Resistor R28 serves as a pre-load resistor to minimize output voltage rising in no-load condition. The pre-load resistor should be no smaller than is necessary to maintain output within specification limits to minimize added dissipation. In this example, the added pre-load dissipation is only 4.8 mW.

LinkSwitch-HP provides an internal current source to bias the BYPASS pin which is necessary for start-up. When the supply is operating and in regulation an external bias is provided from the rectified flyback voltage from the bias winding (D2 and C6). Resistor R9 is sourced from the bias voltage across C6 into the BYPASS pin to provide external bias. The external bias current should set via R9 to be at least 500 μA to guarantee the internal current source of LinkSwitch-HP is turned off as this will allow the supply to operate more efficiently, especially at light load. For best no-load performance the external supply voltage across C6 should be minimized (typically 8-9 V) and the current into the BYPASS pin set by R9 should be as low as possible. Input overvoltage protection is done through sensing the negative forward pulse of feedback winding. When the negative forward voltage is sufficiently high to produce more than 1.15 mA current into the FEEDBACK pin, for 2 consecutive on-cycles the device will stop switching for auto-restart delay period.

Output overvoltage protection is achieved by sensing the flyback pulse through the FEEDBACK pin. When the FEEDBACK pin sees 2.5 V or greater for 16 consecutive cycles, the supply will latch off. If non-latching OVP is desired then changing C5 from 0.47 μF to 4.7 μF will change fault mode accordingly (see Table 3 for details).

OCP protection is accomplished by sensing when the output drops below 0.925 of nominal regulation value for a duration greater than specified delay time. In the example above, the total delay time is about 50 ms. Capacitor C20 extends the default internal delay time of 35 ms (see Figure 6 for details). The latching shut-off option is used in the design above.

The primary current limit of LinkSwitch-HP can be adjusted by selecting the value for R8 (see Table 4 for details). For this design 60% of maximum current limit was chosen. A lower current limit setting is typical for an adapter where lower $R_{DS(ON)}$ is desirable for higher efficiency and also lower thermal rise of LinkSwitch-HP.

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Layout Considerations for eSIP-7C Package

Figure 12 is the layout for a 30 W adapter shown in the schematic Figure 11. An eSIP-7C package is used as indicated by the suffix in LNK6766E which allows the use of a stand-up heat sink. The mounting pin for the heat sink should be electrically isolated. It can be seen that the primary return trace wraps around the LinkSwitch-HP device which acts as a shield around the critical external control related components of LinkSwitch-HP. These components include R7, R8, R19, R20 and C5, C8, C20. Of particular importance is placing the bypass capacitor C5 and COMPENSATION pin noise filter capacitor C8 as close as possible to SOURCE pin with very short trace lengths to COMPENSATION and BYPASS pins as shown. SMD capacitor or electrolytic capacitor can be used for the BYPASS capacitor. Preference will be given to electrolytic capacitor. Using electrolytic capacitor, an additional 100nF ceramic should be also fitted in the BYPASS pin. The ground trace wrap, tight layout and single point grounding to SOURCE pin of these components avoids having noise related issues during peak loads or during line transient such as surge or ESD events.

Another consideration for ESD and line surge is the primary-side termination of the Y capacitor. The Y capacitor C18 should be tied to the positive terminal of the bulk capacitor C2 in order to route the potential of high currents away from the more sensitive primary return traces.

Because of the tight layout common to adapter applications, this design uses triple insulated wire and flying leads for output winding termination to avoid secondary arcing to core during ESD events.

The trace connecting the drain to transformer should be very short and the primary clamp circuitry should be grouped together and away from the more sensitive components. The bias winding return and return of bias capacitor C6 should be routed separately to the negative terminal of the input capacitor C2 away from SOURCE pin.

The secondary rectifying loop that includes the secondary winding, the output diode D8, and the first output capacitor C13 should be as tight as possible to minimize adding series inductance which can reduce high load efficiency and degrade the quality of regulation.

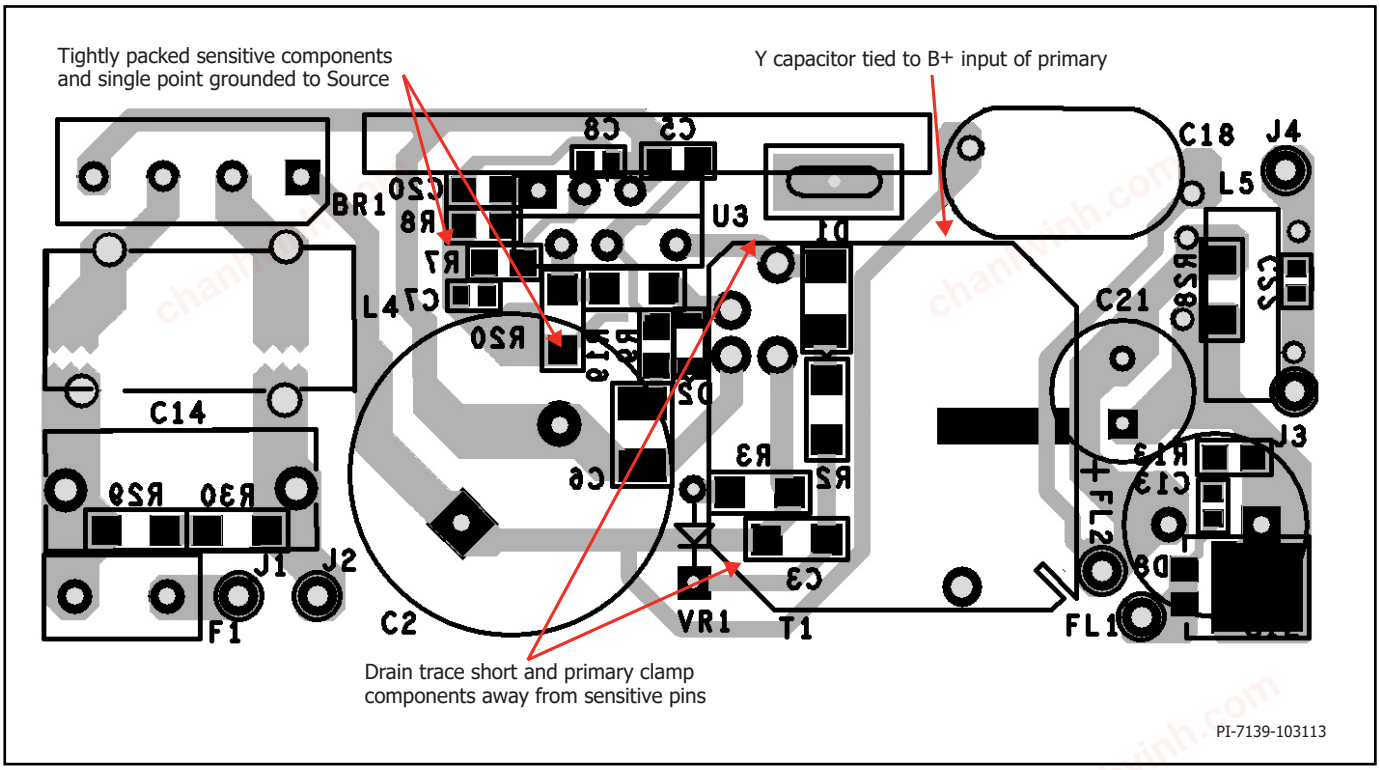


Figure 12. Layout for 30 W Adapter using a eSIP-7C Package (View from Bottom Copper Layer).

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Layout Considerations for eDIP-12B and eSOP-12B Package

The schematic extract in Figure 13 is an example of LinkSwitch-HP used in a dual output LCD monitor supply using eDIP-12B or eSOP-12B package. The SOURCE pins of LinkSwitch-HP provide heat sinking through connection to the source copper pad of PCB. This technique is adequate for device dissipation up to 0.85 W (1/2 square inch of copper area required). Exposed metal tab on the top side of eDIP-12B or bottom side of eSOP-12B package can be also used as heat sink. The layout guidelines described for eSIP-7C are the same for eDIP-12B and eSOP-12B with an added consideration about sensitive component layout. The return referenced components C4, C5, C7, C8, C16, R6, R7, R9 must be placed directly under the LinkSwitch-HP eDIP-12B package as shown in Figure 14 or around the LinkSwitch-HP eSOP-12B package as show in Figure 15. This requires that these components be SMD type as this allows an ideal noise-immune layout. SMD capacitor or electrolytic capacitor can be used for the BYPASS capacitor. Preference will be given to electrolytic capacitor. Using electrolytic capacitor, an additional 100 nF ceramic should be also fitted in the BYPASS pin.

Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. Their small size also makes it ideal for compact power supplies. At least 10 V, 0805 or larger size rated X5R or X7R dielectric capacitors are recommended to ensure that minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Output Power Table Assumptions

- 12 V output.
- Schottky rectification.
- 82% efficiency.
- V_{OR} = 135 V.
- K_P = 0.4 for 85-265 VAC input and K_P = 0.6 for 195-265 VAC input.
- V_{MIN} = 100 V for 85-265 VAC input and V_{MIN} = 250 V for 195-265 VAC input.
- 0.85 W device dissipation for open frame designs with PCB heat sink.

Quick Design Checklist

All LinkSwitch-HP designs should be verified on the bench particularly for specified worst-case stress conditions. The following set of tests are strongly recommended:

A. Maximum drain voltage – Verify that VDS does not exceed 675 V for LNK677X series and 600 V for LNK6X6X series. This gives a 50 V margin for design variations.
B. Maximum drain current – Under all conditions, the maximum Drain current should be below the specified absolute maximum ratings.
C. Thermal check – At rated maximum output power, minimum input voltage and maximum ambient temperature, verify that the maximum allowed temperature is not exceeded for any component in the design. Of particular importance is checking the temperature rise of the major power conversion components such as transformer, output diodes, input bridge, primary clamp circuit and LinkSwitch-HP. Under the stated conditions above, LinkSwitch-HP tab temperature should not exceed 110 °C.

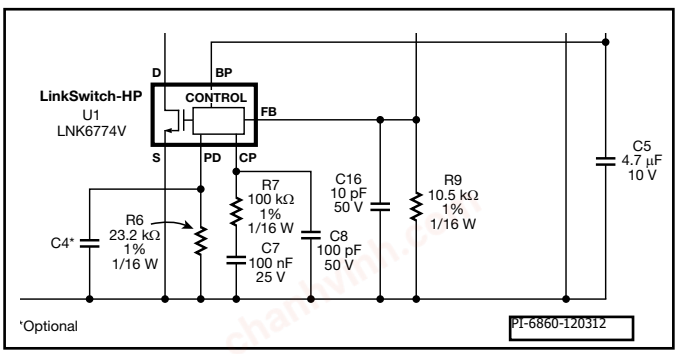


Figure 13. 17 W LCD Monitor Supply (+18 V, +5 V).

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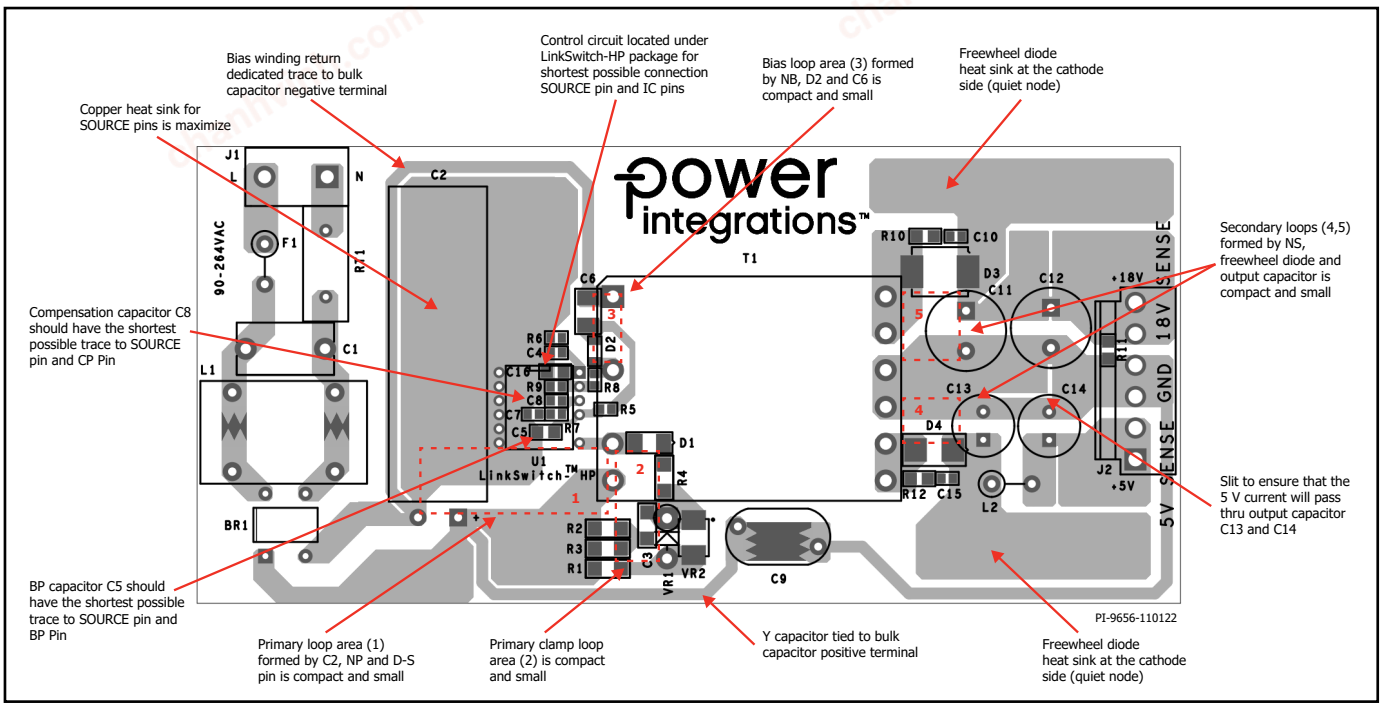


Figure 14. Layout for LCD Monitor Supply using eDIP-12B Package.

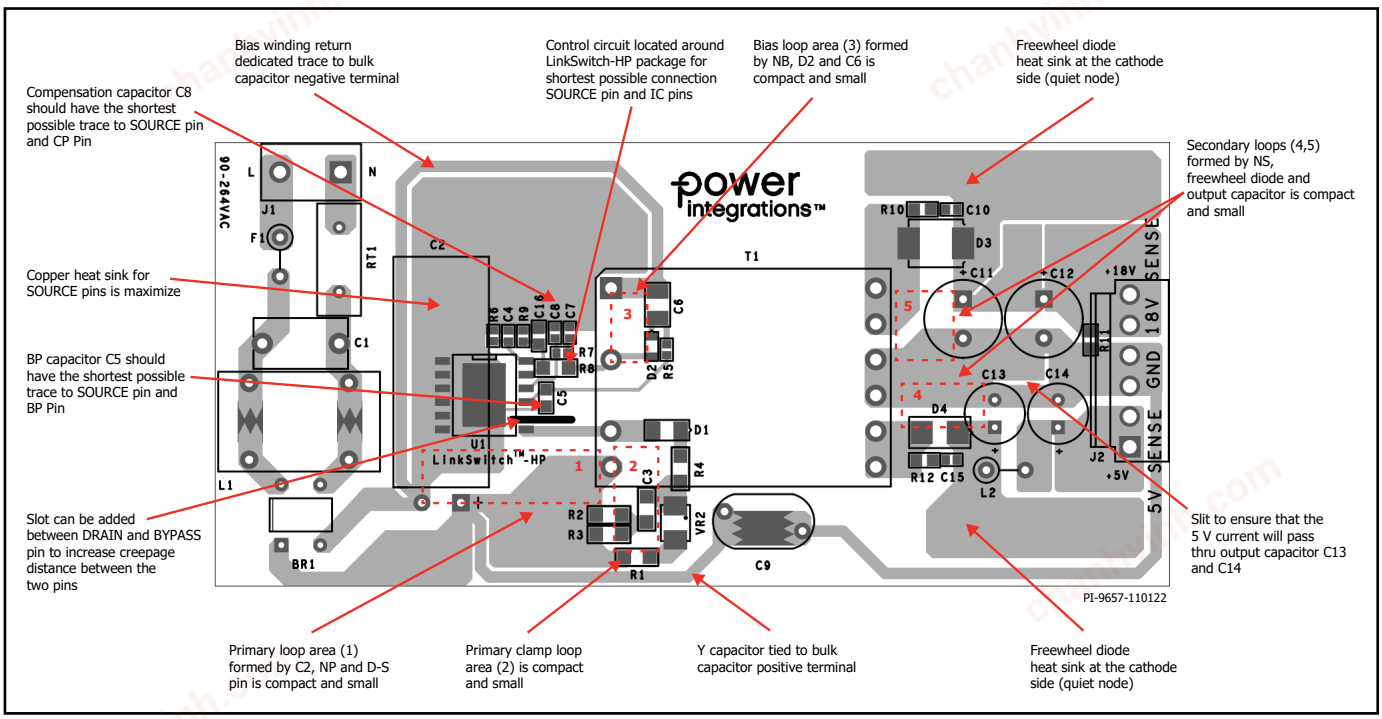


Figure 15. Layout for LCD Monitor Supply using eSOP-12B Package.

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Absolute Maximum Ratings(3)

DRAIN Pin Voltage ..... -0.3 V to 725 V (677x)
DRAIN Pin Voltage ..... -0.3 V to 650 V (666x/676x)
DRAIN Pin Peak Current: ..... 1.6 x $I_{LIMIT(TYP)}$ (1)
BYPASS Pin Voltage..... -0.3 V to 9 V
BYPASS Pin Current.....100 mA
FEEDBACK Pin Voltage .....-0.3 V to 9 V(2)
COMPENSATION Pin Voltage..... -0.3 V to 9 V
PROGRAM/DELAY Pin Voltage..... -0.3 V to 9 V
Storage Temperature .....-65 °C to 150 °C
Operating Junction Temperature ..... -40 °C to 150 °C(4)

Notes:
1. Peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.
2. -1 V for current pulses ≤5 mA out of the pin and a duration of ≤500 ns.
3. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.
4. Normally limited by internal circuitry.

Thermal Resistance

Thermal Resistance: E Package
(θ_{JA}).....105 °C/W(1)
(θ_{JC})..... 2 °C/W(2)
K Package
(θ_{JA}) .....45 °C/W(3), 38 °C/W(4)
(θ_{JC})..... 2 °C/W(2)
V Package
(θ_{JA}) ..... 74 °C/W(3), 63 °C/W(4)
(θ_{JC})..... 2 °C/W(2)

Notes:
1. Free standing with no heat sink.
2. Measured at the back surface of tab.
3. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 0.36 sq. in. (232 mm²), 2 oz. (610 g/m²) copper clad.
4. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 1 sq. in. (645 mm²), 2 oz. (610 g/m²) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Switching Frequency	f_{OSC}	Average value, T_J = +25 °C,		120	132	136	kHz
Switching Frequency Temperature Variation	Δf_{OSC}	0 °C ≤ T_J ≤ +100 °C, See Note A				±10	%
Frequency Jitter Deviation	Δf	f_{OSC} = 128 kHz			±5		kHz
Frequency Jitter Modulation Rate	f_M				250		Hz
Maximum Duty Cycle	DC_{MAX}	$V_{FB} < V_{FB(REF)}$ $V_{FB(REF)}$ = 2 V	T_J = +25 °C	62	64	66	%
Maximum Duty Cycle Temperature Variation	ΔDC_{MAX}		See Note A 0 °C ≤ T_J ≤ +100 °C			±2%	%
Minimum Peak Current to Set Current Limit Ratio	k_{PS}	T_J = +25 °C $di/dt_{(KPS)} = di/dt_{(ILIMIT)}$		22.5	25		%
Multi-Cycle Modulation Switching Frequency	f_{MCM}	T_J = +25 °C		25	32		kHz
Multi-Cycle Modulation Max Off-Time	$T_{MCM(OFF)}$	T_J = +25 °C	LNK666x		0.5		ms
			LNK67xx		4		
Soft-Start Time	t_{SOFT}	T_J = +25 °C			15		ms
Auto-Restart Shut-Down Default Delay	$t_{SD(AR)}$	T_J = +25 °C			35		ms
Auto-Restart	$t_{AR(ON)}$	T_J = +25 °C, t_{SOFT} + $t_{SD(AR)}$			50		ms
	$T_{AR(OFF)1}$	First switch off-period			150		
	$T_{AR(OFF)2}$	Subsequent switch off-periods			1500		

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
Transconductance Amplifier Gain	g_M	T_J = +25 °C		95	115	125	µA/V
Transconductance Amplifier Gain Temperature Variation	Δg_M	0 °C ≤ T_J ≤ +100 °C See Note A				±20	%
Transconductance Amplifier Max Output Current	I_{GM}	T_J = +25 °C		10.0	12.5	15.0	µA
COMPENSATION Pin Input Impedance	Z_{CP}	See Note A		30			MΩ
Bypass (BP) Input							
OVP/UVP/OTP Programming Capacitor Value	C_{BP}	T_J = +25 °C See Table 3 for programming		Typ × 0.7	0.47 4.7 47	Typ × 1.3	µF
BYPASS Pin Voltage	V_{BP}			5.46	5.75	6.04	V
BYPASS Pin Voltage Hysteresis	V_{BPH}			0.85	0.95	1.1	V
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V T_J = +25 °C V_{DS} ≥ 50 V	LNK6xx3	-6.8	-4.8	-2.0	mA
			LNK6xx4-5	-9.2	-6.6	-2.8	
			LNK6xx6-8	-12.0	-8.3	-4.3	
			LNK6xx9	-14.3	-10.1	-4.2	
	I_{CH2}	V_{BP} = 5 V T_J = +25 °C V_{DS} ≥ 50 V	LNK6xx3	-4.7	-2.7	-1.5	mA
			LNK6xx4-5	-7.0	-4.0	-2.2	
			LNK6xx6-8	-8.8	-5.2	-2.9	
			LNK6xx9	-11.5	-6.6	-3.7	
BYPASS Pin Shutdown Threshold Current	I_{BPSD}	T_J = +25 °C		5.7	8.2	10.7	mA
BYPASS Pin Shutdown Delay		T_J = +25 °C			8		Switching Cycles
BYPASS Pin Source Current	I_{BPSC}	V_{BP} = 6 V T_J = +25 °C				-0.5	mA
BYPASS Pin Charge Current Temperature Variation	ΔI_{BPSC}	See Note A			0.5		%/°C
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 2 mA		6.1	6.4	6.7	V
BYPASS Pin Supply Current	I_{BPS1}	T_J = +25 °C, See Note B				525	µA
	I_{BPS2}	MOSFET switching at f_{OSC}	LNKxxx3		0.9	1.2	mA
			LNKxxx4		1.0	1.3	
			LNKxxx5		1.1	1.4	
			LNKxxx6		1.3	1.6	

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Bypass (BP) Input (cont.)							
BYPASS Pin Supply Current	I_{BPS2}	MOSFET switching at f_{OSC}	LNKxxx7		1.4	1.7	mA
			LNKxxx8		1.55	1.85	
			LNKxxx9		1.65	1.95	
Voltage Sense (FB) Input							
FEEDBACK Pin Reference Voltage	V_{FBth}	T_J = +25 °C		1.974	2.000	2.026	V
FEEDBACK Pin Reference Voltage Temperature Variation	$\Delta V_{FB(th)}$	0 °C ≤ T_J ≤ +100 °C See Note A			-0.01		%/°C
Line Undervoltage Turn-On Threshold Current	$I_{FB(UV,REF)}$	T_{ON} = 220 ns, T_J = +25 °C			-250		µA
FEEDBACK Pin Bus Voltage Reference Current Temperature Variation	$\Delta I_{FB(REF)}$	T_{ON} = 220 ns, 0 °C ≤ T_J ≤ +100 °C See Note A				±10	%
Line Undervoltage Turn-Off Threshold Current	$I_{FB(UVOFF)}$	T_{ON} = 220 ns, T_J = +25 °C		-115	-100	-85	µA
Line Undervoltage Turn-Off Delay		T_J = 25 °C			8		Switching Cycles
Line Overvoltage Turn-Off Threshold Current	$I_{FB(OV)}$	T_{ON} = 220 ns, T_J = +25 °C		-1200	-1150	-1100	µA
Line Overvoltage Turn-Off Delay		T_J = +25 °C			2		Switching Cycles
Output Overvoltage Detection Threshold Voltage	$V_{FB(OVP)}$	T_J = +25 °C		2.375	2.5	2.625	V
Output Overvoltage Detection Delay		T_J = +25 °C			16		Switching Cycles
FEEDBACK Pin Auto-Restart Threshold Voltage	$V_{FB(AR)}$	T_J = +25 °C		1.794	1.85	1.906	V
Current Limit Reduction Onset Threshold Current	$I_{FB(LIM)}$	T_{ON} = 220 ns, T_J = +25 °C			-210		µA
Current Limit Reduction Slope	$I_{LIM(LINE)}$	0 °C ≤ T_J ≤ +100 °C	-463 µA < I_{FB} ≤ $I_{FB(LIM)}$		-0.032		%/µA
			I_{FB} < -463 µA		-0.008		
FEEDBACK Pin Sampling Delay Time	T_{SAMP1}	0 °C ≤ T_J ≤ +100 °C	I_{PK} = I_{SET}		2.5	2.65	µs
	T_{SAMP2}		I_{PK} = 0.25 × I_{SET}		1.2	1.3	
Missing Feedback Voltage Protection Sense Delay Time	T_{MFVP}	T_J = +25 °C			0.8		µs

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Voltage Sense (FB) Input (cont.)							
Missing Feedback Voltage Protection Delay					4		Switching Cycles
Multi-Function (PD) Input							
PROGRAM/DELAY Pin Voltage	V_{PD}	T_J = +25 °C		1.20	1.25	1.30	V
PROGRAM/DELAY Pin Time Lower Voltage Threshold	$V_{PD(DL)}$	T_J = +25 °C		0.50	0.535	0.57	V
PROGRAM/DELAY Pin Time Upper Voltage Threshold	$V_{PD(DU)}$	T_J = +25 °C		1.20	1.25	1.30	V
Fast AC Reset Threshold	$V_{PDTHACR}$			3.06	3.4	3.74	V
Remote On/Off Threshold	V_{PDTHRM}	T_J = +25 °C	Threshold	1.25	1.35	1.45	V
			Hysteresis		0.8		
Remote On/Off Delay		T_J = +25 °C			8		Switching Cycles
Circuit Protection							
Self-Protection Current Limit	I_{LIMIT}	LNK6xx3	di/dt = 180 mA/µs T_J = +25 °C	0.716	0.77	0.824	A
		LNK6xx4	di/dt = 245 mA/µs T_J = +25 °C	0.967	1.04	1.113	
		LNK6xx5	di/dt = 305 mA/µs T_J = +25 °C	1.209	1.30	1.391	
		LNK6xx6	di/dt = 460 mA/µs T_J = +25 °C	1.814	1.95	2.087	
		LNK6xx7	di/dt = 610 mA/µs T_J = +25 °C	2.418	2.60	2.782	
		LNK6xx8	di/dt = 705 mA/µs T_J = +25 °C	2.790	3.00	3.210	
		LNK6xx9	di/dt = 800 mA/µs T_J = +25 °C	3.162	3.40	3.638	
Programmed Current Limit Variation	ΔI_{LIMIT}	See Table 3 for programming 0 °C ≤ T_J ≤ +100 °C, See Note A				±7	%
Operational Peak Current Variation	$\Delta I_{PK(OP)}$	$I_{PK(OP)}$ = 25 -100% × I_{LIMIT}, 0 °C ≤ T_J ≤ +100 °C, See Note A				±7	%
Thermal Shutdown Temperature	T_{SD}			135	142	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	C_{BP} = 0.47 µF or C_{BP} = 4.7 µF			75		°C
Leading Edge Blanking Time	t_{LEB}	T_J = +25 °C See Note A		175	220		ns
Current Limit Delay Time	t_{ILD}	T_J = +25 °C			100		ns

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Minimum Switch ON-Time	$T_{ON(MIN)}$	$t_{LEB(MAX)} + t_{ILD(MAX)}$ T_J = +25 °C		325	400	500	ns
Output							
ON-State Resistance	$R_{DS(ON)}$	LNK6xx3 I_D = 100 mA	T_J = +25 °C		6.9	7.97	Ω
			T_J = +100 °C		10.5	12.08	
		LNK6xx4 I_D = 150 mA	T_J = +25 °C		4.6	5.30	
			T_J = +100 °C		7.0	8.09	
		LNK6xx5 I_D = 200 mA	T_J = +25 °C		3.5	4.03	
			T_J = +100 °C		5.4	6.21	
		LNK6xx6 I_D = 300 mA	T_J = +25 °C		2.3	2.65	
			T_J = +100 °C		3.6	4.14	
		LNK6xx7 I_D = 400 mA	T_J = +25 °C		1.8	2.07	
			T_J = +100 °C		2.7	3.11	
		LNK6xx8 I_D = 500 mA	T_J = +25 °C		1.5	1.95	
			T_J = +100 °C		2.3	2.90	
		LNK6xx9 I_D = 600 mA	T_J = +25 °C		1.3	1.70	
			T_J = +100 °C		2.0	2.60	
OFF-State Drain Leakage Current	I_{DSS}	V_{PD} = Floating	V_{DS} = 560 V, T_J = 125 °C			470	µA
			V_{DS} = 325 V, T_J = 100 °C			10	
Breakdown Voltage	BV_{DSS}	LNK677x, V_{PD} = Floating, T_J = +25 °C		725			V
		LNK666x/LNK676x, V_{PD} = Floating, T_J = +25 °C		650			
DRAIN Supply Voltage				50			V
Rise Time	t_R	Measured in a typical flyback Converter application			100		ns
Fall Time	T_F				50		

NOTES:
A. Parameter not tested over specified temperature range. Guaranteed by design and characterization.
B. Average device switching frequency below 1 kHz.

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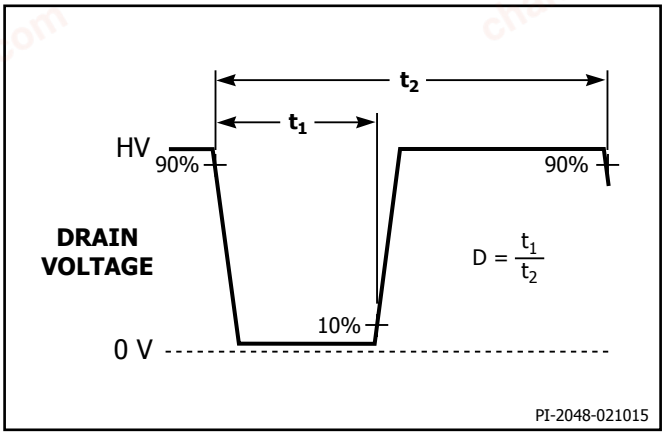


Figure 16. Duty Cycle Measurement.

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Typical Performance Characteristics

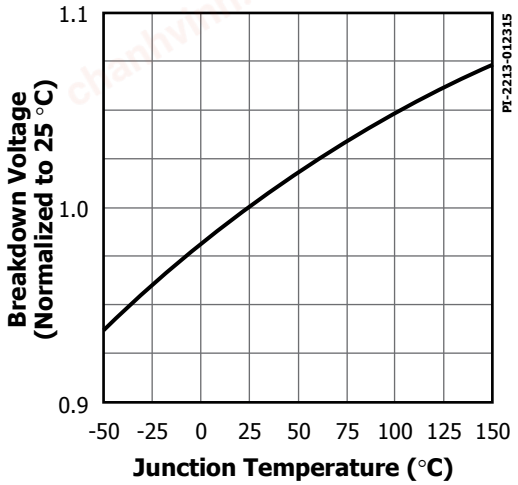


Figure 17. Breakdown vs. Temperature.

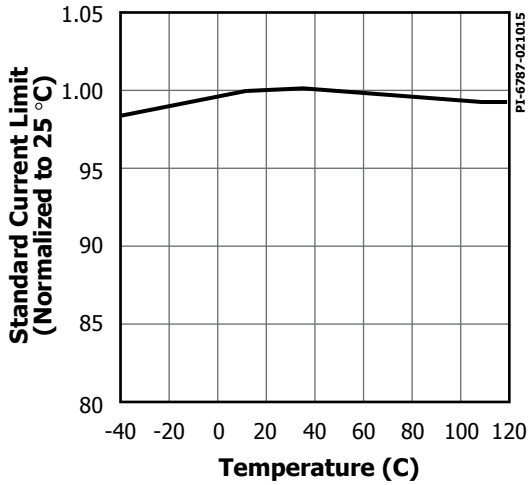


Figure 18. Standard Current Limit vs. Temperature.

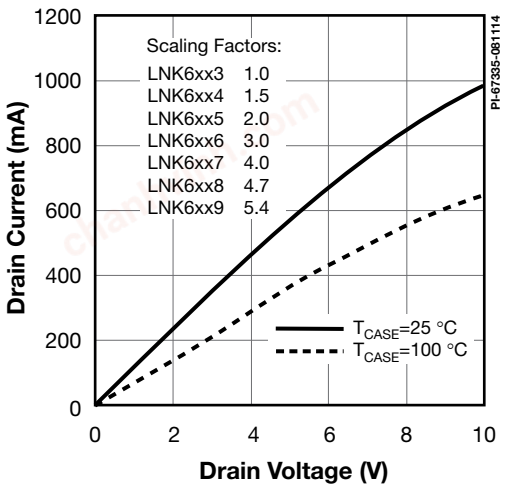


Figure 19. Output Characteristic.

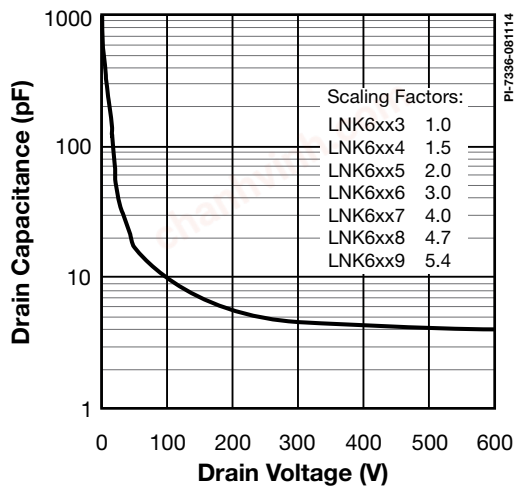


Figure 20. C_{OSS} vs. Drain Voltage.

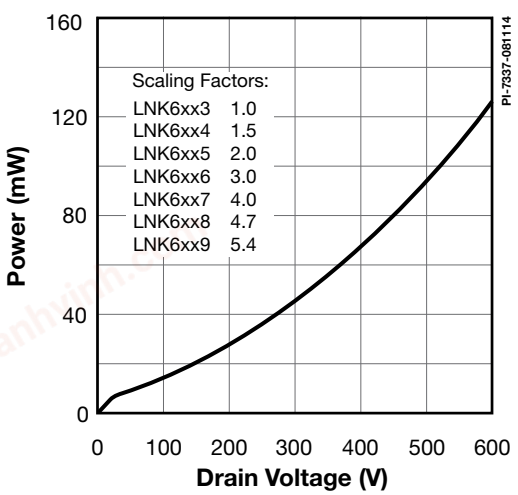


Figure 21. Drain Capacitance Power.

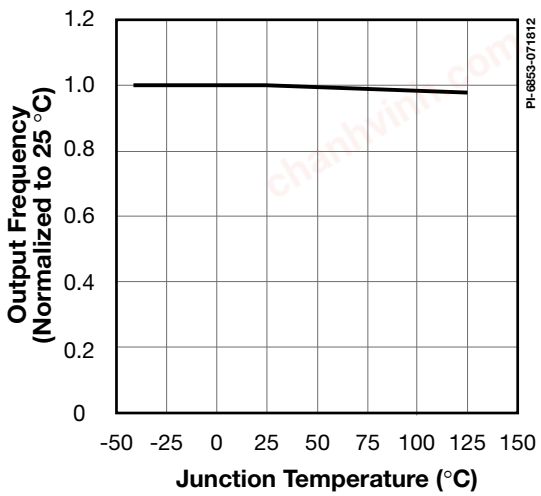


Figure 22. Frequency vs. Temperature.

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Typical Performance Characteristics

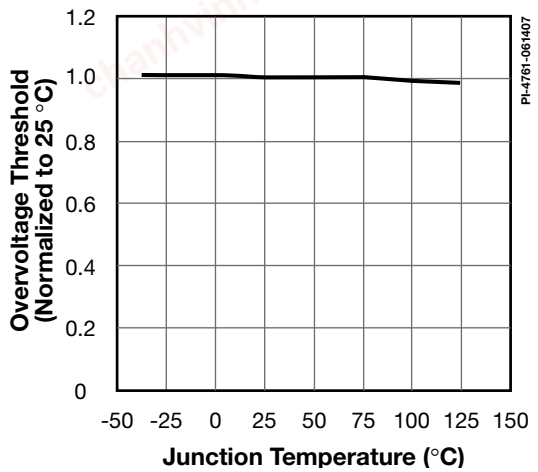


Figure 23. Overvoltage Threshold vs. Temperature.

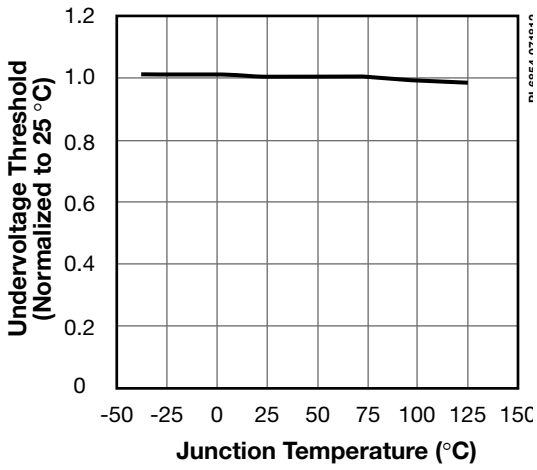


Figure 24. Undervoltage Threshold vs. Temperature.

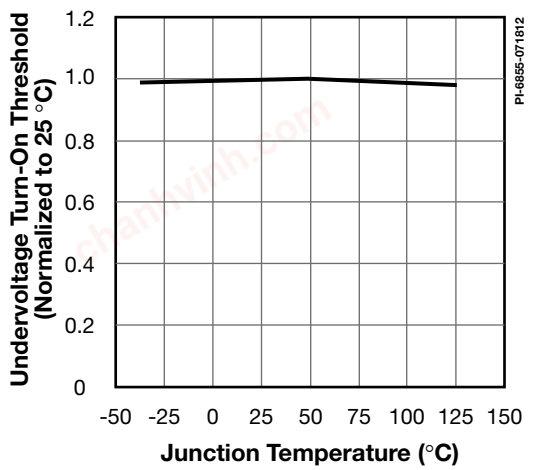


Figure 25. Undervoltage Threshold vs. Temperature.

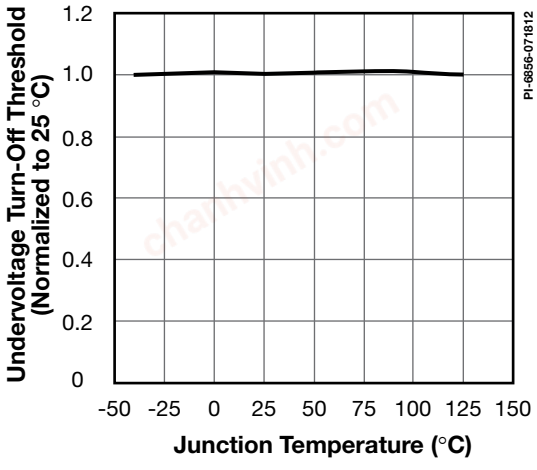


Figure 26. Undervoltage Threshold vs. Temperature.

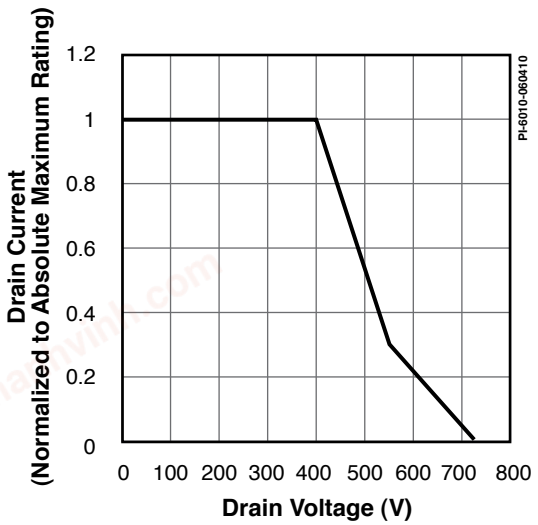


Figure 27. Maximum Allowable Drain Current vs. Drain Voltage (LNK6773-6779).

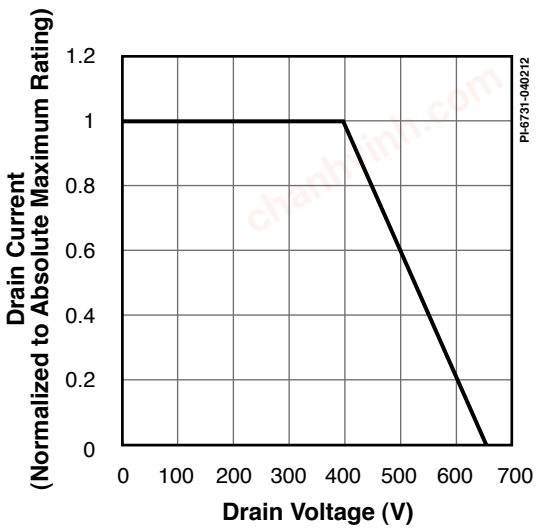
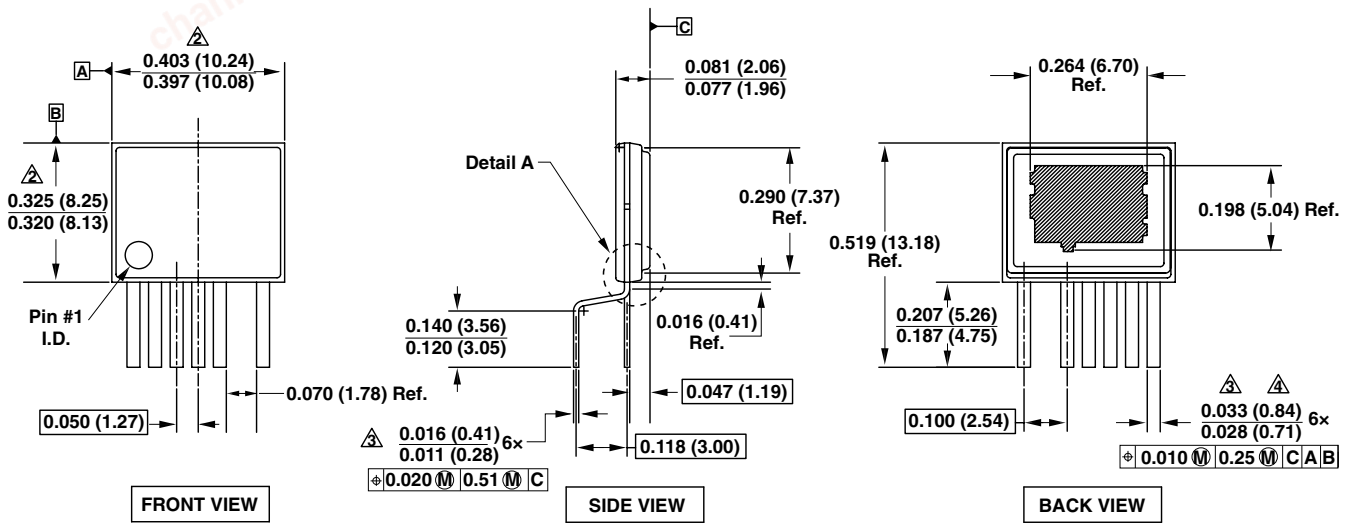
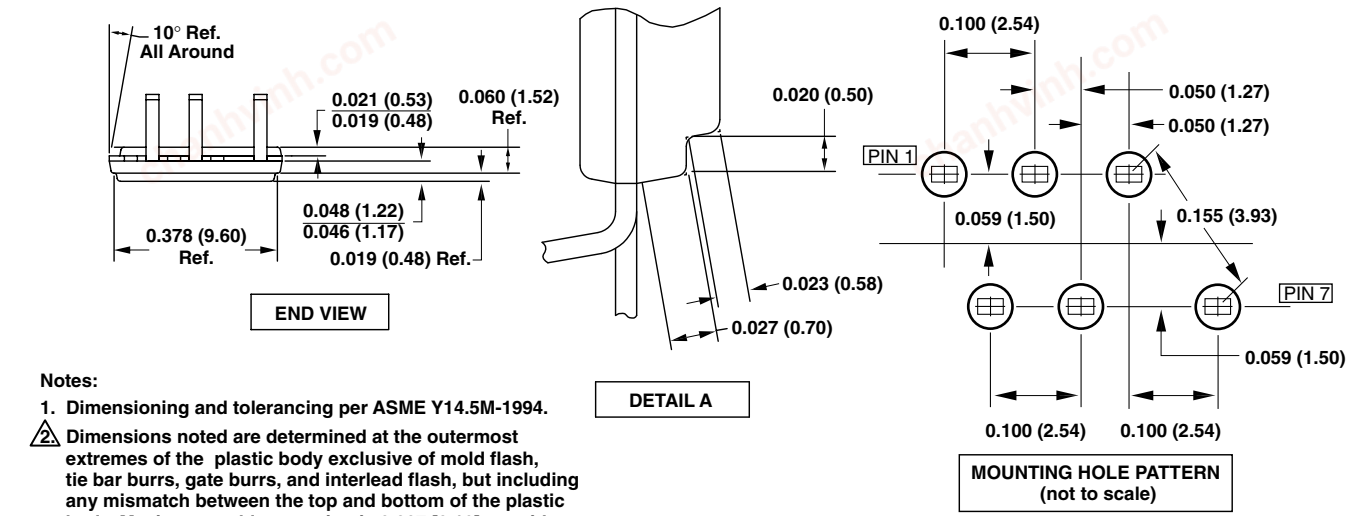


Figure 28. Maximum Allowable Drain Current vs. Drain Voltage (LNK6763-6769/LNK6663-6669).

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eSIP-7C (E Package)





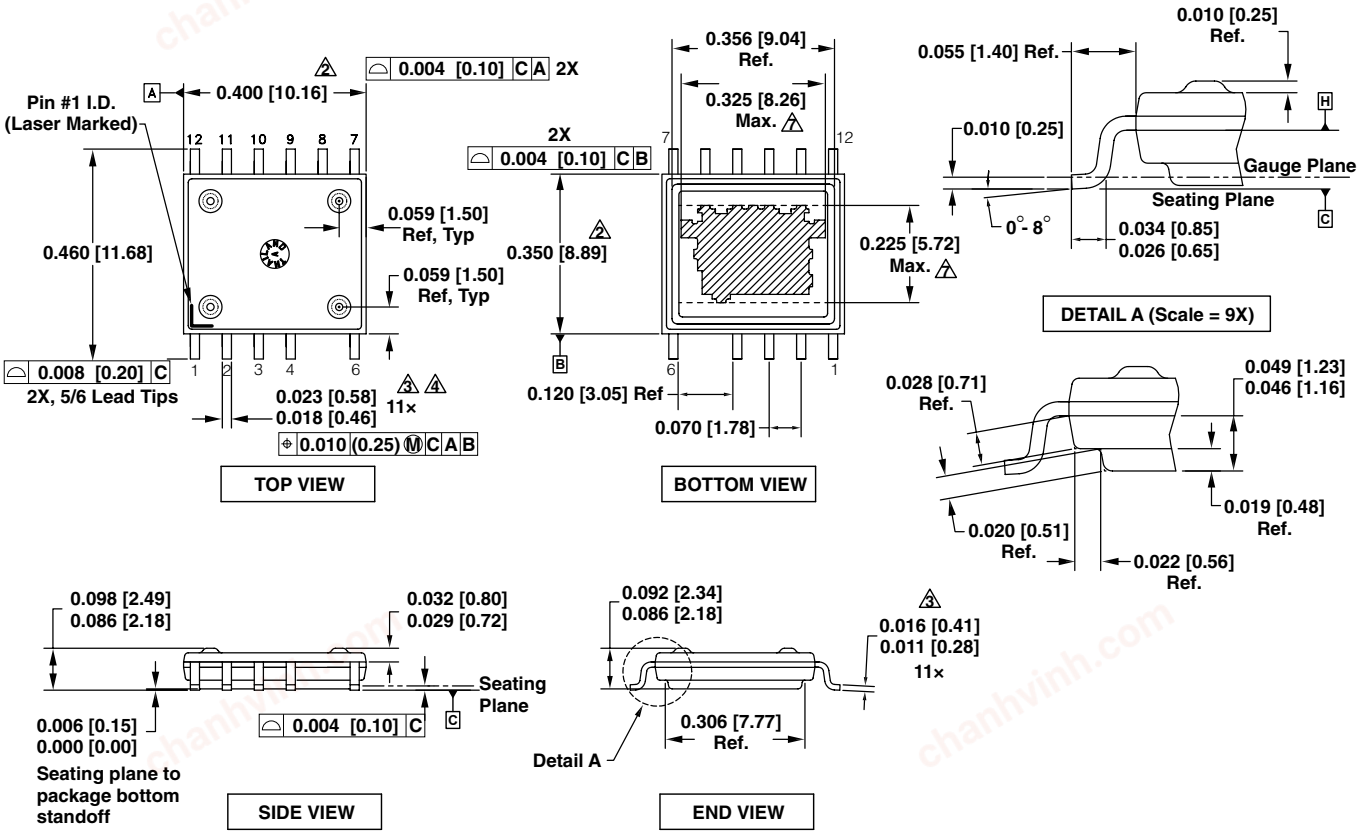
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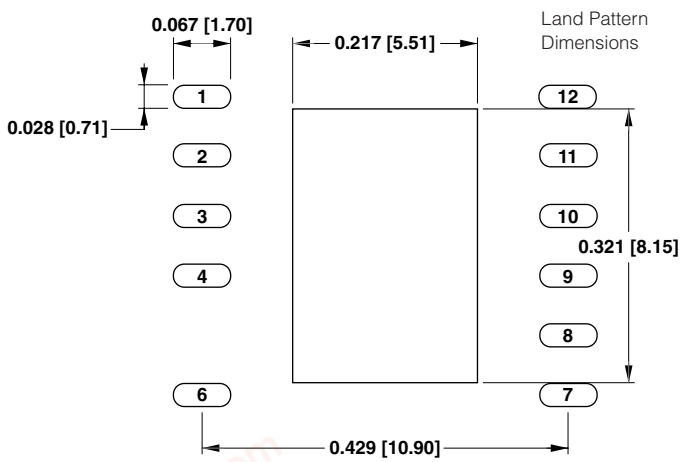
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

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eSOP-12B (K Package)





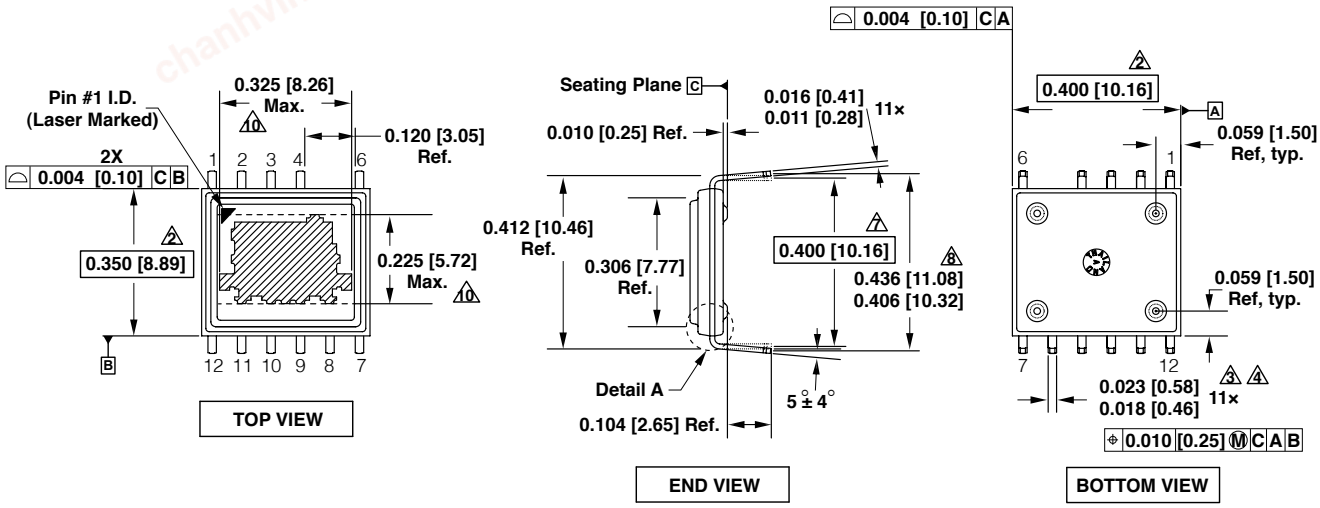
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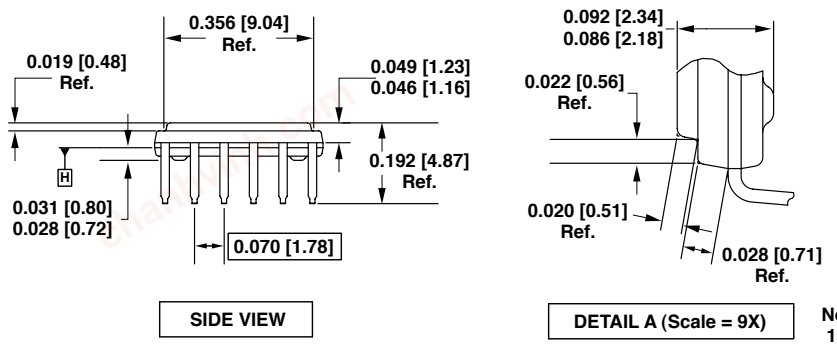
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Exposed pad is nominally located at the centerline of Datums A and B. “Max” dimensions noted include both size and positional tolerances.

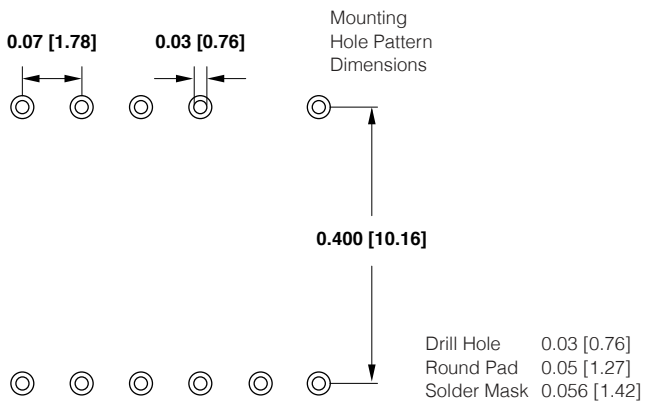
PI-5748a-100311

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eDIP-12B (V Package)







Notes:

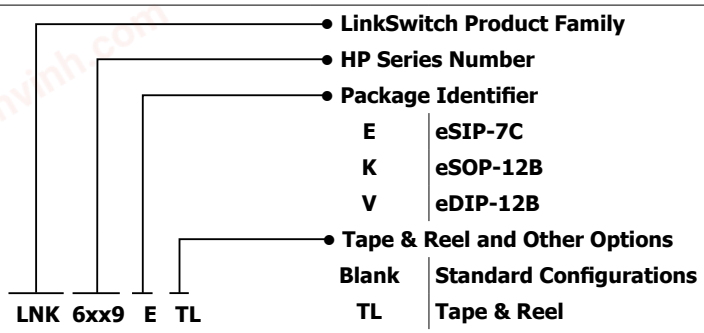
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Measured with the leads constrained to be perpendicular to Datum C.
8. Measured with the leads unconstrained.
9. Lead numbering per JEDEC SPP-012.
10. Exposed pad is nominally located at the centerline of Datums A and B. “Max” dimensions noted include both size and positional tolerances.

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Revision	Notes	Date
A	Initial Release.	08/12
A	Updated Table 2.	08/23/12
A	Updated page 5.	10/24/12
B	Formatting changes. K_{PS} Min value updated.	12/04/12
B	Fixed Table references.	02/26/13
C	Released K package parts. Updated $\Delta V_{FB(th)}$ Typ value on page 14.	03/14
D	Added part size 8 and 9.	08/14
E	Updated with new logo Brand Style.	06/15
F	Added Min and Max values for C_{BP}.	02/21
G	Updated Layout Considerations section, pages 10 and 12 updated Figures 14 and 15.	11/22

Part Ordering Information



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