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LinkSwitch-TN2 Family

Highly Energy Efficient Off-line Switcher IC with Integrated System Level Protection for Low Component-Count Power Supplies

Product Highlights

Highest Performance and Design Flexibility

- Supports buck, buck-boost and flyback topologies
- Excellent load and line regulation
- Selectable device current limit
- 66 kHz operation with accurate current limit
  - Allows the use of low-cost off-the-shelf inductors
  - Reduces size and cost of magnetics and output capacitor
- Frequency jittering reduces EMI filter complexity
- Pin-out simplifies PCB heat sinking

Enhanced Safety and Reliability Features

- Auto-restart for short-circuit and open loop faults
- Output overvoltage protection (OVP)
- Line input overvoltage protection (OVL)
- Hysteretic over-temperature protection (OTP)
- Extended creepage between DRAIN pin and all other pins improves field reliability
- 725 V MOSFET rating for excellent surge withstand
- 900 V MOSFET rating series for industrial or extra safety margin

EcoSmart™– Extremely Energy Efficient

- Standby supply current <100 µA
- On/Off control provides constant efficiency over a wide load range
- Easily meets all global energy efficiency regulations
- No-load consumption <30 mW with external bias

Applications

- Appliances
- Metering
- Smart LED drivers and industrial controls
- IOT, home and building automation

Description

The LinkSwitch™-TN2 family of ICs for non-isolated off-line power supplies provides dramatically improved performance compared to traditional linear or cap-dropper solutions. Designs using the highly integrated LinkSwitch-TN2 ICs are more flexible and feature increased efficiency, comprehensive system level protection and higher reliability. The device family supports buck, buck-boost and flyback converter topologies. Each device incorporates a 725 V / 900 V power MOSFET, oscillator, On/Off control for highest efficiency at light load, a high-voltage switched current source for self-biasing, frequency jittering, fast (cycle-by-cycle) current limit, hysteretic thermal shutdown, and output and input overvoltage protection circuitry onto a monolithic IC.

LinkSwitch-TN2 ICs consume very little current in standby resulting in power supply designs that meet all no-load and standby specifications worldwide. MOSFET current limit modes can be selected through the BYPASS pin capacitor value. The high current limit level provides maximum continuous output current while the low level permits using very low cost and small surface mount inductors. A full suite of protection features enables safe and reliable power supplies protecting the device and the system against input and output overvoltage faults, device over-temperature faults, lost regulation, and power supply output overload or short-circuit faults.

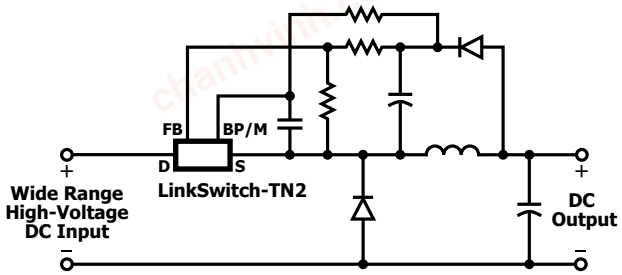


Figure 1. Typical Buck Converter Application (See Application Examples Section for Other Circuit Configurations).



Figure 2. Package Options. P: PDIP-8C, G: SMD-8C, D: SO-8C.

Output Current Table[1]

Product[4]	725 V MOSFET			
	230 VAC ±15%		85-265 VAC	
	MDCM[2]	CCM[3]	MDCM[2]	CCM[3]
LNK3202P/G/D	63 mA	80 mA	63 mA	80 mA
LNK3204P/G/D	120 mA	170 mA	120 mA	170 mA
LNK3205P/G/D	175 mA	270 mA	175 mA	270 mA
LNK3206P/G/D	225 mA	360 mA	225 mA	360 mA
LNK3207P/G/D	360 mA	575 mA	360 mA	575 mA
LNK3208P/G/D	485 mA	775 mA	485 mA	775 mA
LNK3209P/G/D	600 mA	1000 mA	600 mA	1000 mA
Product[4]	900 V MOSFET			
	230 VAC ±15%		85-265 VAC	
	MDCM[2]	CCM[3]	MDCM[2]	CCM[3]
LNK3294P/G	120 mA	170 mA	120 mA	170 mA
LNK3296P/G	225 mA	360 mA	225 mA	360 mA

Table 1. Output Current Table.

Notes:
1. Typical output current in a non-isolated buck converter with devices operating at default current limit and adequate heat sinking. Output power capability depends on respective output voltage and thermal requirements. See Key Applications Considerations Section for complete description of assumptions, including fully discontinuous conduction mode (DCM) operation.
2. Mostly discontinuous conduction mode.
3. Continuous conduction mode.
4. Packages: P: PDIP-8C, G: SMD-8C, D: SO-8C.

The device family is available in three different packages: PDIP-8C, SO-8C, and SMD-8C (725 V PNs only).

This Product is Covered by Patents and/or Pending Patent Applications.

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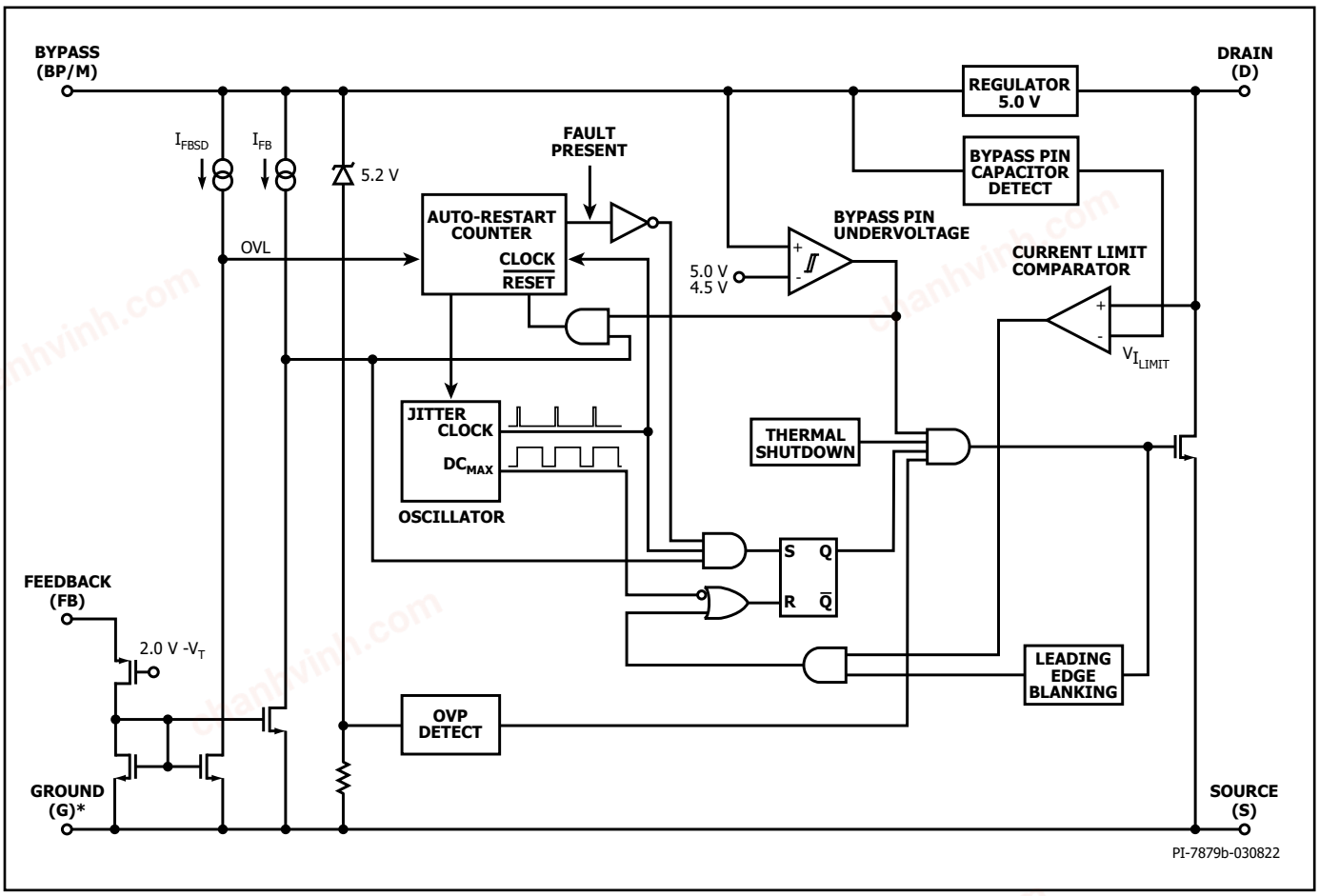


Figure 3. Functional Block Diagram. (*Only size 8 P/G Package)

Pin Functional Description

DRAIN (D) Pin:
Power MOSFET drain connection. Provides internal operating current for both start-up and steady-state operation.

BYPASS (BP/M) Pin:
This pin has multiple functions:

- It is the connection point for an external bypass capacitor for the internally generated 5.0 V supply.
- It is a mode selector for the current limit value, depending on the value of the capacitance added. Use of a 0.1 µF capacitor results in the standard current limit value. Use of a 1 µF capacitor results in the current limit being reduced, allowing design with lowest cost surface mount buck chokes.
- It provides a shutdown function. When the current into the BYPASS pin exceeds I_{BPSD} for a time equal to 2 to 3 cycles of the internal oscillator (f_{OSC}), the device enters auto-restart. This can be used to provide an output overvoltage protection function with external circuitry.

FEEDBACK (FB) Pin:
During normal operation, switching of the power MOSFET is controlled by the FEEDBACK pin. MOSFET switching is terminated when a current greater than I_{FB} (49 µA) is delivered into this pin. Line overvoltage protection is detected when a current greater than I_{FBSD} (670 µA) is delivered into this pin for 2 consecutive switching cycles.

SOURCE (S) Pin:
This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS and FEEDBACK pins.

GROUND (G) Pin:
Size LNK3208/9 P/G package only.
Ground reference for the BYPASS and FEEDBACK.

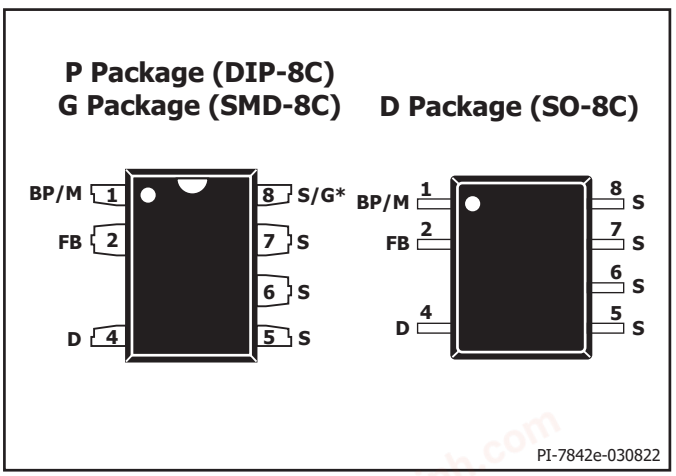


Figure 4. Pin Configuration. (*G for size LNK3208/9)

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LinkSwitch-TN2 Functional Description

LinkSwitch-TN2 combines a high-voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (pulse width modulator) controllers, LinkSwitch-TN2 uses a simple ON/OFF control to regulate the output voltage. The LinkSwitch-TN2 controller consists of an oscillator, feedback (sense and logic) circuit, 5.0 V regulator, BYPASS pin undervoltage circuit, over-temperature protection, line and output overvoltage protection, frequency jittering, current limit circuit, leading edge blanking and a 725 V or 900 V power MOSFET. The LinkSwitch-TN2 incorporates additional circuitry for auto-restart.

Oscillator

The typical oscillator frequency is internally set to an average of f_{OSC} (66 kHz). Two signals are generated from the oscillator: the maximum duty cycle signal ($DC_{(MAX)}$) and the clock signal that indicates the beginning of each cycle.

The LinkSwitch-TN2 oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 4 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 5 illustrates the frequency jitter of the LinkSwitch-TN2.

Soft-Start

At power-up or during a restart attempt in auto-restart, the device applies a soft-start by temporarily reducing the oscillator frequency. LNK3202-07 and LNK329x reduce the frequency to $f_{OSC(SS)}$ (typically 33 kHz. LNK3208 and LNK3209 reduce the oscillator frequency to initially 16.5 kHz followed by a stepwise increase to 22 kHz and 33 kHz over a period of 256 switching cycles. Soft-start terminates and the device continues operating at the nominal oscillator frequency f_{OSC} either after 256 switching cycles or if the output voltage reaches regulation.

Feedback Input Circuit

The feedback input circuit at the FEEDBACK pin consists of a low impedance source follower output set at V_{FB} (2.0 V). When the current delivered into this pin exceeds I_{FB} (49 µA), a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). The sampling is done only at the beginning of each cycle. Subsequent changes in the FEEDBACK pin voltage or current during the remainder of the cycle do not impact the MOSFET enable/disable status. If a current greater than I_{FBSD} is injected into the feedback pin while the MOSFET is enabled for at least two consecutive cycles the part will stop switching and enter auto-restart off-time. Normal switching resumes after the auto-restart off-time expires. This shutdown function allows implementing line overvoltage protection in flyback converters (see Figure 6). The current into the FEEDBACK pin should be limited to less than 1.2 mA.

5.0 V Regulator and 5.2 V Shunt Voltage Clamp

The 5.0 V regulator charges the bypass capacitor connected to the BYPASS pin to V_{BP} by drawing a current from the voltage on the DRAIN, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node for the LinkSwitch-TN2. When the MOSFET is on, the LinkSwitch-TN2 runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the LinkSwitch-TN2 to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 µF is sufficient for both high frequency decoupling and energy storage.

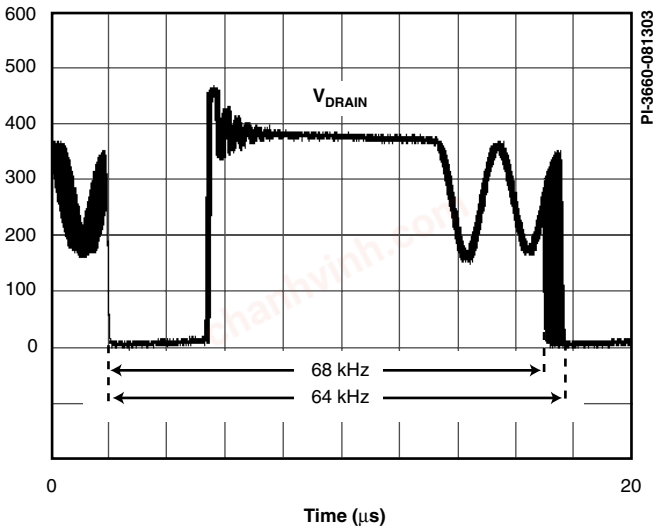


Figure 5. Frequency Jitter.

In addition, there is a shunt regulator clamping the BYPASS pin at $V_{BP(SHUNT)}$ (5.2 V) when current is provided to the BYPASS pin through an external resistor. This facilitates powering of LinkSwitch-TN2 externally through a bias winding to decrease the no-load consumption to about 10 mW (flyback). The device stops switching instantly and enters auto-restart when a current $\geq I_{BPSD}$ is delivered into the BYPASS pin. Adding an external Zener diode from the output voltage to the BYPASS pin allows implementing an hysteretic OVP function in a flyback converter (see Figure 6). The current into the BYPASS pin should be limited to less than 16 mA.

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below $V_{BP}–V_{BPH}$ (approximately 4.5 V). Once the BYPASS pin voltage drops below this threshold, it must rise back to V_{BP} to enable (turn-on) the power MOSFET.

Over-Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is set at T_{SD} (142 °C typical) with a 75 °C (T_{SDH}) hysteresis. When the die temperature rises above T_{SD} the power MOSFET is disabled and remains disabled until the die temperature falls to $T_{SD}–T_{SDH}$, at which point it is re-enabled.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the switching pulse. Current limit can be selected using the BYPASS pin capacitor (0.1 µF for normal current limit / 1 µF for reduced current limit). LinkSwitch-TN2 selects between normal and reduced current limit at power-up prior to switching.

Auto-Restart

In the event of a fault condition such as output overload, output short, or an open-loop condition, LinkSwitch-TN2 enters into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the FEEDBACK pin is pulled high. If the FEEDBACK pin is not pulled high for $t_{AR(ON)}$ (50 ms), the power MOSFET switching is disabled for a time equal to the auto-restart off-time. The first time a fault is asserted the off-time is 150 ms

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($t_{AR(OFF)}$ First Off Period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ Subsequent Periods). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. The auto-restart counter is gated by the switch oscillator.

Hysteretic Output Overvoltage Protection

The output overvoltage protection provided by the LinkSwitch-TN2 IC uses auto-restart that is triggered by a current >I_{BPSD} into the BYPASS pin. In addition to an internal filter, the BYPASS pin capacitor forms an external filter providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and BYPASS pins of the device.

The OVP function can be realized in a flyback converter by connecting a Zener diode from the output supply to the BYPASS pin. The circuit example shown in Figure 6 describes a simple method for implementing the output overvoltage protection. Adding additional filtering can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the OVP Zener diode. The resistor in series with the OVP Zener diode also limits the maximum current into the BYPASS pin. The current should be limited to less than 16 mA.

During a fault condition resulting from loss of feedback, the output voltage will rapidly rise above the nominal voltage. A voltage at the output that exceeds the sum of the voltage rating of the Zener diode connected from the output to the BYPASS pin and bypass voltage, will cause a current in excess of I_{BPSD} injected into the BYPASS pin, which will trigger the auto-restart and protect the power supply from overvoltage.

Line Overvoltage Protection

In a flyback converter LinkSwitch-TN2 can sense indirectly the DC bus overvoltage condition during the power MOSFET on-time by monitoring the current flowing into the FEEDBACK pin depending on circuit configuration. Figure 7 shows one possible circuit implementation. During the MOSFET on-time, the voltage across the secondary winding is proportional to the voltage across the primary winding. The current flowing through emitter and base of transistor Q3 is therefore representing V_{BUS}. Indirect line sensing minimizes power dissipation and is used for line OV protection. The LinkSwitch-TN2 will go into auto- auto-restart mode if the FEEDBACK pin current exceeds the line overvoltage threshold current I_{FBSD} for at least 2 consecutive switching cycles.

In order to have accurate line OV threshold voltage and also for good efficiency, regulation performance and stability, the transformer leakage inductance should be minimized. Low leakage will minimize ringing on the secondary winding and provide accurate line OVP sampling. In some designs, a RC snubber across the rectifier diode may be needed to damp the ringing at the secondary winding when line voltage is sampled.

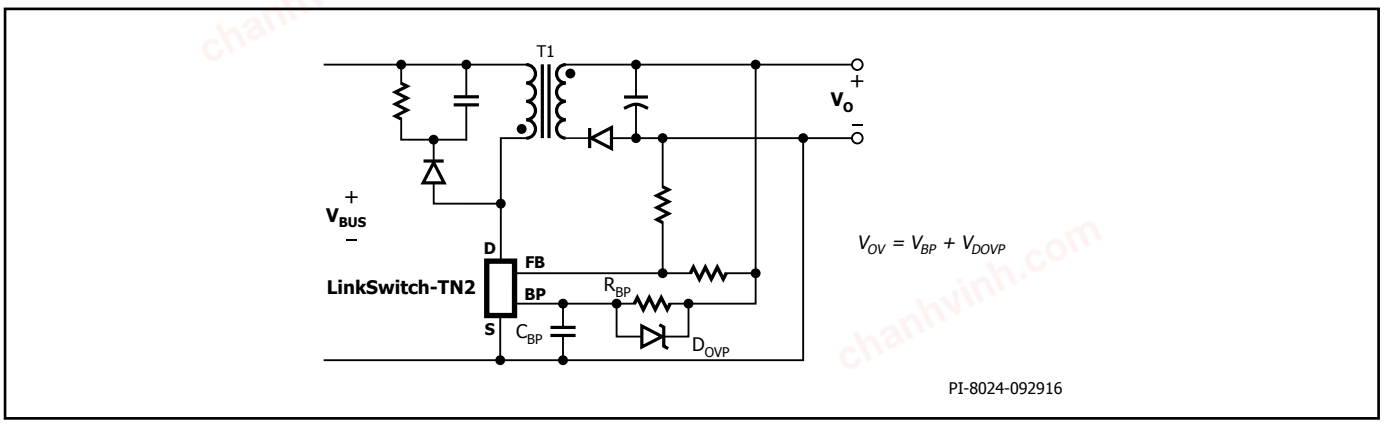


Figure 6. Non-Isolated Flyback Converter with Output Overvoltage Protection.

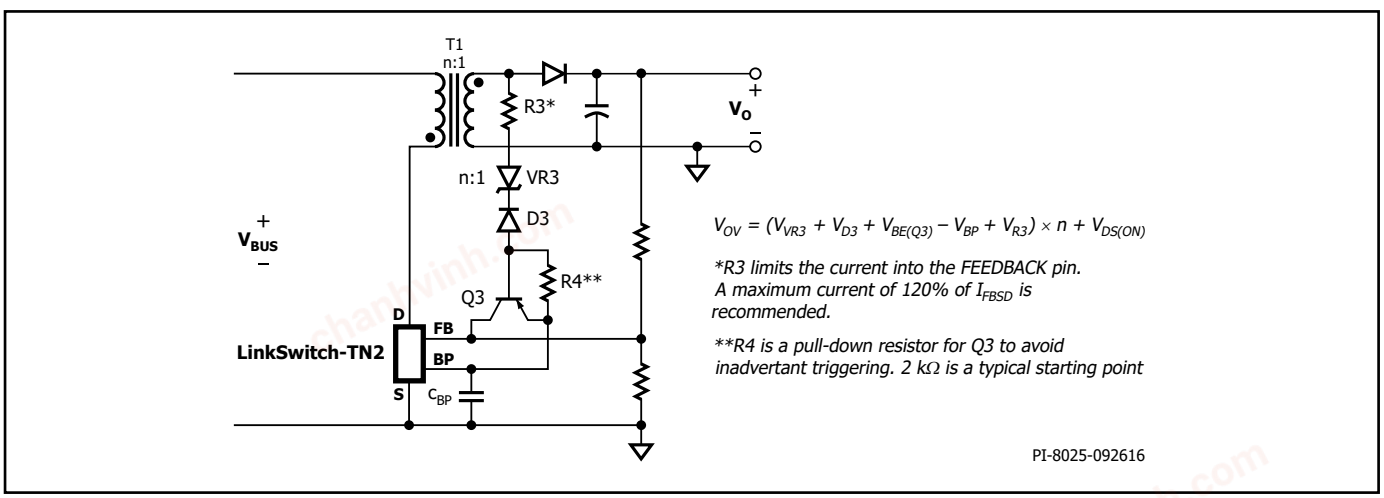


Figure 7. Line-Sensing for Overvoltage Protection by using FEEDBACK Pin.

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Applications Example

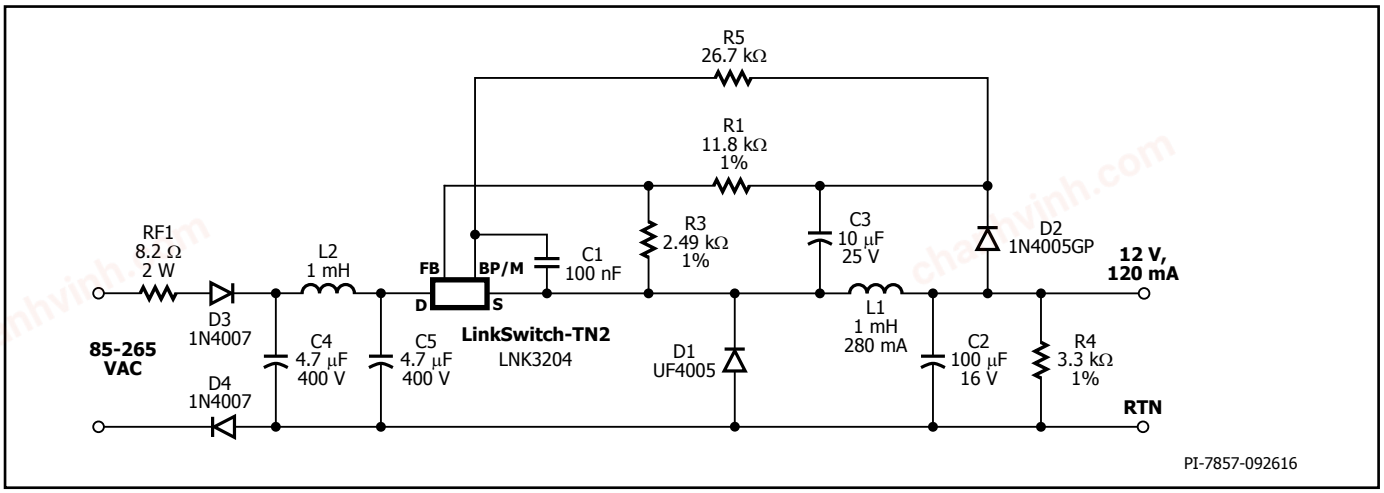


Figure 8. Universal Input, 12 V, 120 mA Constant Voltage Power Supply using LinkSwitch-TN2.

A 1.44 W Universal Input Buck Converter

The circuit shown in Figure 8 is a typical implementation of a 12 V, 120 mA non-isolated power supply used in appliance control such as rice cookers, dishwashers or other white goods. This circuit may also be applicable to other applications such as night-lights, LED drivers, electricity meters, and residential heating controllers, where a non-isolated supply is acceptable.

The input stage comprises fusible resistor RF1, diodes D3 and D4, capacitors C4 and C5, and inductor L2. Resistor RF1 is a flame proof, fusible, wire wound resistor. It accomplishes several functions:

A. Inrush current limitation to safe levels for rectifiers D3 and D4;
B. Differential mode noise attenuation;
C. Acts as an input fuse in the event any other component fails short-circuit (component fails safely open-circuit without emitting smoke, fire or incandescent material).

The power processing stage is formed by the LinkSwitch-TN2, freewheeling diode D1, output choke L1, and the output capacitor C2. The LNK3204 was selected such that the power supply operates in the mostly discontinuous-mode (MDCM). Diode D1 is an ultrafast diode with a reverse recovery time (t_{RR}) of approximately 75 ns, acceptable for MDCM operation. For continuous conduction mode (CCM) designs, a diode with a t_{RR} of ≤35 ns is recommended. Inductor L1 is a standard off-the-shelf inductor with appropriate RMS current rating (and acceptable temperature rise). Capacitor C2 is the output filter capacitor; its primary function is to limit the output voltage ripple. The output voltage ripple is a stronger function of the ESR of the output capacitor than the value of the capacitor itself. Optional resistor R5 supplies the BYPASS pin externally for significantly lower no-load input power and increased efficiency over all load conditions.

To a first order, the forward voltage drops of D1 and D2 are identical. Therefore, the voltage across C3 tracks the output voltage. The voltage developed across C3 is sensed and regulated via the resistor divider R1 and R3 connected to U1's FEEDBACK pin. The values of R1 and R3 are selected such that, at the desired output voltage, the voltage at the FEEDBACK pin is 2.00 V.

Regulation is maintained by skipping switching cycles. As the output voltage rises, the current into the FEEDBACK pin will rise. If this exceeds I_{FB} then subsequent cycles will be skipped until the current reduces below I_{FB}. Thus, as the output load is reduced, more cycles will be skipped and if the load increases, fewer cycles are skipped. To provide overload protection if no cycles are skipped during a 50 ms period, LinkSwitch-TN2 will enter auto-restart, limiting the average output power to approximately 3% of the maximum overload power. Due to tracking errors between the output voltage and the voltage across C3 at light load or no-load, a small pre-load may be required (R4). For the design in Figure 8, if regulation to zero load is required, then this value should be reduced to 2.4 kΩ.

Key Application Considerations

LinkSwitch-TN2 Design Considerations

Output Current Table

Data sheet maximum output current table (Table 1) represents the typical practical continuous output current for both mostly discontinuous conduction mode (MDCM) and continuous conduction mode (CCM) of operation that can be delivered from a given LinkSwitch-TN2 device under the following assumed conditions:

1. Buck converter topology.
2. The minimum DC input voltage is ≥70 V. The value of input capacitance should be large enough to meet this criterion.
3. For CCM operation a KRP* of 0.4.
4. Output voltage of 12 VDC.
5. Efficiency of 75%.
6. A catch/freewheeling diode with t_{RR} ≤75 ns is used for MDCM operation and for CCM operation, a diode with t_{RR} ≤35 ns is used.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 100 °C.

*KRP is the ratio of ripple to peak inductor current.

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LinkSwitch-TN2 Selection and Selection Between MDCM and CCM Operation

Select the LinkSwitch-TN2 device, freewheeling diode and output inductor that gives the lowest overall cost. In general, MDCM provides the lowest cost and highest efficiency converter. CCM designs require a larger inductor and ultrafast (t_{RR} ≤35 ns) freewheeling diode in all cases. It is lower cost to use a larger LinkSwitch-TN2 in MDCM than a smaller LinkSwitch-TN2 in CCM because of the additional external component costs of a CCM design. However, if the highest output current is required, CCM should be employed following the guidelines below.

Topology Options

LinkSwitch-TN2 can be used in all common topologies, with or without an optocoupler and reference to improve output voltage tolerance and regulation. Table 2 provides a summary of these configurations. For more information see the Application Note – LinkSwitch-TN2 Design Guide.

Component Selection

Referring to Figure 8, the following considerations may be helpful in selecting components for a LinkSwitch-TN2 design.

BYPASS Pin Capacitor C1

Capacitor connected from the BYAPSS pin provides decoupling for the controller and also selects current limit. A 0.1 μF or 1 μF capacitor may be used as indicated in the data sheet. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use as they enable placement of capacitors close to the IC and design of compact switching power supplies. 16 V, 25 V or higher X7R dielectric capacitors are recommended to ensure minimum capacitance change under DC bias and temperature.

Freewheeling Diode D1

Diode D1 should be an ultrafast type. For MDCM, reverse recovery time t_{RR} ≤75 ns should be used at a temperature of 70 °C or below. Slower diodes are not acceptable, as continuous mode operation will always occur during startup, causing high leading edge current spikes, terminating the switching cycle prematurely, and preventing the output from reaching regulation. If the ambient temperature is above 70 °C then a diode with t_{RR} ≤35 ns should be used.

For CCM an ultrafast diode with reverse recovery time t_{RR} ≤35 ns should be used. A slower diode may cause excessive leading edge current spikes, terminating the switching cycle prematurely and preventing full power delivery.

Fast recovery and slow recovery diodes should never be used as the large reverse recovery currents can cause excessive power dissipation in the diode and/or exceed the maximum drain current specification of LinkSwitch-TN2.

Feedback Diode D2

Diode D2 can be a low-cost slow diode such as the 1N400X series, however it should be specified as a glass passivated type to guarantee a specified reverse recovery time. To a first order, the forward drops of D1 and D2 should match.

Inductor L1

Choose any standard off-the-shelf inductor that meets the design requirements. A "drum" or "dog bone" "I" core inductor is recommended with a single ferrite element due to its low-cost and very low audible noise properties. However, the inductor should be selected as varnished type in order to get low audible noise. The typical inductance value and RMS current rating can be obtained from the LinkSwitch-TN2 design spreadsheet available within the PI Expert design suite from Power Integrations. Choose L1 greater than or equal to the typical calculated inductance with RMS current rating greater than or equal to calculated RMS inductor current. Care should be taken to ensure that the inductor has sufficient voltage rating as this is a high-voltage application.

Capacitor C2

The primary function of capacitor C2 is to smooth the inductor current. The actual output ripple voltage is a function of this capacitor's ESR. To a first order, the ESR of this capacitor should not exceed the rated ripple voltage divided by the typical current limit of the chosen LinkSwitch-TN2.

Feedback Resistors R1 and R3

The values of the resistors in the resistor divider formed by R1 and R3 are selected to maintain 2.00 V at the FEEDBACK pin. It is recommended that R3 be chosen as a standard 1% resistor of 2.49 kΩ. This ensures good noise immunity by biasing the feedback network with a current of approximately 0.8 mA.

External Bias Resistor R5

To reduce the no-load input power of the power supply, resistor R5, connected from the feedback capacitor C3 to the BYPASS pin, is recommended. This is applicable to the power supply whose output voltage is higher than $V_{BP(SHUNT)}$. To achieve lowest no-load power consumption, the current fed into the BYPASS pin should be slightly higher than 120 μA. For the best full load efficiency and thermal performance, the current fed into the BYPASS pin should be slightly higher than the I_{S2} Max value.

Feedback Capacitor C3

Capacitor C3 can be a low cost general purpose capacitor. It provides a "sample and hold" function, charging to the output voltage during the off time of LinkSwitch-TN2. Its value should be 10 μF to 22 μF; smaller values cause poorer regulation at light load conditions.

Pre-Load Resistor R4

In high-side, direct feedback designs where the minimum load is <3 mA, a pre-load resistor is required to maintain output regulation. This ensures sufficient inductor energy to pull the inductor side of the feedback capacitor C3 to input return via D2. The value of R4 should be selected to provide a minimum output load of 3 mA.

In designs with an optocoupler a Zener diode or reference bias current provides a 1 mA to 2 mA minimum load, preventing "pulse bunching" and increased output ripple at zero load.

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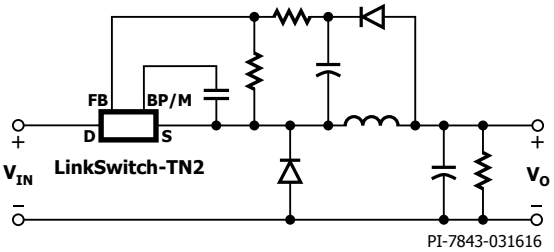
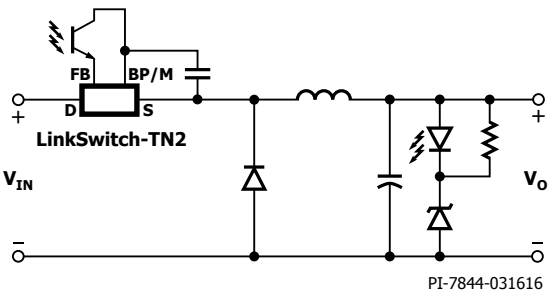
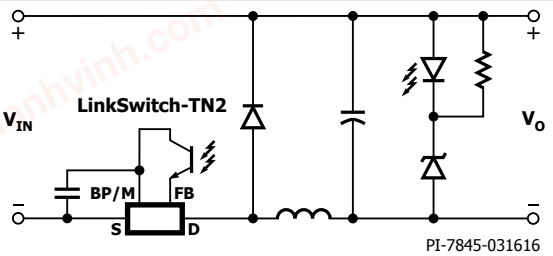
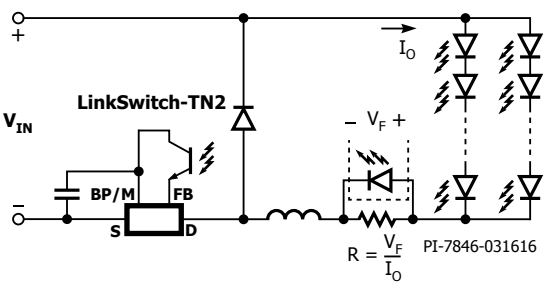
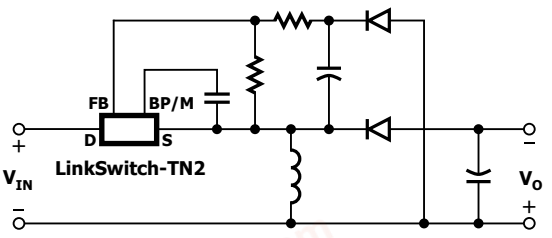
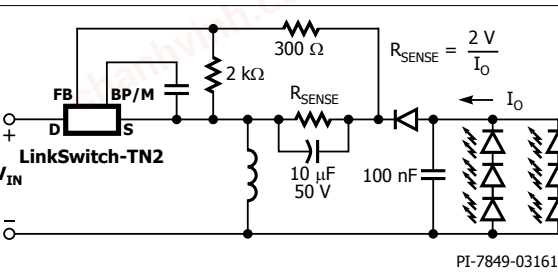
Topology	Basic Circuit Schematic	Key Features
High-Side Buck – Direct Feedback		1. Output referenced to input 2. Positive output (V_O) with respect to $-V_{IN}$ 3. Step down – $V_O < V_{IN}$ 4. Low cost direct feedback (±10% typ.) 5. Requires an output load to maintain regulation
High-Side Buck – Optocoupler Feedback		1. Output referenced to input 2. Positive output (V_O) with respect to $-V_{IN}$ 3. Step down – $V_O < V_{IN}$ 4. Optocoupler feedback - Accuracy only limited by reference choice - Low cost non-safety rated optocoupler - No pre-load required 5. Minimum no-load consumption
Low-Side Buck – Optocoupler Feedback		1. Output referenced to input 2. Negative output (V_O) with respect to $+V_{IN}$ 3. Step down – $V_O < V_{IN}$ 4. Optocoupler feedback - Accuracy only limited by reference choice - Low cost non-safety rated optocoupler - No pre-load required - Ideal for driving LEDs
Low-Side Buck – Constant Current LED Driver		
High-Side Buck-Boost – Direct Feedback		1. Output referenced to input 2. Negative output (V_O) with respect to $+V_{IN}$ 3. Step up/down – $V_O > V_{IN}$ or $V_O < V_{IN}$ 4. Low cost direct feedback (±10% typ.) 5. Fail-safe – output is not subjected to input voltage if the internal power MOSFET fails 6. Ideal for driving LEDs – better accuracy and temperature stability than low-side buck constant current LED driver 7. Requires an output load to maintain regulation
High-Side Buck-Boost – Constant Current LED Driver		

Table 2. Common Circuit Configurations using LinkSwitch-TN2. (continued on next page)

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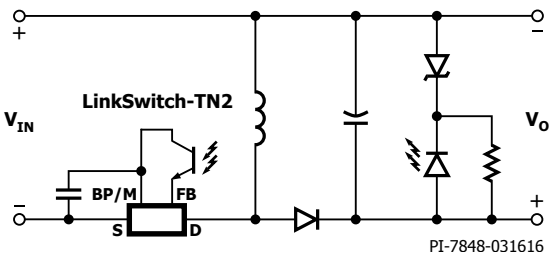
Topology	Basic Circuit Schematic	Key Features
Low-Side Buck-Boost – Optocoupler Feedback		1. Output referenced to input 2. Positive output (V_O) with respect to $+V_{IN}$ 3. Step up/down – $V_O > V_{IN}$ or $V_O < V_{IN}$ 4. Optocoupler feedback - Accuracy only limited by reference choice - Low cost non-safety rated optocoupler - No pre-load required 5. Fail-safe – output is not subjected to input voltage if the internal power MOSFET fails 6. Minimum no-load consumption

Table 2 (cont). Common Circuit Configurations using LinkSwitch-TN2.

LinkSwitch-TN2 Layout Considerations

In the buck or buck-boost converter configuration, since the SOURCE pins in LinkSwitch-TN2 are switching nodes, the copper area connected to SOURCE should be minimized to minimize EMI within the thermal constraints of the design.

In the boost configuration, since the SOURCE pins are tied to DC return, the copper area connected to SOURCE can be maximized to improve heat sinking.

Figures 9a, 9b and 9c are printed circuit board layout design examples for the circuit schematic shown in Figure 8. The loop formed between the LinkSwitch-TN2, inductor (L1), freewheeling diode (D1), and output capacitor (C2) should be kept as small as possible. The BYPASS pin capacitor C1 should be located physically close to the SOURCE (S) and BYPASS (BP) pins. To minimize direct coupling from switching nodes, the LinkSwitch-TN2 should be placed away from AC input lines. It may be advantageous to place capacitors C4 and C5 in-between LinkSwitch-TN2 and the AC input. The second rectifier diode D4 is optional, but may be included for better EMI performance and higher line surge withstand capability.

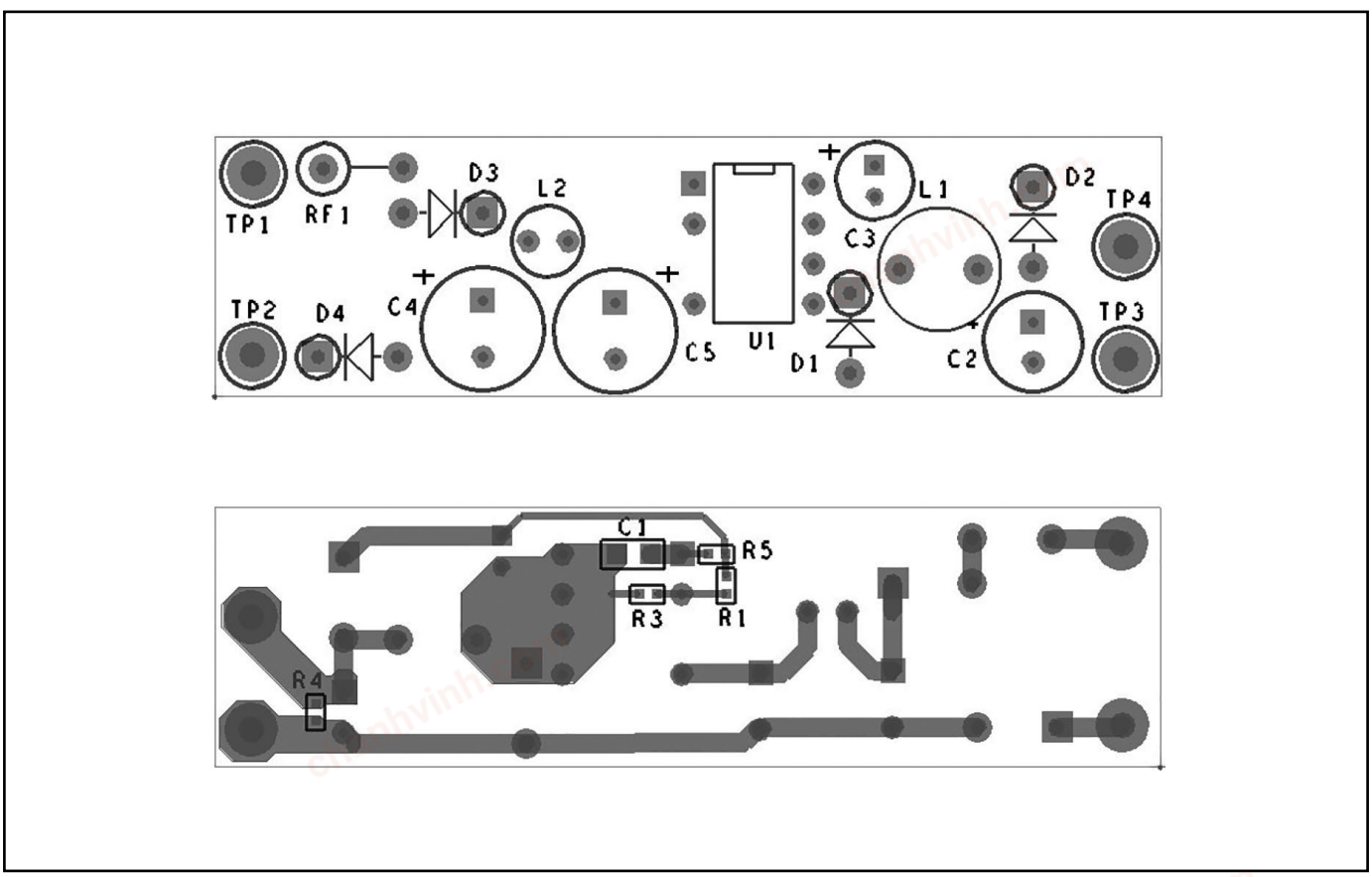


Figure 9a. Recommended Printed Circuit Layout for LinkSwitch-TN2 using P Package.

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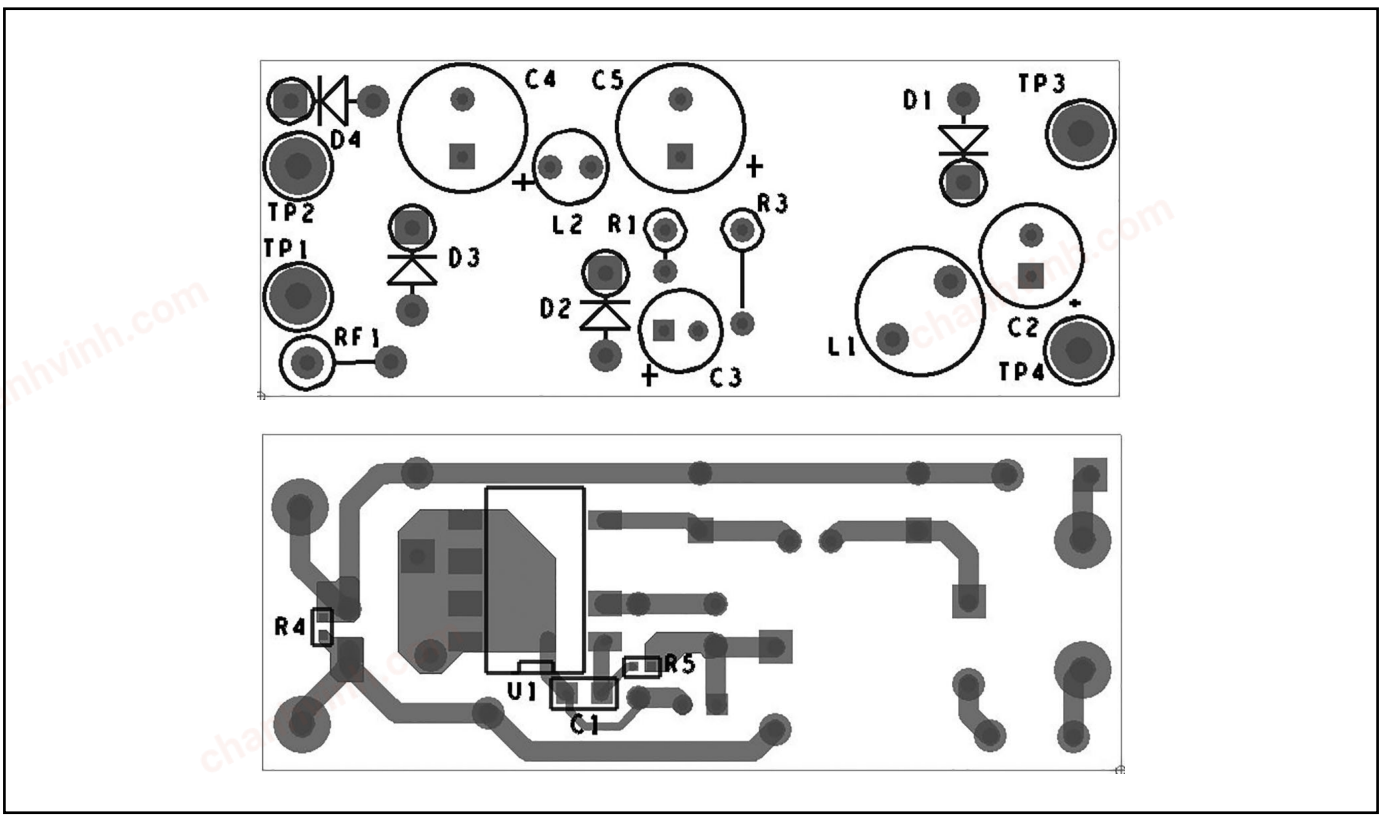


Figure 9b. Recommended Printed Circuit Layout for LinkSwitch-TN2 using G Package.

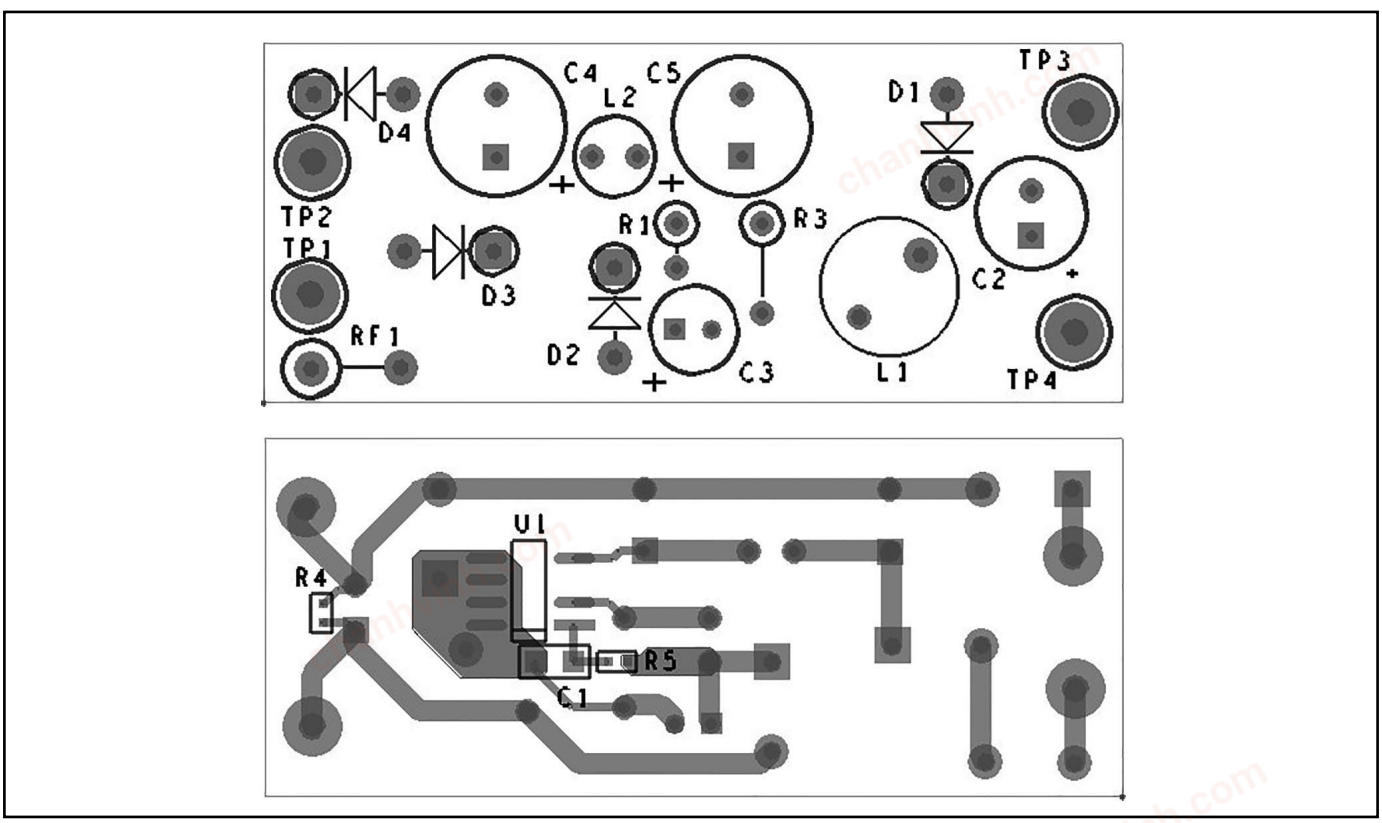


Figure 9c. Recommended Printed Circuit Layout for LinkSwitch-TN2 using D Package.

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Quick Design Checklist

As with any power supply design, all LinkSwitch-TN2 designs should be verified for proper functionality on the bench. The following minimum tests are recommended:

1. Adequate DC Rail Voltage – Check that the minimum DC input voltage does not fall below 70 VDC at maximum load, minimum input voltage.
2. Correct Diode Selection – UF400x series diodes with reverse recovery time of 75 ns or better are recommended only for designs that operate in MDCM at an ambient of 70 °C or below. For designs operating in continuous conduction mode (CCM) and/or higher ambients, then a diode with a reverse recovery time of 35 ns or better, such as the BYV26C, is recommended.
3. Maximum Drain Current – Verify that the peak drain current is below the data sheet peak drain specification under worst-case conditions of highest line voltage, maximum overload (just prior to auto-restart) and highest ambient temperature.
4. Thermal Check – At maximum output power, minimum input voltage and maximum ambient temperature, verify that the LinkSwitch-TN2 SOURCE pin temperature is 100 °C or below. This ensures adequate margin due to variations in $R_{DS(ON)}$ from part to part. If the device temperature of the IC exceeds 85 °C with ambient temperature of 25 °C, it is recommended the next bigger device in the family should be selected for the application. A battery powered thermocouple meter is recommended to make measurements when the SOURCE pins are a switching node. Alternatively, the ambient temperature may be raised to indicate margin to thermal shutdown.

In a LinkSwitch-TN2 design using a buck or buck-boost converter topology, the SOURCE pin is a switching node. Oscilloscope measurements should therefore be made with probe grounded to a DC voltage, such as primary return or DC input rail, and not to the SOURCE pins. The power supply input must always be supplied from an isolated source when doing measurements (e.g. via an isolation transformer).

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Absolute Maximum Ratings(1,5)

DRAIN Pin Voltage: LNK320x ..... -0.3 to 725 V
LNK329x ..... -0.3 to 900 V
DRAIN Pin Peak Current: LNK3202 ..... 600 mA[2]
LNK3204 ..... 1230 mA[2]
LNK3205 ..... 2460 mA[2]
LNK3206 ..... 3750 mA[2]
LNK3207 ..... 3750 mA[2]
LNK3208 ..... 6300 mA[2]
LNK3209 ..... 10200 mA[2]
LNK3294 ..... 968 mA[2]
LNK3296 ..... 3194 mA[2]
FEEDBACK Pin Voltage ..... -0.3 V to 7 V
FEEDBACK Pin Current ..... 100 mA
BYPASS Pin Voltage ..... 0.3 V to 7 V

Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature[3] ..... -40 °C to 150 °C
Lead Temperature[4] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. See Figure 15 and Figure 23, for V_{DS} > 400 V.
3. Normally limited by internal circuitry.
4. 1/16 in. from case for 5 seconds.
5. Maximum ratings specified may be applied, one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

Thermal Resistance

Thermal Resistance: P or G Package:
(θ_{JA}) ..... 70 °C/W[2]; 60 °C/W[3]
(θ_{JC})[1] ..... 11 °C/W
D Package:
(θ_{JA}) ..... 100 °C/W[2]; 80 °C/W[3]
(θ_{JC})[1] ..... 30 °C/W

Notes:
1. Measured on pin 8 (SOURCE) close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm²), 2 oz. (610 g/m²) copper clad.
3. Soldered to 1 sq. in. (645 mm²), 2 oz. (610 g/m²) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 10 (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Output Frequency	f_{OSC}	T_J = 25 °C	Average	62	66	70	kHz
			Peak-Peak Jitter		4		
Maximum Duty Cycle	DC_{MAX}	S2 Open	LNK320x	66	69	73	%
			LNK329x	65	68	72	
FEEDBACK Pin Turnoff Threshold Current	I_{FB}	V_{BP} = 5.0 V to 5.5 V, T_J = 25 °C		44	49	54	µA
FEEDBACK Pin Voltage at Turnoff Threshold	V_{FB}	V_{BP} = 5.0 V to 5.5 V, T_J = 25 °C		1.97	2.00	2.03	V
FEEDBACK Pin Instant Shutdown Current	$I_{FB(SD)}$	T_J = 25 °C		520	675	800	µA
FEEDBACK Pin Instant Shutdown Delay		T_J = 25 °C			2		Switch Cycles
FEEDBACK Pin Voltage at Shutdown Current	$V_{FB(SD)}$	V_{BP} = 5.0 V to 5.5 V, T_J = 25 °C			3.3		V
DRAIN Pin Supply Current	I_{S1}	V_{FB} = 2.1 V (MOSFET Not Switching) See Note A	LNK32xx		75		µA
			LNK3208/9		95		
	I_{S2}	FEEDBACK Open (MOSFET Switching) See Notes A, B	LNK3202		98	160	µA
			LNK3204		113	180	
			LNK3205		141	220	
			LNK3206		165	250	
			LNK3207		190	290	
			LNK3208		275	405	
			LNK3209		300	460	
			LNK3294		120	170	
			LNK3296		225	320	

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 10 (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V T_J = 25 °C		-11	-7	-3	mA
	I_{CH2}	V_{BP} = 4 V T_J = 25 °C		-7.5	-5	-2.5	
BYPASS Pin Voltage	V_{BP}			4.7	5.0	5.2	V
BYPASS Pin Shutdown Threshold Current	$I_{BP(SD)}$	T_J = 25 °C			6	8	mA
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 2 mA		4.9	5.2	5.5	V
BYPASS Pin Voltage Hysteresis	$V_{BP(H)}$		LNK32xx	0.37	0.47	0.57	V
			LNK3208/9	0.35	0.47	0.60	
BYPASS Pin Supply Current	$I_{BP(SC)}$	See Note C		55			µA
Circuit Protection							
Standard Current Limit (C_{BP} = 0.1 µF, See Note D, H)	I_{LIMIT}	di/dt = 55 mA/µs T_J = 25 °C	LNK3202	126	136	146	mA
		di/dt = 250 mA/µs T_J = 25 °C		149	170	191	
		di/dt = 65 mA/µs T_J = 25 °C	LNK3204	240	257	275	
		di/dt = 415 mA/µs T_J = 25 °C		278	317	356	
		di/dt = 75 mA/µs T_J = 25 °C	LNK3205	350	375	401	
		di/dt = 500 mA/µs T_J = 25 °C		394	448	502	
		di/dt = 95 mA/µs T_J = 25 °C	LNK3206	450	482	515	
		di/dt = 610 mA/µs T_J = 25 °C		510	580	650	
		di/dt = 95 mA/µs T_J = 25 °C	LNK3207	725	780	835	
		di/dt = 610 mA/µs T_J = 25 °C		893	1015	1137	
		di/dt = 165 mA/µs T_J = 25 °C	LNK3208	970	1040	1110	
		di/dt = 1000 mA/µs T_J = 25 °C		1131	1285	1440	
		di/dt = 165 mA/µs T_J = 25 °C	LNK3209	1200	1300	1400	
		di/dt = 1000 mA/µs T_J = 25 °C		1413	1600	1787	
		di/dt = 65 mA/µs T_J = 25 °C	LNK3294	240	257	275	
		di/dt = 415 mA/µs T_J = 25 °C		278	317	356	
		di/dt = 95 mA/µs T_J = 25 °C	LNK3296	450	482	515	
		di/dt = 610 mA/µs T_J = 25 °C		510	580	650	

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 10 (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Reduced Current Limit (C_{BP} = 1 µF, See Note D, H)	$I_{LIMIT(RED)}$	di/dt = 28 mA/µs T_J = 25 °C	LNK3202	70	80	90	mA
		di/dt = 170 mA/µs T_J = 25 °C		104	119	134	
		di/dt = 65 mA/µs T_J = 25 °C	LNK3204	180	205	230	
		di/dt = 415 mA/µs T_J = 25 °C		227	258	289	
		di/dt = 75 mA/µs T_J = 25 °C	LNK3205	227	259	291	
		di/dt = 500 mA/µs T_J = 25 °C		292	332	372	
		di/dt = 95 mA/µs T_J = 25 °C	LNK3206	325	370	415	
		di/dt = 610 mA/µs T_J = 25 °C		408	464	520	
		di/dt = 95 mA/µs T_J = 25 °C	LNK3207	545	620	695	
		di/dt = 610 mA/µs T_J = 25 °C		730	830	930	
		di/dt = 165 mA/µs T_J = 25 °C	LNK3208	739	840	941	
		di/dt = 1000 mA/µs T_J = 25 °C		941	1070	1199	
		di/dt = 165 mA/µs T_J = 25 °C	LNK3209	925	1050	1175	
		di/dt = 1000 mA/µs T_J = 25 °C		1194	1350	1506	
		di/dt = 65 mA/µs T_J = 25 °C	LNK3294	180	205	230	
		di/dt = 415 mA/µs T_J = 25 °C		227	258	289	
		di/dt = 95 mA/µs T_J = 25 °C	LNK3296	325	370	415	
		di/dt = 610 mA/µs T_J = 25 °C		408	464	520	
Minimum On-Time	$t_{ON(MIN)}$	LNK3202 See Note I		373	534	687	ns
		LNK3204 See Note I		356	475	594	
		LNK3205 See Note I		412	531	650	
		LNK3206 See Note I		442	591	734	
		LNK3207 See Note I		656	875	1094	
		LNK3208 See Note I		435	580	725	
		LNK3209 See Note I		442	591	734	

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 10 (Unless Otherwise Specified)			Min	Typ	Max	Units
Circuit Protection (cont.)								
Minimum On-Time	$t_{ON(MIN)}$	LNK3294 See Note I			356	480	599	ns
		LNK3296 See Note I			350	550	760	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note E			300	450		ns
Thermal Shutdown Temperature	T_{SD}	See Note F			135	142	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	See Note F				75		°C
Internal Soft-Start	$f_{OSC(SS)}$	LNK32xx	Soft-Start Period See Note E			256		Cycles
			Soft-Start Frequency			33		kHz
		LNK3208/9	Soft-Start Period 1			64		Cycles
			Soft-Start Frequency 1			16.5		kHz
			Soft-Start Period 2			64		Cycles
			Soft-Start Frequency 2			22		kHz
			Soft-Start Period 3			128		Cycles
			Soft-Start Frequency 3			33		kHz
Output								
ON-State Resistance	$R_{DS(ON)}$	LNK3202 I_D = 13 mA		T_J = 25 °C		48	55.2	Ω
				T_J = 100 °C		76	88.4	
		LNK3204 I_D = 25 mA		T_J = 25 °C		24	27.6	
				T_J = 100 °C		38	44.2	
		LNK3205 I_D = 35 mA		T_J = 25 °C		12	13.8	
				T_J = 100 °C		19	22.1	
		LNK3206 I_D = 45 mA		T_J = 25 °C		7	8.1	
				T_J = 100 °C		11	12.9	
		LNK3207 I_D = 45 mA		T_J = 25 °C		7	8.1	
				T_J = 100 °C		11	12.9	
		LNK3208 I_D = 45 mA		T_J = 25 °C		4.25	4.85	
				T_J = 100 °C		5.78	6.60	
		LNK3209 I_D = 45 mA		T_J = 25 °C		2.70	3.20	
				T_J = 100 °C		3.80	4.37	
		LNK3294 I_D = 83 mA		T_J = 25 °C		17	19.6	
				T_J = 100 °C		27	31	
		LNK3296 I_D = 163 mA		T_J = 25 °C		5.3	6.1	
				T_J = 100 °C		8.4	9.7	

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 10 (Unless Otherwise Specified)		Min	Typ	Max	Units
Output (cont.)							
OFF-State Drain Leakage Current	I_{DSS1}	V_{BP} = 5.4 V V_{FB} ≥2.1 V V_{DS} = 80% BV_{DSS} T_J = 125 °C				200	µA
	I_{DSS2}	V_{BPP} = 5.4 V V_{DSS} = 325 V T_J = 25 °C			15		
Breakdown Voltage	BV_{DSS}	V_{BP} = 5.4 V V_{FB} ≥2.1 V T_J = 25 °C	LNK320X	725			V
			LNK329X	900			
DRAIN Pin Supply Voltage		T_J = 25 °C	LNK3202 to LNK3207	18			V
			LNK3208 to LNK3209	25			
Auto-Restart ON-Time	$t_{AR(ON)}$	T_J = 25 °C See Note G			50		ms
Auto-Restart OFF-Time	$t_{AR(OFF)}$	T_J = 25 °C See Note G	First Off Period		150		ms
			Subsequent Periods		1500		
Auto-Restart Duty Cycle	DC_{AR}	Subsequent Periods			3		%

NOTES:

A. Total current consumption is the sum of I_{S1} and I_{DSS} when FEEDBACK pin voltage is = 2.1 V (MOSFET not switching) and the sum of I_{S2} and I_{DSS} when FEEDBACK pin is shorted to SOURCE (MOSFET switching).

B. Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BYPASS pin current at 5.1 V.

C. This current is only intended to supply an optional optocoupler connected between the BYPASS and FEEDBACK pins and not any other external circuitry.

D. For current limit at other di/dt values, refer to Figures 21 and 22.

E. This parameter is guaranteed by design.

F. This parameter is derived from characterization.

G. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency).

H. The BP/M capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application.

I. Measured using circuit in Figure 12 with 50 Ω drain pull-up. The width of the drain pulse is measured as the time from V_{FALL} = 42 V to V_{RISE} = 40 V (VDR = 50 V), for LNK32x6/x5/x4 and as the time from V_{FALL} = 32 V to V_{RISE} = 30 V on rising edge (VDR = 35 V), for LNK3202.

Nominal BP/M Pin Capacitor Value	Tolerance Relative to Minimal Capacitor Value	
	Min	Max
0.1 µF	-60%	+100%
1 µF	-50%	+100%

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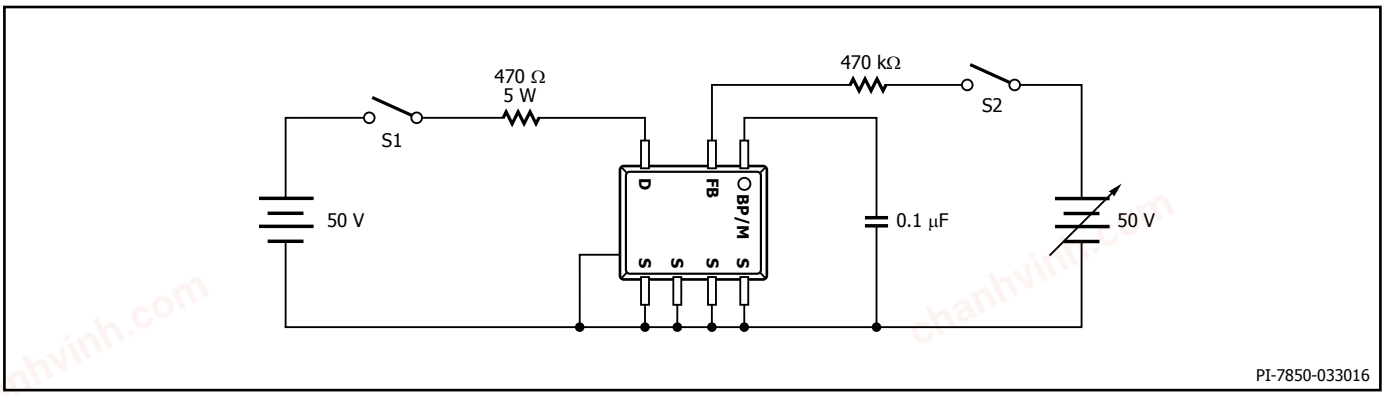


Figure 10. LinkSwitch-TN2 General Test Circuit.

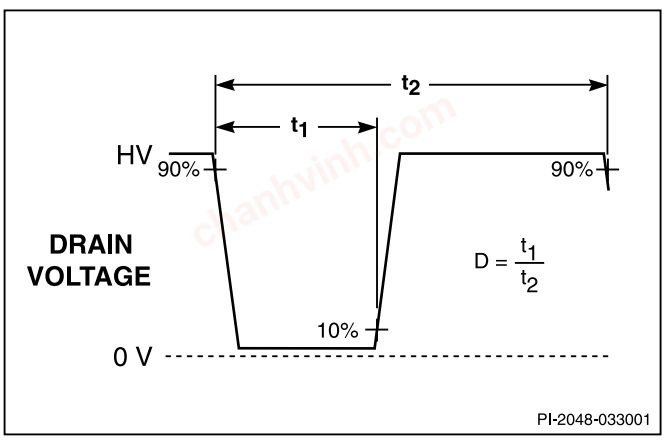


Figure 11. LinkSwitch-TN2 Duty Cycle Measurement.

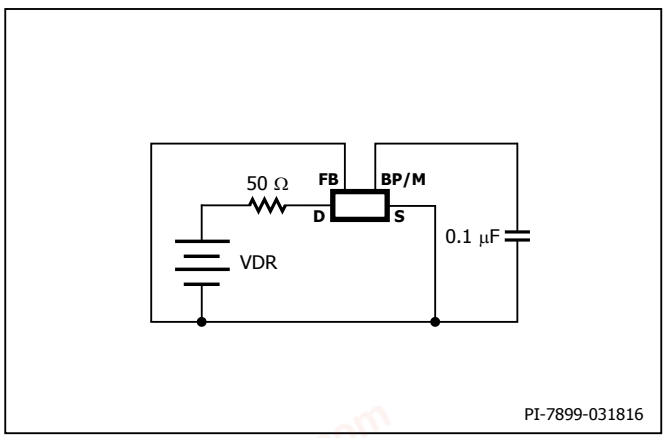


Figure 12. LinkSwitch-TN2 Minimum On-Time Test Circuit.

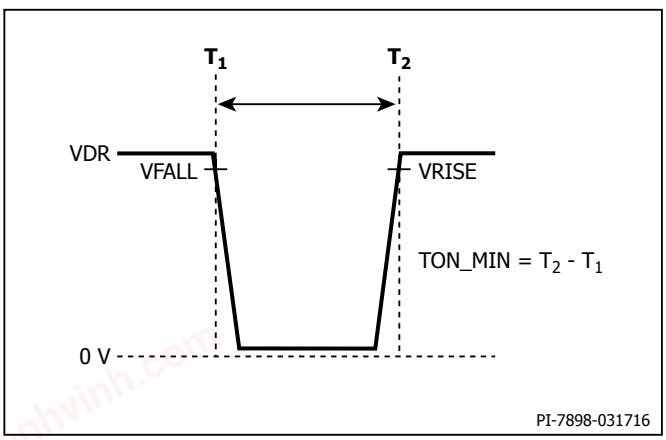


Figure 13. LinkSwitch-TN2 Minimum On-Time Measurement.

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Typical Performance Characteristics

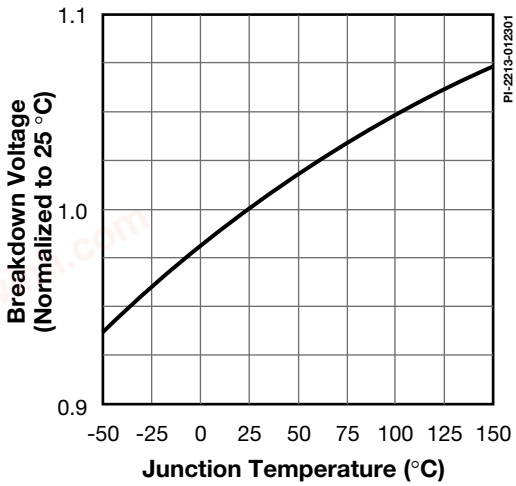


Figure 14. Breakdown vs. Temperature.

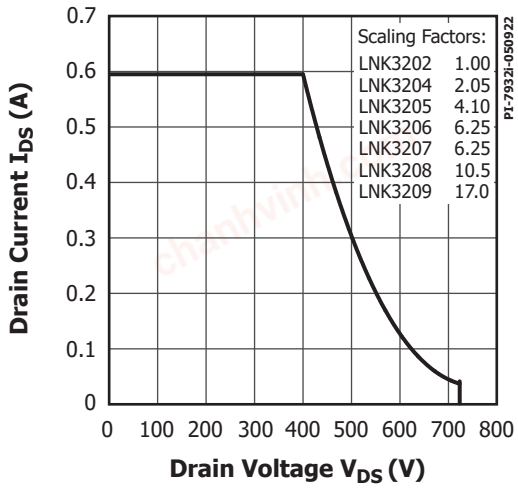


Figure 15. Maximum Allowable Drain Current vs. Drain Voltage.

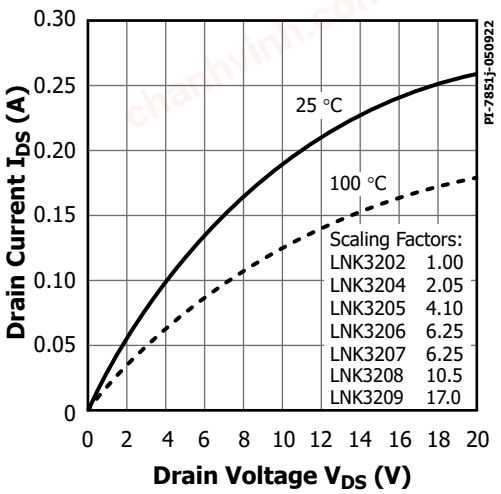


Figure 16. Output Characteristics.

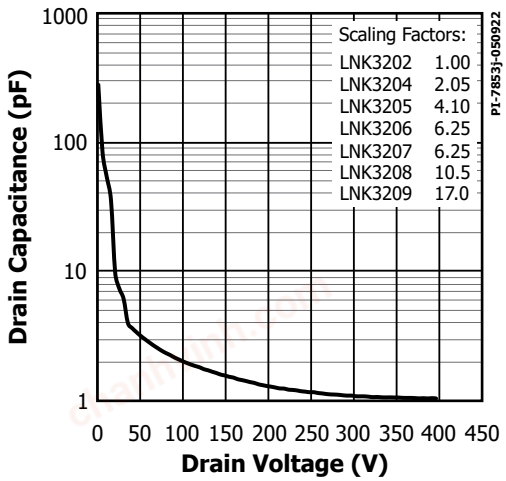


Figure 17. C_{OSS} vs. Drain Voltage.

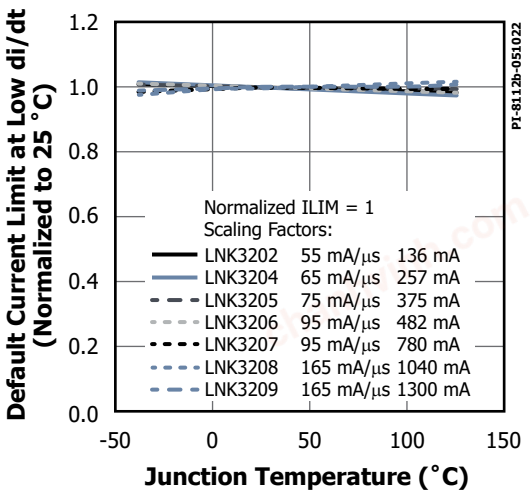


Figure 18. Current Limit vs. Temperature.

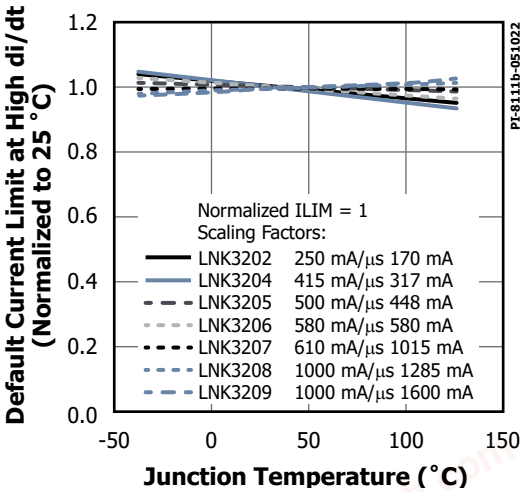


Figure 19. Current Limit vs. Temperature.

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Typical Performance Characteristics

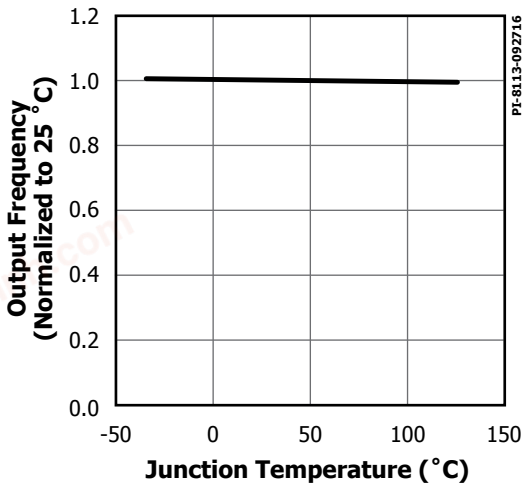


Figure 20. Output Frequency vs. Junction Temperature.

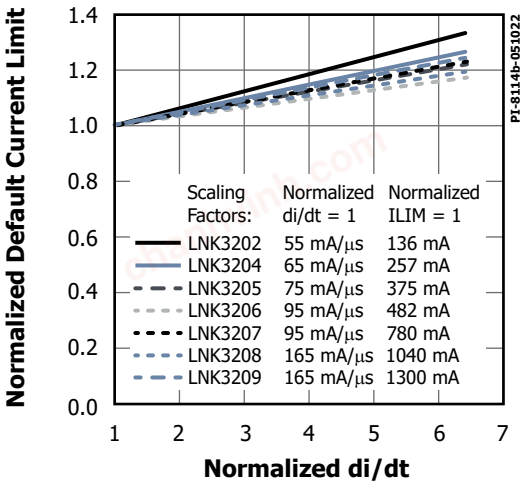


Figure 21. Default Current Limit vs. di/dt.

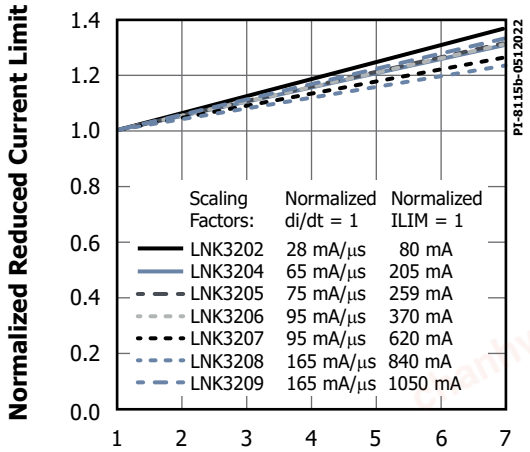


Figure 22. Reduced Current Limit vs. di/dt.

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Typical Performance Characteristics 900 V

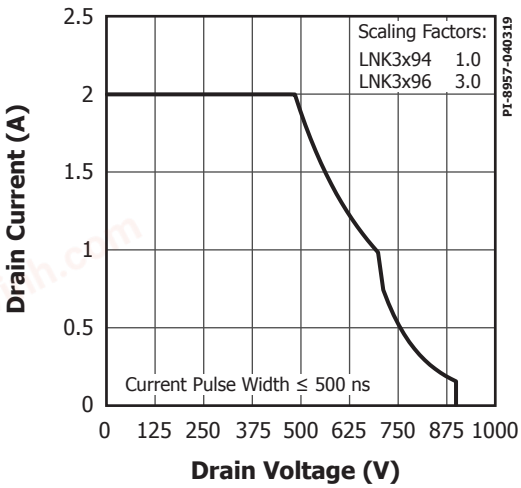


Figure 23. Maximum Allowable Drain Current vs. Drain Voltage.

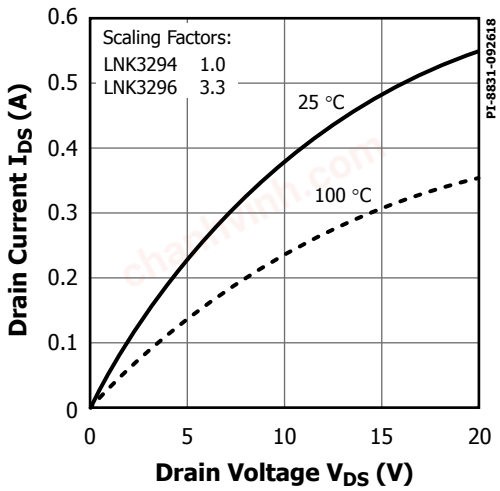


Figure 24. Output Characteristics.

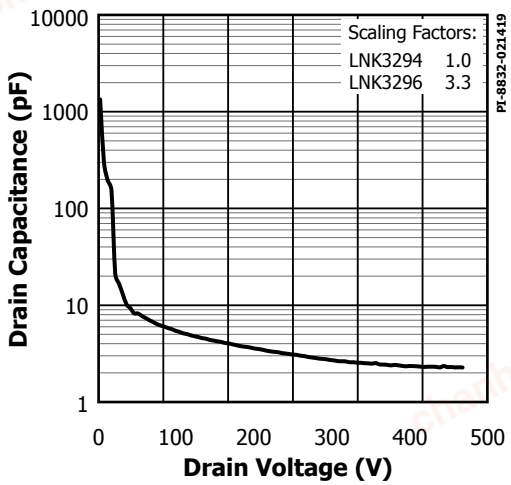


Figure 25. C_{OSS} vs. Drain Voltage.

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Typical Performance Characteristics 900 V

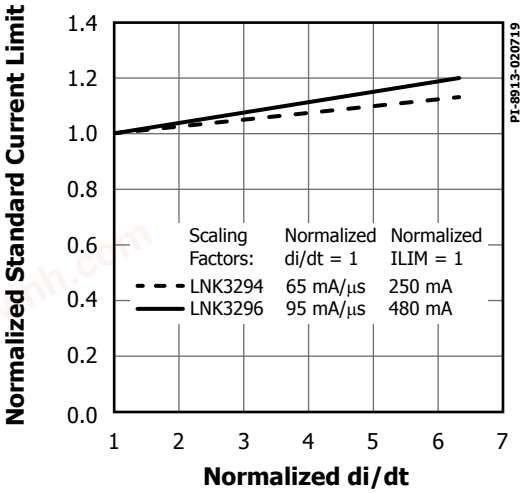


Figure 26. Normalized Current Limit vs. di/dt.

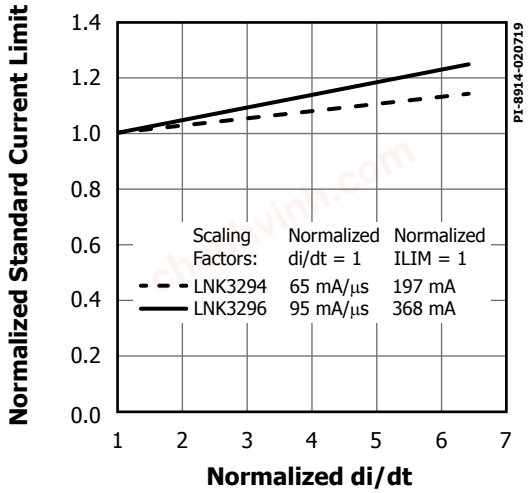


Figure 27. Normalized Current Limit vs. di/dt.

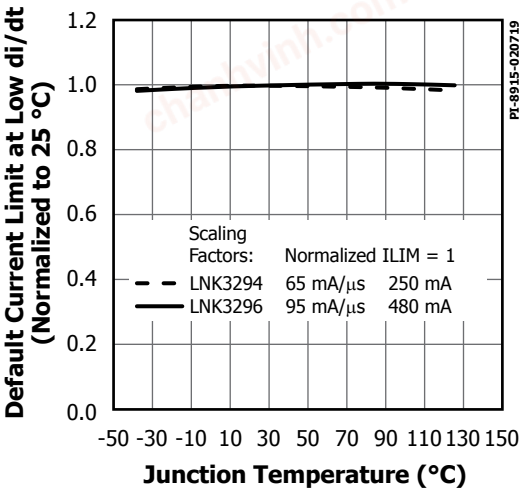


Figure 28. Standard Current Limit at Low Ramp Rate.

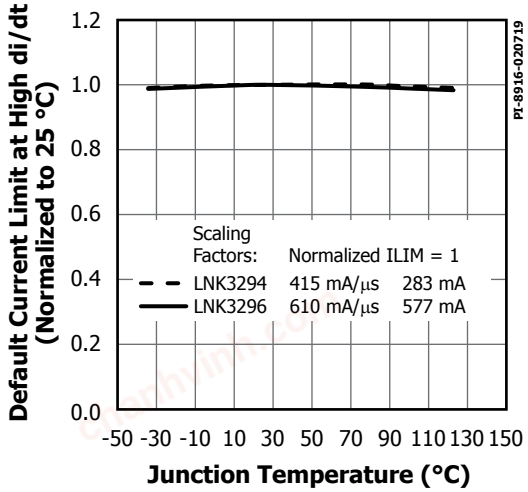


Figure 29. Standard Current Limit at High Ramp Rate.

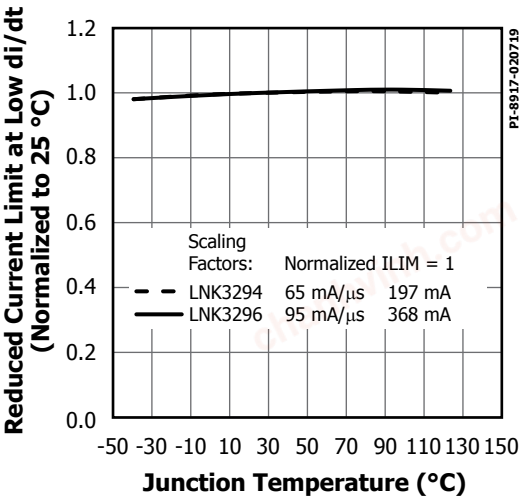


Figure 30. Reduced Current Limit at Low Ramp Rate.

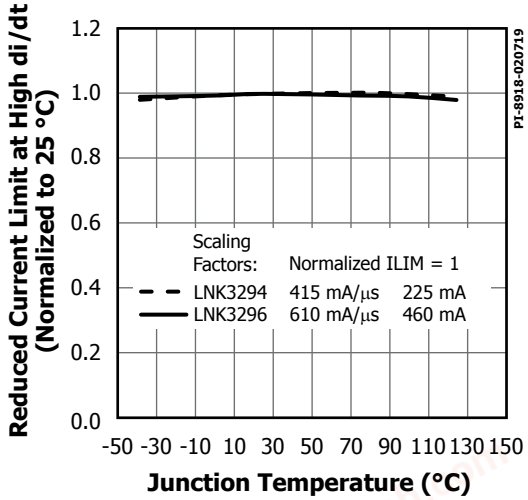
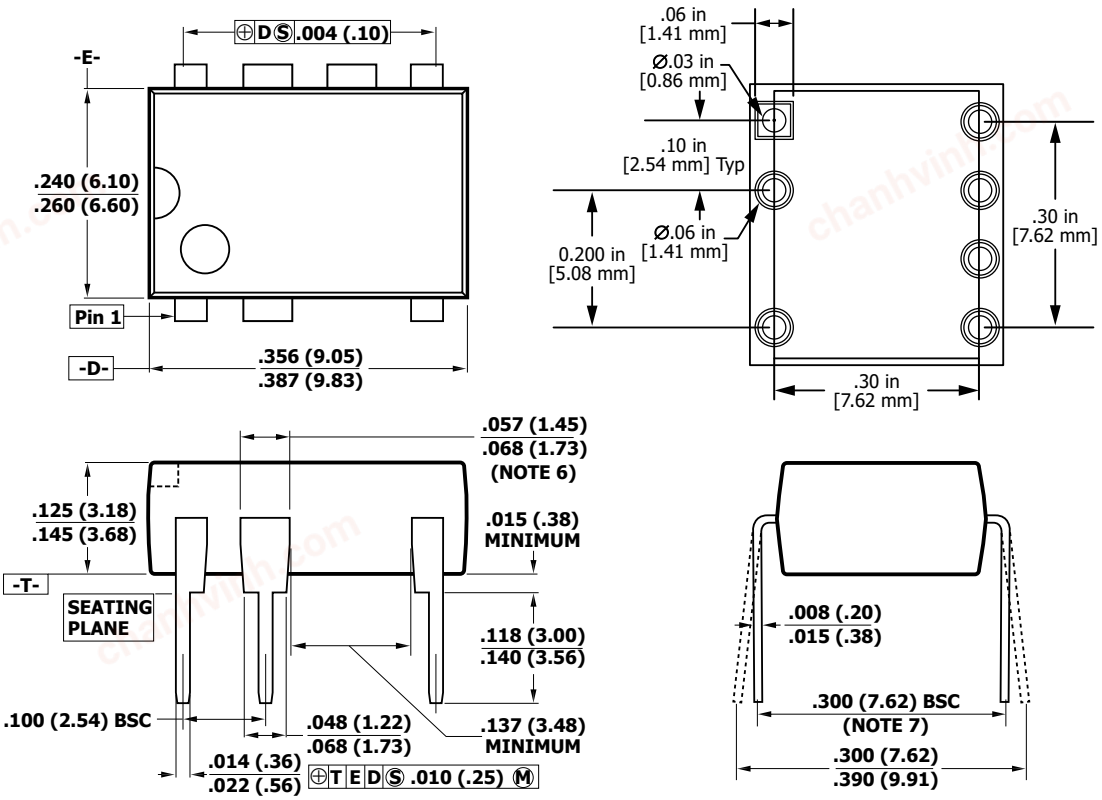


Figure 31. Reduced Current Limit at High Ramp Rate.

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PDIP-8C (P Package)



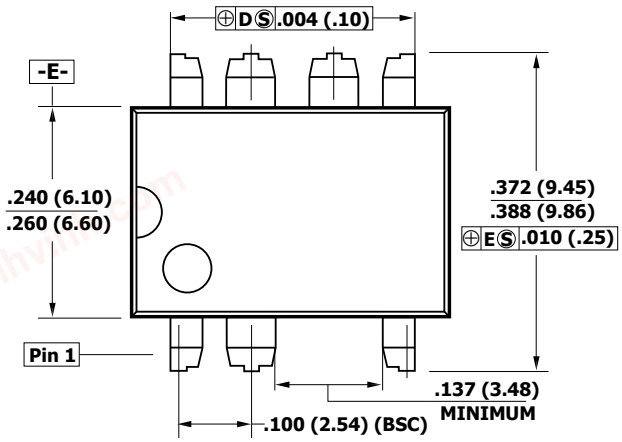
Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clock-wise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.

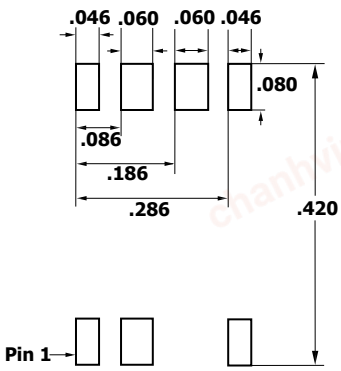
P08C

PI-3933b-092920

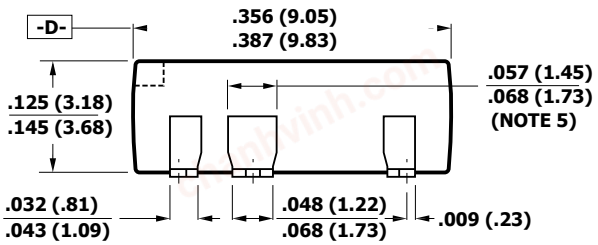
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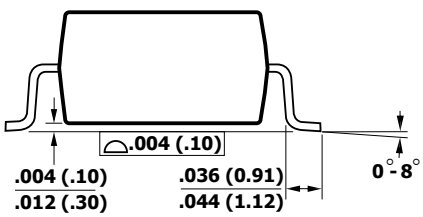
SMD-8C (G Package)





Solder Pad Dimensions





Notes:

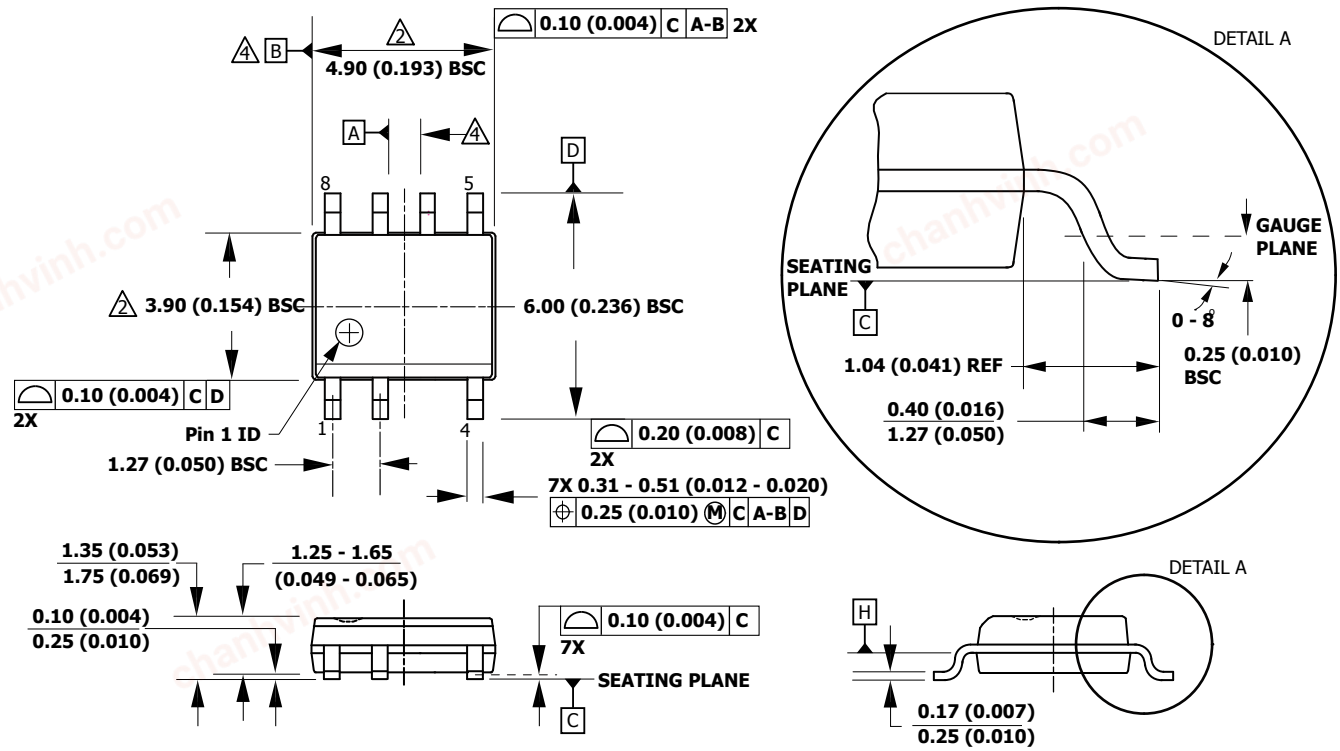
1. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
2. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
3. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 3 is omitted.
4. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
5. Lead width measured at package body.
6. D and E are referenced datums on the package body.

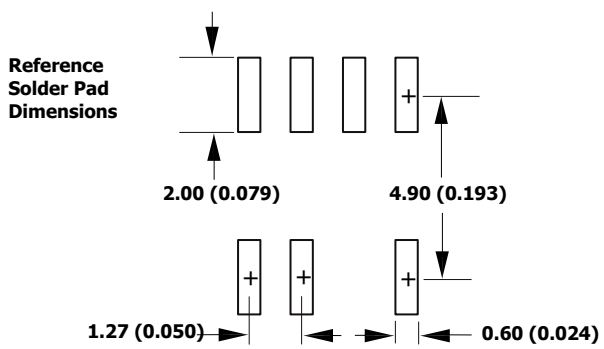
G08C

PI-4015b-072320

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SO-8C (D Package)





Notes:

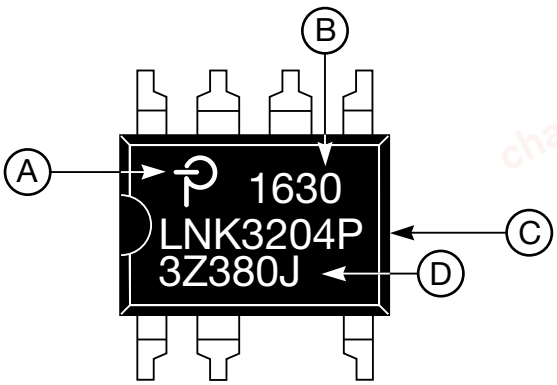
1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-012315

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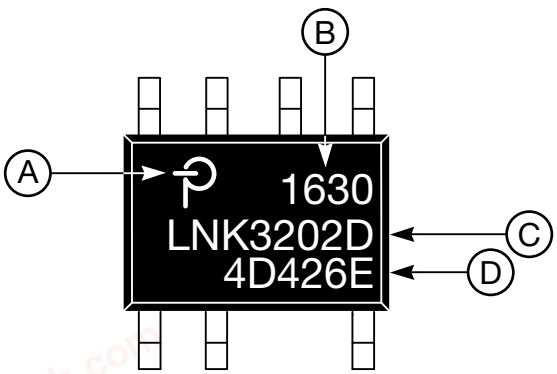
PDIP-8C (P) and SMD-8C (G) PACKAGE MARKING



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-8117-093016

SO-8C (D) PACKAGE MARKING



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-8116-092816

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MSL Table

Part Number	MSL Rating
LNK3202P LNK3204P LNK3294P LNK3205P LNK3206P LNK3207P LNK3208P LNK3209P LNK3294P LNK3296P	N/A
LNK3202G LNK3204G LNK3294G LNK3205G LNK3206G LNK3207G LNK3208G LNK3209G LNK3294G LNK3296G	3
LNK3202D LNK3204D LNK3205D LNK3206D LNK3207D LNK3208D LNK3209D	1

ESD and Latch-Up

Test	Conditions	Results
Latch-up at 125 °C	EIA/JESD78	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	EIA/JESD22-A114-A	> ±2 kV on all pins, except DRAIN Pin for LNK3202 ±1.5 kV
Machine Model ESD	EIA/JESD22-A115-A	> ±200 V on all pins

Part Ordering Information

LNK 3204 G - TL

- **LinkSwitch Product Family**
- **TN2 Series Number**
- **MOSFET Rating**
  - **0** 725 V
  - **9** 900 V
- **Package Identifier (All RoHS Compliant and Halogen Free)**
  - **G** Plastic Surface Mount SMD-8C
  - **P** Plastic PDIP-8C
  - **D** Plastic SO-8C (725 V Family only)
- **Tape & Reel and Other Options**
  - **TL** Tape and Reel, 1 k pcs minimum for G Package. 2.5 k pcs for D Package. Not available for P Package.

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Revision	Notes	Date
A	Preliminary release of 725 V parts.	04/16
B	Introduction release of 725 V parts.	07/16
C	Production release of 725 V parts.	10/16
D	Added IC images on page 1.	10/14/16
E	Updated Note D, Figure 16, V_{FB} parameter.	11/8/16
F	Updated Figures 12 and 13 Captions. Corrected DRAIN Pin Peak Current to match Figure 15 and Corrected Note 2 in Absolute Maximum Ratings Section.	01/06/17
G	Production release of LNK3294 and LNK3296 parts.	02/19
H	Updated Figure 23.	04/19
I	Added Max values for I_{S2} and added I_{DSS2} at T_J - 125 °C.	08/19
J	Updated ESD and Latch-Up table.	01/20
K	Updated per PCN-20321.	08/20
L	Updated per PCN-20331 and added size 7.	10/20
M	Updated $V_{BP(SHUNT)}$ Min and Max values.	10/21/20
N	Introduction release of LNK3208 part.	04/22
O	Introduction release of LNK3209 part.	05/22
P	Production release of LNK3208 and LNK3209 parts.	06/22

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Notes

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