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InnoSwitch4-CZ Family

Off-Line CV/CC ZVS Flyback Integrated Switcher IC with 750 V PowiGaN, Active Clamp Drive and Synchronous Rectification

Product Highlights

Highly Integrated, Compact Footprint

- Zero voltage switching (ZVS) flyback controller with driver for ClampZero™ (active clamp IC)
- Unique control algorithm to enable ZVS in both DCM and CCM
- Robust 750 V PowiGaN™ primary switch
- Steady-state switching frequency up to 140 kHz minimizes transformer size
- Synchronous rectification driver and secondary-side sensing
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Exceptional CV/CC accuracy, independent of external components
- Adjustable accurate output current sense using external sense resistor

EcoSmart™ – Energy Efficient

- Up to 95% efficient
- Less than 30 mW no-load consumption including line sense

Advanced Protection / Safety Features

- Open SR FET-gate detection
- Fast input line UV/OV protection

Optional Features

- Variable output voltage, constant current profiles
- Auto-restart or latching fault response for output OVP/UVP
- Multiple output UV fault thresholds
- Latching or hysteretic primary over-temperature protection

Full Safety and Regulatory Compliance

- Reinforced isolation >4000 VAC
- 100% production HIPOT testing
- UL1577 and TUV (EN60950) safety approved
- Excellent noise immunity enables designs that achieve class "A" performance criteria for EN61000-4 suite; EN61000-4-2, 4-3 (30 V/m), 4-4, 4-5, 4-6, 4-8 (100 A/m) and 4-9 (1000 A/m)

Green Package

- Halogen free and RoHS compliant

Applications

- High density flyback designs up to 110 W
- High efficiency CV/CC power supplies
- High efficiency USB PD adapters

Description

The InnoSwitch™4-CZ family of ICs partners with the ClampZero family of active clamp ICs to dramatically improve the efficiency of flyback power converters, particularly those requiring a compact form-factor. The InnoSwitch4-CZ family incorporates primary and secondary controllers and safety-rated feedback into a single IC.

The combination of InnoSwitch4-CZ with ClampZero greatly reduces system and primary switch losses, allowing for extremely high power densities. InnoSwitch4-CZ also incorporates multiple protection features including output overvoltage and over-current limiting, and over-temperature shutdown. Devices are available that support the common combinations of latching and auto-restart protection mode required by applications such as chargers, adapters, consumer electronics and industrial systems.

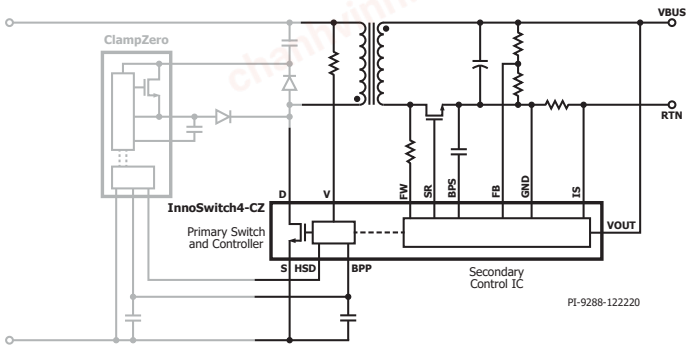


Figure 1. Typical Application schematic



Figure 2. High Creepage, Safety-Compliant InSOP-24D Package.

Output Power Table

Product[3]	85-264 VAC		385 VDC (PFC Input)	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
INN4073C	60 W	70 W	75 W	80 W
INN4074C	75 W	85 W	95 W	100 W
INN4075C	80 W	90 W	105 W	110 W

Table 1. Output Power Table.

Notes:

1. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient. Max output power is dependent on the design. With condition that package temperature must be < 125 °C.
2. Minimum peak power capability.
3. Package: InSOP-24D.

This Product is Covered by Patents and/or Pending Patent Applications.

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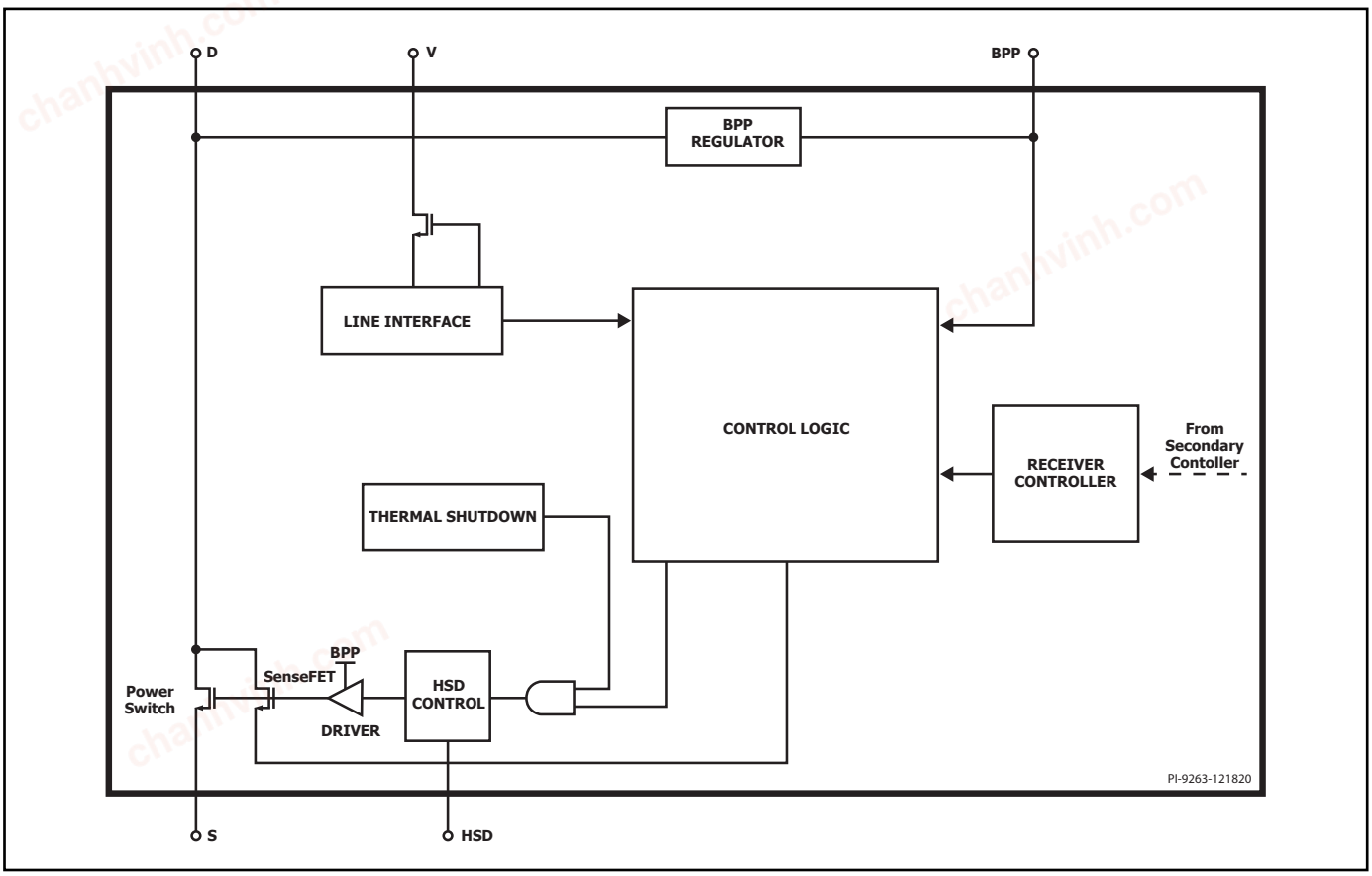


Figure 3. Primary Controller Block Diagram.

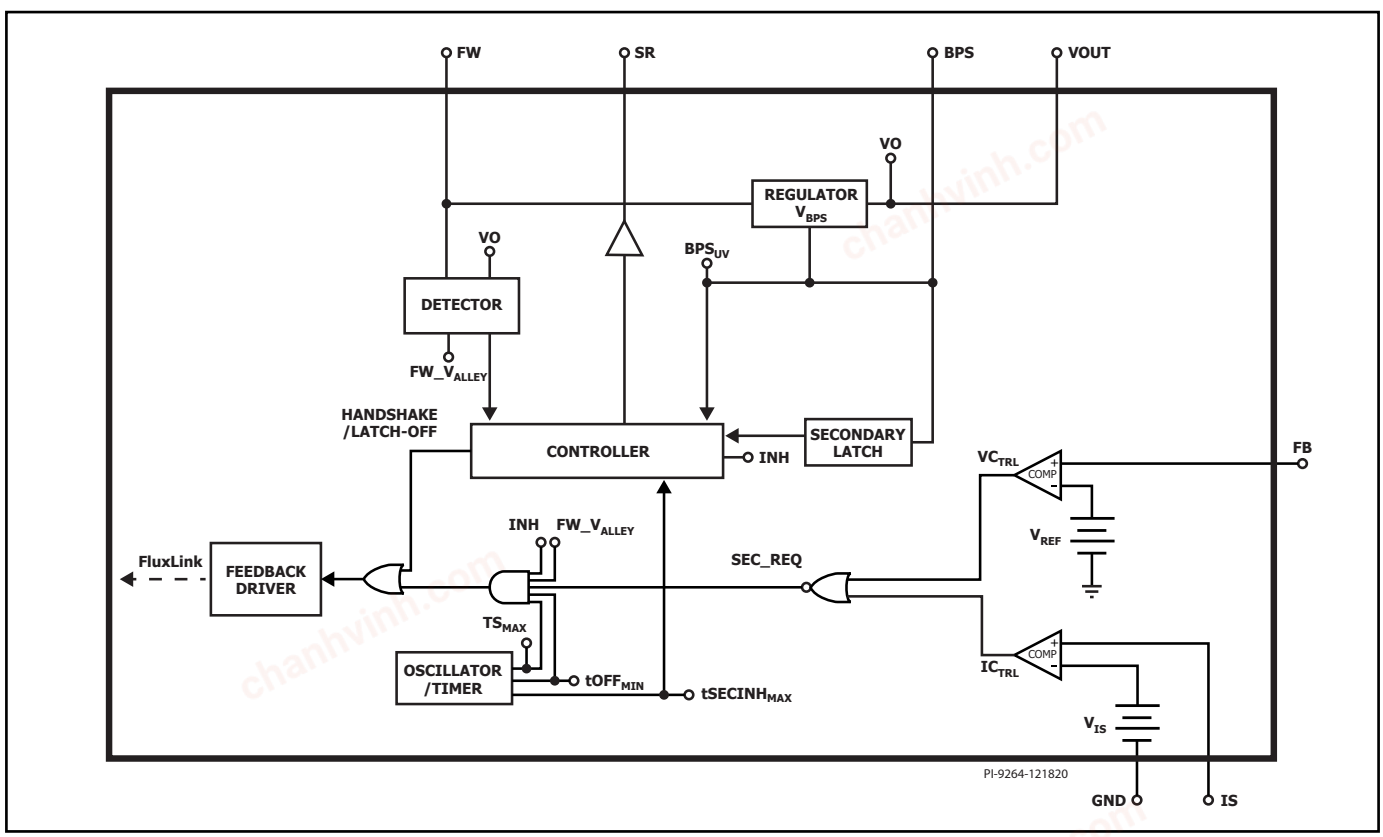


Figure 4. Secondary Controller Block Diagram.

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Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply return output terminals. An external current sense resistor should be connected between this and the GND pin. If current regulation is not required, this pin should be tied to the GND pin.

SECONDARY GROUND (GND) (Pin 2)
GND for the secondary IC. Note this is not the power supply output GND due to the presence of the sense resistor between this and the ISENSE pin.

FEEDBACK (FB) Pin (Pin 3)
Connection to an external resistor divider to set the power supply output voltage.

SECONDARY BYPASS (BPS) Pin (Pin 4)
Connection point for an external bypass capacitor for the secondary IC supply.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 5)
Gate driver for external SR FET. If no SR FET is used connect this pin to GND.

OUTPUT VOLTAGE (VOUT) Pin (Pin 6)
Connected directly to the output voltage, to provide current for the controller on the secondary-side and provide secondary protection.

FORWARD (FWD) Pin (Pin 7)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller when V_{OUT} is below a threshold value.

NC Pin (Pin 8-12)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to GND to disable UV/OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
The connection point for an external bypass capacitor for the primary-side supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1. Must be connected to BP1 pin of Clamp Zero.

HSD Pin (Pin 15)
High-side drive signal for active clamp. Must be connected to IN pin of ClampZero.

SOURCE (S) Pin (Pin 16-19)
These pins are the power switch source connection. It is also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
Power switch drain connection.

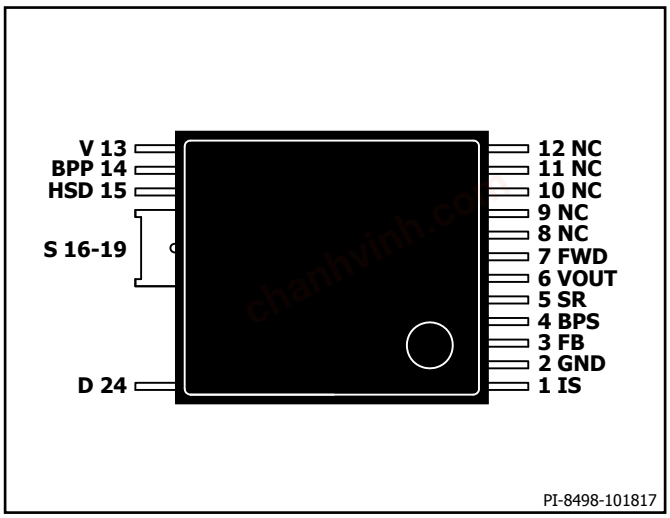


Figure 5. Pin Configuration.

InnoSwitch4-CZ Functional Description

The InnoSwitch4-CZ combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme (FluxLink) using the package lead frame and bond wires to provide a safe, reliable, and cost-effective means to transmit accurate, output voltage and current information from the secondary controller to the primary controller.

The primary controller on InnoSwitch4-CZ is a zero voltage switching (ZVS) flyback controller that has the ability to operate in continuous conduction mode (CCM), and discontinuous conduction mode (DCM) with virtually no switching loss. The controller uses both variable frequency and variable current limit control scheme. The primary controller consists of a frequency jitter oscillator, a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection, leading edge blanking and power switch.

The InnoSwitch4-CZ secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, a constant voltage (CV) and a constant current (CC) control circuit, a 4.5 V regulator on the SECONDARY BYPASS pin, synchronous rectifier FET driver, QR mode circuit (for optimal ZVS in DCM operation), oscillator and timing circuit, and numerous integrated protection features.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller, highlighting the most important features.

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Primary Controller

InnoSwitch4-CZ is a variable frequency controller allowing CCM/DCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch4-CZ to be powered externally through a bias winding, decreasing the no-load consumption to less than 30 mW in a 5 V output design.

Primary Bypass ILIM Programming

InnoSwitch4-CZ ICs allows the user to adjust current limit (ILIM) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used.

There are 2 selectable capacitor sizes – 0.47 µF and 4.7 µF for setting standard and increased ILIM settings respectively.

Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V (V_{BPP} - $V_{BP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to V_{SHUNT} to re-enable turn-on of the power switch.

Primary BYPASS Pin Overvoltage Function

The PRIMARY BYPASS pin has an optional latching OV protection feature. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds I_{SD}, the device will latch-off or disable the power switch switching for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation.

VOUT OV protection is also included as an integrated feature on the secondary controller (see Output Voltage Protection).

Over-Temperature Protection

The thermal shutdown circuitry senses the primary switch die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response.

Hysteretic response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power switch is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

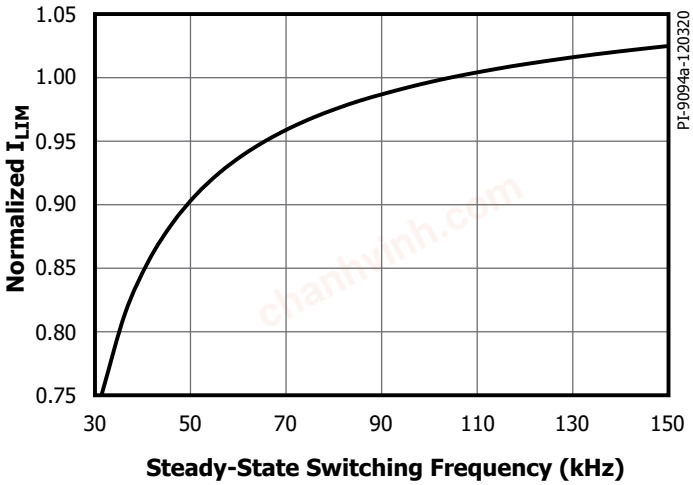


Figure 6. Normalized Primary Current vs. Frequency.

Current Limit Operation

The primary-side controller has a current limit threshold ramp that is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary switch turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At full load, switching cycles have a maximum current approaching 100% I_{LIM}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

Jitter

The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart

In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch4-CZ enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below ~ 3 V or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

In auto-restart, switching of the power switch is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency f_{OVL} for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for > $t_{AR(SK)}$.

The second is included to ensure that if communication is lost, the primary tries to restart. Although this should never be the case in normal operation, it can be useful when system ESD events (for example) causes a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

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The auto-restart is reset as soon as an AC reset occurs.

SOA Protection
In the event that there are two consecutive cycles where the I_{LIM} is reached within ~500 ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or ~25 µs. This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring
The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A sense resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to primary GND.

At power-up, after the primary bypass capacitor is charged and the ILIM state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-in for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of a internal high-voltage MOSFET on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. If the cycle off-time t_{OFF} is greater than 50 µs, the internal high-voltage MOSFET will disconnect the external sense resistor from the internal IC to eliminate current drawn through the sense resistor. The line sensing function will activate again at the beginning of the next switching cycle.

HSD Operation

When the primary controller receives a request from the secondary to begin a conduction cycle the InnoSwitch4-CZ first sends a signal through the HSD pin to turn on the high-side switch in the ClampZero for a fixed time of t_{HSD}. The amount of time required to build up energy in transformer for ZVS is a function of clamp capacitor and transformer leakage inductance. After this on-time, the InnoSwitch4-CZ will wait for a programmed delay (see: HSD to ZVS Delay Programming) before turning on the main primary switch to begin a flyback conduction cycle.

HSD to ZVS Delay Programming
In order to successfully achieve zero voltage switching (ZVS), some delay is necessary between turn-off of the ClampZero switch and conduction of the InnoSwitch4-CZ. At input low-line/full load in CCM operation, the required amount delay is a function of the drain node capacitance and the leakage inductance present in the transformer. To tune this delay t_{LLDL}, a resistor must be placed between the HSD pin and the SOURCE pin. This resistor can program one of four delays. Centering this delay at the lowest point of the Drain voltage is critical for optimizing ZVS operation.

HSD Resistor	Programmed Delay (t_{LLDL})
130 kΩ	80 ns
60 kΩ	100 ns
30 kΩ	120 ns
15 kΩ	140 ns

At input high-line/full load in DCM operation, the required amount delay is a function of the drain node capacitance and the sum of magnetizing and leakage inductance of transformer. The delay is pre-programmed to t_{HLDL} ~430 ns.

This delay switches between t_{LLDL} and t_{HLDL} based on input line voltage information. When the UNDER/OVER VOLTAGE pin current rises above 53.75 µA, the delay becomes t_{HLDL} and remains t_{HLDL} until the current falls by 7.5 µA at which point t_{LLDL} is enabled. Hysteresis is provided to ensure longer delay for high-line ZVS.

Primary-Secondary Handshake
At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from the OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross-conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen
When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in slave mode. If no pulses occurs during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

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Audible Noise Reduction Engine

The InnoSwitch4-CZ features an active audible noise reduction mode whereby the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 7 kHz and 12 kHz – 143 μs and 83 μs. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power switch is inhibited.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered by a 4.5 V (V_{BPS}) regulator which is supplied by either VOUT or FWD. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin voltage is used to determine when to turn off the SR FET in discontinuous mode operation. This is when the voltage across the $R_{DS(ON)}$ of the SR FET drops below zero volts.

In continuous conduction mode (CCM) the SR FET is turned off when the feedback pulse is sent to the primary to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off.

The mid-point of an external resistor divider network between the OUTPUT VOLTAGE and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate the output voltage. The internal voltage comparator reference voltage is V_{FB} (1.265 V).

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins is used to regulate the output current in constant current regulation mode.

Minimum Off-Time

The secondary controller initiates a cycle request using the inductive-connection to the primary. The maximum frequency of secondary-cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency

The maximum switch-request frequency of the secondary controller is f_{SREQ}.

Frequency Soft-Start

At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

The secondary controller temporarily inhibits the FEEDBACK short protection threshold ($V_{FB(OFF)}$) until the end of the soft-start timer ~10 ms. After hand-shake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the 10 ms time period.

In the event of a short-circuit or overload at start-up, the device will move directly into CC (constant-current) mode. The device will go into auto-restart (AR), if the output voltage does not rise above the $V_{FB(AR)}$ threshold before the expiration of the soft-start timer after handshake has occurred.

The secondary controller enables the FEEDBACK pin-short protection mode ($V_{FB(OFF)}$) at the end of the soft-start time period. If the output short maintains the FEEDBACK pin below the short-circuit threshold, the secondary will stop requesting pulses triggering an auto-restart cycle.

If the output voltage reaches regulation within the soft-start time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant-detection programming has already occurred.

Maximum Secondary Inhibit Period

Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30 μs.

Output Voltage Protection

In the event that the sensed voltage on the FEEDBACK pin is 2% higher than the regulation threshold, a bleed current of ~2.5 mA (3 mA max) is applied on the OUTPUT VOLTAGE pin (weak bleed). This bleed current increases to ~200 mA (strong bleed) in the event that the FEEDBACK pin voltage is raised beyond ~10% of the internal FEEDBACK pin reference voltage. The current sink on the OUTPUT VOLTAGE pin is intended to discharge the output voltage after momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

If the voltage on the FEEDBACK pin is sensed to be 20% higher than the regulation threshold, a command is sent to the primary to either latch-off or begin an auto-restart sequence (see Secondary Fault Response in Feature Code Addendum). This integrated V_{OUT} OVP can be used independently from the primary sensed OVP or in conjunction.

FEEDBACK Pin Short Detection

If the sensed FEEDBACK pin voltage is below $V_{FB(OFF)}$ at start-up, the secondary controller will complete the handshake to take control of the primary complete $t_{SS(RAMP)}$ and will stop requesting cycles to initiate auto-restart (no cycle requests made to primary for longer than $t_{AR(SK)}$ second triggers auto-restart).

During normal operation, the secondary will stop requesting pulses from the primary to initiate an auto-restart cycle when the FEEDBACK pin voltage falls below the $V_{FB(OFF)}$ threshold. The deglitch filter on the protection mode is on for less than ~10 μs. By this mechanism, the secondary will relinquish control after detecting that the FEEDBACK pin is shorted to ground.

Auto-Restart Thresholds

The FEEDBACK pin includes a comparator to detect when the output voltage falls below $V_{FB(AR)}$ of V_{FB}, for a duration exceeding $t_{FB(AR)}$. The secondary controller will relinquish control when this fault condition is sensed. This threshold is meant to limit the range of constant current (CC) operation.

SECONDARY BYPASS Pin Overvoltage Protection

The InnoSwitch4-CZ secondary controller features SECONDARY BYPASS pin OV feature similar to PRIMARY BYPASS pin OV feature. When the secondary is in control: in the event the SECONDARY BYPASS pin current exceeds $I_{BPS(SD)}$ (~7 mA) the secondary will send a command to the primary to initiate an auto-restart off-time ($t_{AR(OFF)}$) or latch-off event (see Secondary Fault Response in Feature Code Addendum).

Output Constant Current

The InnoSwitch4-CZ regulates the output current through an external current sense resistor between the ISENSE and SECONDARY

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GROUND pins where the voltage generated across the resistor is compared to an internal reference of $I_{SV(TH)}$ (~35 mV). If constant current regulation is not required, the ISENSE pin must be tied to SECONDARY GROUND pin.

SR Disable Protection

In each cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event that the voltage on the ISENSE pin exceeds approximately 3 times the CC threshold, the SR FET drive is disabled until the surge current has diminished to nominal levels.

SR Static Pull-Down

To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has internal pull down circuit "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection

In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 200 pF, the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above 200 pF, the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.

ZVS Operation in DCM and CCM Operating Modes

In order to improve conversion efficiency and eliminate switching losses, the InnoSwitch4-CZ features a drive signal to the companion Clamp Zero device as means to force the voltage across the primary power switch to zero before every conduction cycle. This mode of operation is automatically engaged in both DCM and CCM, dramatically simplifying system design. In DCM, stress across the high-side clamp switch is minimized to control the timing of the clamp-switch turn on. By restricting conduction cycles to the peak of the drain voltage ring, switching loss across the ClampZero switch is minimized.

Rather than detecting the magnetizing ring peak on the primary-side, the valley voltage of the FORWARD pin voltage as it falls below the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to maximum switching voltage across the primary power switch.

Secondary valley switching is enabled for 20 ms after DCM is detected or when (Forward Pin) ring amplitude (pk-pk) >2 V. Afterwards, valley switching is disabled, at which point switching of the active clamp switch may occur at any time a secondary request is initiated.

The secondary controller includes blanking of ~800 ns to prevent false detection of the primary "ON" cycle when the FORWARD pin rings below ground.

Unlike in InnoSwitch3 devices, the valley switching mode does not play a direct role in initiating the turn-on of the primary-side power switch, instead the active clamp circuit creates the low VDS condition on the primary power switch necessary for the it to operate with ZVS.

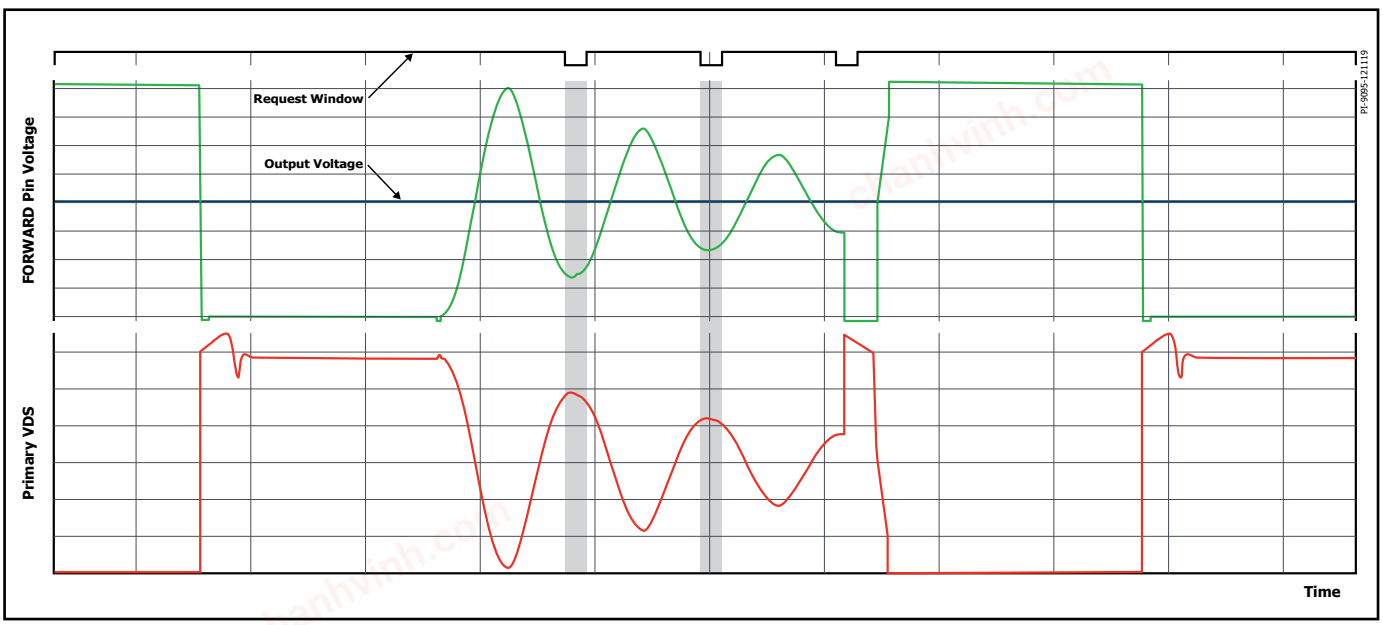


Figure 7. Intelligent Zero Voltage Switching.

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Applications Example

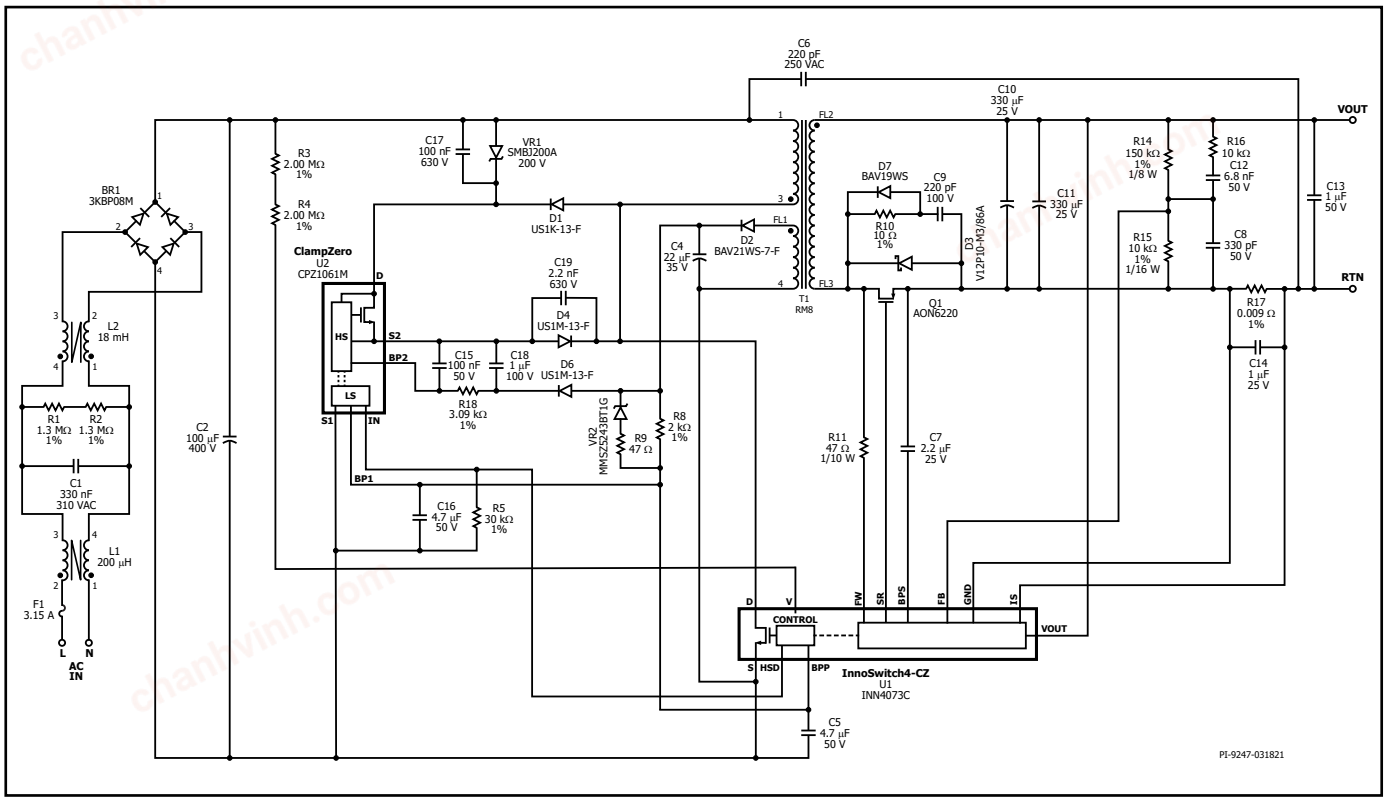


Figure 8. Schematic 20 V / 3.25 A Notebook Adapter Power Supply.

The circuit shown in Figure 8 is a 20 V, 3.25 A single output power supply using INN4073C and CPZ1061M. This single output design is DOE Level 6 and EC CoC v5 compliant.

Input fuse F1 isolates the circuit and provides protection from component failure, and the common mode choke L1 and L2 with capacitor C1 attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitor C2. Y capacitor C6 connected between the power supply output and input helps to reduce common mode EMI.

Resistors R1 and R2 discharge capacitor C1 when the power supply is disconnected from AC mains.

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch4 IC (U1). Resistors R3 and R4 provide input voltage sense protection for undervoltage and overvoltage conditions.

The primary clamp formed by diode D1 and capacitor C17 limits the peak drain voltage of U1 at the instant of turn-off of the switch inside U1. The energy stored in the leakage inductance of transformer T1 will be transferred to capacitor C17. Part of the magnetizing energy will also get transferred to C17 depending on the capacitance value used. VR1 is used to protect the InnoSwitch4 from excessive drain voltages if there is any malfunction of the power supply.

When the FluxLink signal is received from the secondary-side, the InnoSwitch4 generates an HSD signal to turn on the ClampZero device. When the ClampZero IC (U2) turns on, to achieve soft switching of the InnoSwitch4 primary switch, clamp capacitor C17 starts to charge the leakage inductance of the transformer in the case of CCM operation and both the leakage and the magnetizing inductance of the transformer in the case of DCM operation. Ultrafast diodes D1 and D4 are used to divert the transformer current from the body diode of ClampZero's high-side switch to minimize the reverse recovery energy. A small delay is provided from the instant the high-side switch turns off in order to achieve zero voltage switching on the primary switch. This delay is programmable by different resistor values of R5. Capacitor C19 will help reduce the voltage on the ClampZero IC (U2) to provide soft turn-on.

Capacitor C16 is used to provide local decoupling at the BP1 pin. Capacitor C15 provides the decoupling for BP2 pin. Diode D6 and capacitor C18 form a bootstrap circuit to provide the bias for the high-side BP2 pin. This prevents high-side internal tap turn-on and minimizes excess energy loss in drain-tap. Resistor R18 limits the current flowing into the BP2 pin.

The InnoSwitch4 IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C5) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C4. Resistor R8 limits the current being supplied to the PRIMARY BYPASS pin of InnoSwitch4 IC (U1).

Output regulation is achieved using modulation control, where the frequency and ILIM of switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled for a high value of ILIM in the selected ILIM range, and at light load or no-load, most cycles are disabled, and the ones enabled have a low value of ILIM in the selected ILIM range. Once a cycle is enabled, the switch remains on until the primary current ramps to the device current limit for the specific operating state.

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The latch-off/auto-restart primary-side overvoltage protection is obtained using Zener diode VR2 with current limiting resistor R9. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2, which then causes a current to flow into the BPP pin of InnoSwitch4 IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the U1 controller latches off to prevent any further increase in output voltage.

The secondary-side of the InnoSwitch4 IC provides output voltage, output current sensing, and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by SR FET Q1/D3 and filtered by capacitors C10 and C11. Capacitor C13 is used to reduce the high-frequency output voltage ripple. High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced via RCD snubber R10, C9, and D7. Diode D7 minimizes the dissipation in resistor R10.

The gate of Q1 is turned on by the secondary-side controller of IC U1, based on the winding voltage sensed via resistor R11 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR MOSFET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off, when the voltage drop across the MOSFET falls below a threshold of approximately $V_{SR(TH)}$.

The secondary side of the IC U1 is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C7 connected to the BPS pin of IC U1 provides decoupling for the internal circuitry.

Below the constant current (CC) regulation threshold, the device operates in constant voltage mode. During constant voltage (CV) mode operation, output voltage regulation is achieved through sensing the output voltage via divider resistors R14 and R15. The voltage across R15 is fed into the FEEDBACK pin with an internal reference voltage threshold of 1.265 V. The output voltage is regulated so as to achieve a voltage of 1.265 V on the FEEDBACK pin. Capacitor C8 provides noise filtering of the signal at the FEEDBACK pin.

During CC operation, when the output voltage falls, the device directly powers itself from the secondary winding. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C7 via resistor R11 and an internal regulator. This allows output current regulation to be maintained down to ~3.4 V. Output current is sensed by monitoring the voltage drop across resistor R17 between the IS and SECONDARY GROUND pins. A threshold of approximately 35 mV reduces losses. C14 provides filtering on the IS pin from external noise. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current.

Key Application Considerations

Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, 220 V or higher for 230 VAC input or 115 VAC with a voltage-doubler. Input capacitor voltage should be sized to meet these criteria for AC input designs.
2. Efficiency assumptions depend on power level. Smallest device power level assumes efficiency >87% increasing to >92% for the largest device.
3. Transformer primary inductance tolerance of ±7%.
4. Reflected output voltage (VOR) is set to maintain K_P = 0.7 at minimum input voltage for universal line and K_P = 1 for high input line designs (for thermally constrained environment efficiency should be >92% with larger devices).
5. Maximum conduction losses for adapters is limited to 0.6 W, 0.8 W for open frame designs.
6. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 110 °C.
8. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.
9. Below a value of 1, K_P is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_P limit of ≥0.25 is recommended. This prevents the initial current limit (I_{INT}) from being exceeded at switch turn-on.

Primary-Side Overvoltage Protection (Latch-Off/Auto-Restart Mode)

Primary-side output overvoltage protection provided by the InnoSwitch4-CZ IC uses an internal protection depending on H code that is triggered by a threshold current of I_{SD} into the PRIMARY BYPASS pin. In addition to an internal filter, the PRIMARY BYPASS pin capacitor forms an external filter helping noise immunity. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

The primary sensed OVP function can be realized by connecting a series combination of a Zener diode, a resistor and a blocking diode from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin. The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) due to poor coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. This measurement should be ideally done at the lowest input voltage and with highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. It is recommended that a Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered be selected. A forward voltage drop of 1 V can be assumed for the blocking diode. A small signal standard recovery diode is recommended. The blocking diode prevents any reverse current discharging the bias capacitor during start-up. Finally, the value of the series resistor required can be calculated such that a current higher than I_{SD} will flow into the PRIMARY BYPASS pin during an output overvoltage.

Reducing No-Load Consumption

The InnoSwitch-4 IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. Internal current source also charges the BP1 pin decoupling capacitor of the ClampZero device at start up. Use of a bias winding, however, is required to provide supply current to the PRIMARY BYPASS pin, once the InnoSwitch-4 IC has started switching. An auxiliary (bias) winding provided on the transformer serves this purpose. A bias winding driver supply to the PRIMARY BYPASS pin enables design of power supplies with no-load power consumption

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less than 30 mW. The high-side BP2 pin decoupling capacitor of the ClampZero device draws energy from the internal current source of ClampZero device, once the power supply starts switching. Resistor R8 shown in Figure 8 should be adjusted to achieve the lowest no-load input power.

Secondary-Side Overvoltage Protection (Auto-Restart Mode)
The secondary-side output overvoltage protection provided by the InnoSwitch4-CZ IC uses an internal auto restart circuit that is triggered by an input current exceeding a threshold of $I_{BPS(SD)}$ into the SECONDARY BYPASS pin. The direct output sensed OVP function can be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage needs to be the difference between 1.25 × V_{OUT} and 4.5 V – the SECONDARY BYPASS pin voltage. It is necessary to add a low value resistor in series with the OVP Zener diode to limit the maximum current into the SECONDARY BYPASS pin.

Selection of Components

Components for InnoSwitch4-CZ Primary-Side Circuit

BPP Capacitor
A capacitor connected from the PRIMARY BYPASS pin of the InnoSwitch4-CZ IC to GND provides decoupling for the primary-side controller and also selects current limit. A 0.47 µF or 4.7 µF capacitor may be used. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. Their small size also makes it ideal for compact power supplies. At least 10 V, 0805 or larger size rated X5R or X7R dielectric capacitors are recommended to ensure that minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor datasheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Bias Winding and External Bias Circuit
The internal regulator connected from the DRAIN pin of the switch to the PRIMARY BYPASS pin of the InnoSwitch4-CZ primary-side controller charges the capacitor connected to the PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply at least 4 mA of current to the PRIMARY BYPASS pin clamp BP1 and BP2 pins.

The turns ratio for the bias winding should be selected such that 7 V to 8 V minimum is developed across the bias winding at the lowest rated output voltage of the power supply at the lowest load condition. If the voltage is lower than this, no-load input power will increase.

In USB PD or rapid charge applications, the output voltage range is very wide. For example, a 45 W adapter would need to support 5 V, 9 V and 15 V and a 100 W adapter would have output voltages selectable from 5 V to 20 V. Such a wide output voltage variation results in a large change in bias winding output voltage as well. A linear regulator circuit is generally required to limit the current injected into the PRIMARY BYPASS pin of the InnoSwitch4-CZ.

The bias current from the external circuit should be set to max of I_{S1} for InnoSwitch4-CZ + max of $I_{S1(I)}$ for ClampZero to achieve lowest no-load power consumption when operating the power supply at 230 VAC input, (V_{BPP} > 5 V). A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes that can lead to higher radiated EMI.

An aluminum capacitor of at least 22 µF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and load with the lowest input AC supply voltage.

Line UV and OV Protection
Resistors connected from the UNDER/OVER INPUT VOLTAGE pin to the DC bus enable sensing of input voltage to provide line undervoltage and overvoltage protection. For a typical universal input application, a resistor value of 4 MΩ is recommended. Figure 14 shows circuit configurations that only enable either the line UV or the line OV feature.

InnoSwitch4-CZ features a primary sensed OV protection feature that can be used to latch-off the power supply. Once the power supply is latched off, it can be reset if the UNDER/OVER INPUT VOLTAGE pin current is reduced to zero. Once the power supply is latched off, even after the input supply is turned off, it can take considerable amount of time to reset the InnoSwitch4-CZ controller as the energy stored in the DC bus will continue to provide current to the controller. A fast AC reset can be achieved using the modified circuit configuration shown in Figure 15. The voltage across capacitor C5 reduces rapidly after input supply is disconnected reducing current into the INPUT VOLTAGE MONITOR pin of the InnoSwitch4-CZ IC and resetting the InnoSwitch4-CZ controller.

Primary Sensed OVP (Overvoltage Protection)
The voltage developed across the output of the bias winding tracks the power supply output voltage. Though not precise, a reasonably accurate detection of the amplitude of the output voltage can be achieved by the primary-side controller using the bias winding voltage. A Zener diode connected from the bias winding output to the PRIMARY BYPASS pin can reliably detect a secondary overvoltage fault and cause the primary-side controller to latch-off/auto-restart depending on feature code. It is recommended that the highest voltage at the output of the bias winding should be measured for normal steady-state conditions (at full load and lowest input voltage) and also under transient load conditions. A Zener diode rated for 1.25 times this measured voltage will typically ensure that OVP protection will only operate in case of a fault.

Primary-Side Clamp
Clamp Zero IC is used to provide soft switching at turn-on of the Innoswitch4-CZ primary switch as shown in Figure 8. Clamp capacitor C17 stores the leakage energy when the primary switch is turned off and delivers the stored leakage energy to the secondary when the clamp Zero device turns on while simultaneously charging up the leakage inductance in reverse direction in CCM operation and charges both leakage and magnetizing inductance in reverse direction during DCM operation. This prevents the excess voltage spike at the drain during the primary switch turn off on a cycle by cycle basis. VR1 is used across the clamp capacitor just to provide backup protection in case ClampZero IC stops switching due to any circuit fault condition.

It is recommended to choose the value of the clamp capacitor such that ~0.25 times the resonant period of the C_{CLAMP} and L_{LKG} equals the HSD pulse width for CCM designs, and ~0.5 times the resonant period of the C_{CLAMP} and L_{LKG} equals the HSD pulse width in the case of DCM-only designs. Capacitance in the range of 10 nF to 100 nF may be used depending on the design. At least 200 V, 1206 or larger size rated X7R dielectric capacitors are recommended.

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For CCM designs

$$\text{HSD Pulse Width} \sim \frac{\pi}{2}\sqrt{L_{LKG}C_{CLAMP}}$$

For DCM designs

$$\text{HSD Pulse Width} \sim \pi\sqrt{L_{LKG}C_{CLAMP}}$$

Components for InnoSwitch4-CZ Secondary-Side Circuit

SECONDARY BYPASS Pin – Decoupling Capacitor

A 2.2 µF, 10 V / X7R or X5R / 0805 or larger size multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch4-CZ IC. Since the SECONDARY BYPASS pin voltage needs to be 4.5 V before the output voltage reaches the regulation voltage level, a significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. Values lower than 1.5 µF may not offer enough capacitance, and cause unpredictable operation. The capacitor must be located adjacent to the IC pins. At least 10 V is recommended voltage rating to give enough margin from BPS voltage, and 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCC is not recommended for this reason. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor datasheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.5 V. Capacitors with X5R or X7R dielectrics should be used for best results.

When the output voltage of the power supply is 5 V or higher, the supply current for the secondary-side controller is provided by the OUTPUT VOLTAGE (VOUT) pin of the IC as the voltage at this pin is higher than the SECONDARY BYPASS pin voltage. During start-up and operating conditions where the output voltage of the power supply is below 5 V, the secondary-side controller is supplied by current from an internal current source connected to the FORWARD pin. If the output voltage of the power supply is below 5 V and the load at the output of the power supply is very light, the operating frequency can drop significantly and the current supplied to the secondary-side controller from the FORWARD pin may not be sufficient to maintain the SECONDARY BYPASS pin voltage at 4.5 V. For such applications, it is recommended that an additional active preload be used as shown in Figure 9. This load is turned on by the interface IC (or USB PD controller) when the output voltage of the power supply is below 5 V.

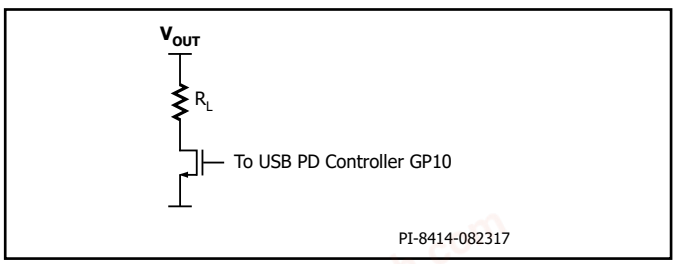


Figure 9. Active Pre-Load Circuit.

FORWARD Pin Resistor

A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current. A higher or lower resistor value should not be used as it can affect device operation such as the timing of the synchronous rectifier drive. Figures 10, 11, 12 and 13 below show examples of unacceptable and acceptable FORWARD pin voltage waveforms. V_D is forward voltage drop across the SR.

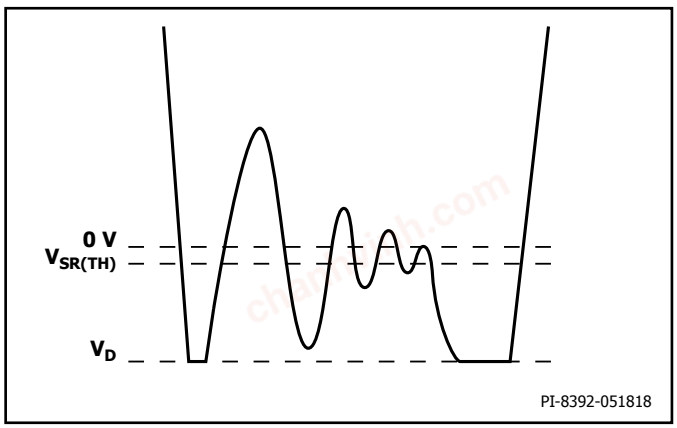


Figure 10. Unacceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

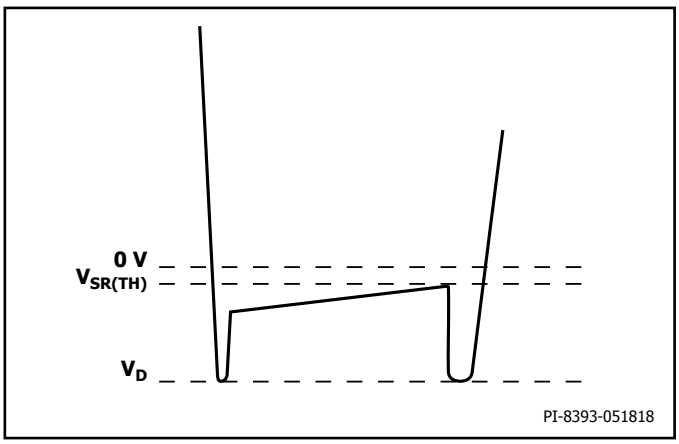


Figure 11. Acceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

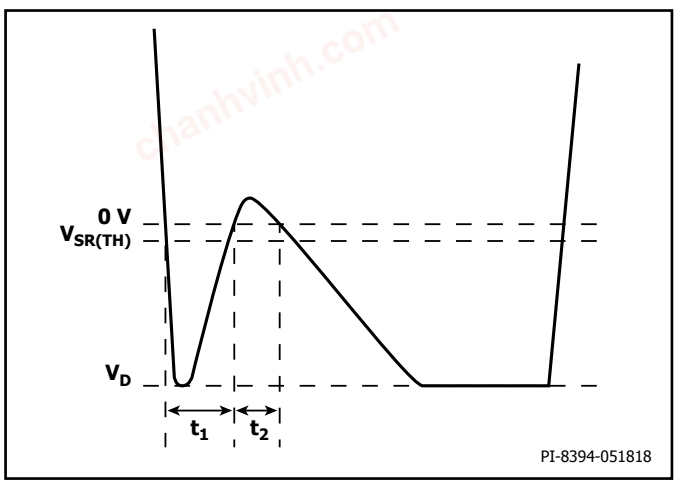


Figure 12. Unacceptable FORWARD Pin Waveform Before Handshake with Body Diode Conduction During Flyback Cycle.

Note:
If $t_1 + t_2 = 1.5\ \mu s \pm 50$ ns, the controller may fail the handshake and trigger a primary bias winding OVP latch-off/auto-restart.

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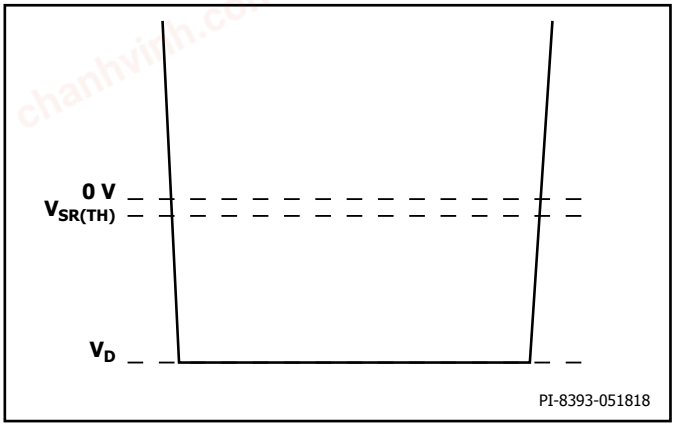


Figure 13. Acceptable FORWARD Pin Waveform Before Handshake with Body Diode Conduction During Flyback Cycle.

SR FET Operation and Selection

Although a simple diode rectifier and filter works for the output, use of an SR FET enables the significant improvement in operating efficiency often necessary to meet the European CoC and the U.S. DoE energy efficiency requirements. The secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch4-CZ IC (no additional resistors should be connected in the gate circuit of the SR FET). The SR FET is turned off once the V_{DS} of the SR FET reaches 0 V.

A FET with 18 mΩ $R_{DS(ON)}$ is appropriate for a 5 V, 2 A output, and a FET with 8 mΩ $R_{DS(ON)}$ is suitable for designs rated with a 12 V, 3 A output. The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.5 V. A FET with a high threshold voltage is therefore not suitable; FETs with a threshold voltage of 1.5 V to 2.5 V are ideal although switches with a threshold voltage (absolute maximum) as high as 4 V may be used provided their data sheets specify $R_{DS(ON)}$ across temperature for a gate voltage of 4.5 V.

A schottky diode is recommended across the SR FET. Since the SR FET gate turns off during the ClampZero switch conduction period, there will be energy transfer to secondary during this period typically about 500 ns. In addition to this there is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the InnoSwitch4-CZ IC detects end of the flyback cycle, voltage across SR FET $R_{DS(ON)}$ reaches 0 V, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET or the external parallel Schottky diode. Use of the Schottky diode parallel to the SR FET may provide higher efficiency, and typically a 1 A surface mount Schottky diode is adequate. However, the gains are modest. An efficiency increase of 0.2% or higher is expected with the addition of Schottky diode for designing with an output current rating >2 A.

The voltage rating of the Schottky diode and the SR FET should be at least 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. 60 V rated FETs and diodes are suitable for most 5 V designs that use a V_{OR} < 60 V, and 100 V rated FETs and diodes are suitable for 12 V designs.

The interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) leads to ringing on the voltage waveform at the instance of voltage reversal at the winding due to primary switch turn-on. This ringing can be suppressed using an RC snubber connected across the SR FET. A snubber resistor in the range of 10 Ω to 47 Ω may be used (higher resistance values lead to noticeable drop in efficiency). A capacitance value of 220 pF to 2.2 nF is adequate for most designs.

Output Capacitor

Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies though the use of aluminum-polymer solid capacitors have gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and high RMS ripple current rating. These capacitors enable the design of ultra-compact chargers and adapters.

Typically, 200 μF to 300 μF of aluminum-polymer capacitance per ampere of output current is adequate. The other factor that influences choice of the capacitance is the output ripple. Ensure that capacitors with a voltage rating higher than the highest output voltage plus sufficient margin be used.

Output Voltage Feedback Circuit

The output voltage FEEDBACK pin voltage is 1.265 V [V_{FB}]. A voltage divider network should be connected at the output of the power supply to divide the output voltage such that the voltage at the FEEDBACK pin will be 1.265 V when the output is at its desired voltage. The lower feedback divider resistor should be tied to the SECONDARY GROUND pin. A 300 pF (or smaller) decoupling capacitor should be connected at the FEEDBACK pin to the SECONDARY GROUND pin of the InnoSwitch4-CZ IC. This capacitor should be placed close to the InnoSwitch4-CZ IC.

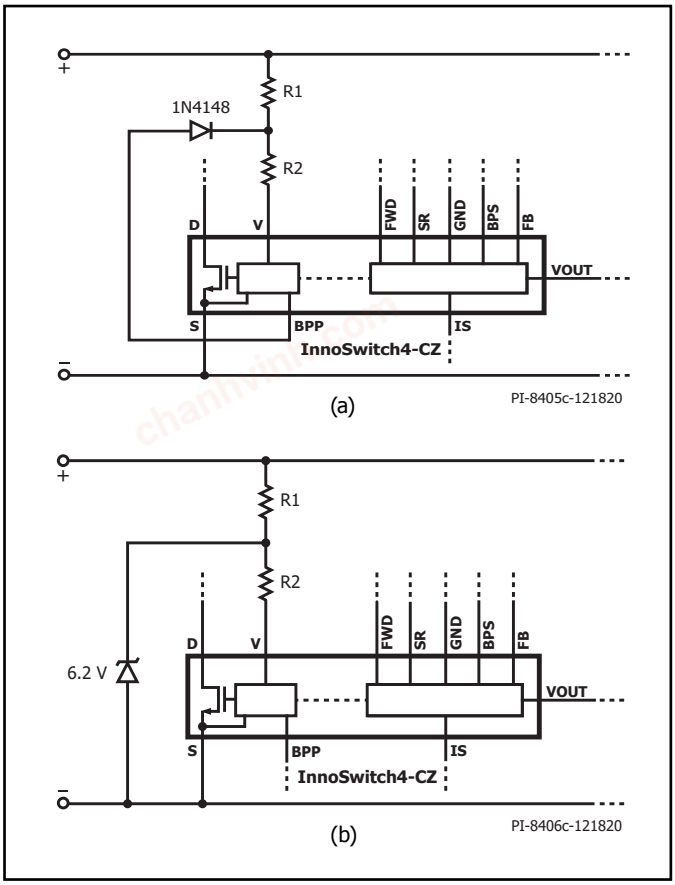


Figure 14. (a) Line OV Only; (b) Line UV Only.

Output Overload Protection

For output voltage below the V_{PK} threshold, the InnoSwitch4-CZ IC will limit the output current once the voltage across the IS and GND pins exceeds the current limit or $I_{SV(TH)}$ threshold. This provides

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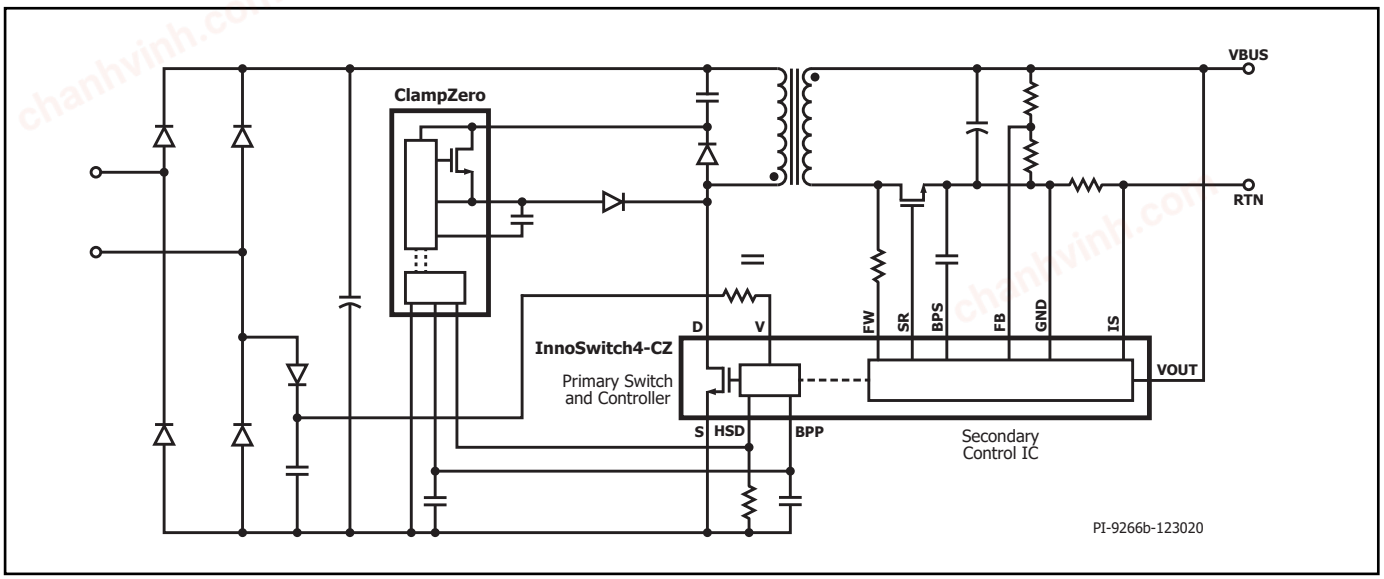


Figure 15. Fast AC Reset Configuration.

current limited or constant current operation. The current limit is set by the programming resistor between the ISENSE and SECONDARY GROUND pins. For any output voltage above the V_{PK} threshold, InnoSwitch4-CZ IC will provide a constant power characteristic. An increase in load current will result in a drop in output voltage such that the product of output voltage and current equals the maximum power set by the product of V_{PK} and set current limit.

Interfacing with USB PD and Rapid Charge Controllers
A micro controller can be used to alter the feedback voltage divider in order to increase or decrease the output voltage. The interface IC can also use the signal from the InnoSwitch4-CZ ISENSE pin to sense output current and provide current, power limiting or protection features.

Recommendations for Circuit Board Layout

See Figure 16 and Figure 17 for a recommended circuit board layout for an InnoSwitch4-CZ based power supply.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors
The PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

Primary Clamp Circuit
Active clamp is used to achieve the ZVS turn-on on the primary switch and to limit the peak voltage on the drain pin at turn-off. ClampZero IC is used along with clamp capacitor to achieve this. To reduce EMI, minimize the loop from the clamp components to the transformer and Innoswitch4-CZ.

Thermal Considerations
The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without compromising EMI performance. Similarly for the output SR switch, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR switch.

Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage.

Y Capacitor
The Y capacitor should be placed directly between the primary input filter capacitor positive terminal and the output positive or return terminal of the transformer secondary. This routes high amplitude common mode surge currents away from the IC. Note – if an input pi-filter (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Output SR Switch
For best performance, the area of the loop connecting the secondary winding, the output SR switch and the output filter capacitor, should be minimized.

ESD
Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD / HIPOT requirements.

The spark gap is best placed directly between output positive rail and one of the AC inputs. In this configuration a 6.2 mm spark gap is often sufficient to meet the creepage and clearance requirements of many applicable safety standards. This is less than the primary to secondary spacing because the voltage across spark gap does not exceed the peak of the AC input.

Drain Node
The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and trace lengths minimized.

The loop area of the loop comprising of the input rectifier filter capacitor, the primary winding and the IC primary-side switch should be kept as small as possible.

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Layout Example

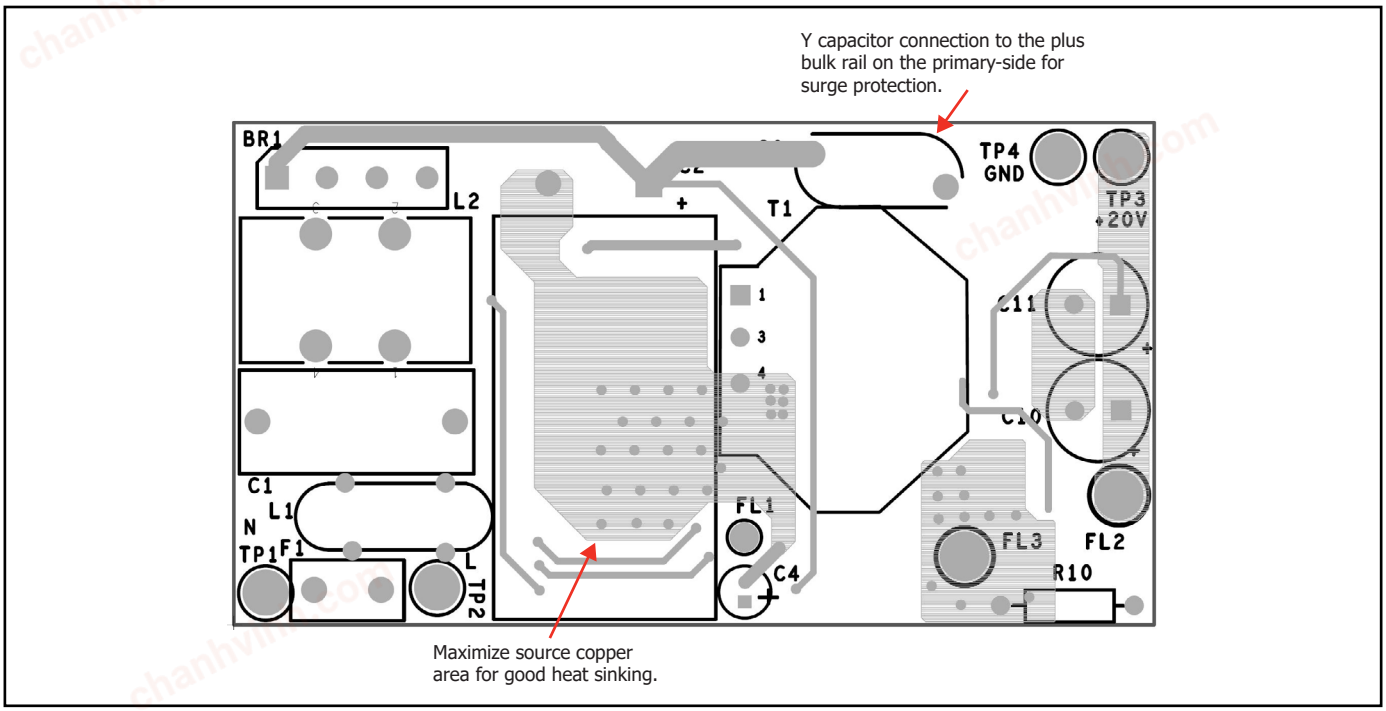


Figure 16. PCB Layout Top Side.

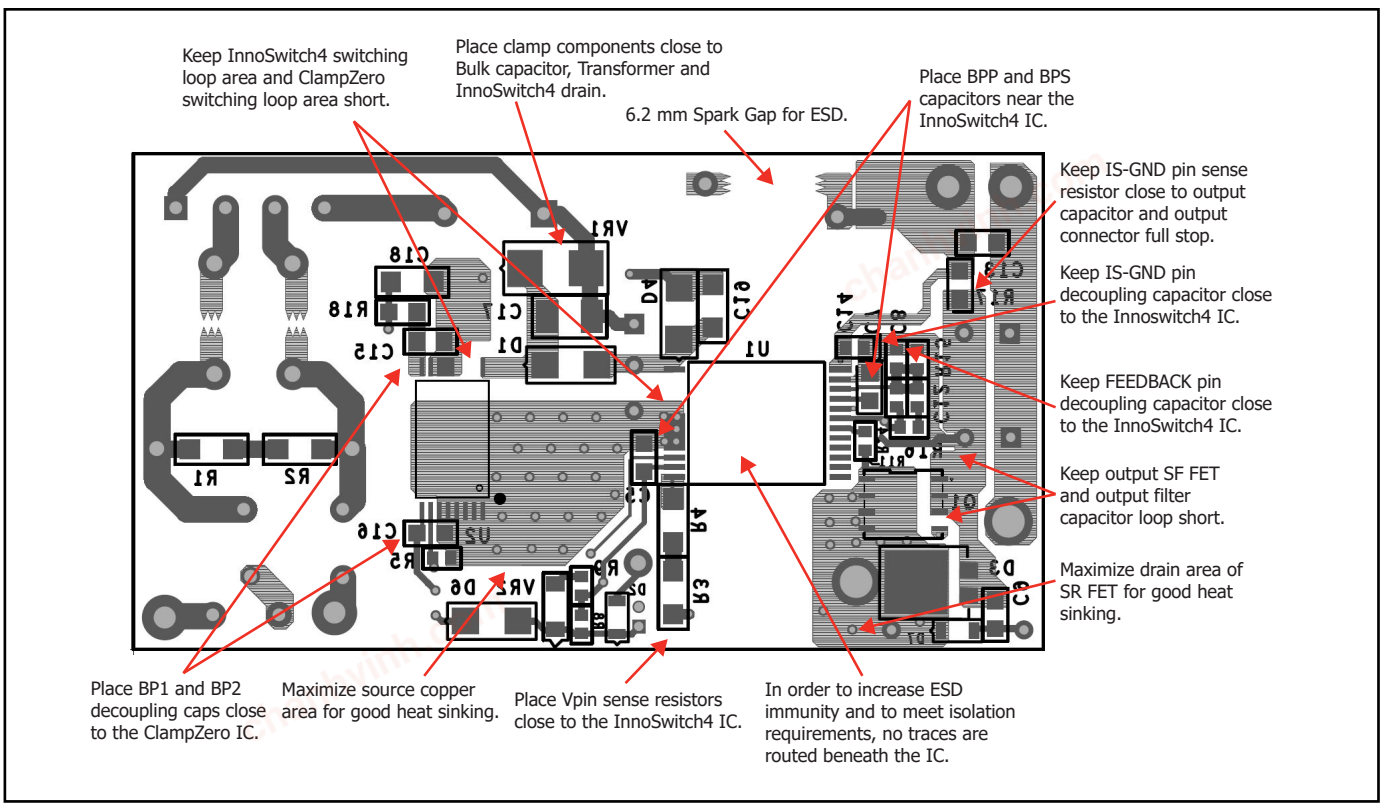


Figure 17. PCB Layout Bottom Side.

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Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area.
2. A small capacitor in parallel to the clamp diode on the primary-side can help reduce radiated EMI.
3. A resistor in series with the bias winding helps reduce radiated EMI.
4. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common mode noise. However, the same performance can be achieved by using shield windings on the transformer. Shield windings can also be used in conjunction with common mode filter inductors at input to improve conducted and radiated EMI margins.
5. Adjusting SR switch RC snubber component values can help reduce high frequency radiated and conducted EMI.
6. A pi-filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI.
7. A 1 µF ceramic capacitor connected at the output of the power supply helps to reduce radiated EMI.

Recommendations for Transformer Design

Transformer design must ensure that the power supply delivers the rated power at the lowest input voltage. The lowest voltage on the rectified DC bus depends on the capacitance of the filter capacitor used. At least 2 µF/W is recommended to always keep the DC bus voltage above 70 V, though 3 µF/W provides sufficient margin. The ripple on the DC bus should be measured to confirm the design calculations for transformer primary-winding inductance selection.

Switching Frequency (f_{SW})

It is a unique feature in InnoSwitch4-CZ that for full load, the designer can set the switching frequency to between 50 kHz to 140 kHz. For a smaller transformer, the full load switching frequency could be set to 130 kHz. When setting the full load switching frequency it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed 140 kHz which may trigger auto-restart due to overload protection.

Reflected Output Voltage, V_{OR} (V)

This parameter describes the effect on the primary switch drain voltage of the secondary-winding voltage during diode/SR conduction which is reflected back to the primary through the turns ratio of the transformer. To make full use of ZVS capability and ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.7 at minimum input voltage for universal input and K_P = 1 for high-line-only conditions.

Consider the following for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch4-CZ device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR switches.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents the V_{OR} should be reduced to get highest efficiency. For output voltages above 15 V, V_{OR} should be higher to maintain an acceptable PIV across the output synchronous rectifier.

Ripple to Peak Current Ratio, K_P

A K_P below 1 indicates continuous conduction mode, where K_P is the ratio of ripple-current to peak-primary-current (Figure 19).

$$K_P \equiv K_{RP} = I_R / I_P$$

A value of K_P higher than 1, indicates discontinuous conduction mode (Figure 18) .In this case K_P is the ratio of primary switch off-time to the secondary diode conduction-time.

$$K_P \equiv K_{DP} = (1 - D) \times T/ t = V_{OR} \times (1 - D_{MAX}) / ((V_{MIN} - V_{DS}) \times D_{MAX})$$

It is recommended that a K_P close to 0.7 at the minimum expected DC bus voltage should be used for most InnoSwitch4-CZ designs. Since InnoSwitch4-CZ provides ZVS benefit a K_P value of <1 results in lower primary-side switch losses and higher transformer efficiency by lowering the primary RMS current.

For a typical USB PD and rapid charge designs which require a wide output voltage range, K_P will change significantly as the output voltage changes. K_P will be high for high output voltage conditions and will drop as the output voltage is lowered. The PIXls spreadsheet can be used to effectively optimize selection of K_P, inductance of the primary winding, transformer turns ratio, and the operating frequency while ensuring appropriate design margins.

Core Type

Choice of a suitable core is dependent on the physical limits of the power supply enclosure. It is recommended that only cores with low loss be used to reduce thermal challenges.

Safety Margin, M (mm)

For designs that require safety isolation between primary and secondary that are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin is important. For universal input designs a total margin of 6.2 mm is typically required – 3.1 mm being used on either side of the winding. For vertical bobbins the margin may not be symmetrical. However if a total margin of 6.2 mm is required then the physical margin can be placed on only one side of the bobbin. For designs using triple insulated wire it may still be necessary to add a small margin in order to meet required creepage distances. Many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance to determine what specific margin is required. As the margin reduces the available area for the windings, the winding area will disproportionately reduce for small core sizes.

It is recommended that for compact power supply designs using an InnoSwitch4-CZ IC, triple insulated wire should be used.

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Primary Layers, L

Primary layers should be in the range of 1 ≤ L ≤ 3 and in general should be the lowest number that meets the primary current density limit (CMA). A value of ≥200 Cmils / Amp can be used as a starting point for most designs. Higher values may be required due to thermal constraints. For universal input designs minimum 2% leakage inductance is required to achieve ZVS during CCM operation. However for DCM only designs it is recommended to minimize leakage inductance. Designs with more than 3 layers are possible but the increased leakage inductance and the physical fit of the windings should be considered. A split primary construction may be helpful for DCM only designs. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. This arrangement is often disadvantageous for low power designs as this typically increases common mode noise and adds cost to the input filtering.

Maximum Operating Flux Density, B_M (Gauss)

A maximum value of 3800 gauss at the peak device current limit (at 180 kHz) is recommended to limit the peak flux density at start-up and under output short-circuit conditions. Under these conditions the output voltage is low and little reset of the transformer occurs during the switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch4-CZ IC provide sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

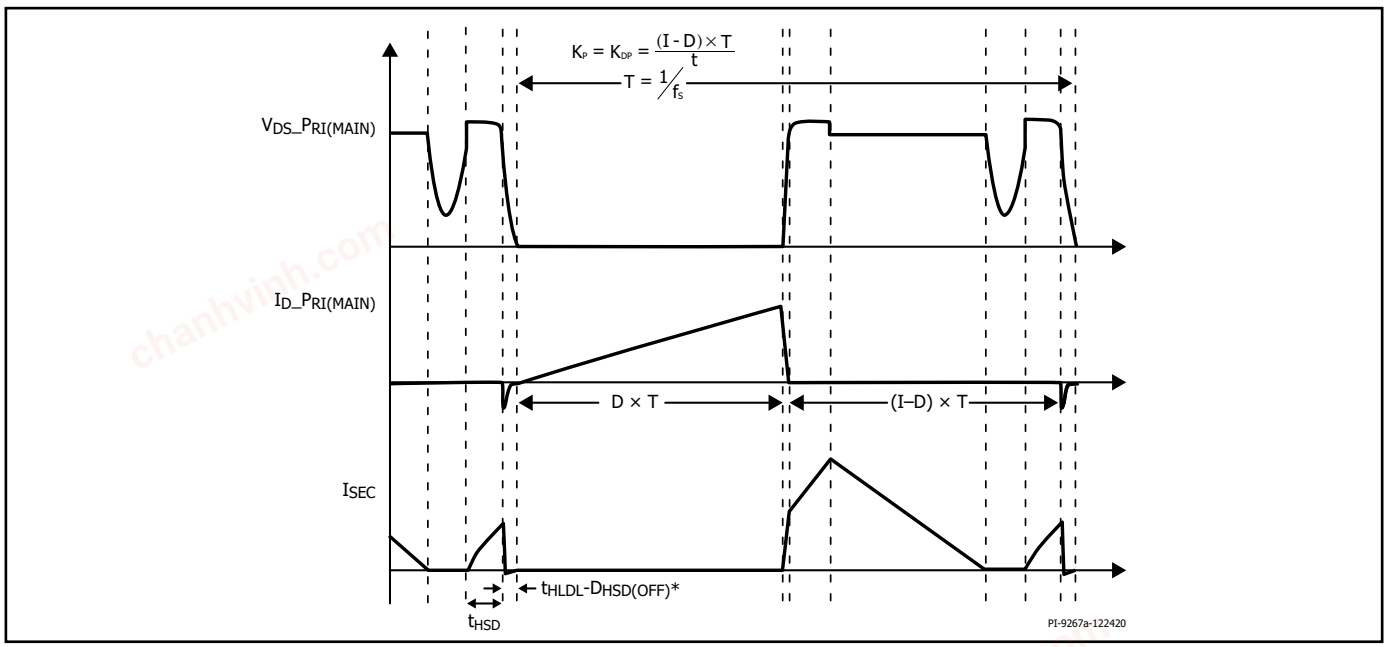


Figure 18. Discontinuous Conduction Mode Current Waveform at High-Line, K_P > 1. *$D_{HSD(OFF)}$ is delay from HSD low to ClampZero OFF, please refer to ClampZero data sheet.

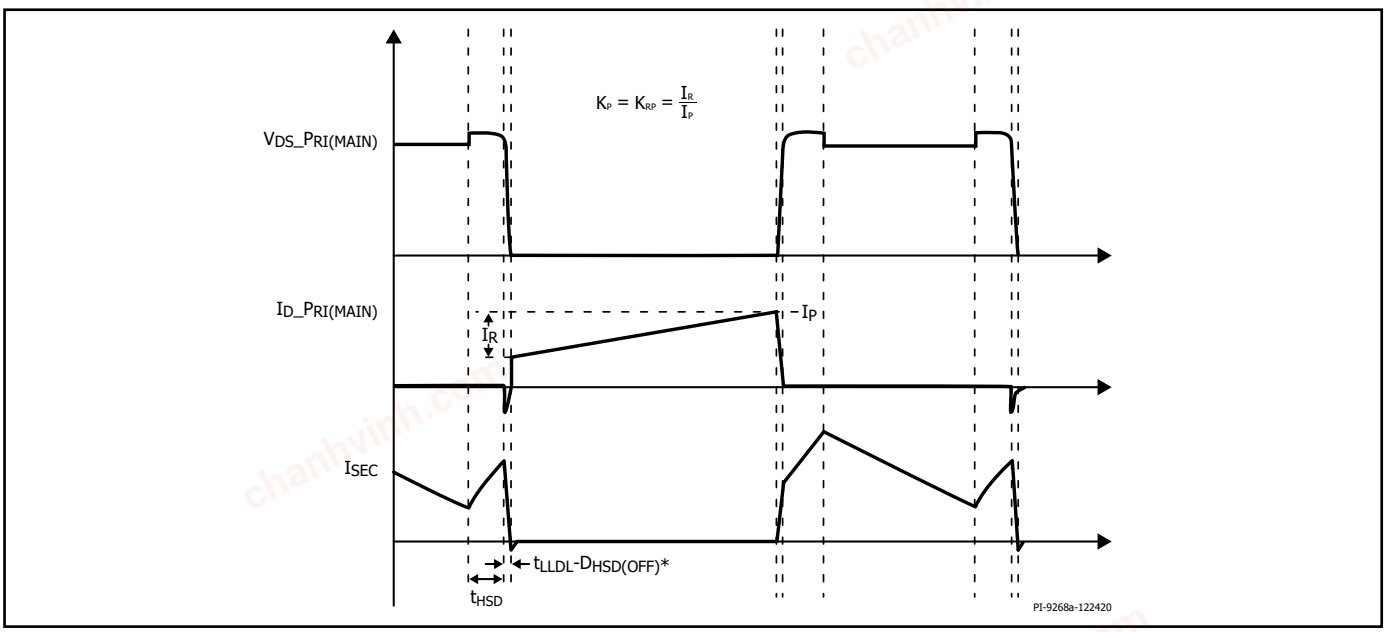


Figure 19. Continuous Conduction Mode Current Waveform at Low-Line, K_P < 1. *$D_{HSD(OFF)}$ is delay from HSD low to ClampZero OFF, please refer to ClampZero data sheet.

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Transformer Primary Inductance, (LP)

Once the lowest operating input voltage, switching frequency at full load, and required VOR are determined, the transformers primary inductance can be calculated. The PIXls design spreadsheet can be used to assist in designing the transformer.

Quick Design Checklist

As with any power supply, the operation of all InnoSwitch4-CZ designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions.

As a minimum, the following tests are strongly recommended:

1. Maximum Drain Voltage – Verify that V_{DS} of InnoSwitch4-CZ and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum drain current for the primary switch should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for InnoSwitch4-CZ IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of the InnoSwitch4-CZ IC. Under low-line, maximum power, a maximum InnoSwitch4-CZ SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Design Considerations When Using PowiGaN Devices

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 20.

V_{OR} is the reflected output voltage across the primary winding when the secondary is conducting. V_{BUS} is the DC voltage connected to one end of the transformer primary winding.

In addition to V_{BUS}+V_{OR}, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch. V_{CLM} in Figure 20 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of V_{BUS}, V_{OR} and V_{CLM}.

V_{OR} and the clamp voltage V_{CLM} should be selected such that the peak drain voltage is lower than 650 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V under abnormal transient operating conditions. This ensures excellent long term reliability and design margin.

To make full use of ZVS capability and ensure flattest efficiency over line/load, set reflected output voltage (VOR) to maintain K_P = 0.7 at minimum input voltage for universal input and $K_P \geq 1$ for high-line-only conditions.

Consider the following for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given PowiGaN device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR FETs.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

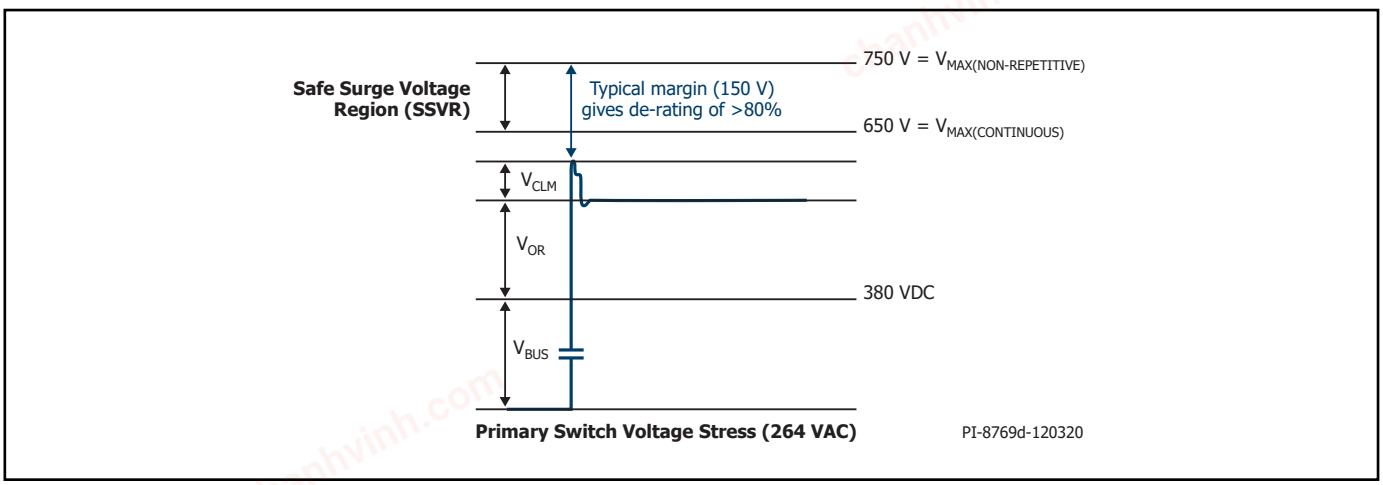


Figure 20. Peak Drain Voltage for 264 VAC Input Voltage.

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There are some exceptions to this. For very high output currents the VOR should be reduced to get highest efficiency. For output voltages above 15 V, VOR should be maintained higher to maintain an acceptable PIV across the output synchronous rectifier.

V_{OR} choice will affect the operating efficiency and should be selected carefully. Table below shows the typical range of V_{OR} for optimal performance:

Output Voltage	Optimal Range for VOR
5 V	45 - 70
12 V	80 - 120
15 V	100 - 135
20 V	120 - 160
24 V	135 - 180

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Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage ..... -0.3 V to 750 V[5]
DRAIN Pin Peak Current: INN4073C ..... 6.5 A[7]
INN4074C ..... 10 A[7]
INN4075C ..... 14 A[7]
BPP/BPS Pin Voltage ..... -0.3 to 6 V
BPP/BPS Current ..... 100 mA
FWD Pin Voltage ..... -1.5 V to 150 V
FB Pin Voltage ..... -0.3 V to 6 V
SR Pin Voltage ..... -0.3 V to 6 V
VOUT Pin Voltage ..... -0.3 V to 27 V
V Pin Voltage ..... -0.3 V to 650 V
HSD Pin Voltage ..... -0.3 V to 6 V
IS Pin Voltage[6] ..... -0.3 V to 0.3 V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[3] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 105 °C
Lead Temperature[4] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. Maximum drain voltage (non-repetive pulse) ..... -0.3 V to 750 V.
   Maximum continuous drain voltage ..... -0.3 V to 650 V.
6. Absolutely maximum voltage for less than 500 µsec is 3 V.
7. Please refer to Figure 24 about maximum voltage and current combinations.

Thermal Resistance

Thermal Resistance:
(θ_{JA}) ..... 81 °C/W[1], 75 °C/W[2]
(θ_{JC}) ..... 18 °C/W[1]

Notes:
1. Soldered to 0.36 sq. inch (232 mm²) 2 oz. (610 g/m²) copper clad.
2. Soldered to 1 sq. inch (645 mm²), 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (16-19) to pin 24	0.6	A
Primary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket)	0.125	W
Package Characteristics			
Clearance		12.1	mm (typ)
Creepage		11.7	mm (typ)
Distance Through Insulation (DTI)		0.4	mm (min)
Transient Isolation Voltage		6	kV (min)
Comparative Tracking Index (CTI)		600	-

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Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Startup Switching Frequency	f_{SW}	T_J = 25 °C		23	25	27	kHz
Jitter Modulation Frequency	f_M	T_J = 25 °C, f_{SW} = 100 kHz		0.80	1.25	1.70	kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C		10.5	16.5	21.5	µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}					$t_{OFF(MIN)}$	µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching) T_J = 25 °C		145	300	425	µA
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at f_{SREQ}) T_J = 25 °C	INN4073C	1.7	2.1	2.7	mA
			INN4074C	2.7	3.2	3.7	
			INN4075C	2.7	3.2	3.7	
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C		-1.75	-1.35	-0.88	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C		-5.98	-4.65	-3.32	
BPP Pin Voltage	V_{BPP}	T_J = 25 °C			5	5.16	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.5		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		5.16	5.36	5.7	V
BPP Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.8	3.15	3.5	V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C		23.1	25.2	27.5	µA
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C		20.5	23	25	µA
Brown-Out Delay Time	t_{UV-}	T_J = 25 °C			35		ms
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C		106	115	118	µA
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C			8		µA
UV/OV Pin Line Overvoltage Recovery Theshold	I_{OV-}	T_J = 25 °C		100			µA

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Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Line Fault Protection							
VOLTAGE Pin Line Over-voltage Deglitch Filter	t_{OV+}	T_J = 25 °C See Note B			3		µs
VOLTAGE Pin Voltage Rating	V_V	T_J = 25 °C		650			V
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF	I_{LIMIT} (Switch switching at 100 kHz)	di/dt = 400 mA/µs T_J = 25 °C	INN4073C	1581	1700	1819	mA
		di/dt = 475 mA/µs T_J = 25 °C	INN4074C	1953	2100	2247	
		di/dt = 500 mA/µs T_J = 25 °C	INN4075C	2139	2300	2461	
Increased Current Limit (BPP) Capacitor = 4.7 µF	$I_{LIMIT+1}$ (Switch switching at 100 kHz)	di/dt = 400 mA/µs T_J = 25 °C	INN4073C	1748	1900	2052	mA
		di/dt = 475 mA/µs T_J = 25 °C	INN4074C	2162	2350	2538	
		di/dt = 500 mA/µs T_J = 25 °C	INN4075C	2374	2576	2786	
Overload Detection Frequency	f_{OVL}	T_J = 25 °C		130	140	151	kHz
BYPASS Pin Latching Shutdown Threshold Current	I_{SD}	T_J = 25 °C		6.0	7.5	11.3	mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C		75	82	89	ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C		1.70	2.00	2.11	sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C			0.20		sec
HSD On-Time	t_{HSD}	T_J = 25 °C		440	500	560	ns

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Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	INN4073C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.52	0.68	Ω
			T_J = 100 °C		0.78	1.02	
		INN4074C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		INN4075C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP} + 0.1$ V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BPP} = V_{BPP} + 0.1$ V V_{DS} = 325 V T_J = 25 °C			15		µA
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			70		°C
Drain Supply Voltage				50			V

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Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary						
Feedback Pin Voltage	V_{FB}	T_J = 25 °C	1.250	1.265	1.280	V
Maximum Switching Frequency	f_{SREQ}	T_J = 25 °C	164	180	194	kHz
Auto-Restart Threshold	$V_{VO(AR)}$	T_J = 25 °C		3.45		V
Output Voltage Pin Auto-Restart Timer	$t_{FB(AR)}$ $t_{VOUT(AR)}$ $t_{IS(AR)}$	T_J = 25 °C		50		ms
BPS Pin Current at No-Load	I_{SNL}	T_J = 25 °C		380	485	µA
BPS Pin Voltage	V_{BPS}		4.3	4.5	4.7	V
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)(TH)}$		3.60	3.80	4.00	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)(H)}$			0.7		V
Current Limit Voltage Threshold	$I_{SV(TH)}$	Set by External Resistor T_J = 25 °C	35.17	36	36.62	mV
FWD Pin Voltage	V_{FWD}		150			V
Minimum Off-Time	$t_{OFF(MIN)}$		1.76	1.9	2.03	µs
BPS Pin Latch Command Shutdown Threshold Current	$I_{BPS(SD)}$		5.2	8.9	12	mA
Feedback Pin Short-Circuit	$V_{FB(OFF)}$	T_J = 25 °C		100		mV

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Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Synchronous Rectifier @ T_J = 25 °C						
SR Pin Drive Voltage	V_{SR}		4.3	4.5	4.7	V
SR Pin Voltage Threshold	$V_{SR(TH)}$			-6	0	mV
SR Pin Pull-Up Current	$I_{SR(PU)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz	125	165	195	mA
SR Pin Pull-Down Current	$I_{SR(PD)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz	315	365	415	mA
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2 nF 10-90%		50		ns
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2 nF 90-10%		25		ns
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 10 mA	6	8.9	10.5	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 10 mA	2.4	3.3	5	Ω

NOTES:

A. This parameter is derived from characterization.

B. This parameter is guaranteed by design.

C. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	BPP Capacitor Minimum	Value Tolerance Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

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Typical Performance Curves

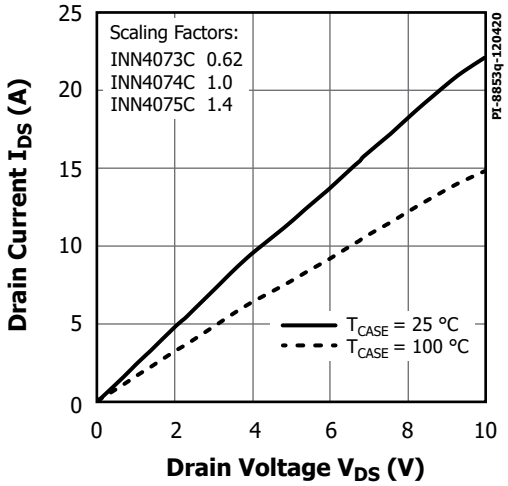


Figure 21. Output Characteristics.

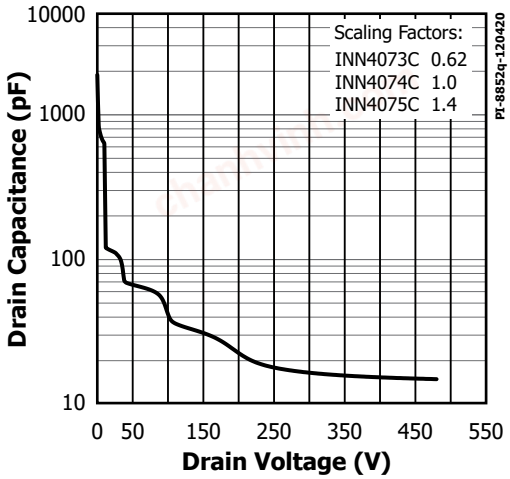


Figure 22. C_{OSS} vs. Drain Voltage.

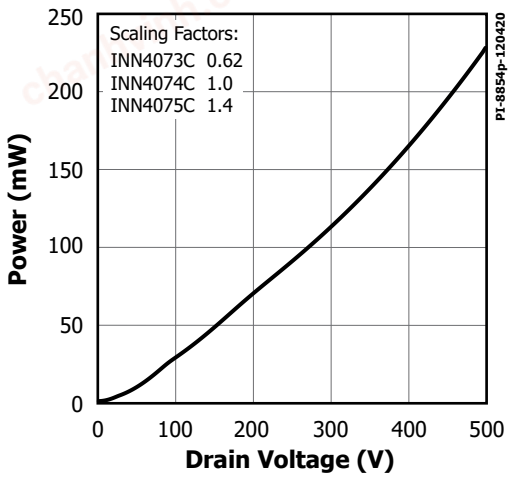


Figure 23. Drain Capacitance Power.

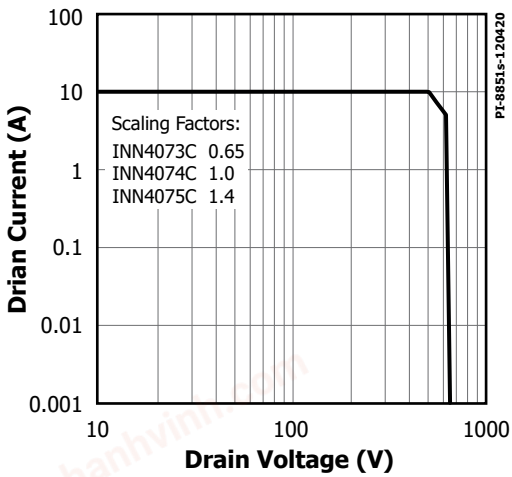


Figure 24. Maximum Allowable Drain Current vs. Drain Voltage.

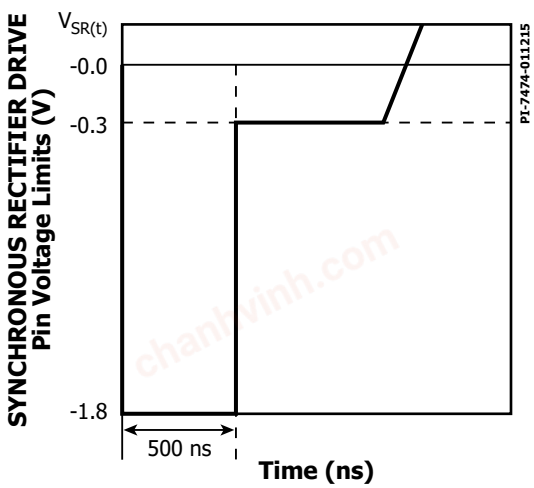


Figure 25. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

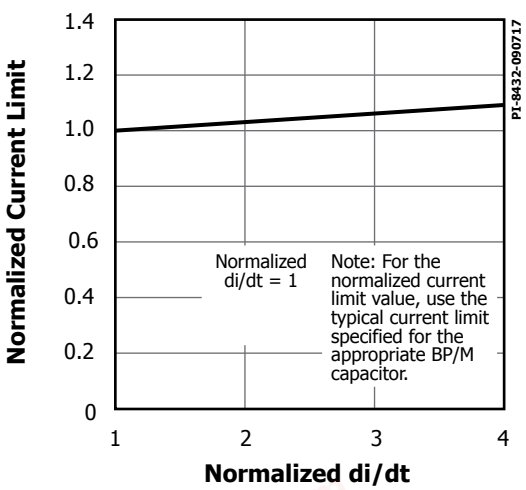
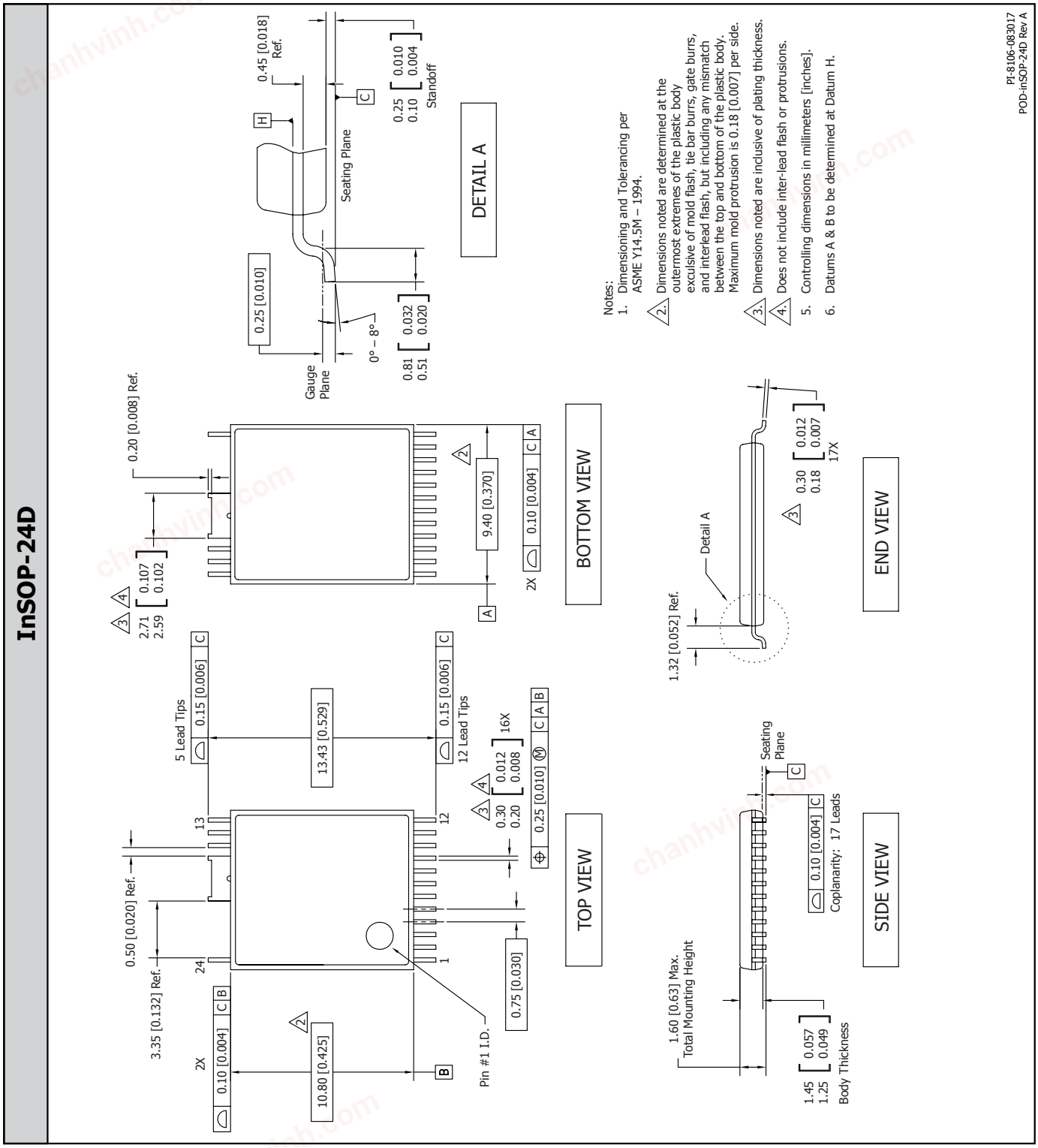


Figure 26. Standard Current Limit vs. di/dt.

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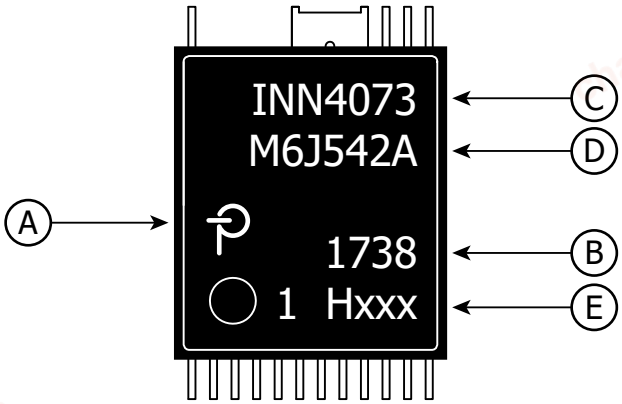


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A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Test Sublot and Feature Code

PI-8727k-123020

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Feature Code Table

Feature Code	AR Threshold	OTP Response	AR and OVL Response	Output Profile	V_{OUT} OVP	Secondary Fault Response	Line OV/UV
H181	63%	Hysteretic	AR	Fixed CC	Enable	AR	Enabled / Enable
H182	3.45 V	Latch-Off	AR	Fixed CC	–	Latch-Off	Enabled / Enable
H183	63%	Latch-Off	Latch-Off	Fixed CC	–	Latch-Off	Enabled / Enable
H185	OL	Hysteretic	AR	CV only	Enable	AR	Enabled / Enable
H186	OL	Hysteretic	AR	CV only	Enable	Latch-Off	Disabled / Enabled

MSL Table

Part Number	MSL Rating
INN4073C - INN4075C	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information

INN 4073 C - H181 - TL

- **InnoSwitch4-CZ Product Family**
- **CZ Series Number**
- **Package Identifier**
  - C | InSOP-24D
- **Features Code**
- **Tape & Reel and Other Options**
  - TL | Tape & Reel, 2 k pcs per reel.

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Notes

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Revision	Notes	Date
B	Code A release.	12/20
C	Corrected Typ value for $I_{SR(PD)}$.	02/21
D	Updated Figure 8.	03/21
E	Updated per DSC-21151 Primary-Side Current Rating on page 19.	04/21
F	Removed H184 Feature Code from Feature Code Table on page 28.	05/21

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