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# H-Bridge in APM16 Series for LLC and Phase-shifted DC-DC Converter

# NXV65HR82DS1, NXV65HR82DS2, NXV65HR82DZ1, NXV65HR82DZ2

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### Features

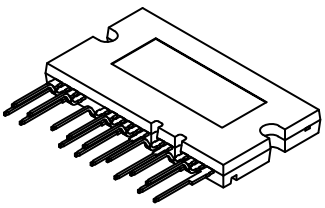
- SIP or DIP H−Bridge Power Module for On−board Charger (OBC) in EV or PHEV
- 5 kV/1 s Electrically Isolated Substrate for Easy Assembly
- Creepage and Clearance per IEC60664−1, IEC 60950−1
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- Lead Free, RoHS and UL94V−0 Compliant
- Automotive Qualified per AEC Q101 and AQG324 Guidelines

### Applications

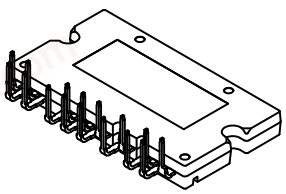
- DC−DC Converter for On−board Charger in EV or PHEV

### Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and $CO_2$ Emission
- Simplified Assembly, Optimized Layout, High Level of Integration, and Improved Thermal Performance



**APMCA−A16**
**16 LEAD**
**CASE MODGF**



**APMCA−B16**
**16 LEAD**
**CASE MODGJ**

### MARKING DIAGRAM

XXXXXXXXXX
ZZZ ATYWW
NNNNNNN

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.

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## Pin Configuration and Block Diagram

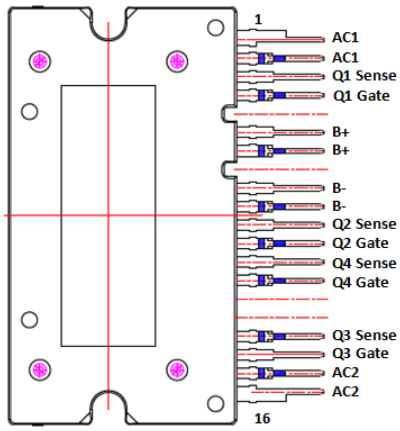



**Figure 1. Pin Configuration**

**Table 1. PIN DESCRIPTION**

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1, 2 | AC1 | Phase 1 Leg of the H−Bridge |
| 3 | Q1 Sense | Source Sense of Q1 |
| 4 | Q1 Gate | Gate Terminal of Q1 |
| 5, 6 | B+ | Positive Battery Terminal |
| 7, 8 | B− | Negative Battery Terminal |
| 9 | Q2 Sense | Source Sense of Q2 |
| 10 | Q2 Gate | Gate Terminal of Q2 |
| 11 | Q4 Sense | Source Sense of Q4 |
| 12 | Q4 Gate | Gate Terminal of Q4 |
| 13 | Q3 Sense | Source Sense of Q3 |
| 14 | Q3 Gate | Gate Terminal of Q3 |
| 15, 16 | AC2 | Phase 2 Leg of the H−Bridge |

*Block Diagram*

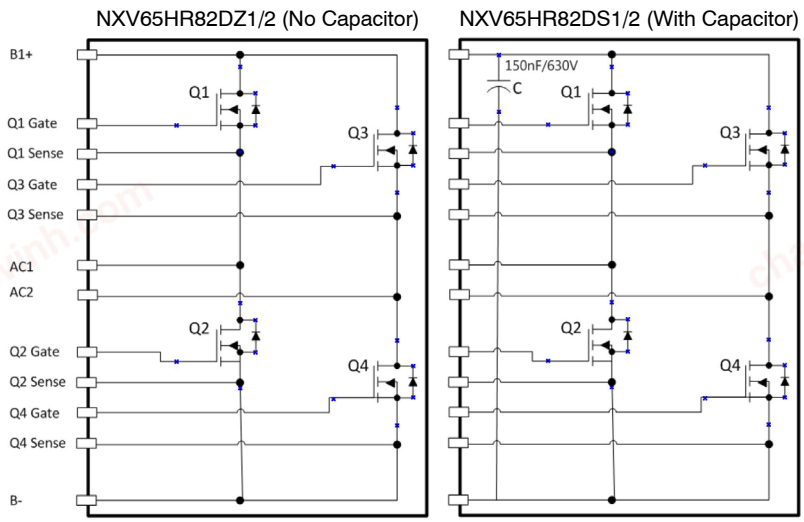



**Figure 2. Schematic**

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**Table 2. ABSOLUTE MAXIMUM RATINGS** ($T_J$ = 25°C, Unless Otherwise Specified)

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $V_{DS}$ (Q1~Q4) | Drain−to−Source Voltage | 650 | V |
| $V_{GS}$ (Q1~Q4) | Gate−to−Source Voltage | ±20 | V |
| $I_D$ (Q1~Q4) | Drain Current Continuous ($T_C$ = 25°C, $V_{GS}$ = 10 V) (Note 1) | 26 | A |
| | Drain Current Continuous ($T_C$ = 100°C, $V_{GS}$ = 10 V) (Note 1) | 17 | A |
| $P_D$ | Power Dissipation (Note 1) | 126 | W |
| $T_J$ | Maximum Junction Temperature | −55 to +150 | °C |
| $T_C$ | Maximum Case Temperature | −40 to +125 | °C |
| $T_{STG}$ | Storage Temperature | −40 to +125 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum continuous current and power, without switching losses, to reach $T_J$ = 150°C respectively at $T_C$ = 25°C and $T_C$ = 100°C; defined by design based on MOSFET $R_{DS(ON)}$ and $R_{\theta JC}$ and not subject to production test

**Table 3. SINGLE PULSE AVALANCHE ENERGY**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $E_{AS}$ (Q1~Q4) | Single Pulsed Avalanche Energy (Note 2) | 510 | mJ |
| $E_{AS}$ (Q1~Q4) | Single Pulsed Avalanche Energy (Note 2) | 21 | mJ |
| $I_{AS}$ | Avalanche Current | 4.8 | A |

2. 510 mJ is characterized at $T_J$ = 25°C, L = 44.3 mH, $I_{AS}$ = 4.8 A, $V_{DD}$ = 145 V.
   21 mJ is 100% tested at $T_J$ = 25°C, L = 1 mH, $I_{AS}$ = 4.8 A, $V_{DD}$ = 145 V.

**Table 4. COMPONENTS (FOR NXV65HR82DS1 AND NXV65HR82DS2 ONLY)**

| Supplier | Part Number | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Murata (Note 3) | GCJ43QR7LV154KXJ1 | Capacitance | 135 | 150 | 165 | nF |
| | | VDC Rating | – | 630 | – | V |

3. Please refer to datasheet of the Murata capacitor

### DBC Substrate

0.63 mm $Al_2O_3$ alumina with 0.3 mm copper on both sides. DBC substrate is NOT nickel plated.

### Lead Frame

OFC copper alloy, 0.50 mm thick. Plated with 8 um to 25.4 um thick Matte Tin

### Flammability Information

All materials present in the power module meet UL flammability rating class 94V−0.

### Compliance to RoHS Directives

The power module is 100% lead free and RoHS compliant 2000/53/C directive.

### Solder

Solder used is a lead free SnAgCu alloy.

Solder presents high risk to melt at temperature beyond 210°C. Base of the leads, at the interface with the package body, should not be exposed to more than 200°C during mounting on the PCB or during welding to prevent the re−melting of the solder joints.

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**Table 5. ELECTRICAL SPECIFICATIONS** ($T_J$ = 25°C, Unless Otherwise Specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain−to−Source Breakdown Voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 V | 650 | – | – | V |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 0.97 mA | 3.0 | – | 5.0 | V |
| $R_{DS(ON)}$ | Q1 – Q4 MOSFET On Resistance | $V_{GS}$ = 10 V, $I_D$ = 20 A | – | 73 | 82 | mΩ |
| $R_{DS(ON)}$ | Q1 – Q4 MOSFET On Resistance | $V_{GS}$ = 10 V, $I_D$ = 20 A, $T_J$ = 125°C (Note 4) | – | 133 | – | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 20 V, $I_D$ = 20 A (Note 4) | – | 29 | – | S |
| $I_{GSS}$ | Gate−to−Source Leakage Current | $V_{GS}$ = ±30 V, $V_{DS}$ = 0 V | −100 | – | +100 | nA |
| $I_{DSS}$ | Drain−to−Source Leakage Current | $V_{DS}$ = 650 V, $V_{GS}$ = 0 V | – | – | 10 | μA |
| **DYNAMIC CHARACTERISTICS** (Note 4) | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 400 V<br>$V_{GS}$ = 0 V<br>f = 1 MHz | – | 3608 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 72.3 | – | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 5.56 | – | pF |
| $C_{oss(eff)}$ | Effective Output Capacitance | $V_{DS}$ = 0 to 520 V<br>$V_{GS}$ = 0 V | – | 448 | – | pF |
| $R_g$ | Gate Resistance | f = 1 MHz | – | 1.7 | – | Ω |
| $Q_{g(tot)}$ | Total Gate Charge | $V_{DS}$ = 380 V<br>$I_D$ = 20 A<br>$V_{GS}$ = 0 to 10 V | – | 79.7 | – | nC |
| $Q_{gs}$ | Gate−to−Source Gate Charge | | – | 24.9 | – | nC |
| $Q_{gd}$ | Gate−to−Drain “Miller” Charge | | – | 31.9 | – | nC |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | |
| $t_{on}$ | Turn−on Time | $V_{DS}$ = 400 V<br>$I_D$ = 20 A<br>$V_{GS}$ = 10 V<br>$R_G$ = 4.7 Ω | – | 96 | – | ns |
| $t_{d(on)}$ | Turn−on Delay Time | | – | 54 | – | ns |
| $t_r$ | Turn−on Rise Time | | – | 42 | – | ns |
| $t_{off}$ | Turn−off Time | | – | 117 | – | ns |
| $t_{d(off)}$ | Turn−off Delay Time | | – | 84 | – | ns |
| $t_f$ | Turn−off Fall Time | | – | 33 | – | ns |
| **BODY DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source−to−Drain Diode Voltage | $I_{SD}$ = 20 A, $V_{GS}$ = 0 V | – | 1.1 | – | V |
| $T_{rr}$ | Reverse Recovery Time | $V_{DS}$ = 520 V, $I_D$ = 20 A,<br>$d_I/d_t$ = 100 A/μs (Note 4) | – | 107 | – | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 430 | – | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Defined by design, not subject to production test

**Table 6. THERMAL RESISTANCE**

| Parameters | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $R_{\theta JC}$ (per chip) | Q1~Q4 Thermal Resistance Junction−to−Case (Note 5) | – | 0.7 | 0.99 | °C/W |
| $R_{\theta JS}$ (per chip) | Q1~Q4 Thermal Resistance Junction−to−Sink (Note 6) | – | 1.32 | – | °C/W |

5. Test method compliant with MIL STD 883−1012.1, from case temperature under the chip to case temperature measured below the package at the chip center, Cosmetic oxidation and discoloration on the DBC surface allowed
6. Defined by thermal simulation assuming the module is mounted on a 5 mm Al−360 die casting material with 30 um of 1.8 W/mK thermal interface material

**Table 7. ISOLATION** (Isolation resistance at tested voltage from the base plate to control pins or power terminals.)

| Test | Test Conditions | Isolation Resistance | Unit |
|---|---|---|---|
| Leakage @ Isolation Voltage (Hi−Pot) | $V_{AC}$ = 5 kV, 50 Hz | 100M < | Ω |

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## PARAMETER DEFINITIONS

Reference to Table 5: Parameter of Electrical Specifications

| | |
|---|---|
| $BV_{DSS}$ | Q1 – Q4 MOSFET Drain–to–Source Breakdown Voltage<br>The maximum drain–to–source voltage the MOSFET can endure without the avalanche breakdown of the body– drain P–N junction in off state.<br>The measurement conditions are to be found in Table 5.<br>The typ. Temperature behavior is described in Figure 13 |
| $V_{GS(th)}$ | Q1 – Q4 MOSFET Gate to Source Threshold Voltage<br>The gate–to–source voltage measurement is triggered by a threshold ID current given in conditions at Table 4.<br>The typ. Temperature behavior can be found in Figure 12 |
| $R_{DS(ON)}$ | Q1 – Q4 MOSFET On Resistance<br>$R_{DS(on)}$ is the total resistance between the source and the drain during the on state.<br>The measurement conditions are to be found in Table 5.}<br>The typ behavior can be found in Figure 10 and Figure 11 as well as Figure 17 |
| $g_{FS}$ | Q1 – Q4 MOSFET Forward Transconductance<br>Transconductance is the gain in the MOSFET, expressed in the Equation below.<br>It describes the change in drain current by the change in the gate–source bias voltage: $g_{fs} = [ -\Delta I_{DS} / \Delta V_{GS} ]_{VDS}$ |
| $I_{GSS}$ | Q1 – Q4 MOSFET Gate–to–Source Leakage Current<br>The current flowing from Gate to Source at the maximum allowed $V_{GS}$<br>The measurement conditions are described in the Table 5. |
| $I_{DSS}$ | Q1 – Q4 MOSFET Drain–to–Source Leakage Current<br>Drain – Source current is measured in off state while providing the maximum allowed drain–to-source voltage and the gate is shorted to the source.<br>$I_{DSS}$ has a positive temperature coefficient. |

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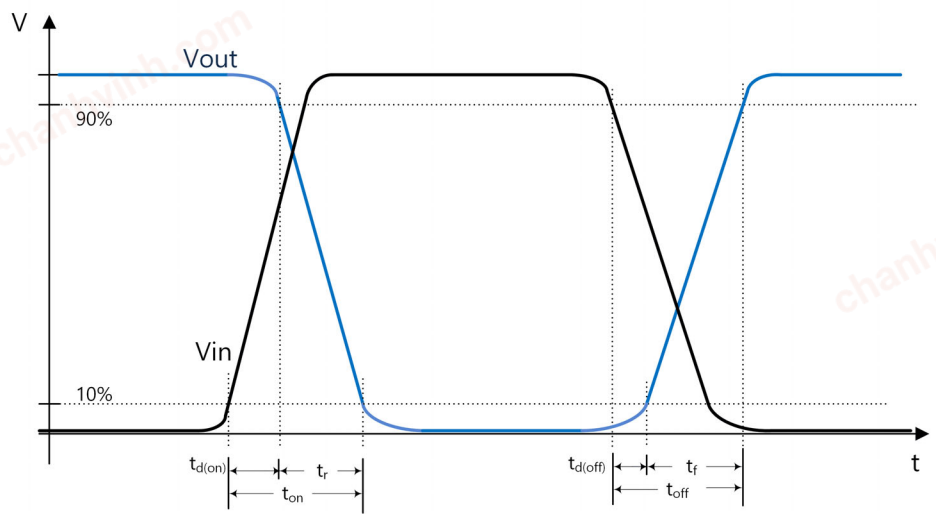



**Figure 3. Timing Measurement Variable Definition**

**Table 8. PARAMETER OF SWITCHING CHARACTERISTICS**

| | |
|---|---|
| Turn−On Delay ($t_{d(on)}$): | This is the time needed to charge the input capacitance, Ciss, before the load current ID starts flowing.<br>The measurement conditions are described in the Table 5.<br>For signal definition please check Figure 3 above. |
| Rise Time ($t_r$): | The rise time is the time to discharge output capacitance, Coss.<br>After that time the MOSFET conducts the given load current ID.<br>The measurement conditions are described in the Table 5.<br>For signal definition please check Figure 3 above. |
| Turn−On Time ($t_{on}$): | Is the sum of turn−on−delay and rise time |
| Turn−Off Delay ($t_{d(off)}$): | td(off) is the time to discharge Ciss after the MOSFET is turned off.<br>During this time the load current ID is still flowing<br>The measurement conditions are described in the Table 5.<br>For signal definition please check Figure 3 above. |
| Fall Time ($t_f$): | The fall time, tf, is the time to charge the output capacitance, Coss.<br>During this time the load current drops down and the voltage VDS rises accordingly.<br>The measurement conditions are described in the Table 5.<br>For signal definition please check Figure 3 above. |
| Turn−Off Time ($t_{off}$): | Is the sum of turn−off−delay and fall time |

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## TYPICAL CHARACTERISTICS

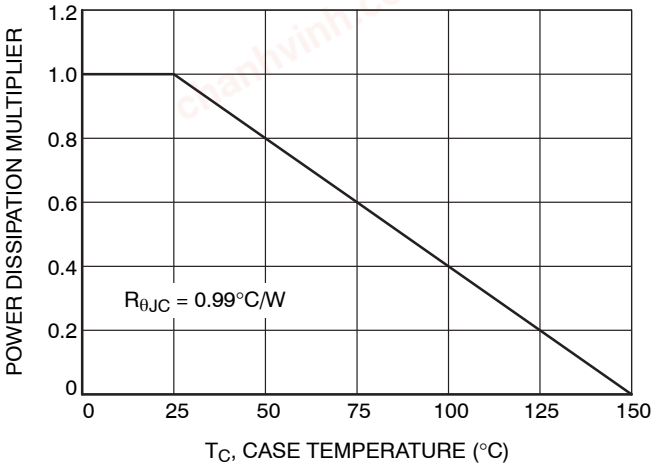



**Figure 4. Normalized Power Dissipation vs. Case Temperature**

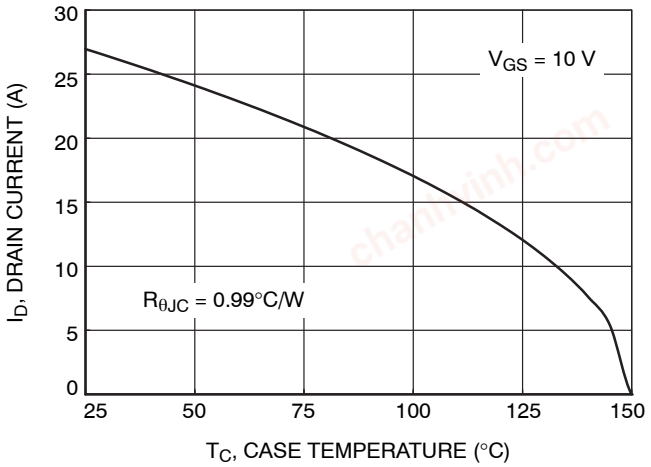



**Figure 5. Maximum Continuous $I_D$ vs. Case Temperature**

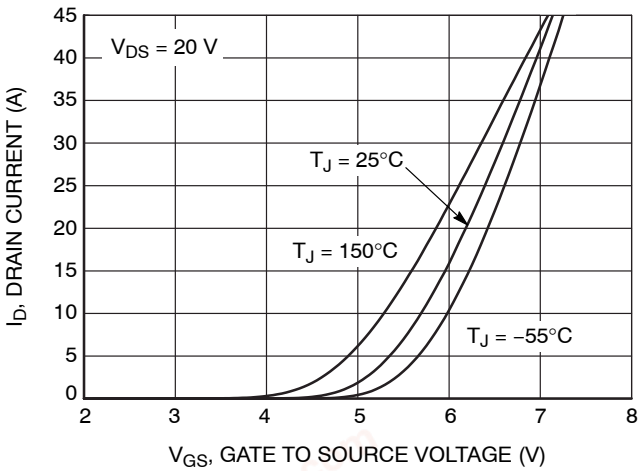



**Figure 6. Transfer Characteristics**

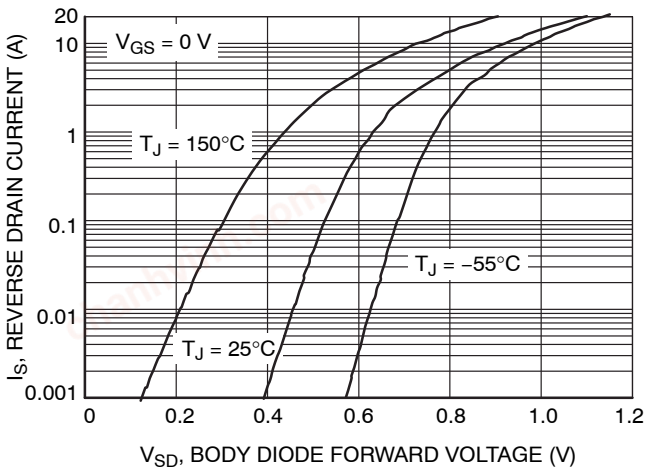



**Figure 7. Forward Diode**

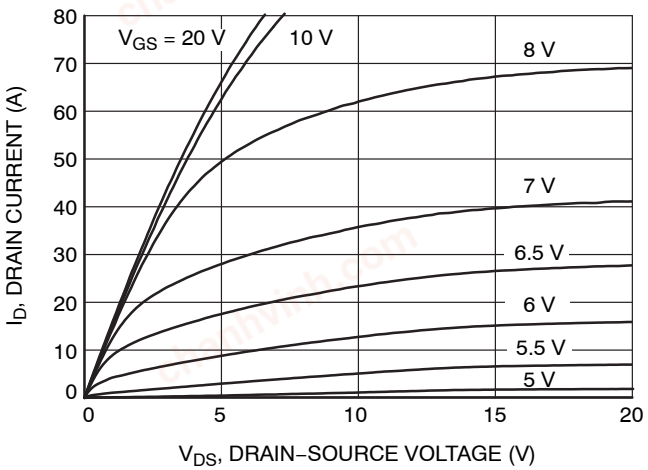



**Figure 8. Saturation (25°C)**

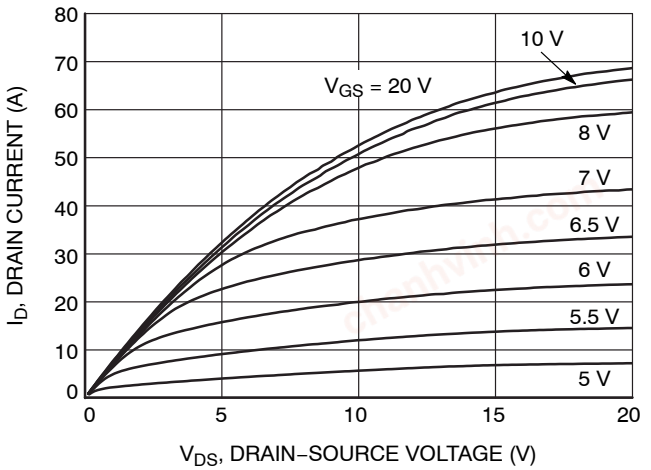



**Figure 9. Saturation (150°C)**

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## TYPICAL CHARACTERISTICS (continued)

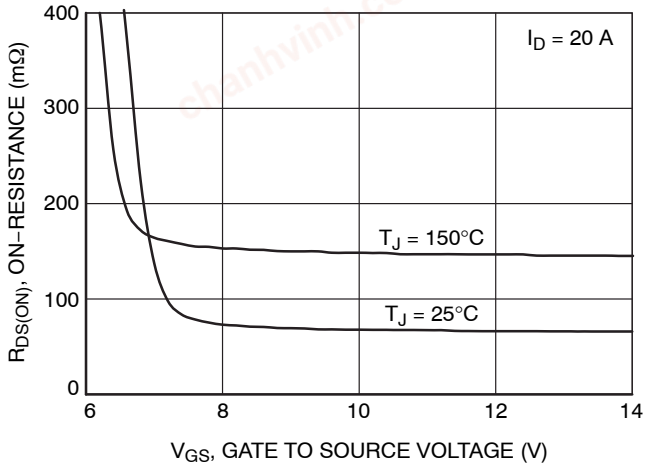



**Figure 10. On−Resistance vs. Gate−to−Source Voltage**

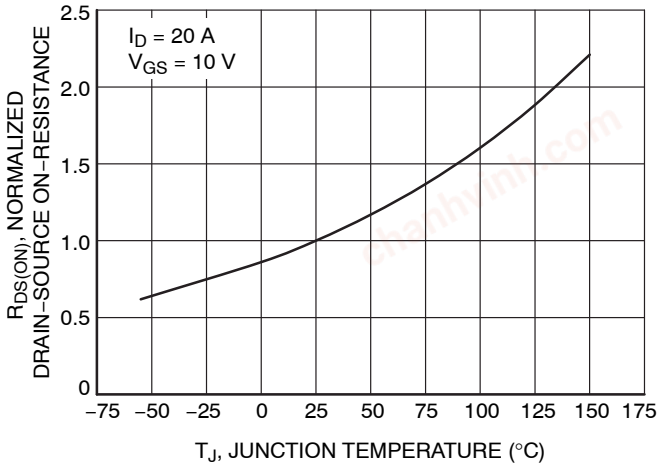



**Figure 11. $R_{DS(norm)}$ vs. Junction Temperature**

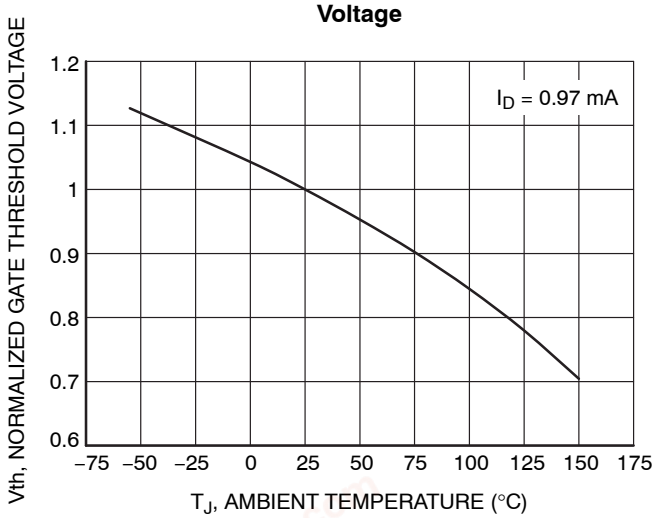



**Figure 12. Normalized $V_{th}$ vs. Temperature**

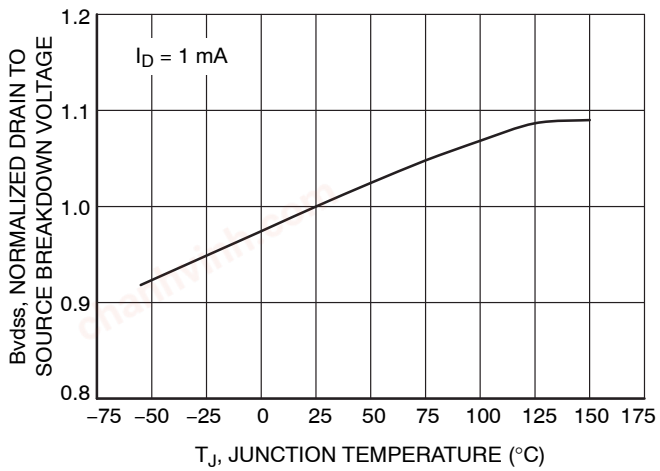



**Figure 13. Breakdown Voltage vs. Temperature**

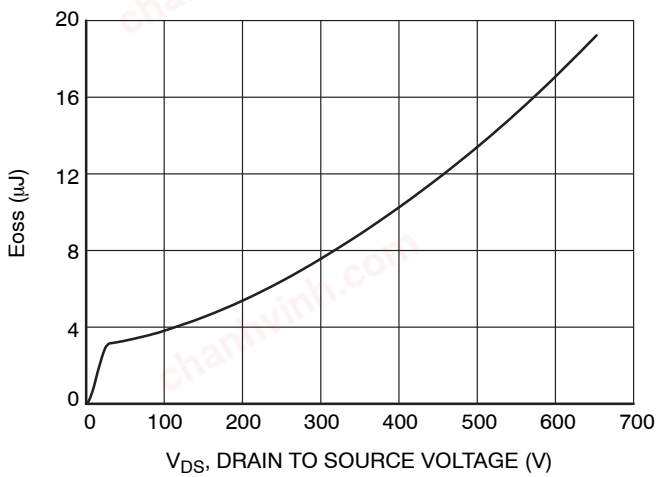



**Figure 14. Eoss vs. Drain−to−Source Voltage**

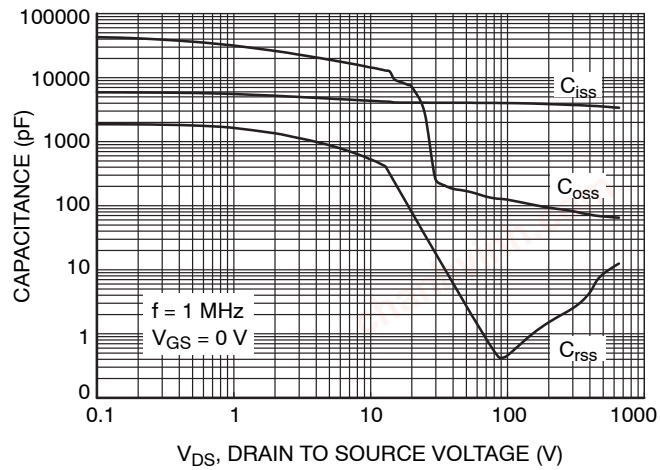



**Figure 15. Capacitance Variation**

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## TYPICAL CHARACTERISTICS (continued)

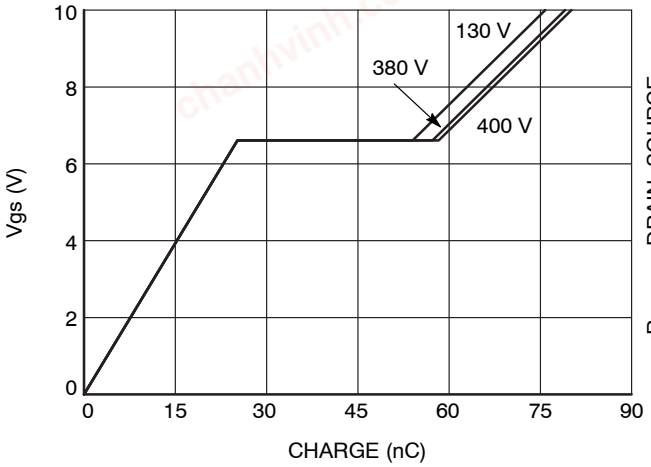



Figure 16. Gate Charge

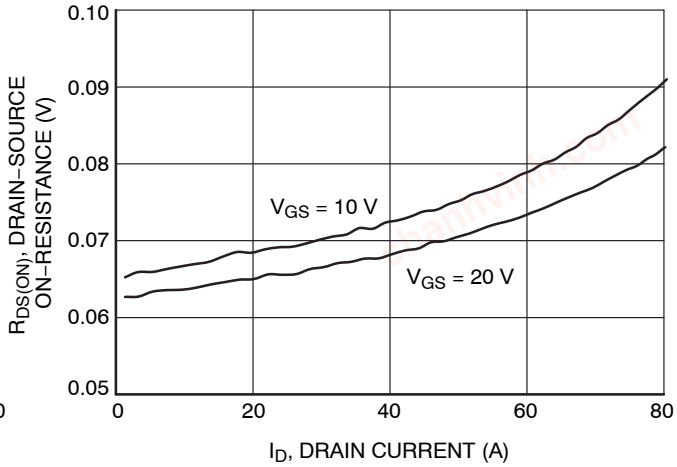



Figure 17. $R_{DS(ON)}$ vs. $I_D$

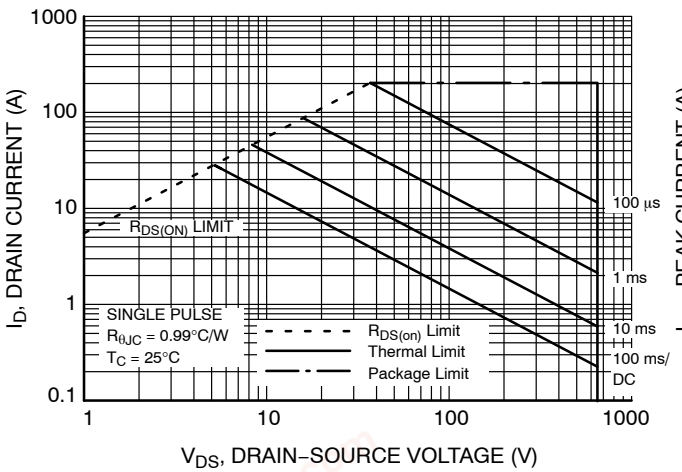



Figure 18. Safe Operating Area

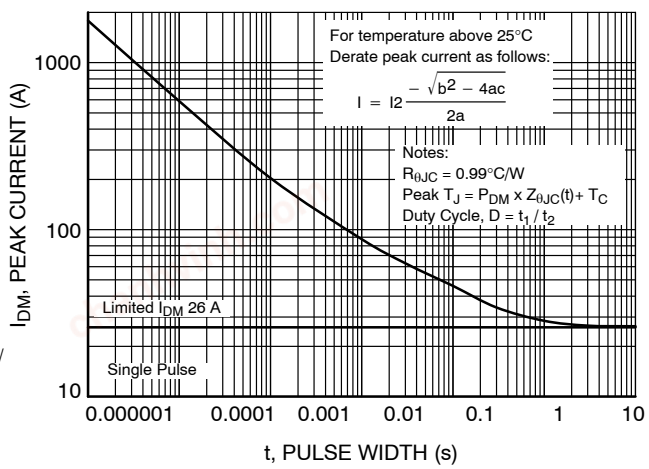



Figure 19. Peak Current Capability

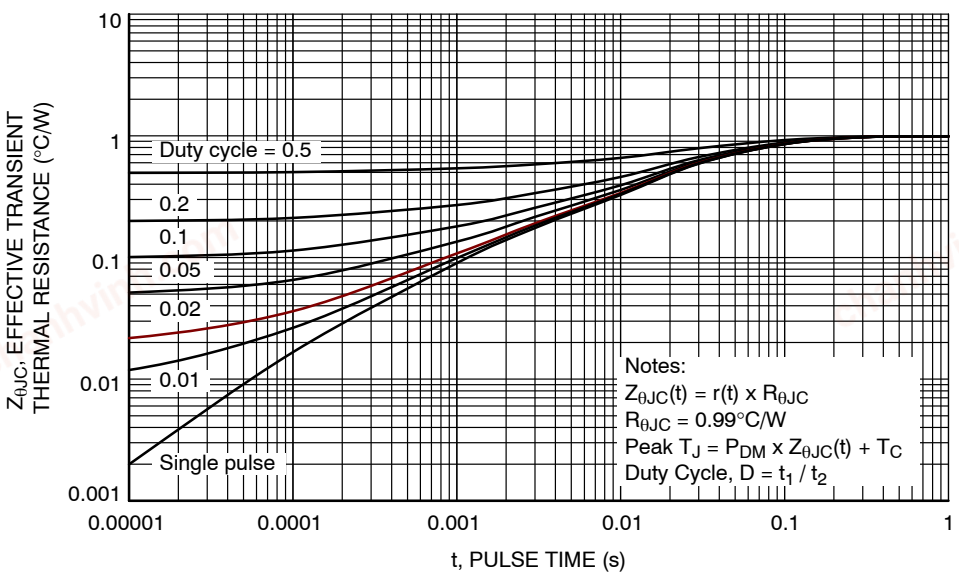



Figure 20. Transient Thermal Impedance

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## ORDERING INFORMATION

| Part Number | Package | Lead Forming | Snubber Capacitor Inside | DBC Material | Pb−Free and RoHS Compliant | Operating Temperature ($T_A$) | Packing Method |
|---|---|---|---|---|---|---|---|
| NXV65HR82DS1 | APM16−CAA | Y−Shape | Yes | $Al_2O_3$ | Yes | −40°C~125°C | Tube |
| NXV65HR82DS2 | APM16−CAB | L−Shape | Yes | $Al_2O_3$ | Yes | −40°C~125°C | Tube |
| NXV65HR82DZ1 | APM16−CAA | Y−Shape | No | $Al_2O_3$ | Yes | −40°C~125°C | Tube |
| NXV65HR82DZ2 | APM16−CAB | L−Shape | No | $Al_2O_3$ | Yes | −40°C~125°C | Tube |

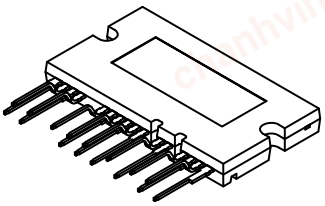
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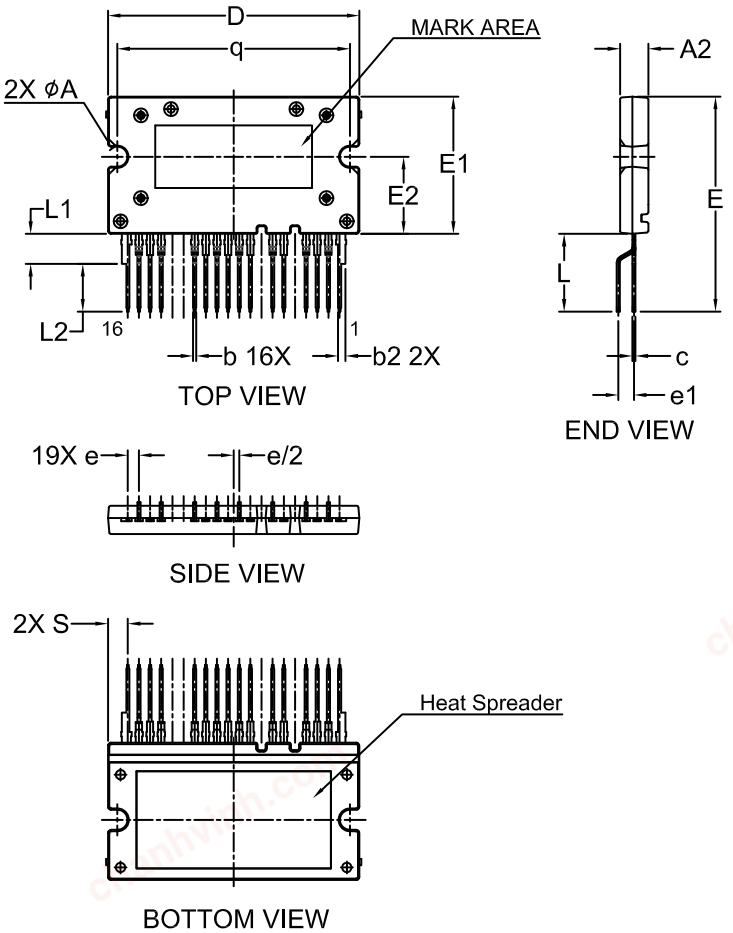
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

**APMCA−A16 / 16LD, AUTOMOTIVE MODULE**
CASE MODGF
ISSUE B

DATE 08 OCT 2020






NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A2 | 4.30 | 4.50 | 4.70 |
| b | 0.45 | 0.50 | 0.60 |
| b2 | 1.15 | 1.20 | 1.30 |
| c | 0.45 | 0.50 | 0.60 |
| D | 39.90 | 40.10 | 40.30 |
| E | 33.80 | 34.30 | 34.80 |
| E1 | 21.70 | 21.90 | 22.10 |
| E2 | 12.10 | 12.30 | 12.50 |
| e | 1.478 | 1.778 | 2.078 |
| e1 | 2.20 | 2.50 | 2.80 |
| L | 12.10 | 12.40 | 12.70 |
| L1 | 4.80 REF | | |
| L2 | 7.30 | 7.60 | 7.90 |
| q | 36.85 | 37.10 | 37.35 |
| S | 3.159 REF | | |
| ϕA | 2.95 | 3.20 | 3.45 |

### GENERIC MARKING DIAGRAM*

XXXXXXXXXXXXXXXX
ZZZ ATYWW
NNNNNNN

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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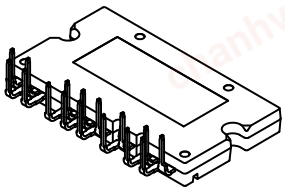
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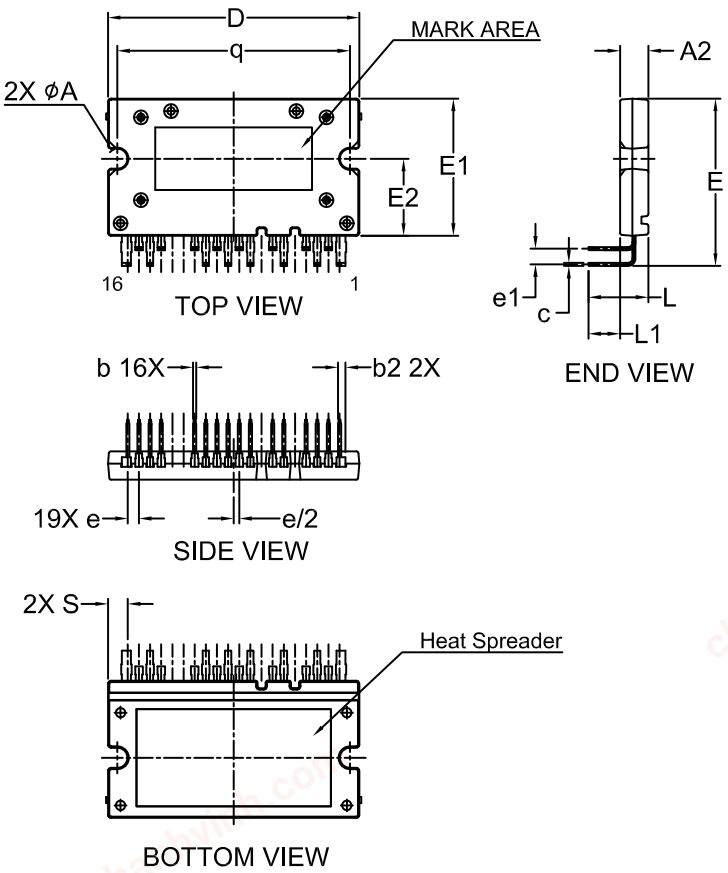
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

**APMCA−B16 / 16LD, AUTOMOTIVE MODULE**
CASE MODGJ
ISSUE B

DATE 03 NOV 2020






NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A2 | 4.30 | 4.50 | 4.70 |
| b | 0.45 | 0.50 | 0.60 |
| b2 | 1.15 | 1.20 | 1.30 |
| c | 0.45 | 0.50 | 0.60 |
| D | 39.90 | 40.10 | 40.30 |
| E | 26.20 | 26.70 | 27.20 |
| E1 | 21.70 | 21.90 | 22.10 |
| E2 | 12.10 | 12.30 | 12.50 |
| e | 1.478 | 1.778 | 2.078 |
| e1 | 2.20 | 2.50 | 2.80 |
| L | 9.20 | 9.55 | 9.90 |
| L1 | 5.05 REF | | |
| q | 36.85 | 37.10 | 37.35 |
| S | 3.159 REF | | |
| ϕA | 2.95 | 3.20 | 3.45 |

**GENERIC MARKING DIAGRAM***

XXXXXXXXXXXXXXXX
ZZZ ATYWW
NNNNNNN

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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