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DATA SHEET
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Silicon Carbide (SiC) Module – EliteSiC, 7 mohm, 1200 V, SiC M3S MOSFET, Full Bridge, F2 Package

Product Preview

NXH007F120M3F2PTHG

The NXH007F120M3F2PTHG is a power module containing 7 mΩ / 1200 V SiC MOSFET full−bridge and a thermistor with HPS DBC in an F2 package.

Features

- 7 mΩ / 1200 V M3S SiC MOSFET Full−Bridge
- HPS DBC
- Thermistor
- Options with Pre−Applied Thermal Interface Material (TIM) and without Pre−Applied TIM
- Press−Fit Pins
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

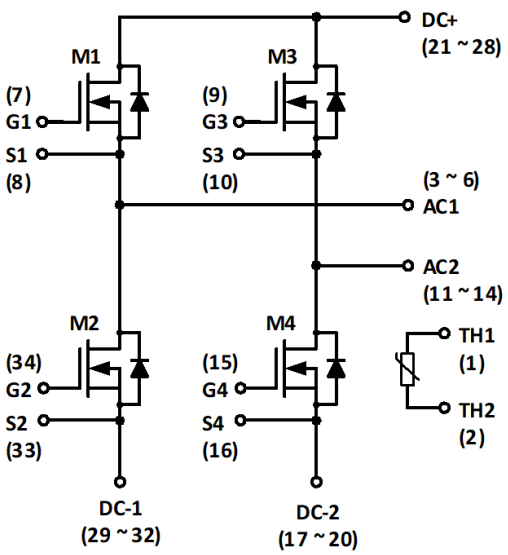
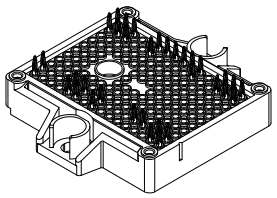


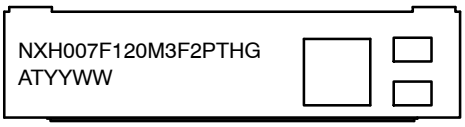
Figure 1. NXH007F120M3F2PTHG Schematic Diagram

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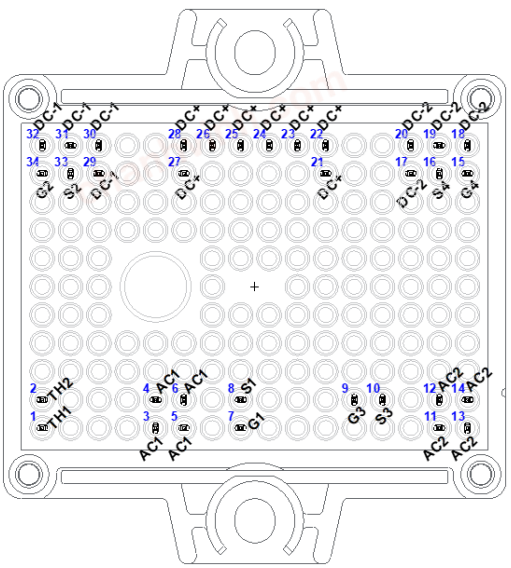
PIM34 56.7x42.5 (PRESS FIT)
CASE 180HU

MARKING DIAGRAM



NXH007F120M3F2PTHG	= Specific Device Code
AT	= Assembly & Test Site Code
YWW	= Year and Work Week Code

PIN CONNECTIONS



See Pin Function Description for pin names

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	TH1	Thermistor Connection 1
2	TH2	Thermistor Connection 2
3	AC1	Center point of full bridge 1
4	AC1	Center point of full bridge 1
5	AC1	Center point of full bridge 1
6	AC1	Center point of full bridge 1
7	G1	M1 Gate (High side switch)
8	S1	M1 Kelvin Source (High side switch)
9	G3	M3 Gate (High side switch)
10	S3	M3 Kelvin Source (High side switch)
11	AC2	Center point of full bridge 2
12	AC2	Center point of full bridge 2
13	AC2	Center point of full bridge 2
14	AC2	Center point of full bridge 2
15	G4	M4 Gate (Low side switch)
16	S4	M4 Kelvin Source (Low side switch)
17	DC−2	DC Negative Bus connection
18	DC−2	DC Negative Bus connection
19	DC−2	DC Negative Bus connection
20	DC−2	DC Negative Bus connection
21	DC+	DC Positive Bus connection
22	DC+	DC Positive Bus connection
23	DC+	DC Positive Bus connection
24	DC+	DC Positive Bus connection
25	DC+	DC Positive Bus connection
26	DC+	DC Positive Bus connection
27	DC+	DC Positive Bus connection
28	DC+	DC Positive Bus connection
29	DC−1	DC Negative Bus connection
30	DC−1	DC Negative Bus connection
31	DC−1	DC Negative Bus connection
32	DC−1	DC Negative Bus connection
33	S2	M2 Kelvin Source (Low side switch)
34	G2	M2 Gate (Low side switch)

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
SiC MOSFET			
Drain−Source Voltage	V_{DSS}	1200	V
Gate−Source Voltage	V_{GS}	+22/−10	V
Continuous Drain Current @ T_c = 80°C (T_J = 175°C)	I_D	149	A
Pulsed Drain Current (T_J = 175°C) (Note 2)	I_{Dpulse}	447	A
Maximum Power Dissipation (T_J = 175°C)	P_{tot}	353	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C
THERMAL PROPERTIES			
Storage Temperature Range	T_{stg}	−40 to 150	°C
INSULATION PROPERTIES			
Isolation Test Voltage, t = 1 s, 60 Hz	V_{is}	4800	V_{RMS}
Creepage Distance		12.7	mm
CTI		600	
Substrate Ceramic Material		HPS	
Substrate Ceramic Material Thickness		0.38	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. Height difference between horizontal plane and substrate copper bottom.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 1200 V, T_J = 25°C	I_{DSS}	–	–	300	μA
Drain−Source On Resistance	V_{GS} = 18 V, I_D = 120 A, T_J = 25°C	$R_{DS(ON)}$	–	7.5	10	mΩ
	V_{GS} = 18 V, I_D = 120 A, T_J = 125°C		–	12.1	–	
	V_{GS} = 18 V, I_D = 120 A, T_J = 150°C		–	13.6	–	
	V_{GS} = 18 V, I_D = 120 A, T_J = 175°C		–	15.9	–	
Gate−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 60 mA	$V_{GS(TH)}$	2.04	2.72	4.4	V
Recommended Gate Voltage		V_{GOP}	−3	–	+18	V
Gate Leakage Current	V_{GS} = −10 V / 22 V, V_{DS} = 0 V	I_{GSS}	–	–	±3	μA
Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 800 V	C_{ISS}	–	9090	–	pF
Reverse Transfer Capacitance		C_{RSS}	–	37	–	
Output Capacitance		C_{OSS}	–	484	–	

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Total Gate Charge	V_{GS} = −3/18 V, V_{DS} = 800 V, I_D = 40 A	$Q_{G(TOTAL)}$	–	407	–	nC
Gate−Source Charge		Q_{GS}	–	42	–	
Gate−Drain Charge		Q_{GD}	–	93	–	
Internal Gate Resistance	f = 1 MHz	R_{GINT}	–	0.5	–	Ω
Turn−on Delay Time	T_J = 25°C V_{DS}= 800 V, I_D = 120 A V_{GS} = −3/18 V, R_G = 2 Ω	$t_{d(on)}$	–	37.2	–	ns
Rise Time		t_r	–	12	–	
Turn−off Delay Time		$t_{d(off)}$	–	121.6	–	
Fall Time		t_f	–	13.2	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	1.69	–	mJ
Turn−off Switching Loss per Pulse		E_{OFF}	–	0.5	–	
Turn−on Delay Time	T_J = 150°C V_{DS}= 800 V, I_D = 120 A V_{GS} = −3/18 V, R_G = 2 Ω	$t_{d(on)}$	–	34.8	–	ns
Rise Time		t_r	–	14	–	
Turn−off Delay Time		$t_{d(off)}$	–	131.6	–	
Fall Time		t_f	–	14	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	2.23	–	mJ
Turn off Switching Loss per Pulse		E_{OFF}	–	0.6	–	
Diode Forward Voltage	I_{SD} = 120 A, T_J = 25°C, V_{GS} = −3 V	V_{SD}	–	5.03	6	V
	I_{SD} = 120 A, T_J = 125°C, V_{GS} = −3 V		–	4.81	–	
	I_{SD} = 120 A, T_J = 150°C, V_{GS} = −3 V		–	4.73	–	
Thermal Resistance − Chip−to−Case	M1, M2, M3, M4	R_{thJC}	–	0.269	–	°C/W
Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, A = 2.8 W/mK	R_{thJH}	–	0.462	–	°C/W
THERMISTOR CHARACTERISTICS						
Nominal Resistance	T = 25°C	R_{25}	–	5	–	kΩ
	T = 100°C	R_{100}	–	493	–	Ω
	T = 150°C	R_{150}	–	159.5	–	Ω
Deviation of R_{100}	T = 100°C	ΔR/R	−5	–	5	%
Power Dissipation − Recommended Limit	0.15 mA, Non−self−heating Effect	P_D	–	0.1	–	mW
Power Dissipation − Absolute Maximum	5 mA	P_D	–	34.2	–	mW
Power Dissipation Constant			–	1.4	–	mW/K
B−value	B(25/50), tolerance ±2%		–	3375	–	K
B−value	B(25/100), tolerance ±2%		–	3436	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH007F120M3F2PTHG	NXH007F120M3F2PTHG	F2FULLBR: Case 180HU Press−fit Pins with pre−applied thermal interface material (TIM) (Pb−Free / Halide Free)	20 Units / Blister Tray

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TYPICAL CHARACTERISTIC (M1/M2 SiC MOSFET CHARACTERISTIC)

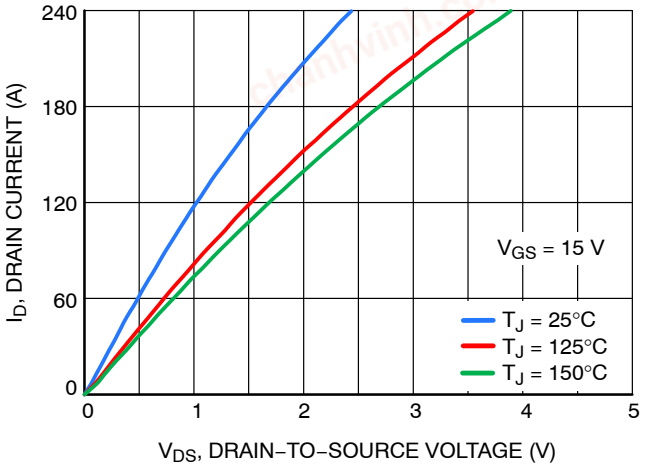


Figure 2. MOSFET Typical Output Characteristic V_{GS} = 15 V

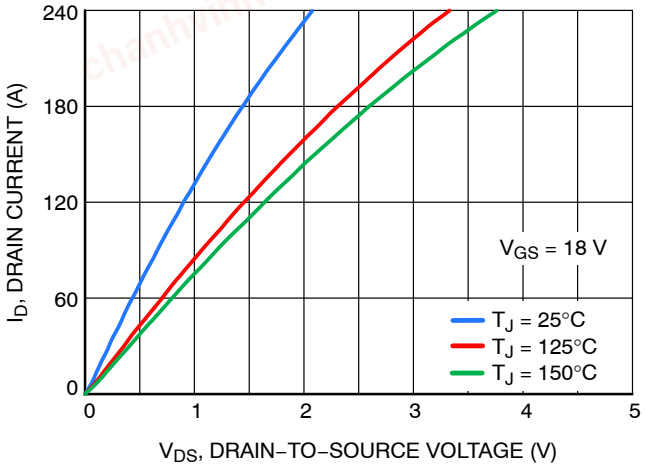


Figure 3. MOSFET Typical Output Characteristic V_{GS} = 18 V

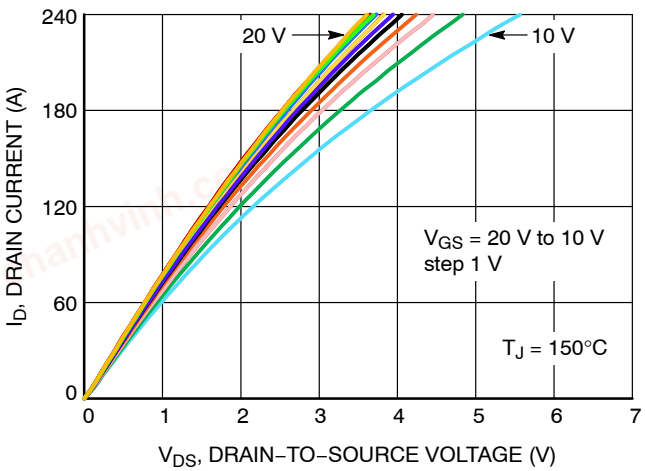


Figure 4. MOSFET Typical Output Characteristic V_{GS} = var.

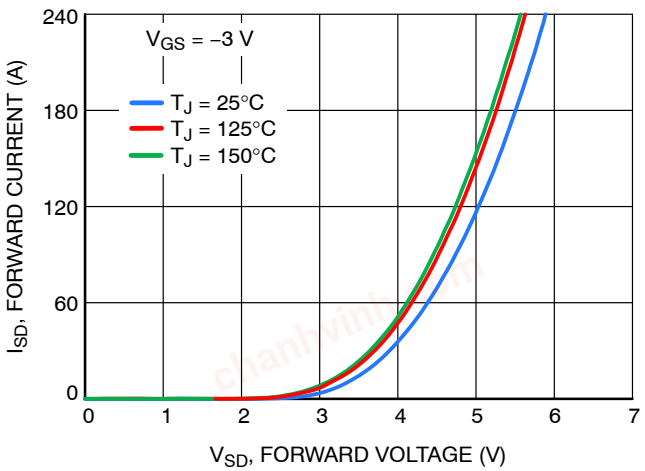


Figure 5. Body Diode Forward Characteristic

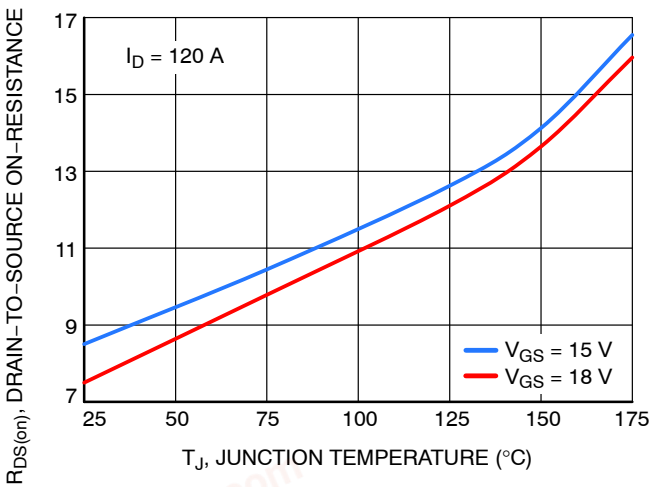


Figure 6. RDS(ON) Drain−to−Source ON Resistance vs. Junction Temperature

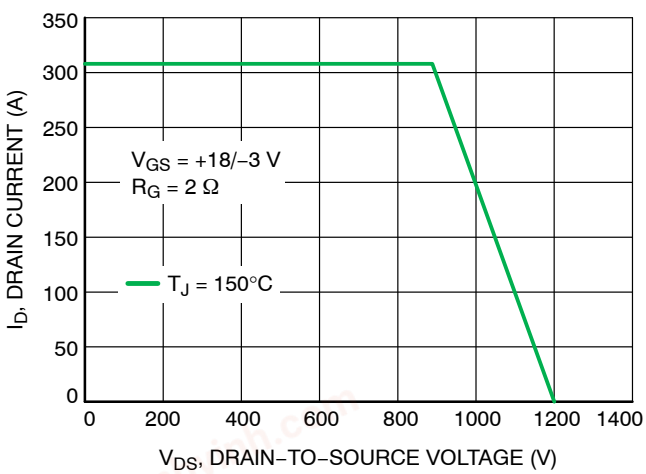


Figure 7. Reverse Bias Safe Operating Area (RBSOA)

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TYPICAL CHARACTERISTIC (M1/M2 SiC MOSFET CHARACTERISTIC)

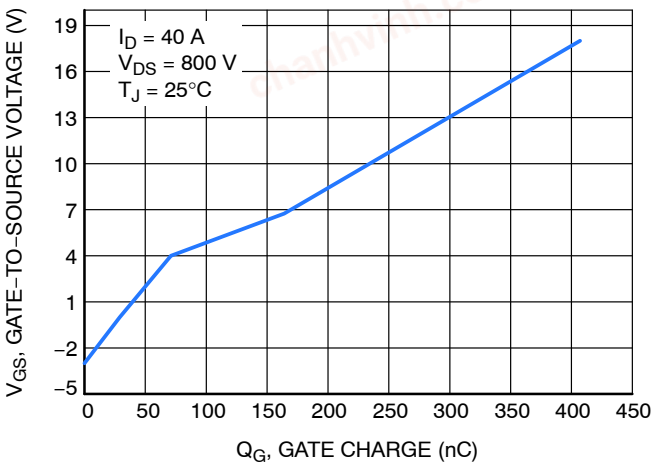


Figure 8. Gate−to−Source Voltage vs. Gate Charge

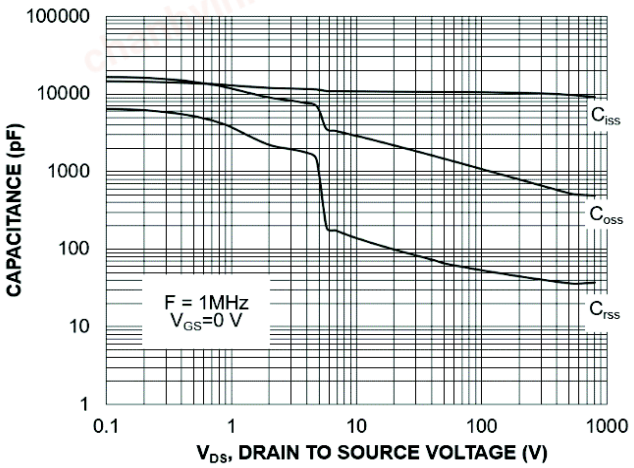


Figure 9. Capacitance vs. Voltage Drain−to−Source

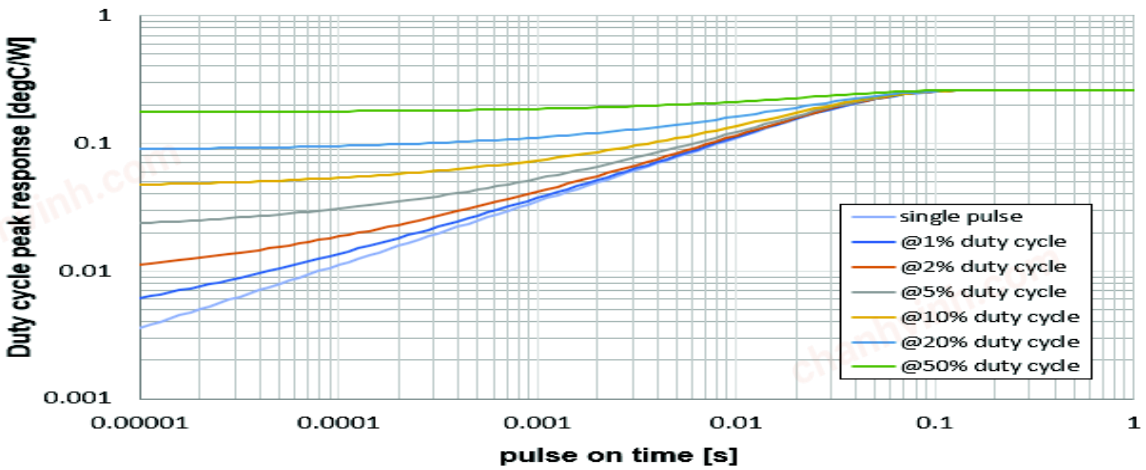


Figure 10. Duty Cycle Response vs. Pulse On Time

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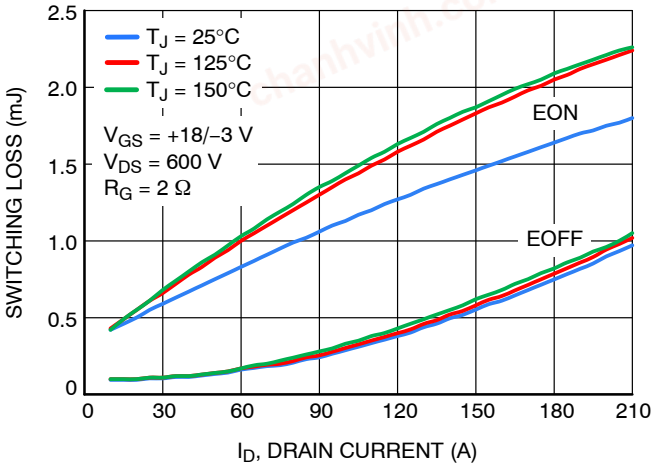


Figure 11. Switching Loss vs. Drain Current V_{DS} = 600 V

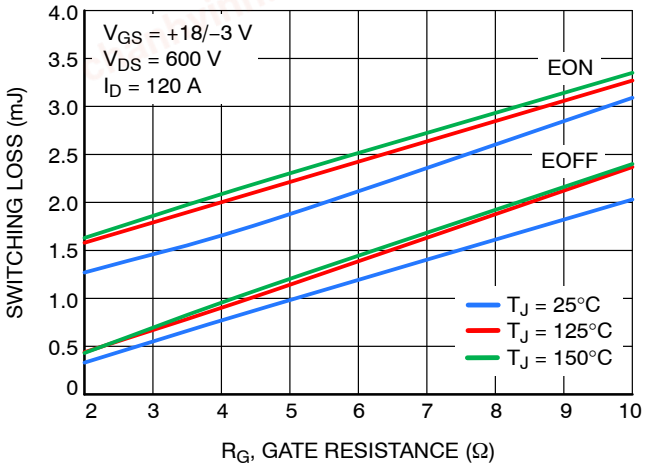


Figure 12. Switching Loss vs. Gate Resistance V_{DS} = 600 V

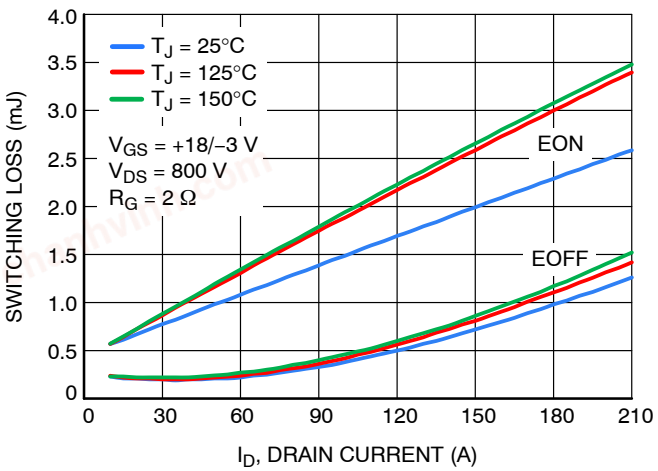


Figure 13. Switching Loss vs. Drain Current V_{DS} = 800 V

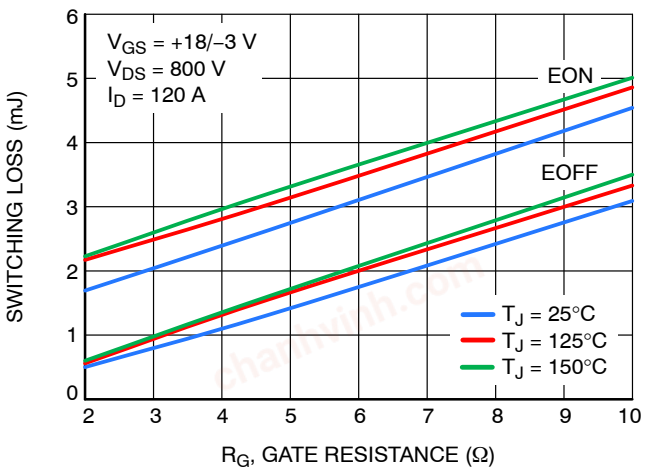


Figure 14. Switching Loss vs. Gate Resistance V_{DS} = 800 V

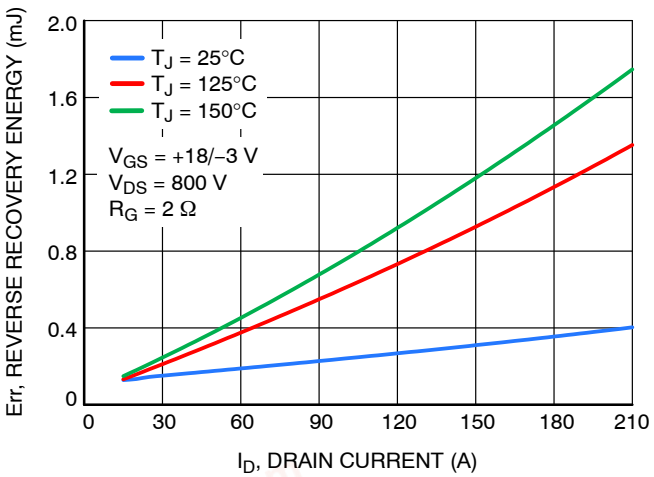


Figure 15. Reverse Recovery Energy vs. Drain Current V_{DS} = 800 V

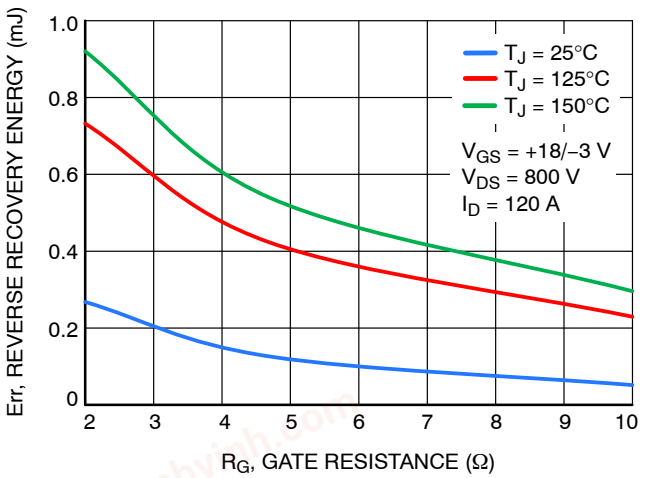


Figure 16. Reverse Recovery Energy vs. Gate Resistance V_{DS} = 800 V

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TYPICAL CHARACTERISTIC (M1/M2 SiC MOSFET CHARACTERISTIC)

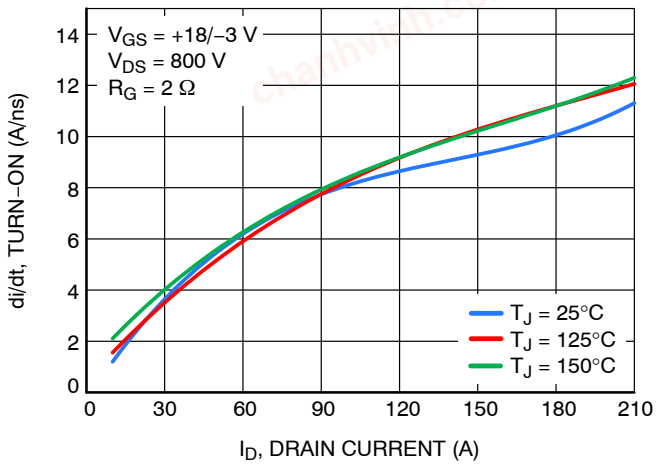


Figure 17. di/dt Turn ON vs. Drain Current V_{DS} = 800 V

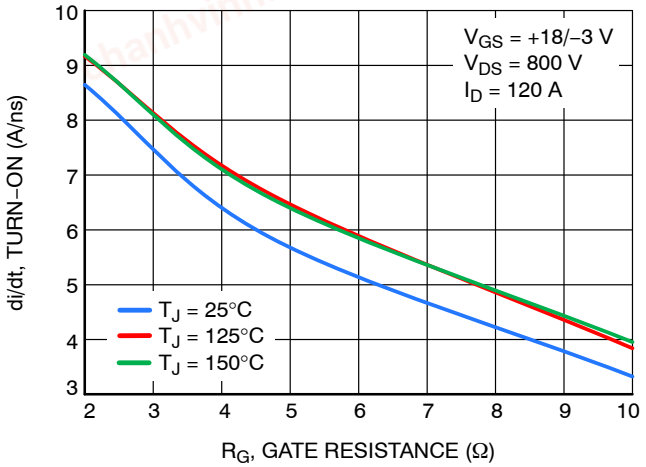


Figure 18. di/dt Turn ON vs. Gate Resistance V_{DS} = 800 V

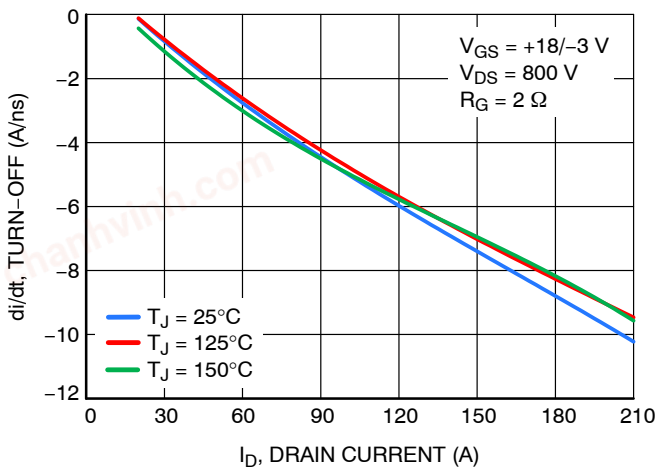


Figure 19. di/dt Turn OFF vs. Drain Current V_{DS} = 800 V

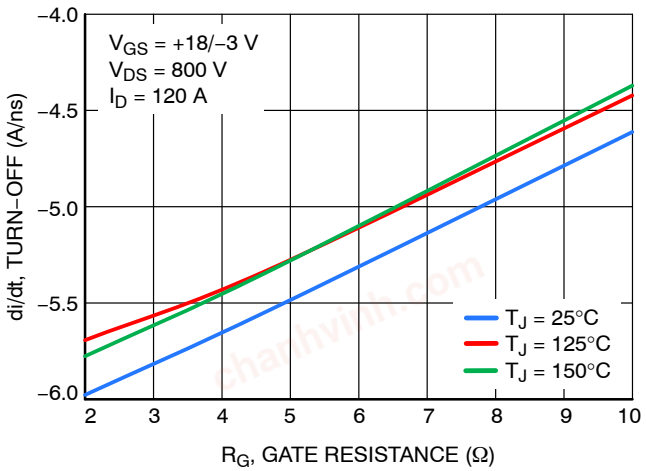


Figure 20. di/dt Turn OFF vs. Gate Resistance V_{DS} = 800 V

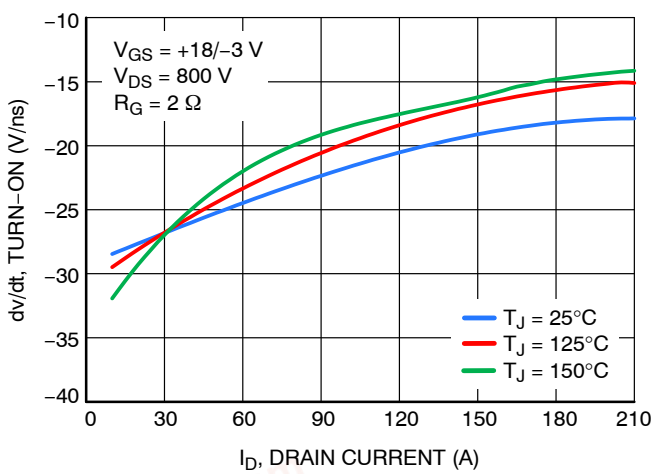


Figure 21. dv/dt Turn ON vs. Drain Current V_{DS} = 800 V

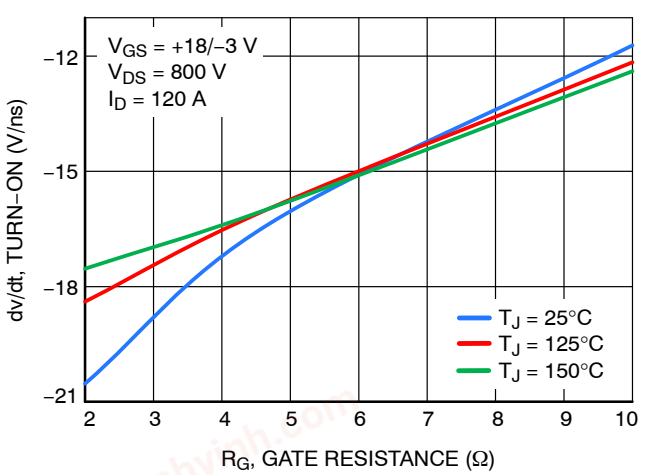


Figure 22. dv/dt Turn ON vs. Gate Resistance V_{DS} = 800 V

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TYPICAL CHARACTERISTIC (M1/M2 SiC MOSFET CHARACTERISTIC)

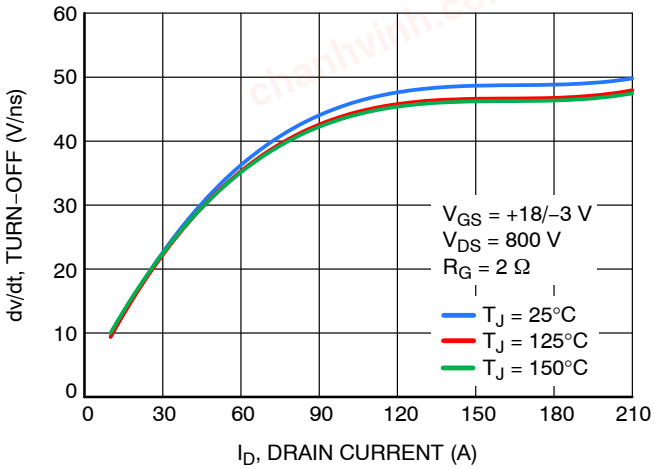


Figure 23. dv/dt Turn OFF vs. Drain Current V_{DS} = 800 V

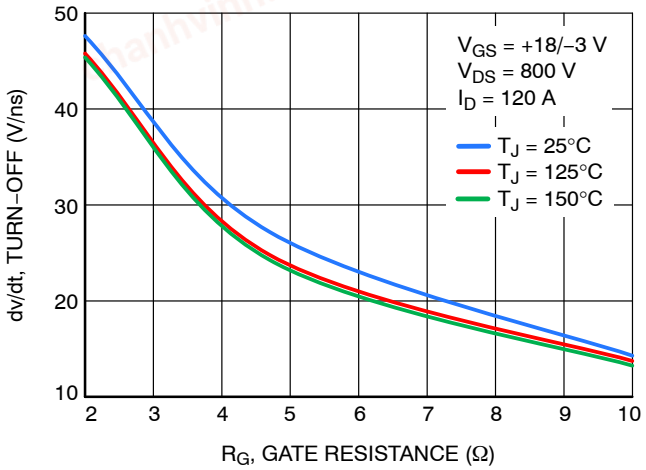


Figure 24. dv/dt Turn OFF vs. Gate Resistance V_{DS} = 800 V

Table 1. CAUER NETWORKS

Cauer Element #	Rth (K/W)	Cth (Ws/K)
1	0.0197	0.0062
2	0.0360	0.0335
3	0.0915	0.0468
4	0.1151	0.1685
5	0.0162	0.1198

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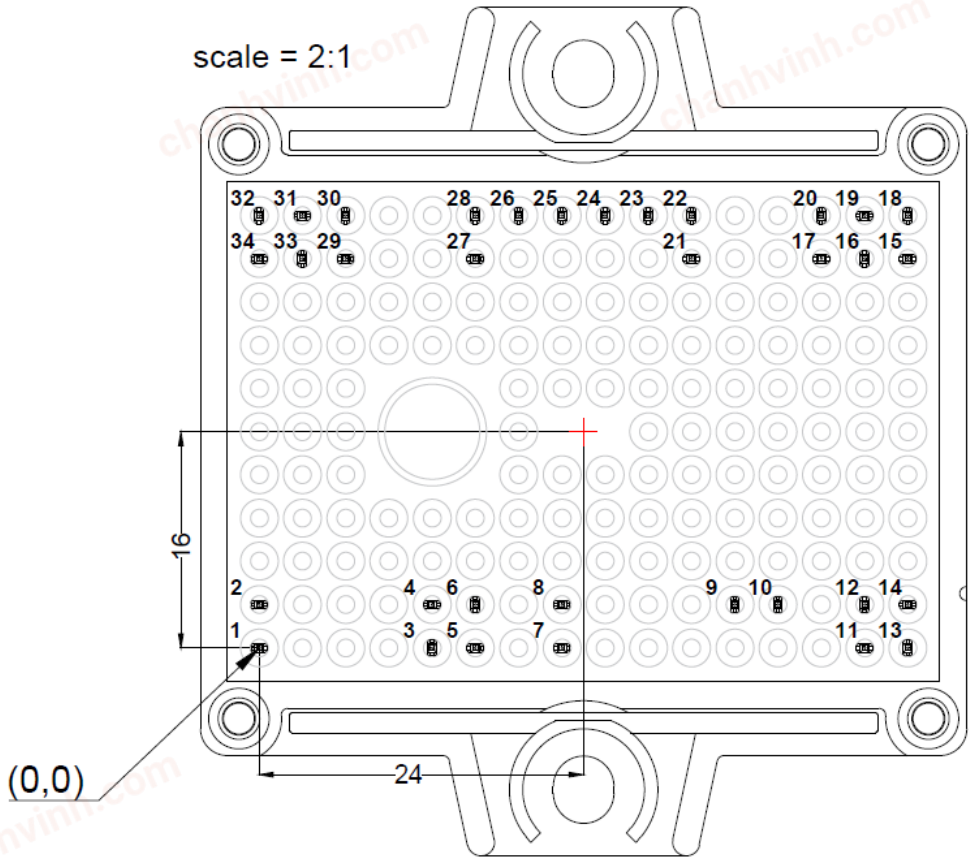


Figure 25.

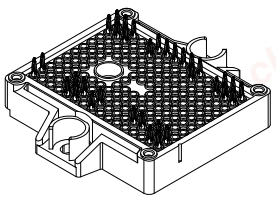
Pin position

Pin #	X	Y	Function	Pin #	X	Y	Function
1	0	0	TH1	18	48	32	DC-2
2	0	3.2	TH2	19	44.8	32	DC-2
3	12.8	0	AC1	20	41.6	32	DC-2
4	12.8	3.2	AC1	21	32	28.8	DC+
5	16	0	AC1	22	32	32	DC+
6	16	3.2	AC1	23	28.8	32	DC+
7	22.4	0	G1	24	25.6	32	DC+
8	22.4	3.2	S1	25	22.4	32	DC+
9	35.2	3.2	G3	26	19.2	32	DC+
10	38.4	3.2	S3	27	16	28.8	DC+
11	44.8	0	AC2	28	16	32	DC+
12	44.8	3.2	AC2	29	6.4	28.8	DC-1
13	48	0	AC2	30	6.4	32	DC-1
14	48	3.2	AC2	31	3.2	32	DC-1
15	48	28.8	G4	32	0	32	DC-1
16	44.8	28.8	S4	33	3.2	28.8	S2
17	41.6	28.8	DC-2	34	0	28.8	G2

Figure 26.

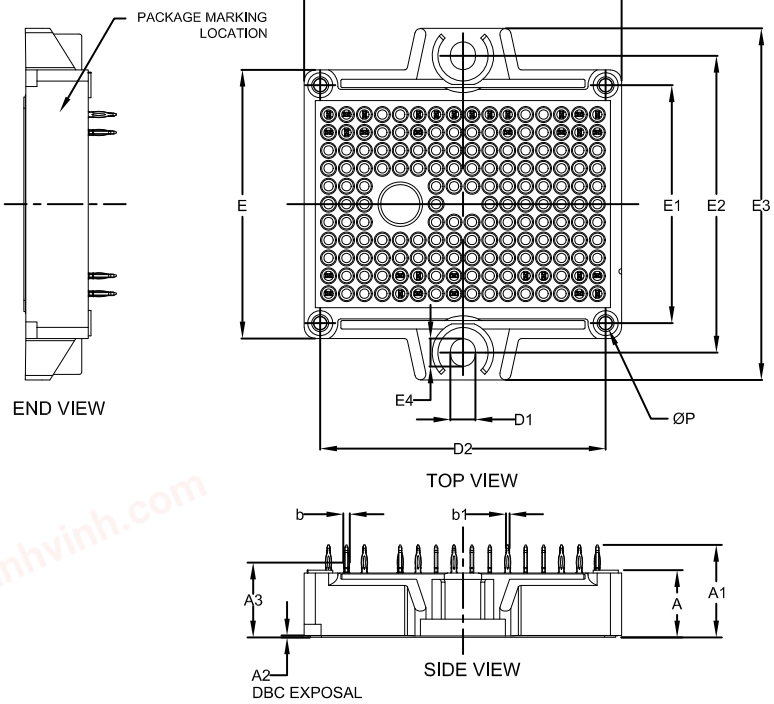
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



PIM34 56.70x42.50x12.00
CASE 180HU
ISSUE A

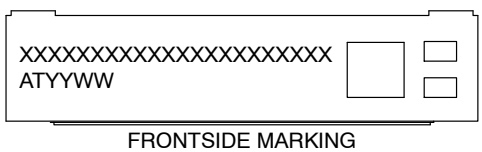
DATE 07 FEB 2024



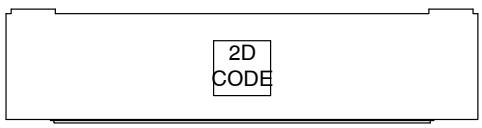
NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS ± 0.4mm
3. PRESS FIT PIN

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.10	16.50	16.90
A2	0.00	0.35	0.60
A3	12.85	13.35	13.85
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	56.40	56.70	57.00
D1	4.40	4.50	4.60
D2	50.85	51.00	51.15
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40

GENERIC MARKING DIAGRAM*



FRONTSIDE MARKING



BACKSIDE MARKING

XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**PIM34 56.70x42.50x12.00**		**PAGE 1 OF 2**

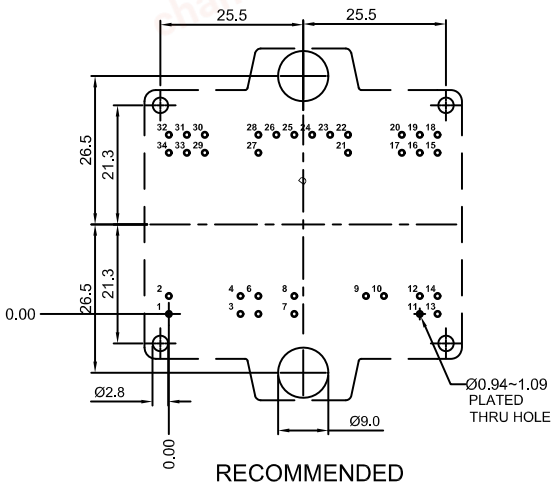
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PIM34 56.70x42.50x11.50
CASE 180HU
ISSUE A

DATE 07 FEB 2024



RECOMMENDED
MOUNTING PATTERN

* For additional Information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Note2:

Pin	X	Y	Pin	X	Y
1	0	0	18	48	32
2	0	3.2	19	44.8	32
3	12.8	0	20	41.6	32
4	12.8	3.2	21	32	28.8
5	16	0	22	32	32
6	16	3.2	23	28.8	32
7	22.4	0	24	25.6	32
8	22.4	3.2	25	22.4	32
9	35.2	3.2	26	19.2	32
10	38.4	3.2	27	16	28.8
11	44.8	0	28	16	32
12	44.8	3.2	29	6.4	28.8
13	48	0	30	6.4	32
14	48	3.2	31	3.2	32
15	48	28.8	32	0	32
16	44.8	28.8	33	3.2	28.8
17	41.6	28.8	34	0	28.8

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