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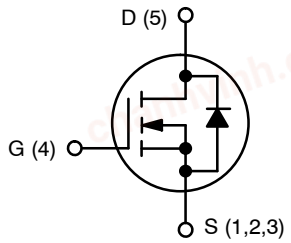
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DATA SHEET
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MOSFET – Power, Single N-Channel, STD Gate, SO8FL
80 V, 3.5 mΩ, 119 A

NTMFS4D0N08X

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	3.5 mΩ @ 10 V	119 A

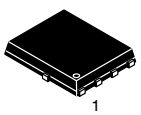


N–CHANNEL MOSFET

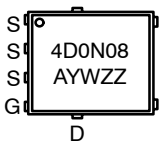
Features
- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- Synchronous Rectification (SR) in DC–DC and AC–DC
- Primary Switch in Isolated DC–DC Converter
- Motor Drives

MARKING DIAGRAM



DFN5 (SO–8FL)
CASE 488AA



4D0N08 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceabililty

ORDERING INFORMATION
See detailed ordering, marking and shipping information on page 3 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain–to–Source Voltage		V_{DSS}	80	V
Gate–to–Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	119	A
	T_C = 100°C		84	
Power Dissipation (Note 1)	T_C = 25°C	P_D	107	W
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs	I_{DM}	469	A
Pulsed Source Current (Body Diode)		I_{SM}	469	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to +175	°C
Source Current (Body Diode)		I_S	162	A
Single Pulse Avalanche Energy (I_{PK} = 44 A) (Note 3)		E_{AS}	97	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Surface–mounted on FR4 board using 1 in^2 pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} of 97 mJ is based on started TJ = 25 C, I_{AS} = 44 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.4	°C/W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	39	

4. Surface–mounted on FR4 board using 1 in^2 pad, 1 oz. Cu.
5. R_{JA} is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	80			V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C		31.7		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25°C			1	μA
		V_{DS} = 80 V, T_J = 125°C			250	
Gate–to–Source Leakage Current	I_{GSS}	V_{DS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain–to–Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 27 A		3.0	3.5	mΩ
		V_{GS} = 6 V, I_D = 13 A		4.8	6.4	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 133 μA	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 133 μA		–7.5		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 27 A		85		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz		2400		pF
Output Capacitance	C_{OSS}			700		
Reverse Transfer Capacitance	C_{RSS}			11		
Output Charge	Q_{OSS}			50		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 6 V, V_{DD} = 40 V, I_D = 27 A		21		
		V_{GS} = 10 V, V_{DD} = 40 V, I_D = 27 A		33		nC
Threshold Gate Charge	$Q_{G(TH)}$			7		
Gate–to–Source Charge	Q_{GS}			11		
Gate–to–Drain Charge	Q_{GD}			5		
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance	R_G	f = 1 MHz		0.7		Ω
SWITCHING CHARACTERISTICS						
Turn–On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 40 V, I_D = 27 A, R_G = 2.5 Ω		21		ns
Rise Time	t_r			6		
Turn–Off Delay Time	$t_{d(OFF)}$			30		
Fall Time	t_f			5		
SOURCE–TO–DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 27 A, T_J = 25°C		0.82	1.2	V
		V_{GS} = 0 V, I_S = 27 A, T_J = 125°C		0.66		

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 1000 A/μs, I_S = 27 A, V_{DD} = 40 V		21		ns
Charge Time	t_a			11		
Discharge Time	t_b			10		
Reverse Recovery Charge	Q_{RR}			130		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS4D0N08XT1G	4D0N08	DFN5 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TYPICAL CHARACTERISTICS

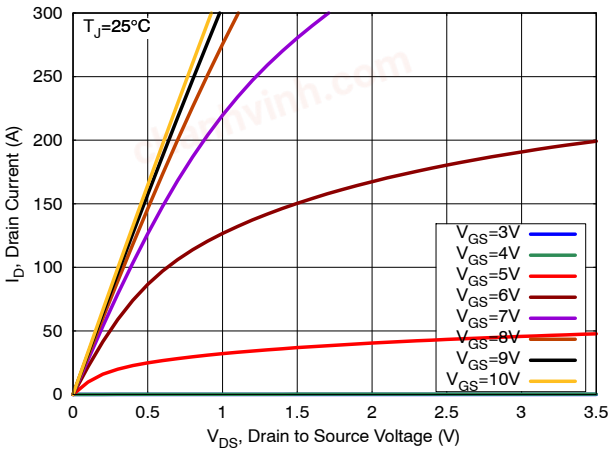


Figure 1. On−Region Characteristics

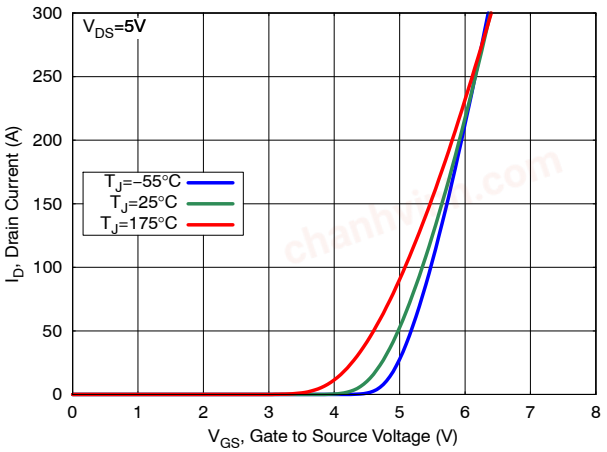


Figure 2. Transfer Characteristics

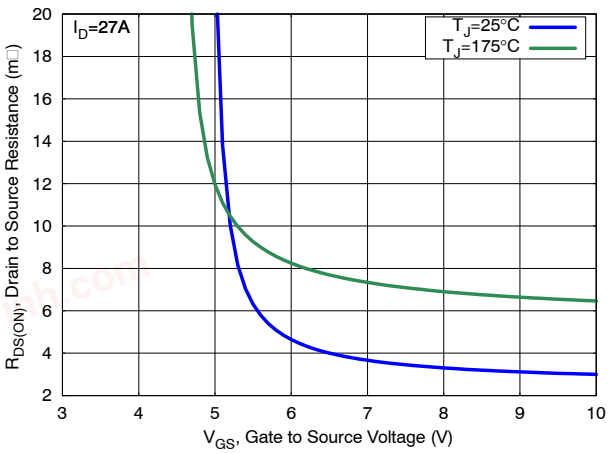


Figure 3. On−Resistance vs. Gate Voltage

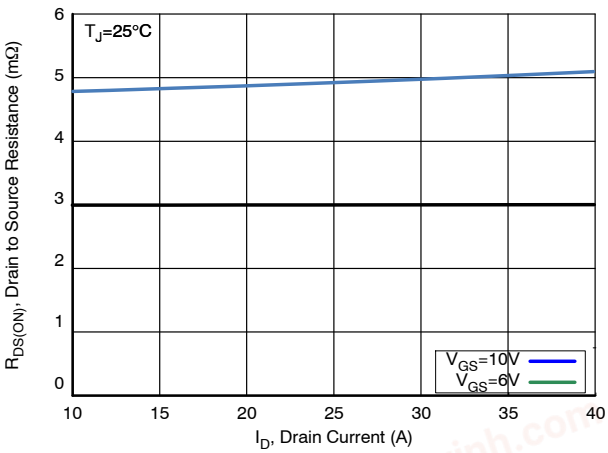


Figure 4. On−Resistance vs. Drain Current

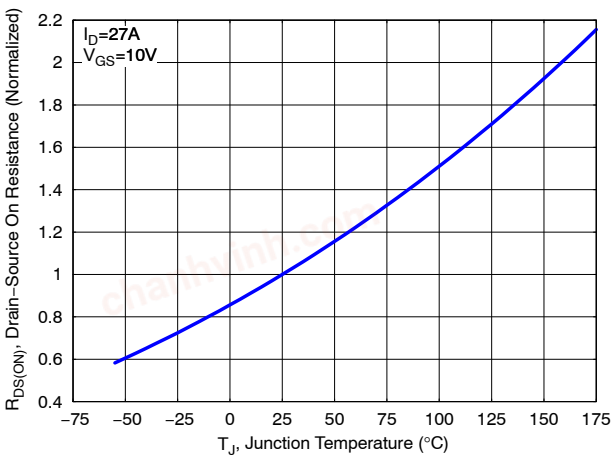


Figure 5. Normalized ON Resistance vs. Junction Temperature

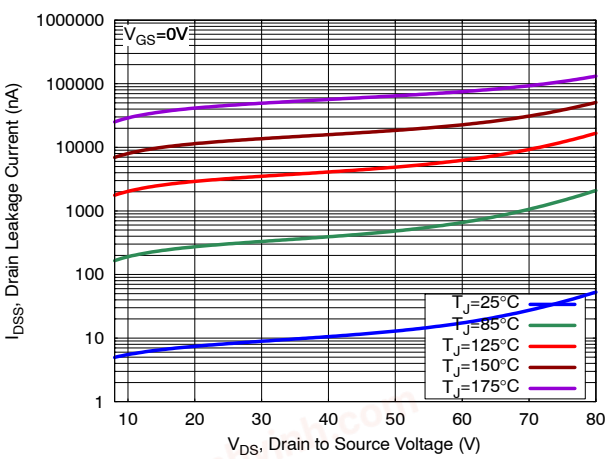


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS

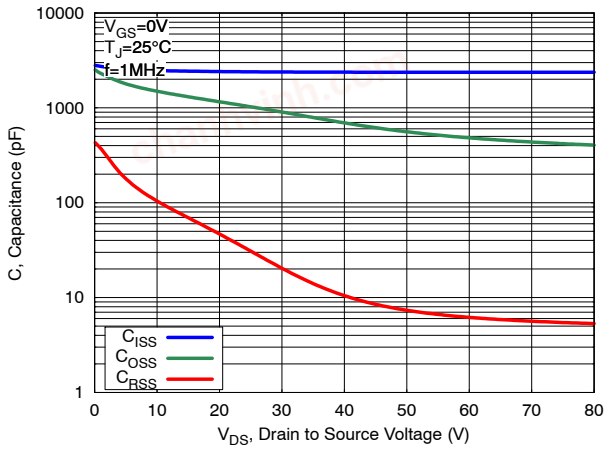


Figure 7. Capacitance Characteristics

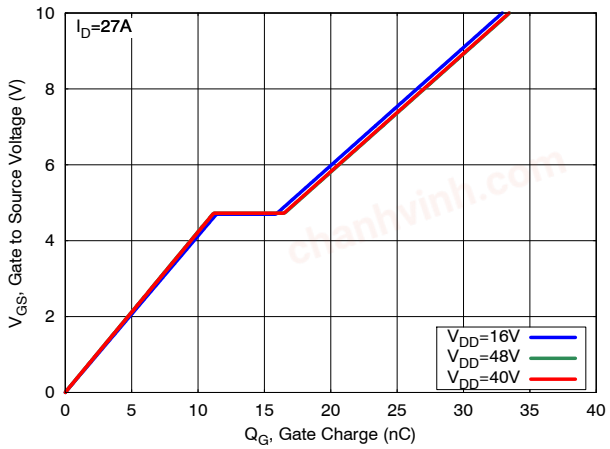


Figure 8. Gate Charge Characteristics

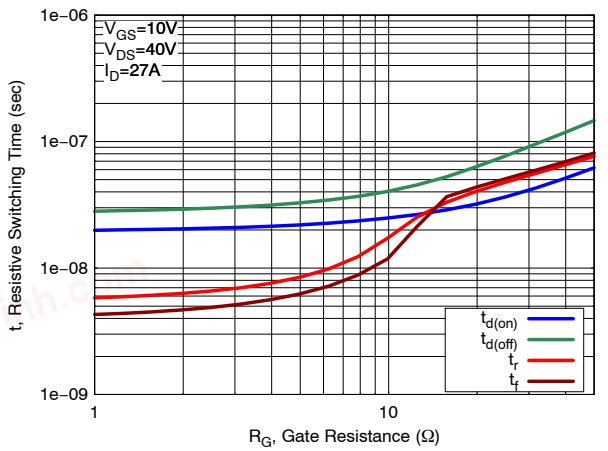


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

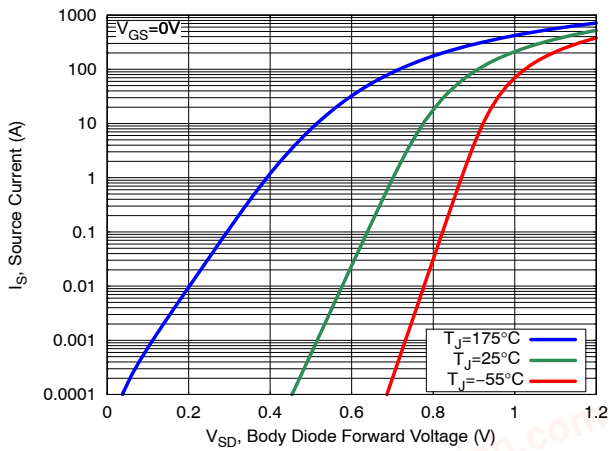


Figure 10. Diode Forward Characteristics

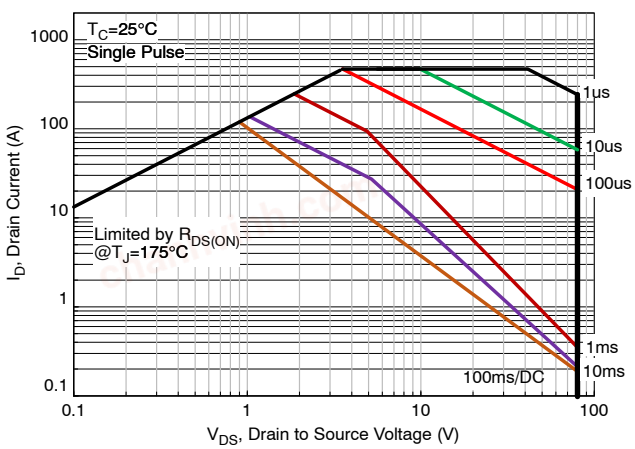


Figure 11. Safe Operating Area (SOA)

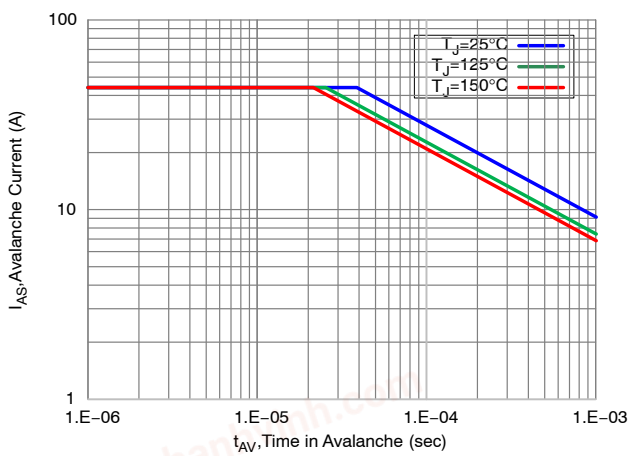


Figure 12. Avalanche Current vs Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

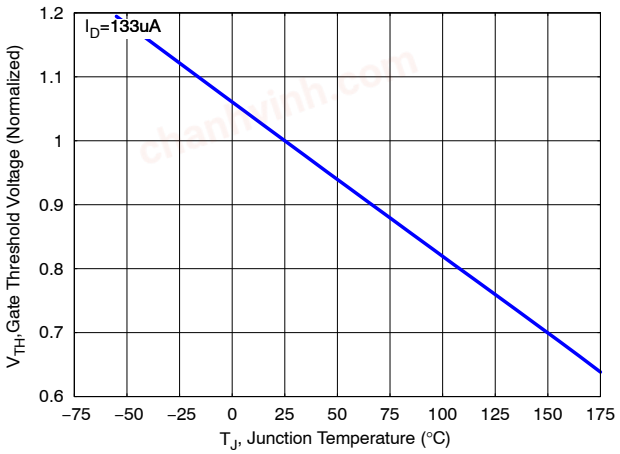


Figure 13. Gate Threshold Voltage vs Junction Temperature

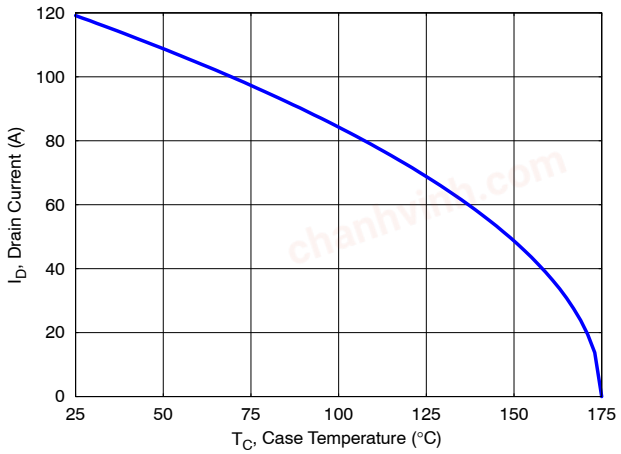


Figure 14. Maximum Current vs. Case Temperature

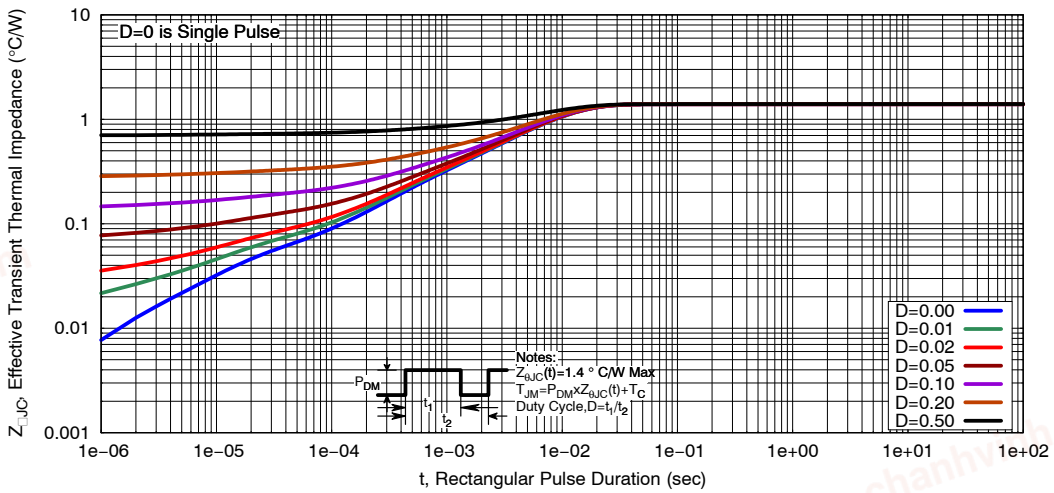
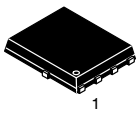


Figure 15. Transient Thermal Response

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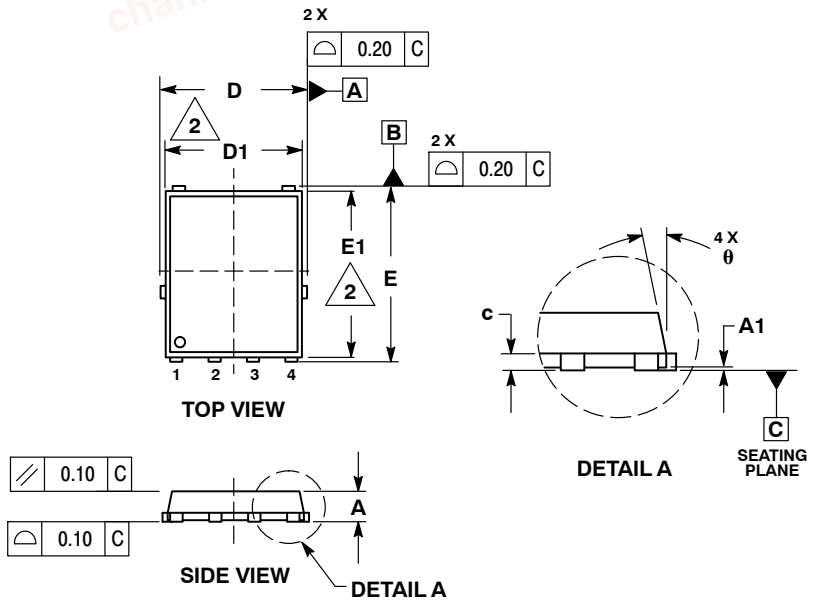
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

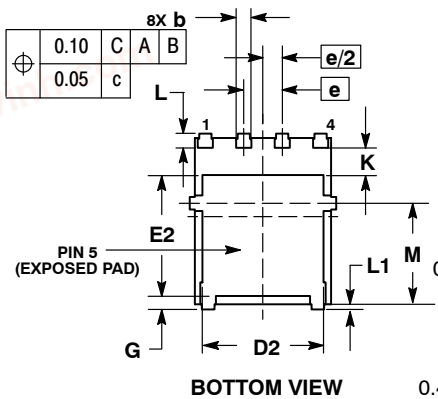
SCALE 2:1

DATE 25 JUN 2018

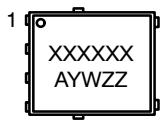


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	---	12 °



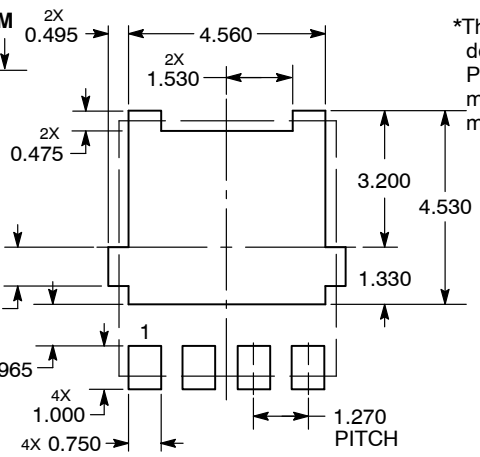
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**	**PAGE 1 OF 1**

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