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NTHS5441

Power MOSFET

−20 V, −5.3 A, P−Channel ChipFET™

Features

- Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package
- Pb−Free Package is Available

Applications

- Power Management in Portable and Battery−Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	5 sec	Steady State	Unit
Drain−Source Voltage	V_{DS}	−20		V
Gate−Source Voltage	V_{GS}	±12		V
Continuous Drain Current (T_J = 150°C) (Note 1) T_A = 25°C T_A = 85°C	I_D	 −5.3 −3.8	 −3.9 −2.8	A
Pulsed Drain Current	I_{DM}	±20		A
Continuous Source Current (Note 1)	I_S	−5.3	−3.9	A
Maximum Power Dissipation (Note 1) T_A = 25°C T_A = 85°C	P_D	 2.5 1.3	 1.3 0.7	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150		°C

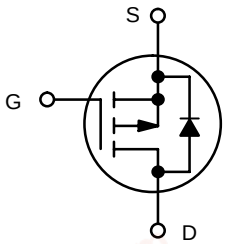
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

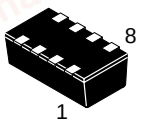
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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−20 V	46 mΩ @ −4.5 V	−5.3 A

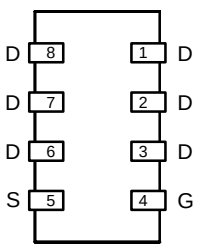


P−Channel MOSFET

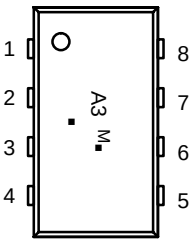


ChipFET
CASE 1206A
STYLE 1

PIN CONNECTIONS



MARKING DIAGRAM



A3 = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTHS5441T1	ChipFET	3000/Tape & Reel
NTHS5441T1G	ChipFET (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction−to−Ambient (Note 2) $t \leq 5$ sec Steady State	$R_{\theta JA}$	 40 80	 50 95	°C/W
Maximum Junction−to−Foot (Drain) Steady State	$R_{\theta JF}$	15	20	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250$ μA	−0.6		−1.2	V
Gate−Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16$ V, $V_{GS} = 0$ V			−1.0	μA
		$V_{DS} = -16$ V, $V_{GS} = 0$ V, $T_J = 85°C$			−5.0	
On−State Drain Current (Note 3)	$I_{D(on)}$	$V_{DS} \leq -5.0$ V, $V_{GS} = -4.5$ V	−20			A
Drain−Source On−State Resistance (Note 3)	$r_{DS(on)}$	$V_{GS} = -3.6$ V, $I_D = -3.7$ A $V_{GS} = -4.5$ V, $I_D = -3.9$ A	− −	0.050 0.046	0.06 −	Ω
		$V_{GS} = -2.5$ V, $I_D = -3.1$ A		0.070	0.083	
Forward Transconductance (Note 3)	g_{fs}	$V_{DS} = -10$ V, $I_D = -3.9$ A		12		mhos
Diode Forward Voltage (Note 3)	V_{SD}	$I_S = -2.1$ A, $V_{GS} = 0$ V		−0.8	−1.2	V
Dynamic (Note 4)						
Total Gate Charge	Q_G	$V_{DS} = -10$ V, $V_{GS} = -4.5$ V, $I_D = -3.9$ A		9.7	22	nC
Gate−Source Charge	Q_{GS}			1.2		
Gate−Drain Charge	Q_{GD}			3.6		
Input Capacitance	C_{iss}	$V_{DS} = -5.0$ Vdc, $V_{GS} = 0$ Vdc, f = 1.0 MHz		710		pF
Output Capacitance	C_{oss}			400		
Reverse Transfer Capacitance	C_{rss}			140		
Turn−On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 10$ Ω $I_D \cong -1.0$ A, $V_{GEN} = -4.5$ V, $R_G = 6$ Ω		14	30	ns
Rise Time	t_r			22	55	
Turn−Off Delay Time	$t_{d(off)}$			42	100	
Fall Time	t_f			35	70	
Source−Drain Reverse Recovery Time	t_{rr}	$I_F = -1.1$ A, di/dt = 100 A/μs		30	60	

2. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

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TYPICAL ELECTRICAL CHARACTERISTICS

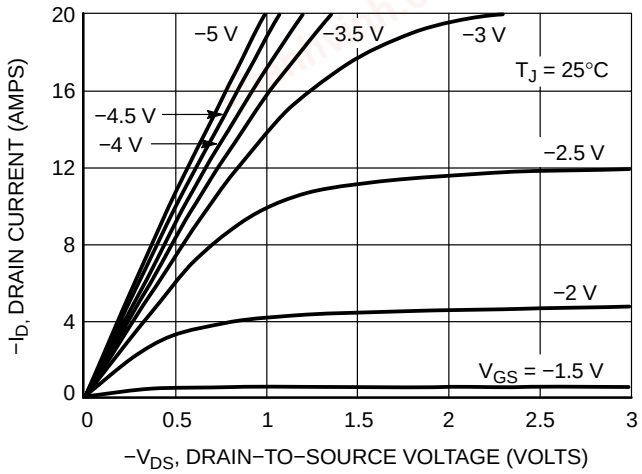


Figure 1. On−Region Characteristics

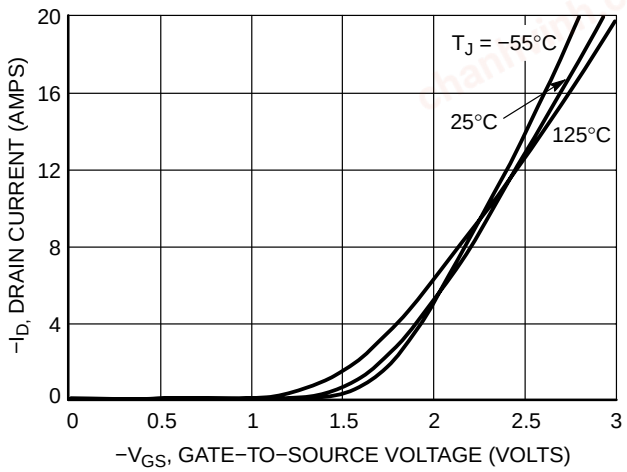


Figure 2. Transfer Characteristics

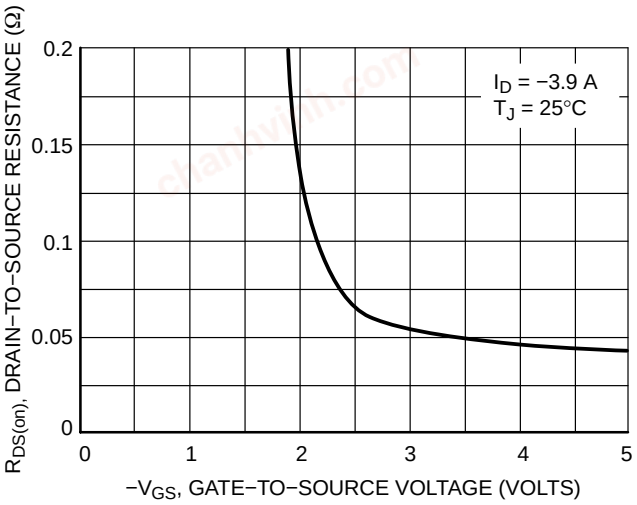


Figure 3. On−Resistance versus Gate−to−Source Voltage

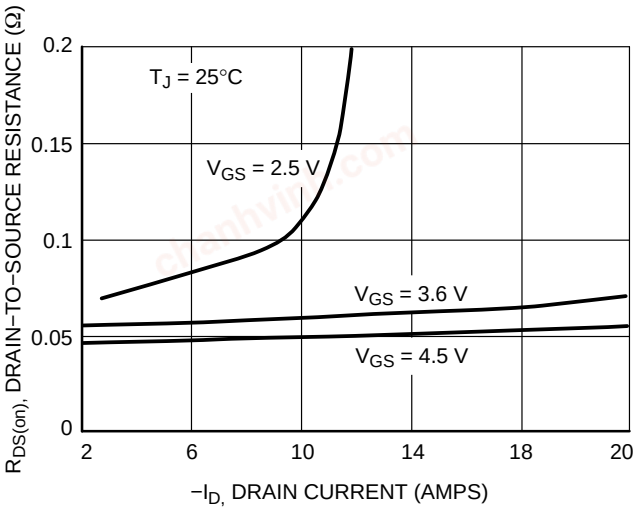


Figure 4. On−Resistance versus Drain Current and Gate Voltage

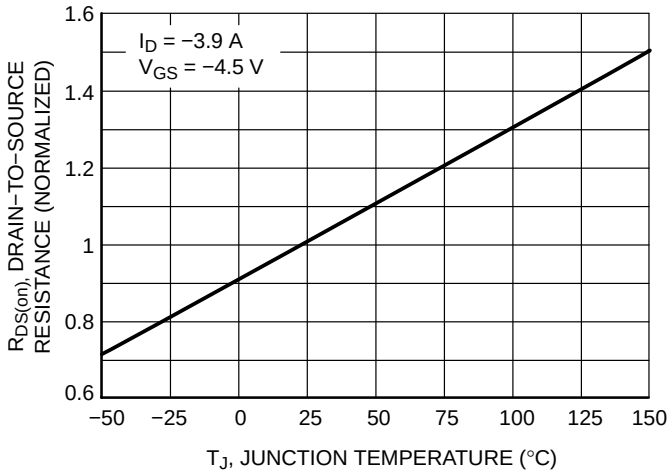


Figure 5. On−Resistance Variation with Temperature

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TYPICAL ELECTRICAL CHARACTERISTICS

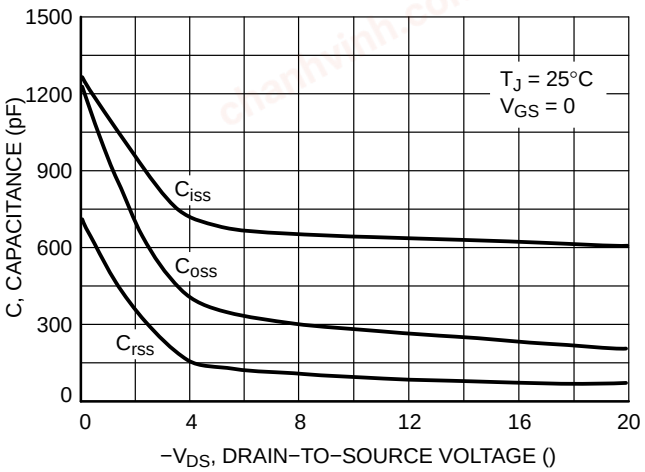


Figure 6. Capacitance Variation

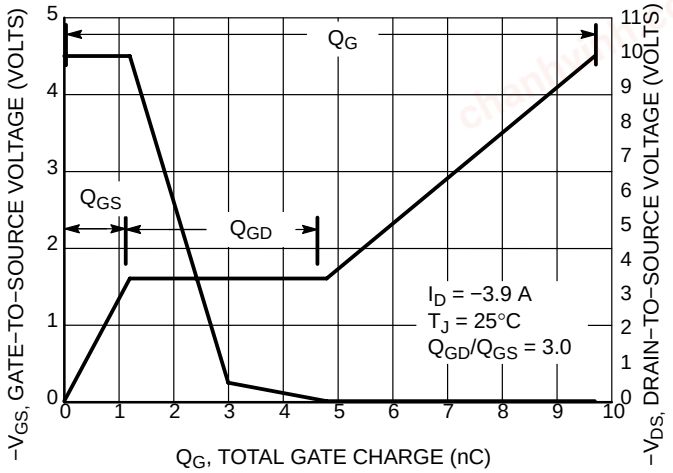


Figure 7. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

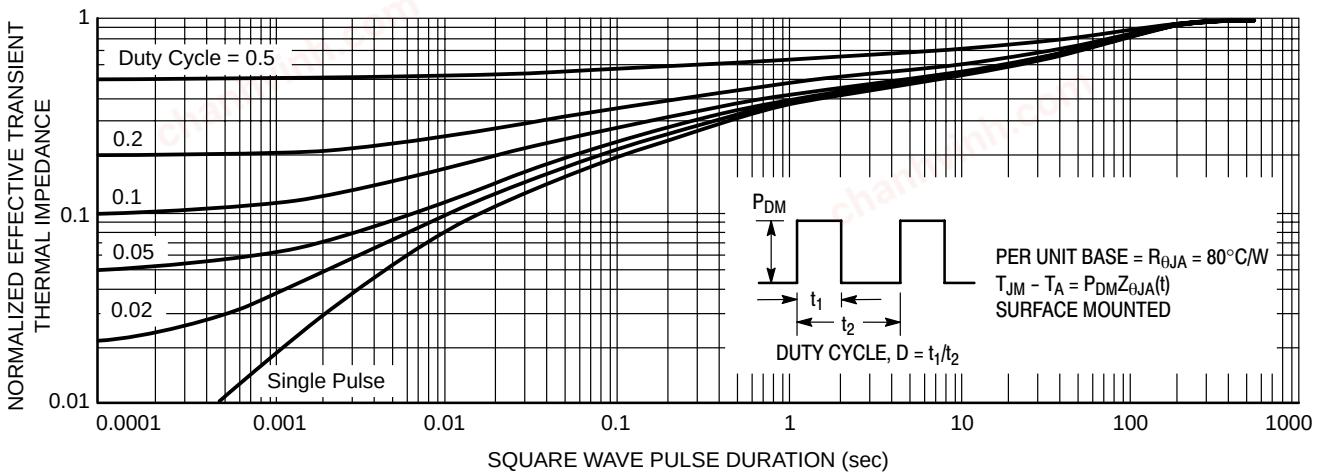


Figure 8. Normalized Thermal Transient Impedance, Junction−to−Ambient

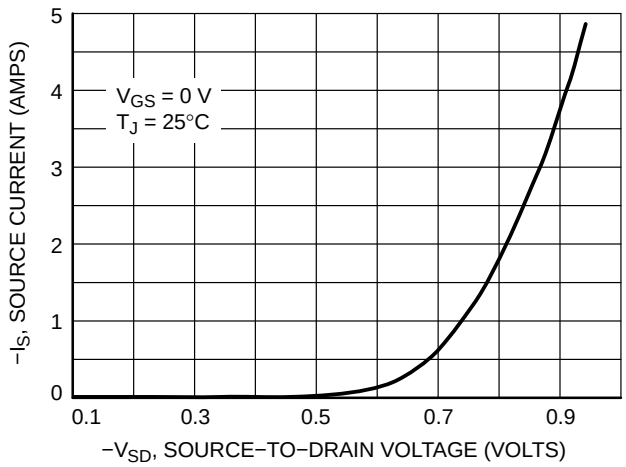


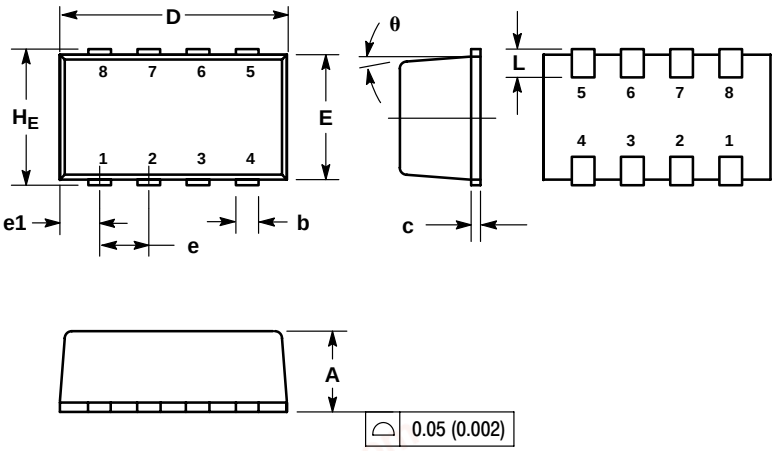
Figure 9. Diode Forward Voltage versus Current

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PACKAGE DIMENSIONS

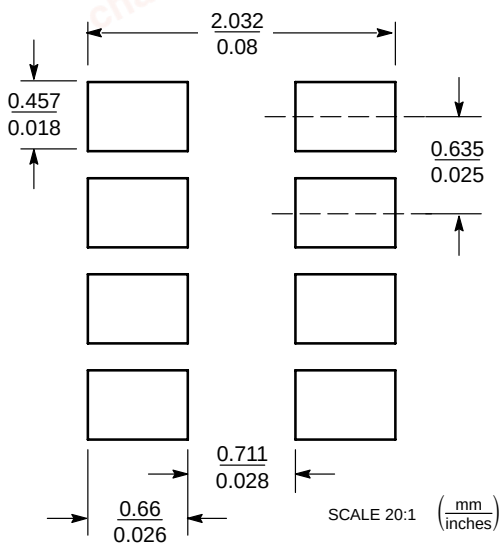
ChipFET™
CASE 1206A−03
ISSUE G



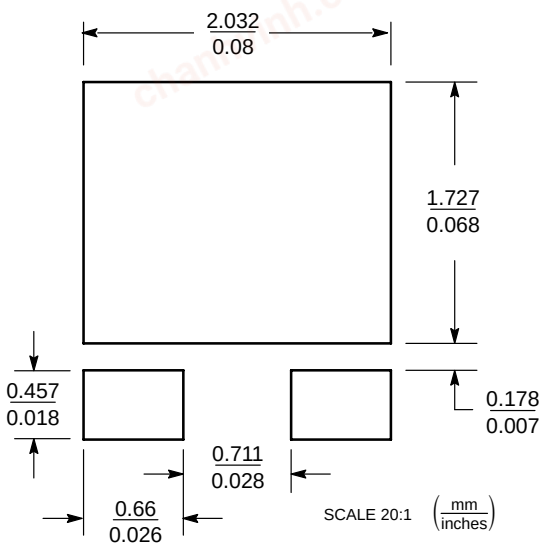
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e		0.65 BSC			0.025 BSC	
e1		0.55 BSC			0.022 BSC	
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ		5° NOM			5° NOM	

SOLDERING FOOTPRINT*



Basic



Styles 1 and 4

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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