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DATA SHEET
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LDO Regulator - Very Low I_q, Window Watchdog, Enable and Reset

150 mA

NCV8768C

The NCV8768C is a 150 mA LDO regulator with integrated window watchdog and reset functions dedicated for microprocessor applications. Its robustness allows the NCV8768C to be used in severe automotive environments. Very low quiescent current as low as 23 μA typical makes it suitable for applications permanently connected to the battery, requiring very low quiescent current with or without load. The Enable function can be used for further decreasing the quiescent current down to 1 μA.

The NCV8768C contains protection functions as current limit and thermal shutdown.

Features

- Output Voltage Options: 3.3 V and 5 V
- Output Voltage Accuracy: ±1.5% (T_J = 25°C to 125°C)
- Output Current up to 150 mA
- Very Low Quiescent Current: Typ 23 μA
- Very Low Dropout Voltage
- Enable Function
- Microprocessor Compatible Control Functions:
  - Reset with Adjustable Power−on Delay
  - Window Watchdog
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features:
  - Current Limitation
  - Reverse Output Current
  - Thermal Shutdown
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain

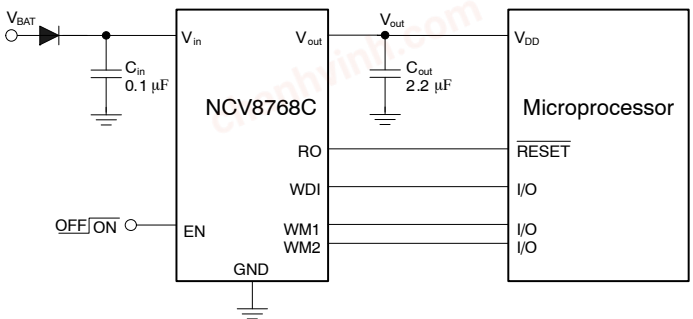
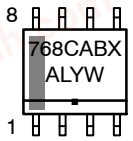


Figure 1. Application Schematic

MARKING DIAGRAMS

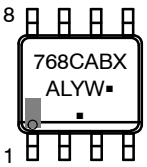


SOIC−8
CASE 751





SOIC−8 EP
CASE 751AC



768CAB =Specific Device Code
X = Voltage Options
= 5 V (X = 5)
= 3.3 V (X = 3)
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

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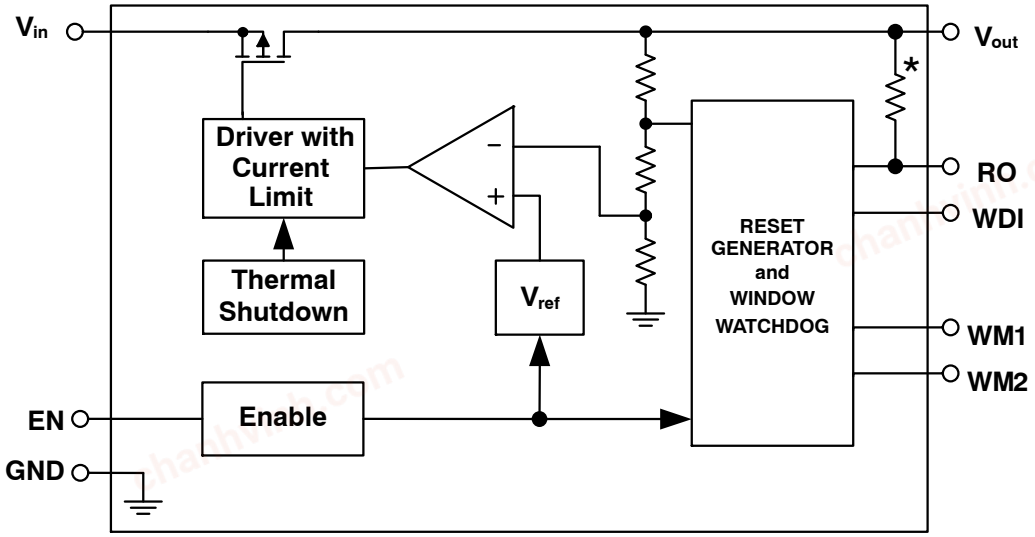


Figure 2. Simplified Block Diagram

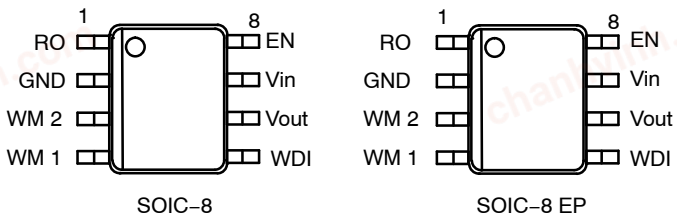


Figure 3. Pin Connections
(Top View)

PIN FUNCTION DESCRIPTION

Pin No. SOIC−8	Pin No. SOIC−8 EP	Pin Name	Description
1	1	RO	Reset Output. 30 kΩ internal Pull−Up resistor connected to V_{out} for 5.0 V version and Open Drain output for 3.3 V version. RO goes Low when V_{out} drops by more than 7% from nominal.
2	2	GND	Power Supply Ground.
3	3	WM2	Watchdog Mode Bit 2; High impedance pin for Watchdog and Reset mode selection. Connect to V_{out}, GND or to I/O pin of the microprocessor.
4	4	WM1	Watchdog Mode Bit 1; High impedance pin for Watchdog and Reset mode selection. Connect to V_{out}, GND or to I/O pin of the microprocessor.
5	5	WDI	Watchdog Input; Trigger Input for Watchdog pulses. When not used, connect to V_{out} or GND.
6	6	V_{out}	Regulated Output Voltage. Connect 2.2 μF capacitor with ESR < 6 Ω to ground.
7	7	V_{in}	Positive Power Supply Input. Connect 0.1 μF capacitor to ground.
8	8	EN	Enable Input; low level disables the IC.
	EPAD	Exposed Pad	Connect to Ground potential or leave it unconnected.

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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 1) DC Load Dump − Suppressed (Note 4)	V_{in}	 −0.3 −	 40 45	V
Output Voltage (Note 2)	V_{out}	−0.3	7.0	V
Enable Voltage DC Load Dump − Suppressed (Note 4)	V_{EN}	 −0.3 −	 40 45	V
Reset Output Voltage (Note 3)	V_{RO}	−0.3	7.0	V
Watchdog Input Voltage	V_{WDI}	−0.3	7.0	V
Watchdog Mode 1 Voltage	V_{WM1}	−0.3	7.0	V
Watchdog Mode 2 Voltage	V_{WM2}	−0.3	7.0	V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. The Output voltage must not exceed the Input voltage.
3. The Reset Output voltage must not exceed the Output voltage.
4. Load Dump Test B (with centralized load dump suppression) according to ISO 16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO 16750−1.

ESD CAPABILITY (Note 5)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−1	1	kV

5. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2017)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018.

LEAD SOLDERING TEMPERATURE AND MSL (Note 6)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level SOIC−8 SOIC−8EP	MSL	 1 2		−

6. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS (Note 7, 8)

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 Thermal Resistance, Junction−to−Ambient Thermal Reference, Junction−to−Case Top Thermal Resistance, Junction−to−Case Top Thermal Resistance, Junction−to−Case Bottom	 $R_{\theta JA}$ Ψ_{JC_TOP} $R_{\theta JC_TOP}$ $R_{\theta JC_BOTTOM}$	 171.8 28.9 95.3 65.4	°C/W
Thermal Characteristics, SOIC−8 EP Thermal Resistance, Junction−to−Ambient Thermal Reference, Junction−to−Case Top Thermal Resistance, Junction−to−Case Top Thermal Resistance, Junction−to−Case Bottom	 $R_{\theta JA}$ Ψ_{JC_TOP} $R_{\theta JC_TOP}$ $R_{\theta JC_BOTTOM}$	 84.3 26.4 103.9 15	°C/W

7. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
8. Mounted onto a 80 x 80 x 1.6 mm single layer FR4 board (645 sq mm, 1 oz. Cu, steady state).

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RECOMMENDED OPERATING RANGES (Note 9)

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 10)	V_{in}	4.5	40	V
Junction Temperature	T_J	−40	150	°C
Output Capacitor (Note 11)	C_{out}	1.0	–	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

9. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
10. Minimum V_{in} = 4.5 V or (V_{out} + V_{DO}), whichever is higher.
11. Including deratings.

ELECTRICAL CHARACTERISTICS

V_{in} = 13.5 V, C_{in} = 0.1 μF, C_{out} = 2.2 μF. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless otherwise noted and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C. (Notes 12 and 13)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage (Accuracy %) 3.3 V 5.0 V	T_J = 25°C to 125°C V_{in} = 4.5 V to 16 V, I_{out} = 0.1 mA to 100 mA V_{in} = 5.55 V to 16 V, I_{out} = 0.1 mA to 100 mA	V_{out}	 3.2505 4.925 (−1.5%)	 3.3 5.0	 3.3495 5.075 (+1.5%)	V
Output Voltage (Accuracy %) 3.3 V 5.0 V	 V_{in} = 4.5 V to 40 V, I_{out} = 0 mA to 100 mA V_{in} = 4.5 V to 16 V, I_{out} = 0 mA to 150 mA V_{in} = 5.55 V to 40 V, I_{out} = 0 mA to 100 mA V_{in} = 5.7 V to 16 V, I_{out} = 0 mA to 150 mA	V_{out}	 3.234 3.234 4.9 4.9 (−2%)	 3.3 3.3 5.0 5.0	 3.366 3.366 5.1 5.1 (+2%)	V
Line Regulation 3.3 V 5.0 V	 V_{in} = 4.5 V to 28 V, I_{out} = 5 mA V_{in} = 5.55 V to 28 V, I_{out} = 5 mA	Reg_{line}	−20	0	20	mV
Load Regulation	I_{out} = 0.1 mA to 150 mA	Reg_{load}	−40	−3	40	mV
Dropout Voltage (Note 14) 5.0 V	I_{out} = 100 mA I_{out} = 150 mA	V_{DO}	– –	195 300	450 600	mV
DISABLE AND QUIESCENT CURRENT						
Disable Current	V_{EN} = 0 V,T_J < 125°C	I_{DIS}	–	0.010	1	μA
Quiescent Current (I_q = I_{in} − I_{out})	I_{out} = 100 μA, T_J = 25°C I_{out} = 100 μA I_{out} = 0 μA, T_J = 25°C I_{out} = 0 μA	I_q	– – – –	23 – 20 –	32 35 29 32	μA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 0.96 x V_{out_nom}	I_{LIM}	205	365	525	mA
Short Circuit Current Limit	V_{out} = 0 V	I_{SC}	205	365	525	mA
REVERSE OUTPUT CURRENT PROTECTION						
Reverse Output Current Protection	V_{EN} = 0 V, I_{out} = −1 mA	V_{out_rev}	–	1.4	5.5	V
PSRR						
Power Supply Ripple Rejection (Note 15)	f = 100 Hz, 0.5V_{pp}	PSRR	–	85	–	dB
ENABLE THRESHOLDS						
Enable Input Threshold Voltage Logic High Logic Low		$V_{th(EN)}$	 – 0.8	 1.75 1.65	 2.5 –	V
Enable Input Current Logic High Logic Low	 V_{EN} = 5 V V_{EN} = 0 V	 I_{EN_ON} I_{EN_OFF}	 – –	 3.5 0.010	 5 1	μA

12. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
13. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
14. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.5 V. If V_{out} < 5 V, then V_{DO} = V_{in} − V_{out}. Maximum dropout voltage value is limited by minimum input voltage V_{in} = 4.5 V recommended for guaranteed operation at maximum output current.
15. Values based on design and/or characterization.

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ELECTRICAL CHARACTERISTICS

V_{in} = 13.5 V, C_{in} = 0.1 μF, C_{out} = 2.2 μF. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless otherwise noted and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C. (Notes 16 and 17)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
WINDOW WATCHDOG						
Watchdog Mode Bit 1 Threshold Voltage Voltage Increasing, Logic High Voltage Decreasing, Logic Low		 $V_{WM1,H}$ $V_{WM1,L}$	 – 0.8	 1.80 1.65	 2.65 –	V
Watchdog Mode Bit 2 Threshold Voltage Voltage Increasing, Logic High Voltage Decreasing, Logic Low		 $V_{WM2,H}$ $V_{WM2,L}$	 – 0.8	 1.80 1.65	 2.65 –	V
Watchdog Input WDI Threshold Voltage Voltage Increasing, Logic High Voltage Decreasing, Logic Low		 $V_{WDI,H}$ $V_{WDI,L}$	 – 0.8	 1.90 1.65	 2.65 –	V
Watchdog Input WDI Current Logic High Logic Low	 $V_{WDI,H}$ = 5 V $V_{WDI,L}$ = 0 V	 $I_{WDI,H}$ $I_{WDI,L}$	 – –	 0.6 0.010	 4 1	μA
WDI Pulse Width (Note 18)		t_{w_WDI}	1.2	–	–	ms
Ignore Window Time	Fast: WM2 = L Slow: WM1 = L AND WM2 = H	t_{IW}	25.6 51.2	32.0 64.0	38.4 76.8	ms
Open Window Time	Fast: WM2 = L Slow: WM1 = L AND WM2 = H	t_{OW}	25.6 51.2	32.0 64.0	38.4 76.8	ms
Closed Window Time	Fast: WM2 = L Slow: WM1 = L AND WM2 = H	t_{CW}	25.6 51.2	32.0 64.0	38.4 76.8	ms
Window Watchdog Trigger Time (Note 19)	Fast: WM2 = L Slow: WM1 = L AND WM2 = H	t_{WD}	– –	48 96	– –	ms
Watchdog Deactivation Current Threshold 3.3 V 5.0 V	I_{out} decreasing V_{in} > 4.5 V V_{in} > 5.55 V	$I_{out_WD_OFF}$	 0.5 0.5	 1.65 1.75	 – –	mA
Watchdog Activating Current Threshold 3.3 V 5.0 V	I_{out} increasing V_{in} > 4.5 V V_{in} > 5.55 V	$I_{out_WD_ON}$	 – –	 2 2	 5 5	mA
RESET OUTPUT RO						
Input Voltage Reset Threshold 3.3 V	V_{in} decreasing, V_{out} > V_{RT}	V_{in_RT}	–	3.8	4.2	V
Output Voltage Reset Threshold 3.3 V 5.0 V	V_{out} decreasing V_{in} > 4.5 V V_{in} > 5.7 V	V_{RT}	 90 90	 93 93	 96 96	$\%V_{out_nom}$
Reset Hysteresis		V_{RH}	–	2.0	–	$\%V_{out_nom}$
Maximum Reset Sink Current 3.3 V 5.0 V	 V_{out} = 3 V, V_{RO} = 0.25 V V_{out} = 4.5 V, V_{RO} = 0.25 V	I_{ROmax}	 1.3 1.75	 5.9 5.5	 – –	mA
Reset Output Low Voltage	V_{out} > 1 V, I_{RO} < 200 μA	V_{ROL}	–	0.02	0.25	V
Reset Output High Voltage 5.0 V		V_{ROH}	4.5	5	–	V
Reset High Level Leakage Current 3.3 V		I_{ROLK}	–	0.010	1	μA

16. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
17. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
18. Minimal WDI Pulse Width to ensure valid RO signal. Shorter WDI pulses may not be captured, resulting in an incorrect Reset behavior.
19. Recommended for typical trigger time. $t_{WD} = t_{CW} + 1/2 * t_{OW}$

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ELECTRICAL CHARACTERISTICS

V_{in} = 13.5 V, C_{in} = 0.1 μF, C_{out} = 2.2 μF. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless otherwise noted and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C. (Notes 20 and 21)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RESET OUTPUT RO						
Integrated Reset Pull Up Resistor 5.0 V		R_{RO}	15	30	50	kΩ
Reset Delay Time	Fast: WM1 = L AND WM2 = L Slow:WM1 = H OR (WM1 = L AND WM2 = H)	t_{RD}	12.8 25.6	16 32	19.2 38.4	ms
Reset Reaction Time (See Figure 38)		t_{RR}	16	26	38	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 22)		T_{SD}	150	175	195	°C
Thermal Shutdown Hysteresis (Note 22)		T_{SH}	–	10	–	°C

20. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
21. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
22. Values based on design and/or characterization.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

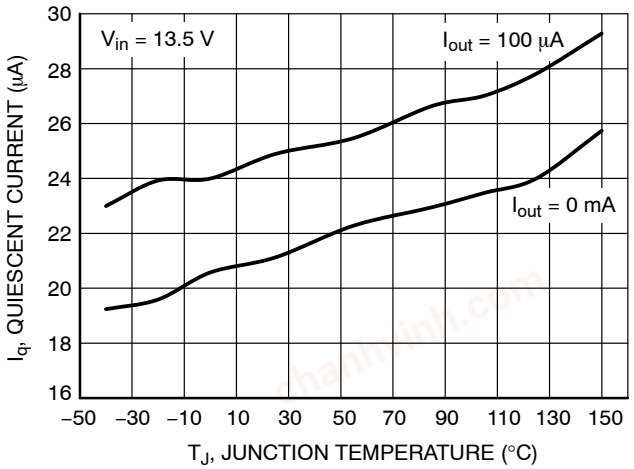


Figure 4. Quiescent Current vs. Temperature (5 V option)

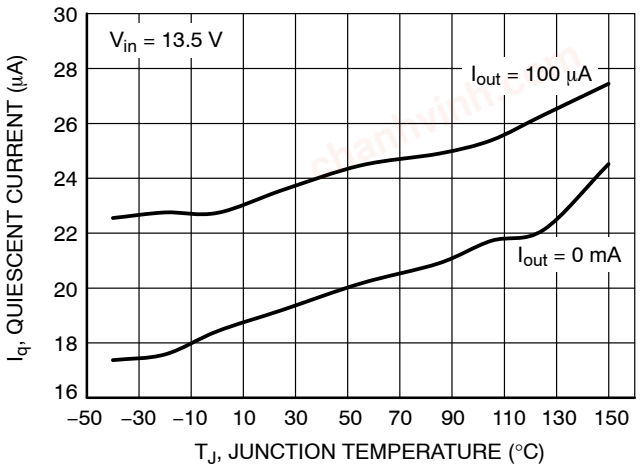


Figure 5. Quiescent Current vs. Temperature (3.3 V option)

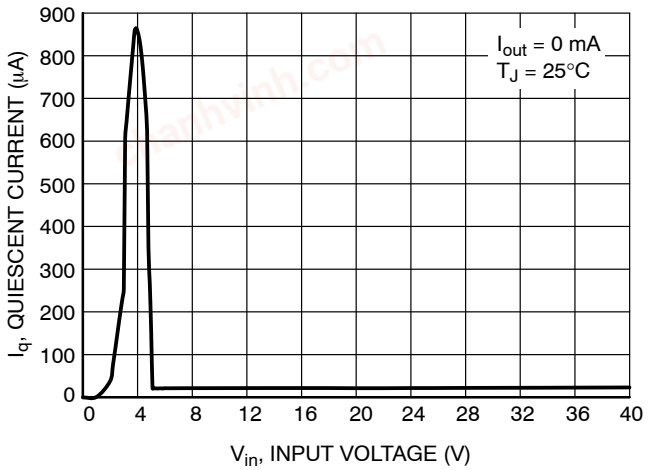


Figure 6. Quiescent Current vs. Input Voltage (5 V option)

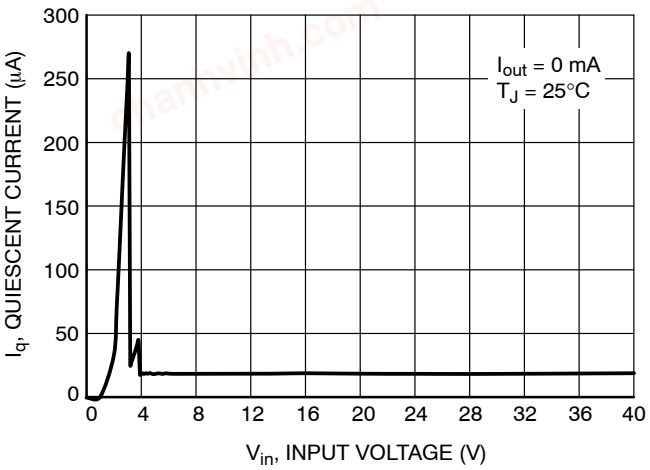


Figure 7. Quiescent Current vs. Input Voltage (3.3 V option)

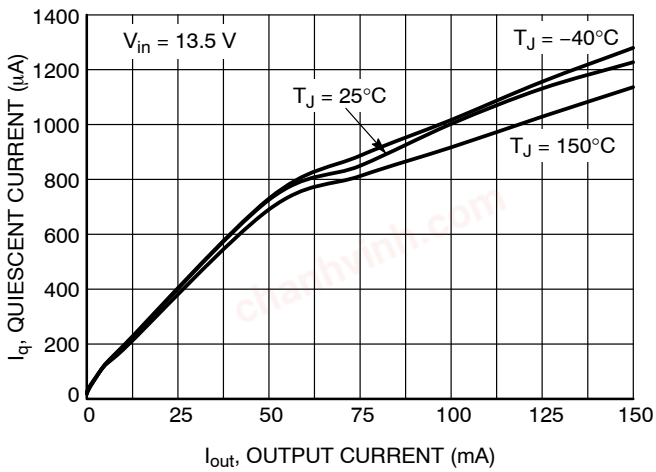


Figure 8. Quiescent Current vs. Output Current (5 V option)

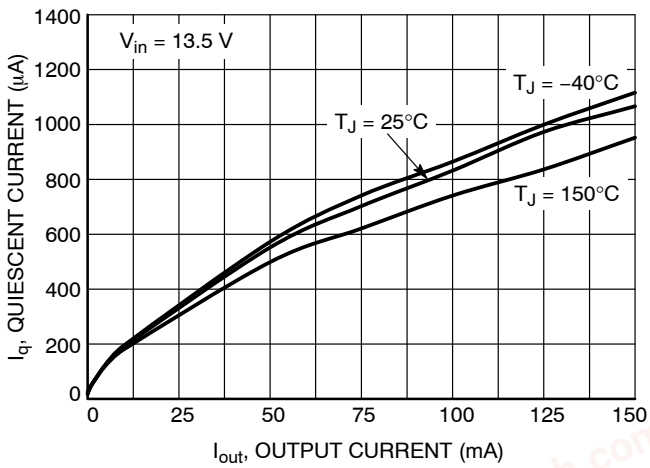


Figure 9. Quiescent Current vs. Output Current (3.3 V option)

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TYPICAL CHARACTERISTICS

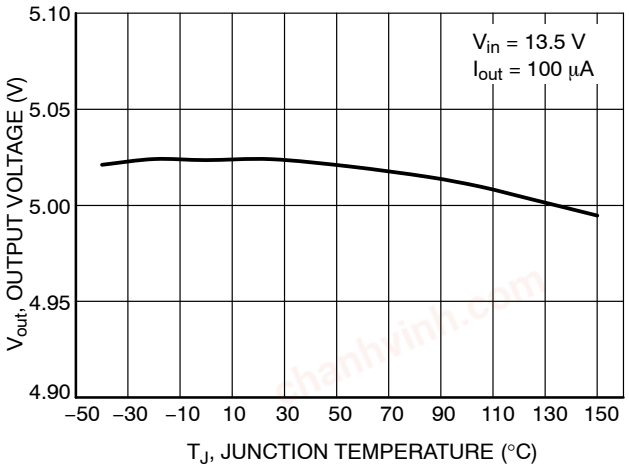


Figure 10. Output Voltage vs. Temperature (5 V option)

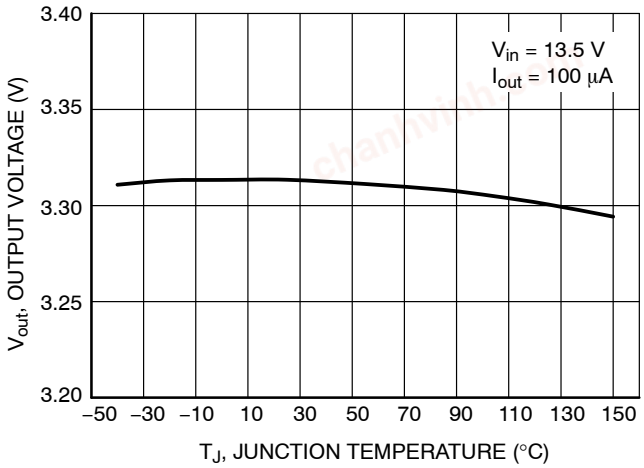


Figure 11. Output Voltage vs. Temperature (3.3 V option)

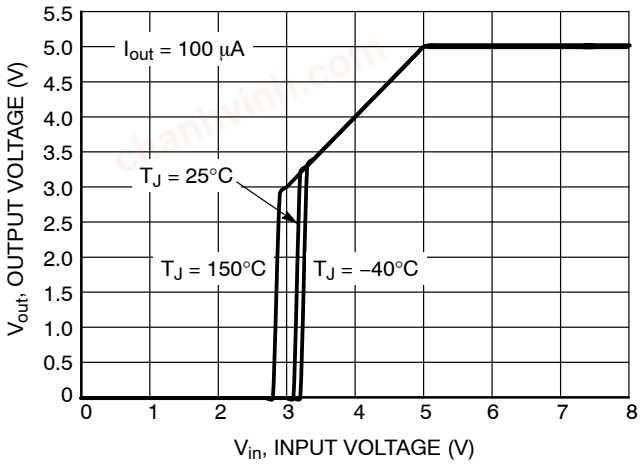


Figure 12. Output Voltage vs. Input Voltage (5 V option)

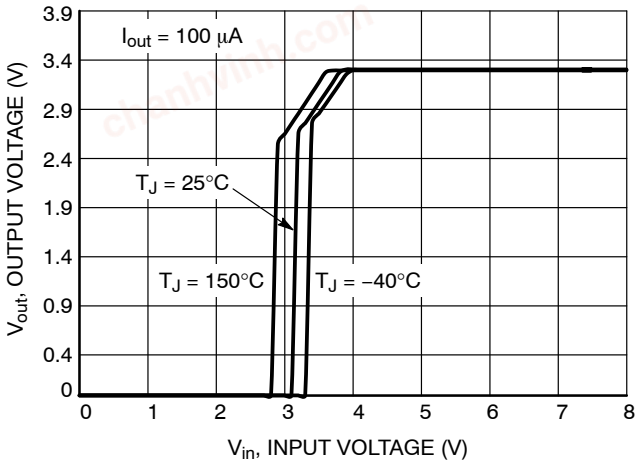


Figure 13. Output Voltage vs. Input Voltage (3.3 V option)

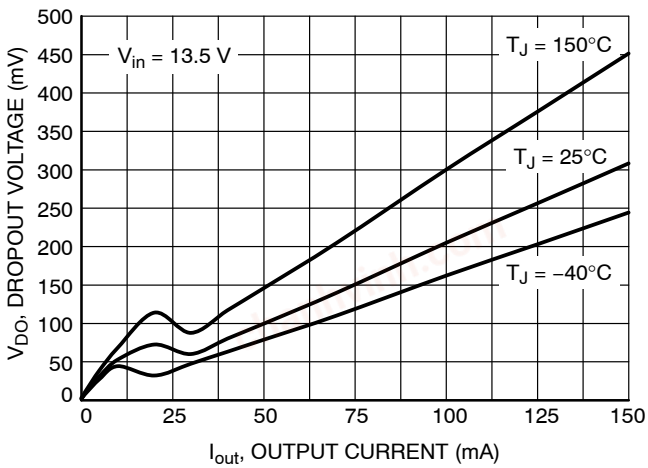


Figure 14. Dropout Voltage vs. Output Current (5 V option)

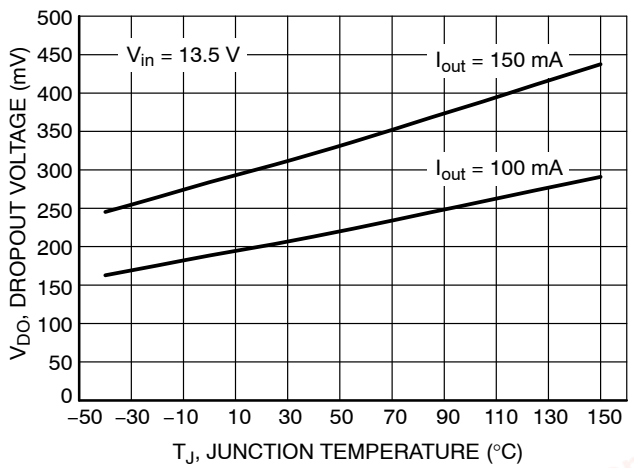


Figure 15. Dropout Voltage vs. Temperature (5 V option)

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TYPICAL CHARACTERISTICS

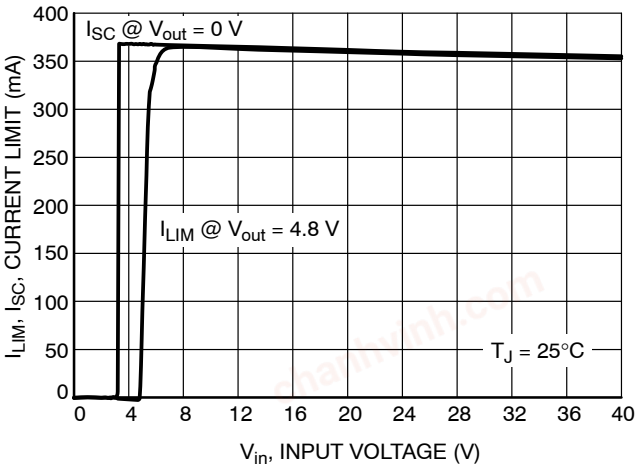


Figure 16. Current Limit vs. Input Voltage (5 V option)

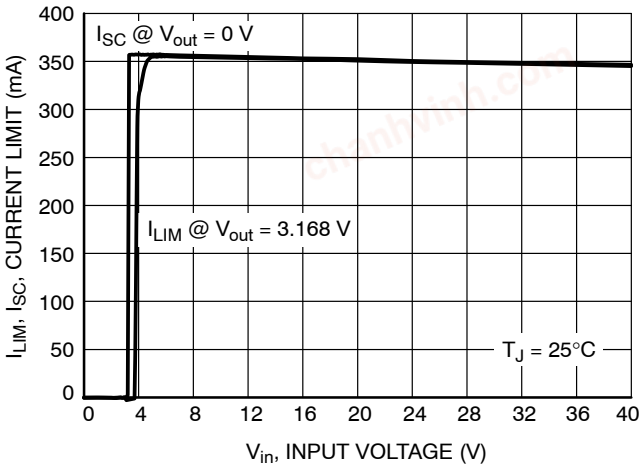


Figure 17. Current Limit vs. Input Voltage (3.3 V option)

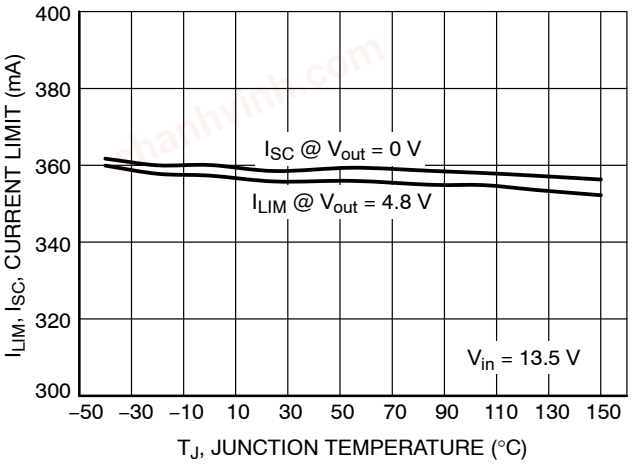


Figure 18. Current Limit vs. Temperature (5 V option)

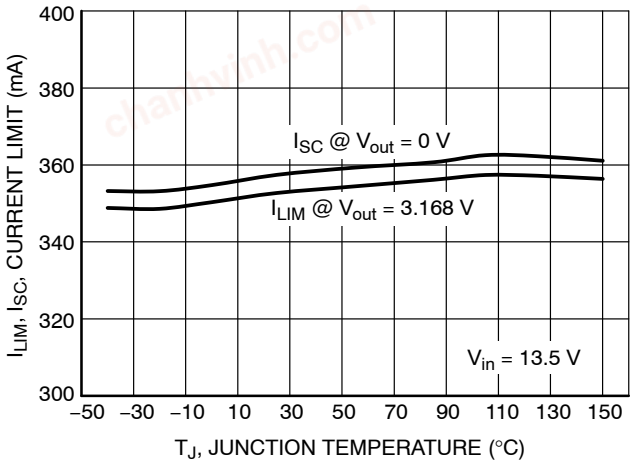


Figure 19. Current Limit vs. Temperature (3.3 V option)

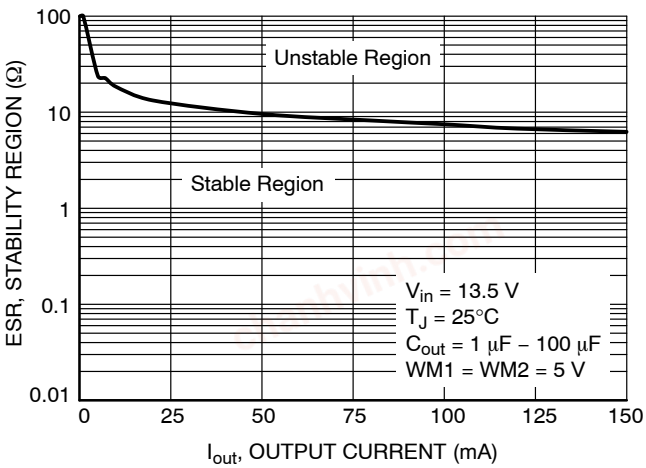


Figure 20. C_{out} ESR Stability Region vs. Output Current (5 V option)

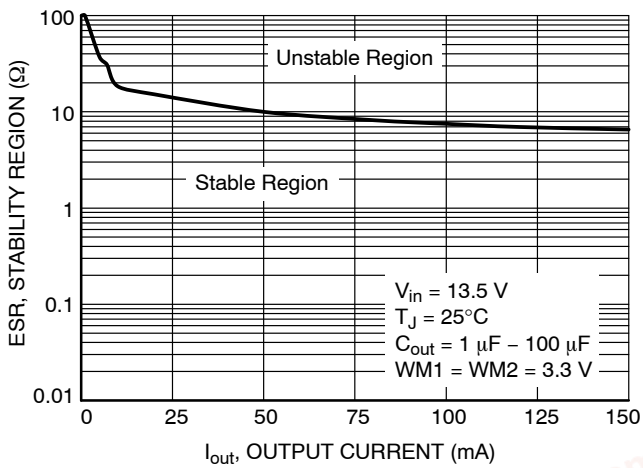


Figure 21. C_{out} ESR Stability Region vs. Output Current (3.3 V option)

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TYPICAL CHARACTERISTICS

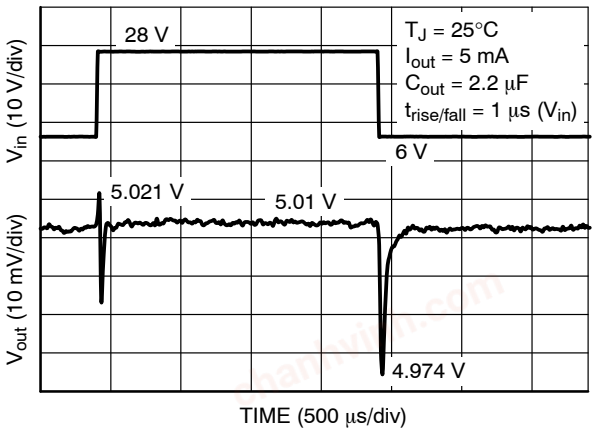


Figure 22. Line Transients (5 V option)

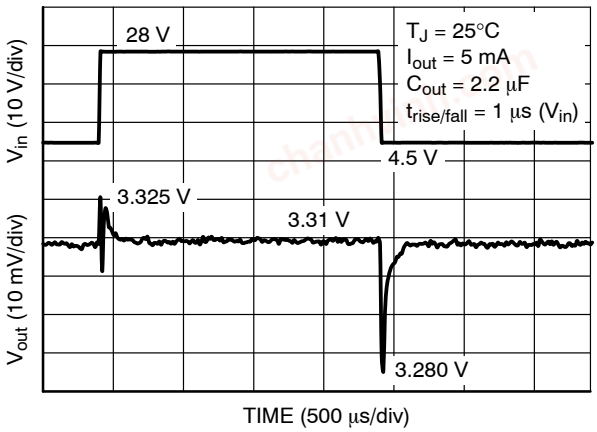


Figure 23. Line Transients (3.3 V option)

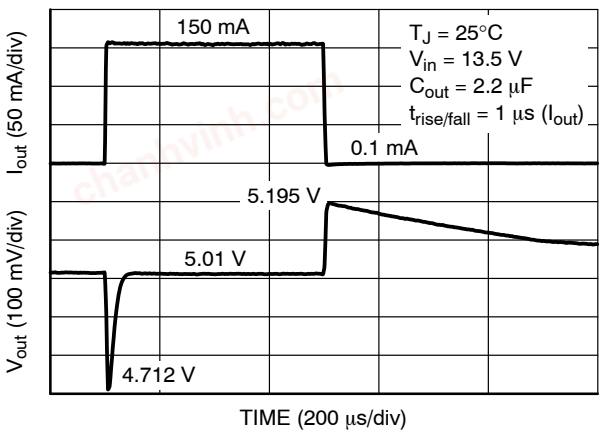


Figure 24. Load Transients (5 V option)

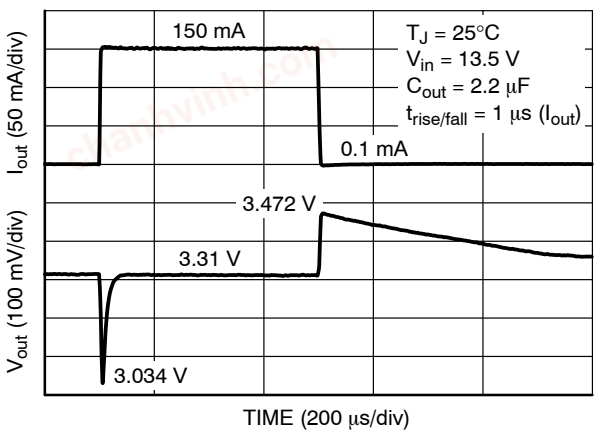


Figure 25. Load Transients (3.3 V option)

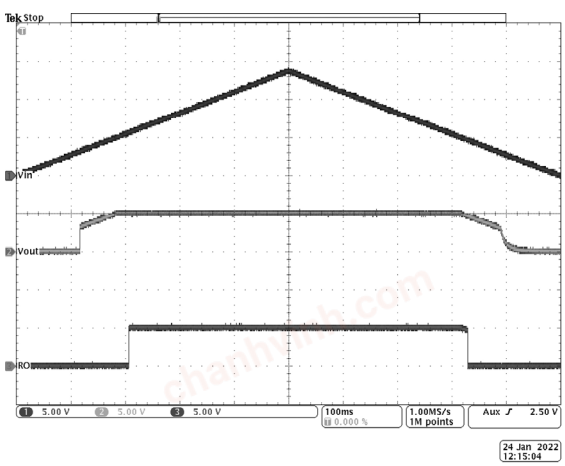


Figure 26. Power Up/Down Response (5 V option)

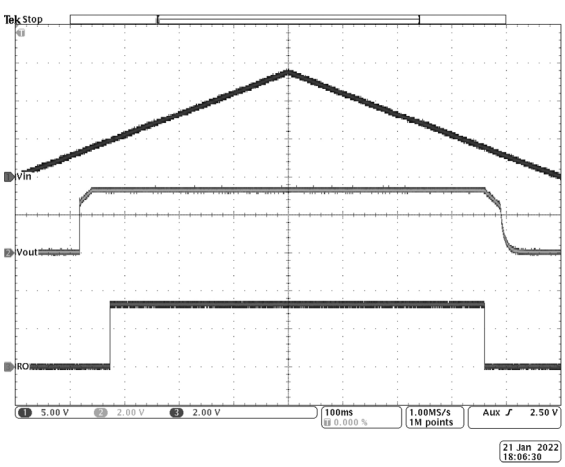


Figure 27. Power Up/Down Response (3.3 V option)

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TYPICAL CHARACTERISTICS

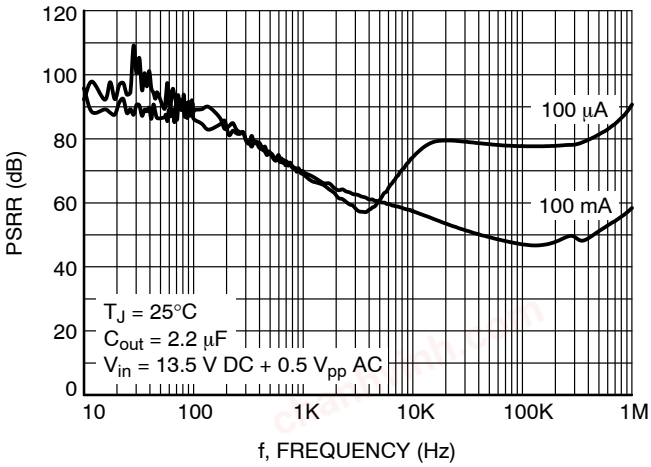


Figure 28. PSRR vs. Frequency (5 V option)

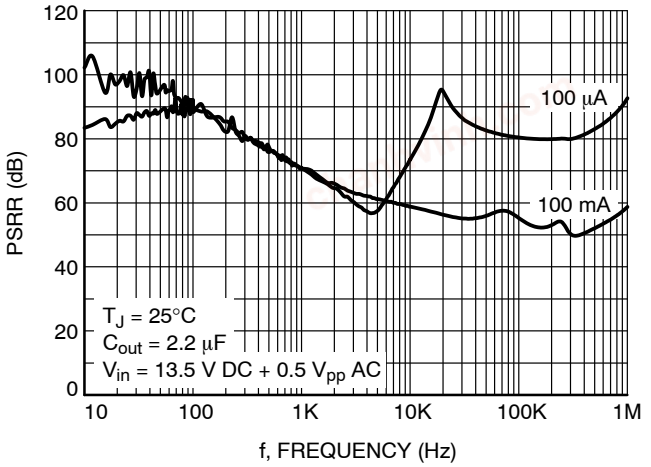


Figure 29. PSRR vs. Frequency (3.3 V option)

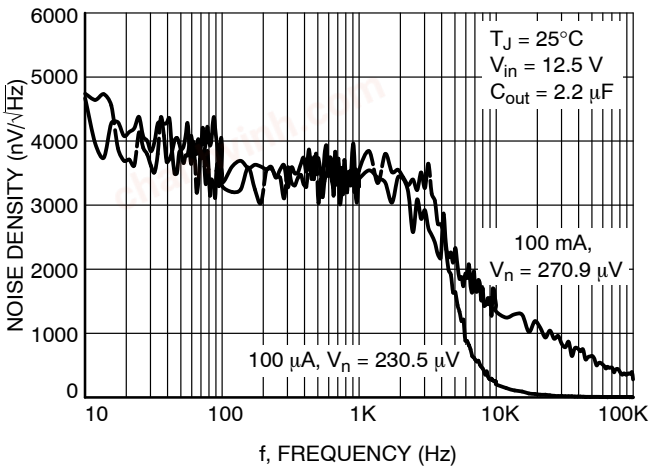


Figure 30. Noise vs. Frequency (5 V option)

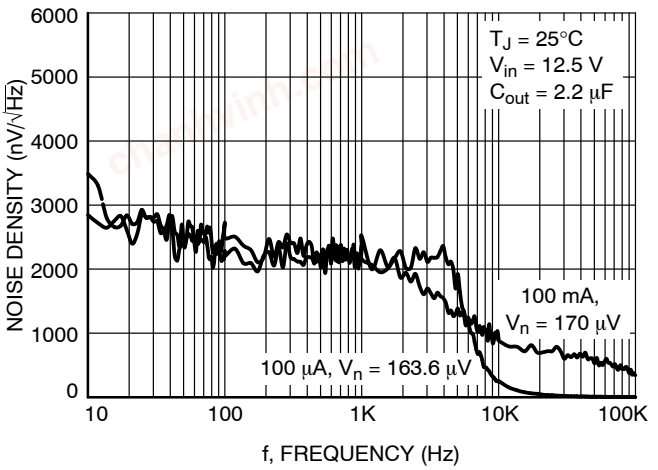


Figure 31. Noise vs. Frequency (3.3 V option)

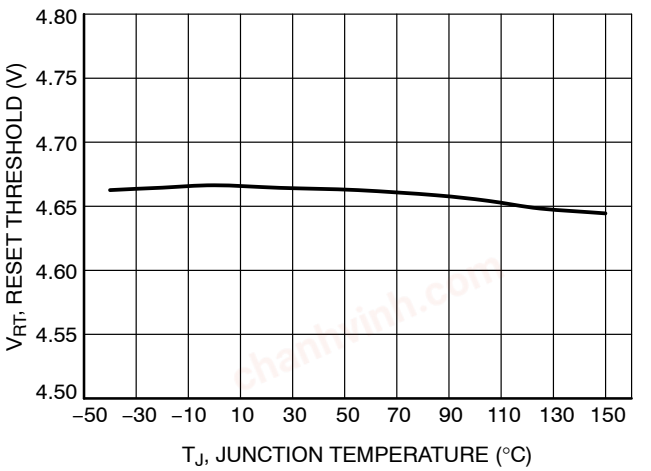


Figure 32. Reset Threshold vs. Temperature (5 V option)

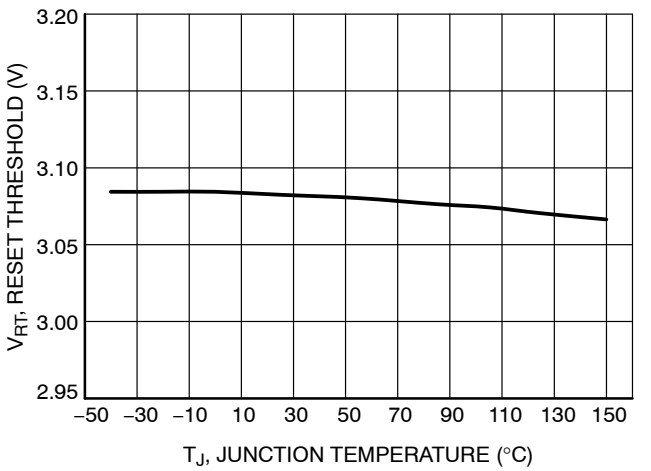


Figure 33. Reset Threshold vs. Temperature (3.3 V option)

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TYPICAL CHARACTERISTICS

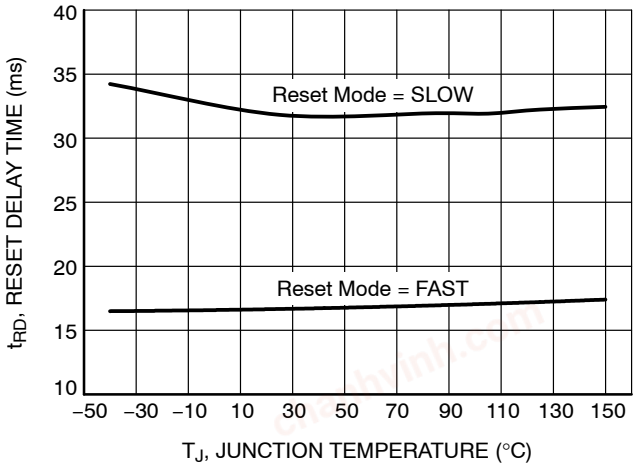


Figure 34. Reset Delay Time vs. Temperature

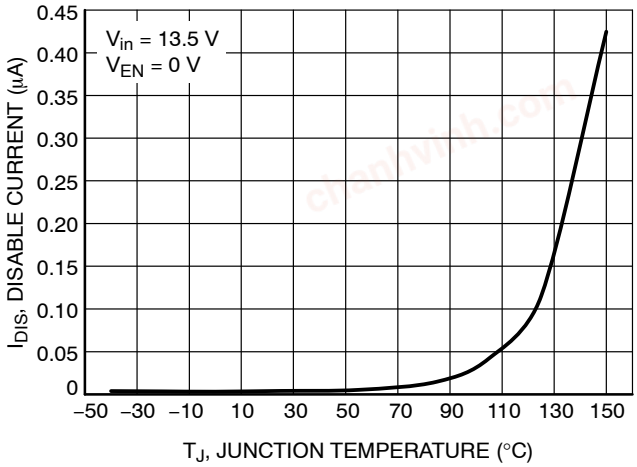


Figure 35. Disable Current vs. Temperature

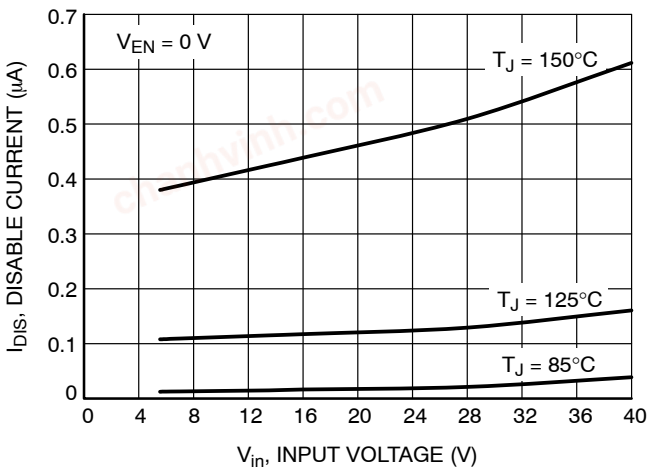


Figure 36. Disable Current vs. Input Voltage

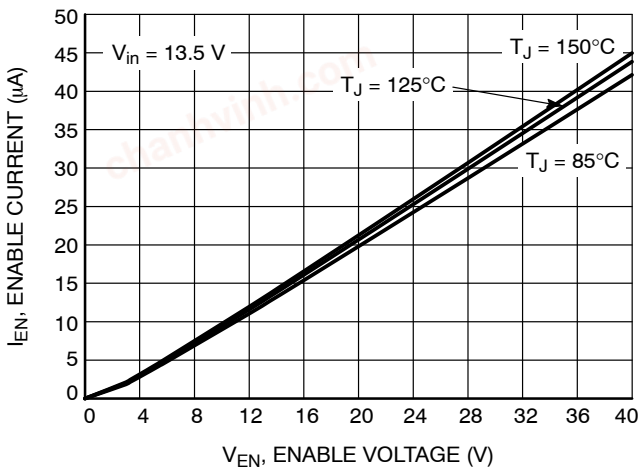


Figure 37. Enable Current vs. Enable Voltage

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TYPICAL CHARACTERISTICS

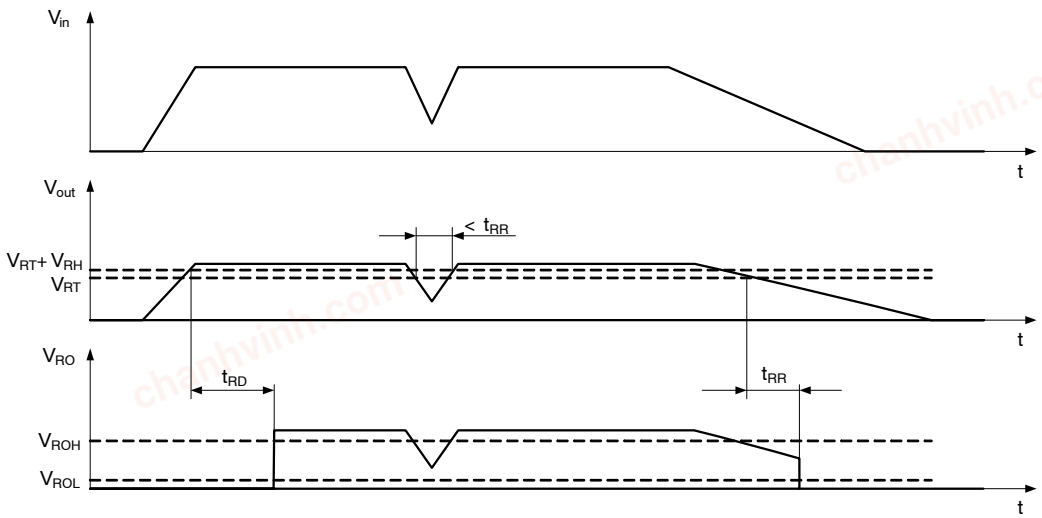
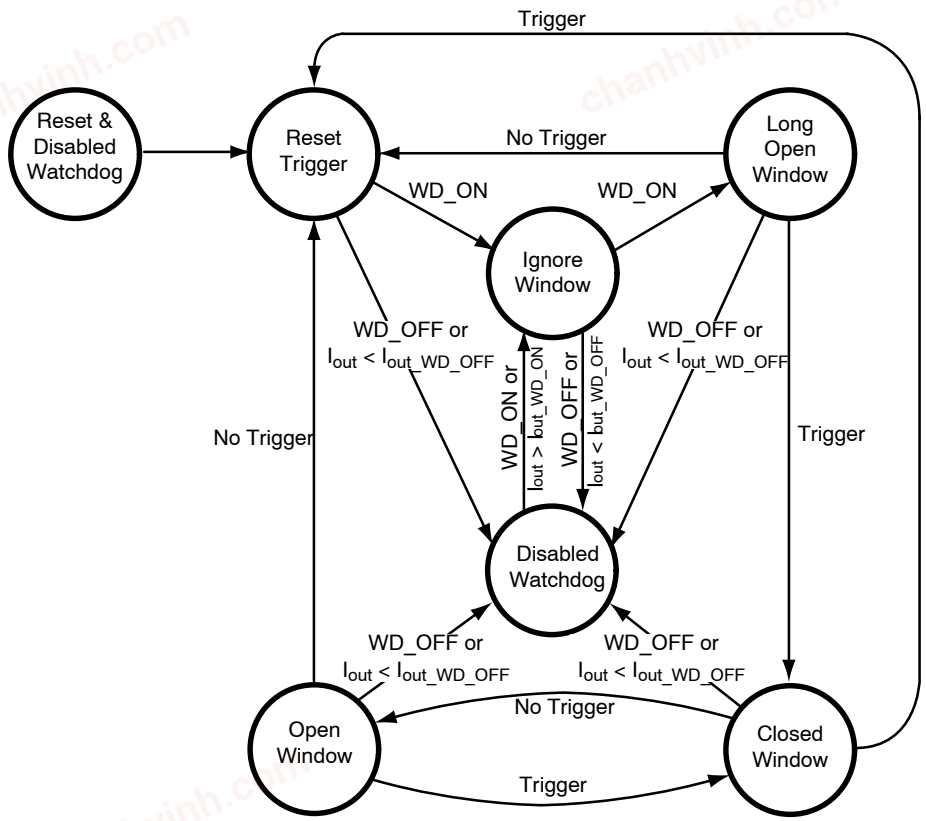


Figure 38. Reset Function and Timing Diagram



WM1	L	L	H	H
WM2	L	H	L	H
Window Watchdog Mode	FAST	SLOW	FAST	OFF
Reset Mode	FAST	SLOW	SLOW	SLOW

Figure 39. Window Watchdog State Diagram, Watchdog and Reset Modes

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TYPICAL CHARACTERISTICS

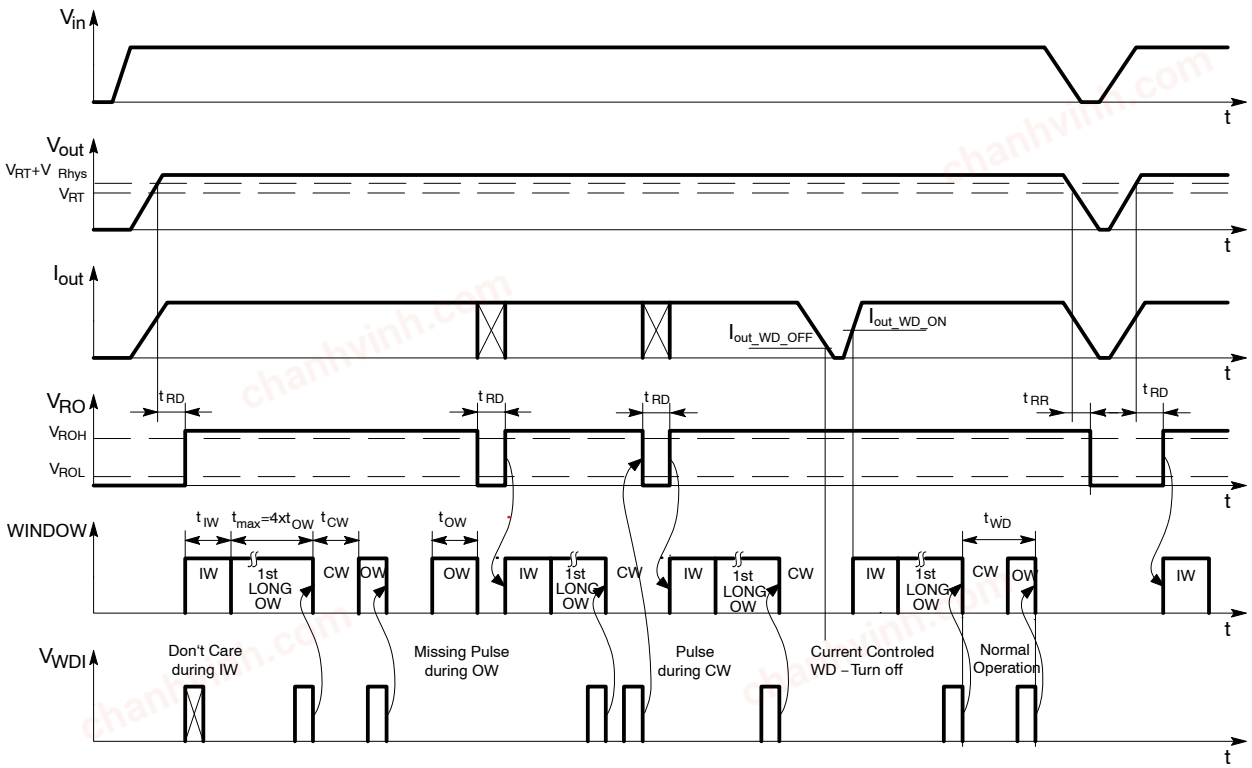


Figure 40. Window Watchdog Signal Diagram

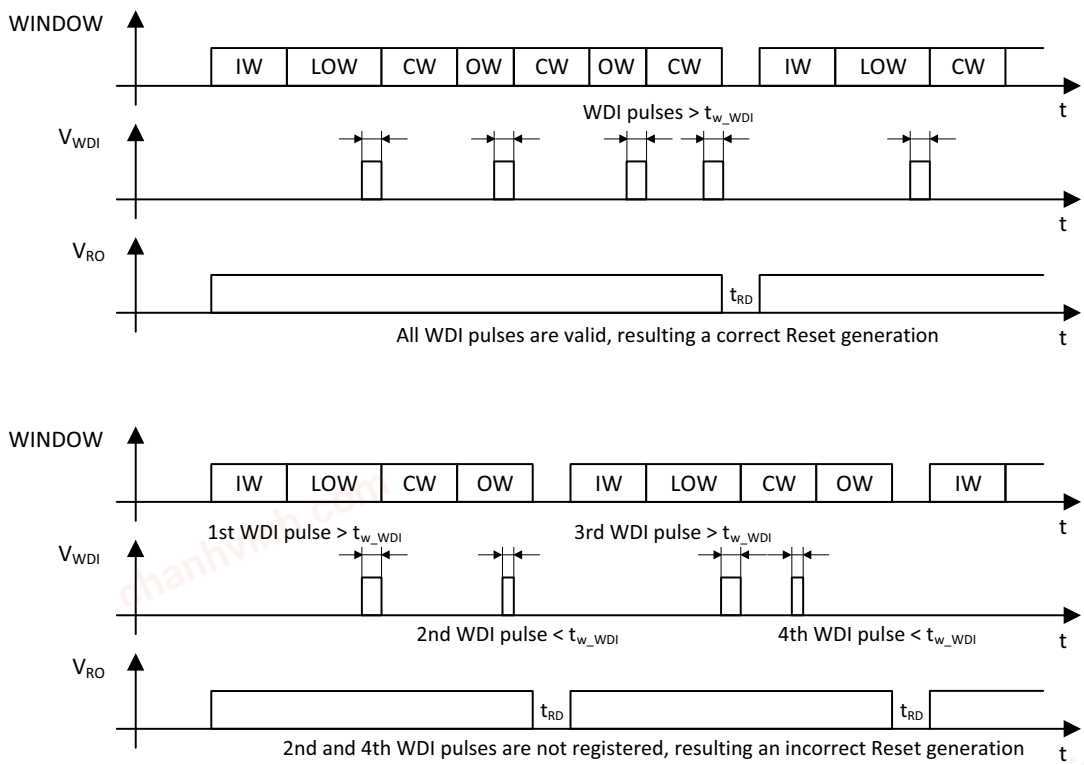


Figure 41. Valid WDI trigger signal

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DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent Current

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output current.

Current Limit and Short Circuit Current Limit

Current Limit is the value of output current at which output voltage drops below 96% of its nominal value. Short Circuit Current Limit is the output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in case that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is the maximum allowed power dissipation for the particular package or the power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV8768C regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figures 4 to 41.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8768C package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The NCV8768C is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR versus Output Current is shown in Figures 20 and 21. The minimum output decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

Enable Operation

The Enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this datasheet.

Reset Operation

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 38. This is in the form of a logic signal on RO. Output voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to V_{out} = 1.0 V. The Reset Output (RO) circuitry includes a

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pull−up resistor (30 kΩ) internally connected to the output (V_{out}). No external pull−up is necessary.

For voltage option 3.3 V RO is open drain output and external pull−up resistor is required.

Reset signal is also generated in case when input voltage decreases below its minimum operating limit (4.5 V). The Input Voltage Reset Threshold is typically 3.8 V. This applies only to voltage options with nominal value below minimum operating input voltage (3.3 V).

Window Watchdog Operation

The watchdog slow, fast or off state is set by pins WM1 and WM2 (see table in Figure 39). The timing values used in this description refer to typ. values when WM1 and WM2 are connected to GND (fast watchdog and reset timing). The state diagram of the window watchdog (WWD) and the watchdog and reset mode selection table is shown in Figure 39. The WWD timing is shown in Figure 40. After power−on, the reset output signal at the RO pin (microprocessor reset) is kept LOW for the reset delay time t_{RD} (16 ms). RO signal transition from LOW to HIGH triggers the ignore window (IW) with duration of t_{IW} (32 ms). During this window the signal at the WDI pin is ignored. When IW ends a long open window with maximum duration of (128 ms, $t_{max} = 4 * t_{OW}$) is started. When a valid trigger signal is detected during long open window, a closed window (CW) with duration of t_{CW} (32 ms) is initialized immediately. WDI signal transition from HIGH to LOW is taken as a trigger. The WDI pulse to generate valid trigger should be longer than the Minimum WDI Pulse Width (t_{w_WDI}) and it has to be present before end of the long window. Valid WDI trigger signal is shown in Figure 41. When CW ends a standard open window (OW) with maximum duration of t_{OW} (32 ms) is initiated immediately. The OW ends immediately when valid trigger appears at WDI input. For normal operation the microprocessor timing of WDI pulses must be stable and correspond to t_{WD}. A reset signal is generated (RO goes LOW) if there is no valid trigger (missing pulse at WDI pin) during OW or if a pre−trigger occurs during the CW (unexpected pulse at WDI pin).

Thermal Considerations

As power in the NCV8768C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8768C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation, which the NCV8768C can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, then the NCV8768C soldered on 645 mm^2 single layer PCB, 1 oz copper area, FR4 can dissipate up to 0.72 W in SOIC−8 and 1.48 W for SOIC−8 EP package when the ambient temperature (T_A) is 25°C. See Figures 42 and 43 for $R_{\theta JA}$ versus PCB area. The power dissipated by the NCV8768C can be calculated from the following equations:

$$P_D = V_{in}(I_q @ I_{out}) + I_{out}(V_{in} - V_{out}) \qquad \text{(eq. 2)}$$

or

$$V_{in(MAX)} = \frac{P_{D(MAX)} + (V_{out} \times I_{out})}{I_{out} + I_q} \qquad \text{(eq. 3)}$$

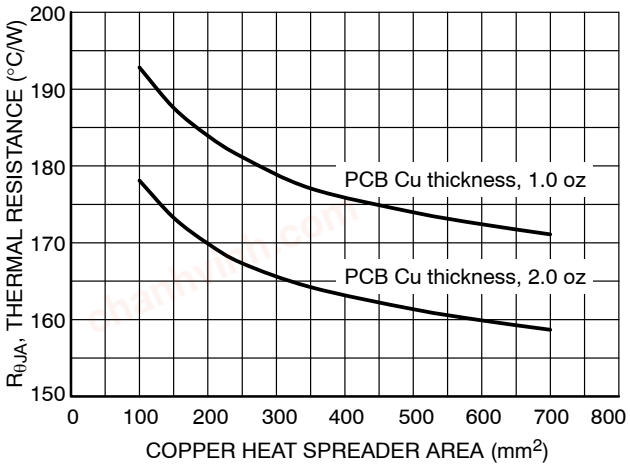


Figure 42. $R_{\theta JA}$ vs. PCB Copper Area (SOIC−8)

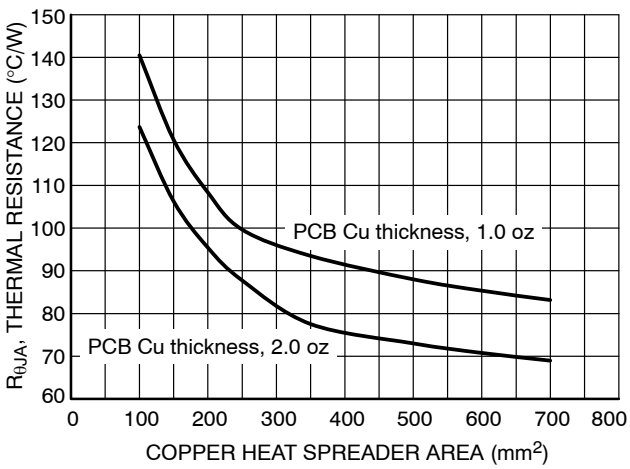


Figure 43. $R_{\theta JA}$ vs. PCB Copper Area (SOIC−8 EP)

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8768C, and make traces as short as possible.

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ORDERING INFORMATION

Device	V_{out}	t_{RD} Fast/ Slow	IW/OW/CW Time Fast/ Slow	1st LOW Time Fast/ Slow	V_{RT}	Output Current WW ON/ OFF	Marking	Package	Shipping†
NCV8768CD50ABR2G	5.0 V	16 / 32 ms	32 / 64 ms	128 / 256 ms	93%	Yes	768CAB5	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV8768CPD50ABR2G	5.0 V	16 / 32 ms	32 / 64 ms	128 / 256 ms	93%	Yes	768CAB5	SOIC−8 EPAD (Pb−Free)	2500 / Tape & Reel
NCV8768CD33ABR2G	3.3 V	16 / 32 ms	32 / 64 ms	128 / 256 ms	93%	Yes	768CAB3	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

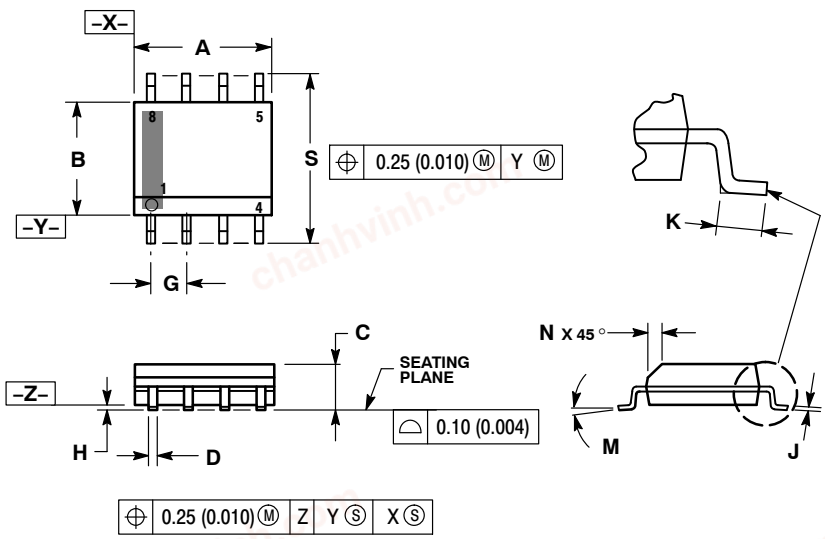
NOTE: Contact factory for other package, output voltage, timing and reset threshold options

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NCV8768C

PACKAGE DIMENSIONS

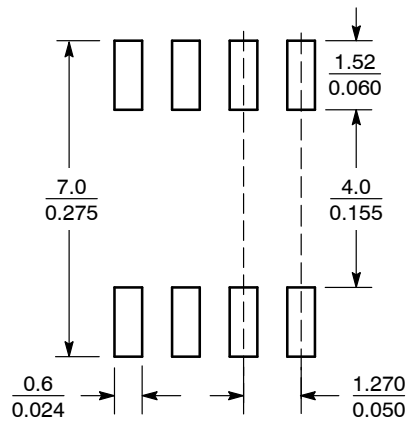
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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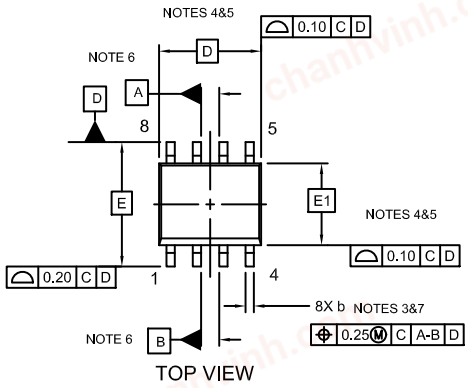
NCV8768C

PACKAGE DIMENSIONS

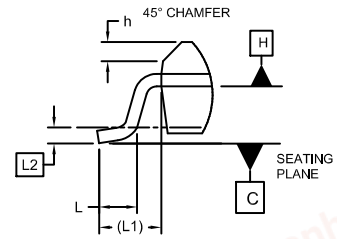
SOIC−8 EP
CASE 751AC
ISSUE D

NOTES:

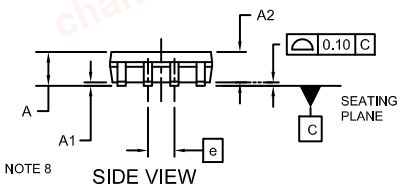
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



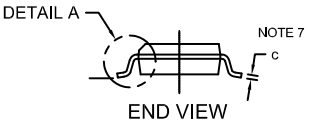
TOP VIEW



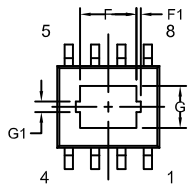
DETAIL A



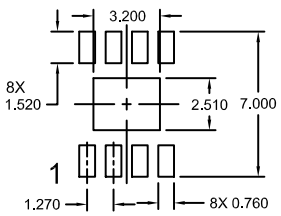
SIDE VIEW



END VIEW



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	−−	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

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