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DATA SHEET
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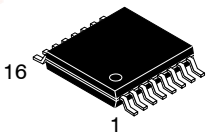
1-Channel Automotive LED Driver

H–Bridge 1.5 A, 60 V – TSSOP16–EP

NCV78514



TSSOP16–EP
CASE 948BV

The NCV78514 is a part of the **onsemi** LED driver solution family for the automotive market. It's main emphasis is on supporting MCU less applications by integrating smart features like derating based on input voltage and temperature of the LED string. The device is optimized for a one channel LED driver unit and is based on a H–Bridge topology with a synchronous Buck switches and asynchronous Boost with external low side NMOSFET and Schottky diode. Supplying in a constant current mode a single LED string between 2 and 20 LEDs.

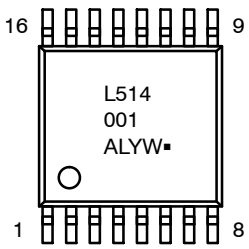
This enables the design of a single PCB design solution or with a separate module approach.

The LED string current is set with a current–encoding resistor. The actual current through the LED string is sensed with a sense resistor.

Features

- Support for MCU Less Application
- Integrated Derating Mechanisms
- Fixed Switching Frequency at 400 kHz
- Input Operating Range from 5 V – 21 V
- Warm Start Management below 9 V
- Withstands Load Dump up to 45 V
- Output Voltage Range up to 60 V
- External Programmable Current 200 mA – 1500 mA
- Pulse Width Modulation from 80 Hz to 600 Hz
- LED Current Dimming Frequency 400 Hz
- External NTC / PTC for LED–temperature
- Spread Spectrum
- Status and Error Mode Handling
- AEC–Q100 Qualified and PPAP Capable

MARKING DIAGRAM



L514001 = Specific Device Code
A = Assembly Location
L = Wafer Lot
YW = Year & Work Week
▪ = Pb–Free Indicator Microdot

ORDERING INFORMATION

Device	Package	Shipping†
NCV78514PA0R2G	TSSOP16–EP (Pb–Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Typical Application

- Fog Lamp
- Cornering Light
- Logo Projection
- Logo Lighting

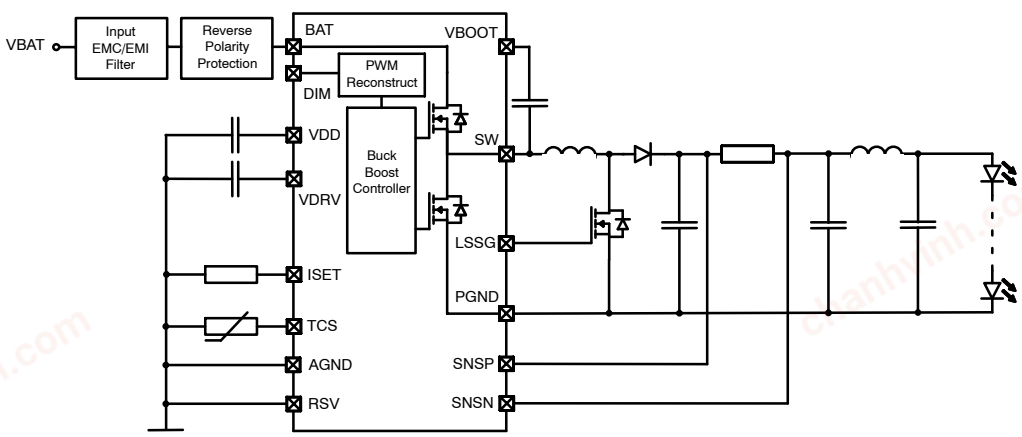


Figure 1. Typical Application Circuit

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FUNCTIONAL BLOCK DIAGRAM

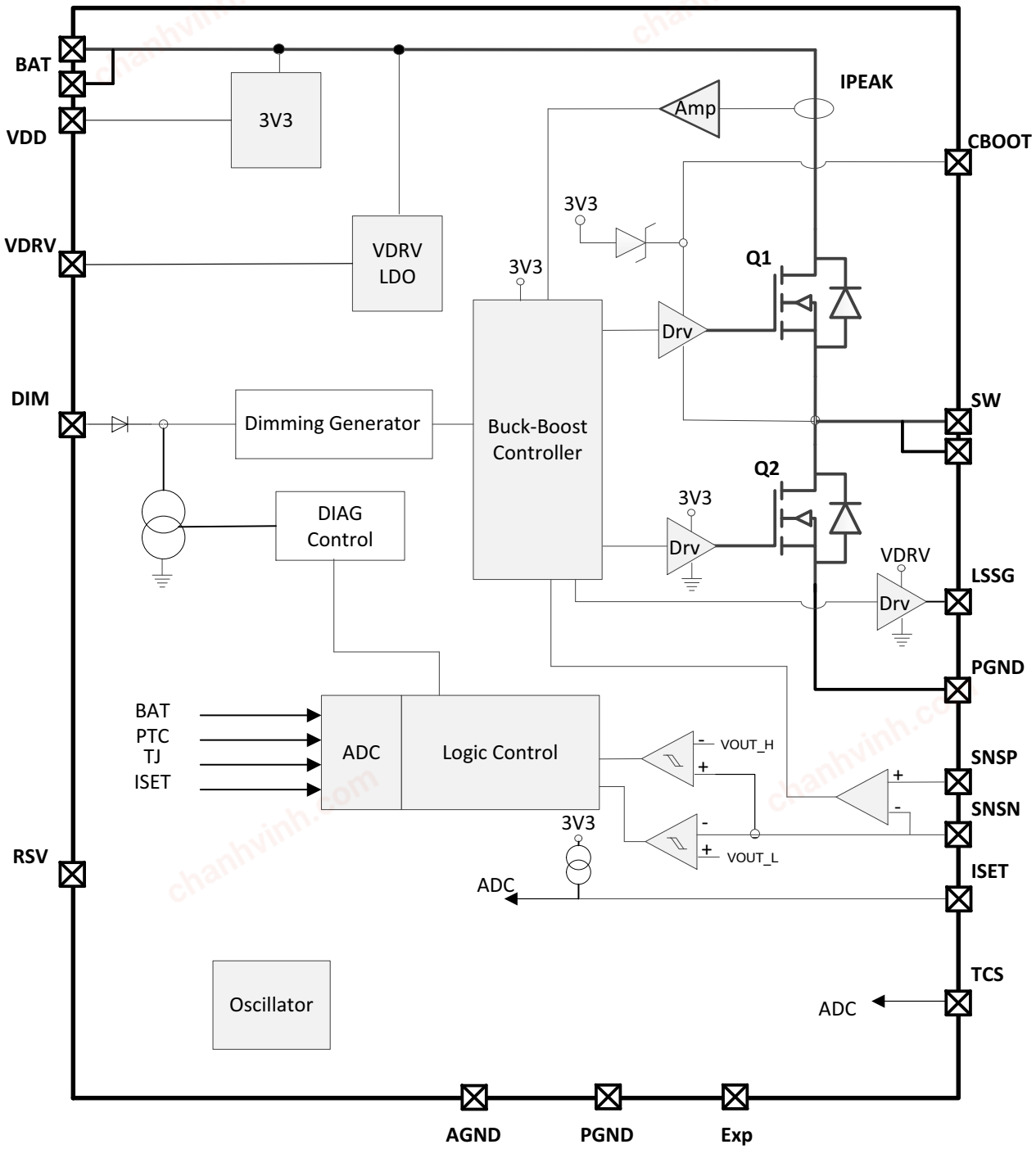

Figure 2. Block Diagram

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PIN OUT DESCRIPTION

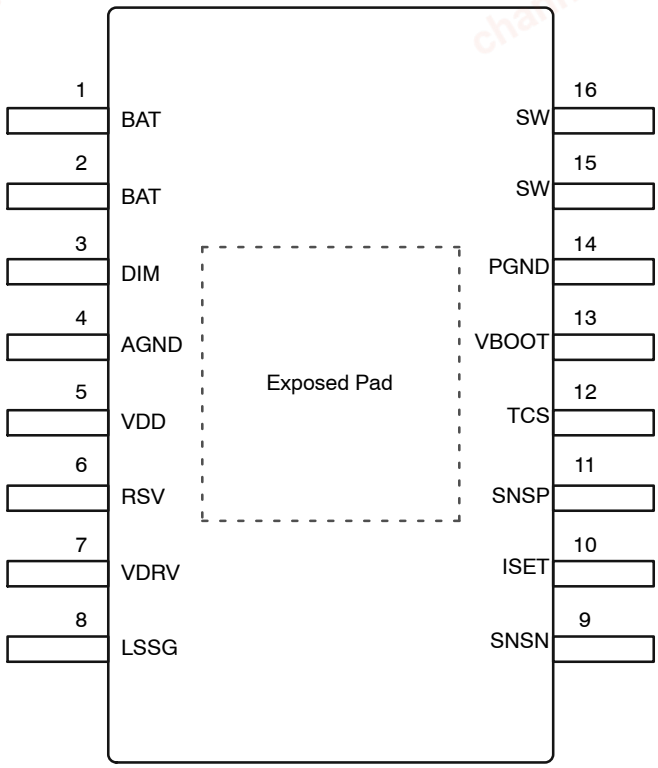

Figure 3. Pin Out (Top View)

Table 1. PIN FUNCTION DESCRIPTION

Number	Name	Description
1, 2	BAT	Input supply voltage, coming from the Battery or ECU, through reverse blocking protection and input Pi filter. Pin 1 and pin 2 must be connected together.
3	DIM	Enable/disable function, including LED current dimming function and error status function.
4	AGND	Must be connected directly to the analog ground plane.
5	VDD	3V3 low dropout output pin. A capacitor must be connected between this pin and ground. Must not be used for external load.
6	RSV	Reserved for production test. Must be connected directly to the analog ground plane in the application.
7	VDRV	VDRV regulator output for the external gate driver. A capacitor must be connected between this pin and ground. Must not be used for external load.
8	LSSG	Gate drive of the boost, low side NMOS.
9	SNSN	Voltage feedback of the current sense, LED side
10	ISET	LED current−encoding resistor connection (RSET connection or VSET voltage).
11	SNSP	Voltage feedback of the current sense, H−Bridge side
12	TCS	Temperature coefficient sensor connection. Compatible with both NTC and PTC sensors.
13	VBOOT	Bootstrap pin.
14	PGND	Power ground.
15, 16	SW	Switching node for the inductor connection. Pin 15 and pin 16 must be connected together.
Exposed pad	ExP	Thermal Pad for power dissipation. Must be connected to the power ground local plane for noise optimization.

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MAXIMUM RATINGS

Pin voltages listed below are referenced to ground plane.

Table 2. MAXIMUM RATINGS

Symbol	Parameter description	Min	Max	Unit
AM_BAT	BAT pin. Main Power Input.	−0.3	45	V
AM_DIM	DIM pin. Signal Input	−20	45	V
AM_RSV	RSV pin Signal Input.	−0.3	3.6	V
AM_VDD	VDD pin. Local Power Supply Output	−0.3	3.6	V
AM_ISET	ISET pin. Signal Input	−0.3	70	V
AM_TCS	TCS pin. Signal Input	−0.3	70	V
AM_VDRV	VDRV pin. Power Output	−0.3	5.5	V
AM_LSSG	LSSG pin. Power Output	−0.3	5.5	V
AM_SW	SW pin. Power Output	−0.3	45	V
AM_VBOOT	VBOOT pin, referring to ground. Power Input	Max of (V_{SW}−0.3,−0.3)	V_{SW}+3.6	V
AM_SNSP	SNSP pin. Signal Input	−0.3	70	V
AM_SNSN	SNSN pin. Signal Input	−0.3	70	V
AM_TS	Storage Temperature Range	−55	150	°C
AM_TJ	Maximum Junction Temperature (Note 1)	−40	P_TJ_OFF	°C
EOS_HBM	ESD Withstand Voltage (Human Body Model)	2		kV
EOS_CDM_CORNER	ESD Withstand Voltage (CDM). BAT, SW, LSSG, SNSN	750		V
EOS_CDM	ESD Withstand Voltage (CDM), all other pins than corners	500		V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The maximum functional operating temperature range can be limited by the IC thermal shutdown: P_TJ_OFF.

RECOMMENDED OPERATING CONDITIONS

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality outside the operating ranges described in this section is not warranted. Operating outside the recommended operating ranges for extended periods of time may lead to a not functional device or affect device reliability. A mission profile is a substantial part of the operation conditions; hence the Customer must contact **onsemi** in order to mutually agree in writing on the allowed missions profile(s) in the application.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter Description	Min	Max	Unit
P_BAT_OP	BAT Range − Operating	P_UVLO_operating	P_OVLO_operating	V
P_BAT_MAX	BAT Range − Full Power	9	P_OVLO_operating	V
P_VOUT	DC to DC VOUT Range	5.6	60	V
P_TA	IC Ambient Temperature Range	−40	125	°C
P_TJ	IC Junction Temperature Range (Notes 2 and 3)	−40	150	°C
P_OUTPUT_POWER	Output Power		20	W
P_IC_POWER	On−chip Power Dissipation with the recommended heatsink performance		2	W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. The parametric characteristics of the circuit are not guaranteed outside the parametric operating junction temperature range.
3. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc. No more than 100 cumulated hours in life time above P_TJ.

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Table 4. THERMAL INFORMATION (Note 4)

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
RTHETA_JC	Junction to exposed pad thermal resistance		3.2		°C/W	

4. Includes also typical solder thickness under the Exposed Pad (EP).

ELECTRICAL CHARACTERISTICS

In the electrical table of this section, the Min and Max Limits apply for ambient temperature from −40°C to 125°C and junction temperature from −40°C to +150°C and for VBAT from 5 V to 21 V unless otherwise specified. Typical values are referenced to T_J = + 25°C, VBAT = 14.0 V.

Table 5. BAT ELECTRICAL CHARACTERISTIC TABLE

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_UVLO_starting	Under−voltage comparator rising edge − BAT rising	7.75	8	8.25	V	
P_UVLO_operating	Under−voltage comparator falling edge − BAT falling			5	V	
P_OVLO_operating	Over−voltage comparator BAT rising edge	20		21	V	
P_OVLO_starting	Over−voltage comparator BAT falling edge	18		19	V	
P_OVLO_hyst	Over−voltage hysteresis, falling	1.5		2.3	V	
P_OVLO_FALL	BAT falling for rearming after an overvoltage		20		ms	
P_BAT_IWAIT	BAT pin Wait current, UVLO <BAT< OVLO no switching DIM=0 or FAULT/STOP modes			8	mA	

Table 6. POWER TREE TABLE

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_VDD	LDO supply voltage, BAT > P_UVLO_operating		3.3		V	(Note 5)
P_VDD_CLAMP	VDD Current limit, BAT > P_UVLO_operating	30	55		mA	
P_C_{VDD}	VDD output capacitance, including derating	2.2		4.7	μF	
P_VDRV	VDRV supply voltage, BAT > P_UVLO_operating		5		V	(Note 5)
P_VDRV_CLAMP	VDRV Current limit, BAT > P_UVLO_operating	40	60		mA	
P_C_{VDRV}	VDRV output capacitance, including derating	2.2		4.7	μF	
P_PORB_R	Power on reset threshold, VDD rising		2.95		V	
P_PORB_F	Power on reset threshold, VDD falling		2.5		V	

5. Loaded up to the minimum clamp value

Table 7. DC−DC CONVERTER TABLE

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_HSS_RON	High side switch resistance from BAT to SW		75		mΩ	
P_LSS_RON	Low side switch resistance from SW to PGND		260		mΩ	
P_IPEAK	IPEAK protection of the inductor		4.5		A	
P_EFFICIENCY1	DC to DC efficiency, buck mode, BAT 14 V, VLED 9 V, 1.5 A		90		%	
P_EFFICIENCY2	DC to DC efficiency, boost mode, BAT 14 V, VLED 44 V, 0.4 A		90		%	
P_EFFICIENCY3	DC to DC efficiency, buck−boost mode, BAT14 V, VLED 13 V, 1 A		90		%	
P_DC_Buck_Max	Max duty cycle in Buck Mode (BAT > VLED), from Buck to Buck−Boost		80		%	
P_DC_Boost_Min	Min duty cycle in Boost Mode (BAT < VLED), from Boost to Buck−Boost		23		%	

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Table 7. DC−DC CONVERTER TABLE (continued)

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_SWITCH_FREQ	DC to DC switching frequency	360	400	440	kHz	
P_FSSMB	Spread Spectrum Modulation Bandwidth, of the SWITCH_FREQ	±5	±6	±10	%	
P_FSSMF	Spread Spectrum Modulation Frequency	11.97	13.3	14.65	kHz	
P_ILED_MAX	Maximum output current − RSET= 715 Ω − no dimming − no derating	1.425	1.5	1.575	A	
P_ILED_MIN	Minimum output current − RSET= 10 kΩ − no dimming − no derating	0.18	0.2	0.22	A	
P_ILEDCLAMP	LED Current de−rating minimum value in case of derating, plateau option 50%		100		mA	
P_ILED_ACCURACY_200	ILED accuracy for a 200 mA programmed current − no dimming (RSET = 10 kΩ)	−10		+10	%	
P_ILED_ACCURACY_1500	ILED accuracy for a 1500 mA programmed current − no dimming _(RSET = 715 Ω)	−5		+5	%	
P_RSENSE	ILED Current sensing resistor value	99	100	101	mΩ	
P_LSSG_PD	LSSG Gate Pull−down impedance − Isink 40 mA	1.5	3	6	Ω	
P_LSSG_PUP	LSSG Gate Pull−up impedance − Isource 40 mA	1.5	3	6	Ω	
P_EXT_LX	Buck Boost inductor value	8	10	12	μH	
P_EXT_C_{BOOT}	Boost strap capacitor. Including DC bias derating	100		220	nF	
P_EXT_ISET	ISET capacitor for EMC	0.1		2.2	μF	
P_EXT_C_{BAT}	BAT pin decoupling capacitor. Including DC bias derating	1	2	4.7	μF	
P_EXT_C_{VOUT}	Vout pin decoupling capacitor. Including DC bias derating	1	2	4.7	μF	
P_EXT_CIN_INPUT_PI	Cin of the input Pi Filter	4.7		10	μF	
P_EXT_COUT_INPUT_PI	Cout of the input Pi Filter	10		30	μF	
P_EXT_LX_INPUT_PI	Inductor of the input Pi Filter	2.2		3.3	μH	
P_EXT_CIN_OUTPUT_PI	Cin of the output Pi Filter	2.2		2x4.7	μF	
P_EXT_COUT_OUTPUT_PI	Cout of the output Pi Filter	0.680		1	μF	
P_EXT_LX_OUTPUT_PI	Inductor of the output Pi Filter	2.2		3.3	μH	

Table 8. DIM TABLE

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_DIM_IN_DIG	Input duty cycle range, digital mode	1		100	%	(Note 6)
P_DIM_OUT_DIG	Output duty cycle range, digital mode	1		100	%	
P_DIM_FREQ	Valid frequency on DIM	80		600	Hz	
P_DIM_FREQ_IN_MIN_HYST	Hysteresis of the minimum valid frequency	−1	−2	−3	%	
P_DIM_FREQ_ACC	Accuracy of the frequency thresholds			10	%	
P_DIM_FREQ_IN_MAX_HYST	Hysteresis of the maximum valid frequency	1	2	3	%	
P_DIM_FREQ_OUT	Output frequency of the DIM reconstruction (from DIM input frequency)	360	400	440	Hz	
P_DIM_DC_ACC	DIM dimming reconstruction accuracy based on DCDC Switching Activity Ratio. From DIM in to LSSG or SW.	−1		1	%	(Note 7)
P_DIM_DETECT	Detection time of a valid DIM.		25	30	ms	
P_DIM_REMOVAL	Detection time of DIM removal	80	90	100	ms	

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Table 8. DIM TABLE (continued)

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_FULL_STARTUP	DC to DC output start up time from valid BAT applied – Automatic mode / Direct turn ON, P_FADING_TIME=0	20	25	30	ms	
P_DIM_SLOPE	Total time constant of the ILED setting from dimming mode to normal mode		125		ms	
P_DIM_Vih	DIM pin high logic level (4.5 V overdrive)	3.5			V	(Note 8)
P_DIM_Vil	DIM pin low logic level			2	V	
P_DIM_IQ	No LED Error P_UVLO_operating < BAT < P_OVLO_operating, DIM valid Referring to ILED derating summary table	10		14	mA	
P_DIM_IFAULT	LED Error P_UVLO_operating < BAT < P_OVLO_operating, DIM valid No LED Error BAT < P_UVLO_operating. DIM valid Referring to Protection and error management summary table	0.4		0.7	mA	

6. An input duty cycle on DIM pin over 98 % is considered as a 100 % output duty cycle.
7. P_DIM_DC_ACC represents the digital reconstruction of the DIM input duty cycle. The ILED average and P_FULL_STARTUP depend on the component choice, like Schottky leakages and/or lower capacitor values. Referring to Ta max 105°C
8. A 4.5 V overdrive on DIM slope must be respected to not create additional delay on the PWM reconstruction.

Table 9. RSET PARAMETRIC TABLE

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_RSET_RANGE	RSET pull down resistor valid range	0.4		15	kΩ	
P_RSET_RANGE_ACC	RSET range accuracy			10	%	
P_TIMEOUT_RSET	Timeout for an out−of−range RCOD value			100	ms	
P_SET_RSET	RSET reading duration from an UVLO rising edge	4.5	5	5.5	s	

Table 10. LED CURRENT CONTROL WITH LOW VBAT TABLE

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_BAT_LOW	Poor BAT voltage (ADC reading)	8.7	9	9.3	V	
P_DEB_BAT	VBAT time before derating, when VBAT < P_BAT_LOW	7	10	13	ms	
P_DTC_BAT	ILED derating time constant in case of VBAT < P_BAT_LOW, rising and falling		256		ms	
P_ILED_BAT_STEP	Step to Step Current De−rating granularity			2.5	%	

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Table 11. IC THERMAL THRESHOLDS TABLE

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_TJWARN	Warning threshold for a LED Current de−rating starting value		130		°C	
P_TJ_HYST	Rearming threshold after a direct TSD (no derating)		135		°C	
P_TJ_REG	LED Current de−rating end value (ILED = P_ILED_TJILED over this threshold)		150		°C	
P_TJ_OFF	Protection for the maximum Junction Temperature. DC to DC is turned off over this value.		170		°C	
P_ILED_TJ	End de−rating output current ratio, percentage of the ISET		60		%	
P_TJ_FALL	Response time + timer, falling for rearming		20		ms	
P_ILED_TJ_STEP	Step to Step Current De−rating ratio		1.3	2.5	%	

Table 12. THERMAL COEFFICIENT SENSOR PIN TABLES

Symbol	Parameter	Min	Typ	Max	Unit	Notes
P_VTCS_{START}	Derating start voltage on TCS		0.57		* V_{VDD}	
P_VTCS_{END}	Derating end voltage on TCS		0.39		* V_{VDD}	
P_ISTOP	Relative to I_{SET}, Default Option		60		%	
P_TFAULT	Timer before an error is reported on DIM pin	20	30	100	ms	
P_TDER_SLOPE	Derating slope in percentage of ILED	0.15	0.2	0.25	%/ms	
P_TCS_PD	Internal pull down for pin floating event, measured at 1 V	0.3		2	MΩ	

Table 13. SNSP AND SNSN THRESHOLDS TABLE

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
P_VOUT_L	LED under voltage threshold (LED string shorted), falling		1.5		V	
P_VOUT_SU	Start up threshold, Current sense feedback, rising		1.825		V	
P_VOUT_L_IDLE_SU	Blanking time where the VLED low comparator is not activated during start up, from switching activity		10		ms	
P_VOUT_H	LED over voltage threshold (LED string opened), rising	62	64	66	V	
P_SNSPN_OPEN	Of the programmed ICOD. The comparator is debounced.	135		195	%	
P_SNSPN_SHORT	Differential voltage of the VLED N and P pins. The comparator is debounced.		5		mV	
P_SNSPN_SHORT_SU	Blanking time at start up, from switching activity (sum of Ton in DIM dimming case)		8		ms	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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DETAILED OPERATING DESCRIPTION

BAT ELECTRICAL DESCRIPTION

For a proper operation and a safe start−up sequence, an under−voltage comparator senses the BAT pin. Its own wide hysteresis protects against slow battery rising and falling behavior.

An overvoltage comparator turns off the DC−to−DC controller in case of a too high or inappropriate battery voltage is applied. The IC starts again when the input voltage retrieves to normal level, below the OVLO_operating minus hysteresis.

POWER TREE

The single channel LED driver is supplied from the BAT pin.

BAT can be supplied from the car battery, for instance by a SmartFET. Two local supplies are generated from BAT: VDD and VDRV.

VDD supplies most of the internal circuitry and is decoupled with the CVDD capacitor. VDRV supplies the driver of the external low side Boost switch and is decoupled with the CVDRV capacitor.

No external components or system (except the respective decoupling capacitors and potential TCS pull−up resistor) are allowed to be connected to VDD and VDRV pins.

DC−DC BUCK – BOOST CONVERTER OPERATION

The NCV78514 is powered from an automotive battery and operates with a fixed switching frequency SWITCH_FREQ, DIM mode (duty cycle modulation).

It is designed to supply a constant current between ILED_MAX and ILED_MIN into a single LED string, programmed by a pull−down resistor connected on ISET pin.

The synchronous Buck integrates the high side and the low side switch. Whereas the asynchronous boost utilizes an external low side N−MOSFET and a Schottky diode.

The constant LED current is achieved by sensing peak current through integrated high side switch.

The sensed peak current is compared to voltage over the RSENSE resistor, which is in series with LED string.

The output voltage varies with number of LEDs in series and programmed output current.

When the input voltage is well above the differential output voltage between LED+ and LED − (Voltage across the LEDs), the DC−DC converter is in buck mode (BAT > VLED).

Consequently, the LSSG pin used to drive the low side switch in boost mode, is then deactivated (retained to GND).

Upon the buck operation, integrated high side and low side switches, transfer the energy from the input to the inductor. Their resistances are represented by the P_HSS_RON and P_LSS_RON parameters. The high side switch is driven from bootstrap capacitor Cboot (HSS gate voltage = BAT + VDD − Vf).

During the ton time, HSS is turned on, and LSS is made non−conductive. The peak current is tracked during this phase. The conductivity of integrated switches is inverted during the toff phase. Behaving like a synchronous buck converter until the maximum duty cycle is reached (DC_Buck_Max).

In case of the BAT is close to the output voltage, the IC enters in the 4−phases cycle, called the Buck−Boost mode. The LSSG is then re−activated and the 3 switches (both integrated switches and external N−MOSFET) will be alternatively controlled, where the sequence depends on BAT voltage in reference to VLED.

During boost phase, LSS is open and HSS is closed. Allowing to continuously track the Inductor IPEAK current.

The ton boost phase (inductor current increasing phase) is when external N−MOSFET is on, and no current crosses the schottky diode (VLED > schottky anode voltage).

The external N−MOSFET is made non−conductive during the inductor discharge phase (toff).

The inductor is protected by an IPEAK protection. The current is measured internally, through the high side switch. The IPEAK is set at P_IPEAK. The maximum output power will be limited in case of IPEAK event. The output power limitation due to IPEAK protection mainly occurs in Boost mode and in case of Battery cranking.

In case of IPEAK event, no error is reported to DIM pin.

SPREAD SPECTRUM FREQUENCY MODULATION

Spread spectrum is a technique using frequency modulation to achieve lower peak electromagnetic interference (EMI).

It is an elegant and complementary solution with filtering and shielding techniques to improve EMC performance.

In order to “spread” the peak to broader band, the internal oscillator frequency is modulated, decreasing the peak amplitude at the center frequency and at the frequency’s harmonics. This results in lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators.

The adopted spread spectrum technic results in double peak triangle modulation, on FSSMB frequency range, and FSSMB frequency modulation.

DIM PIN – DIMMING DESCRIPTION

The average current through the LEDs can be reduced in a dimming fashion, with an external signal applied on DIM pin.

The input signal frequency at DIM can be freely chosen in the DIM_FREQ frequency range while the output frequency is constant at FREQ_OUT.

The input signal is validated by the device before actual dimming is applied on LED string (two periods).

An input frequency outside the DIM_FREQ_IN range is considered as no DIM available (or disappearance) thus the LED string is maintained off (or switched off).

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Digital Dimming

A first dimming functionality is achieved by applying a square input signal on the DIM pin.

The input duty cycle range is valid in the DIM_DC_IN range and is reconstructed on the output with an identical duty cycle (DIM_DC_OUT).

A duty cycle above 98% is considered as a 100 % duty cycle. The current into the LEDs is then no more dimmed, and set to the DC current, programmed by RSET.

As soon as the part achieves 100 % duty cycle, the part enters in automatic mode.

At start up, the NCV78514 starts after the second identified valid duty cycle.

A duty cycle change, to a higher or lower value, makes a linear change of the LED current. The time to reach new current is proportional to difference of new and previous duty cycle and is described below.

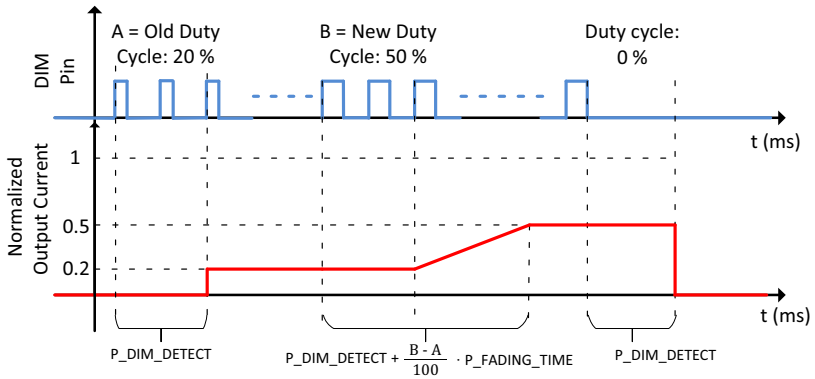

Figure 4. ILED Setting Slope in Digital Dimming Mode

Automatic Fading

Automatic fading mode is activated if the voltage applied to PWM pin is not alternating during the P_DIM_DETECT period. When the PWM pin is held active for this period, the output current will reach programmed value after P_FADING_TIME and the current rise will be logarithmic. When logic 0 is applied for another period of P_DIM_DETECT, the output current will start to decline to in logarithmic manner. Zero output current will be reached after P_FADING_TIME.

Remark: depending on the output conditions (I.E low current level, high LED number), the small duty cycle values can create long turn on time of the LED string.

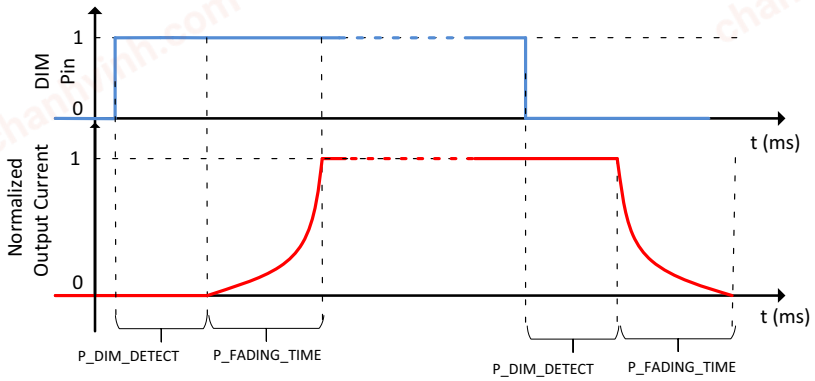

Figure 5. ILED Setting Slope, Automatic Fading Mode

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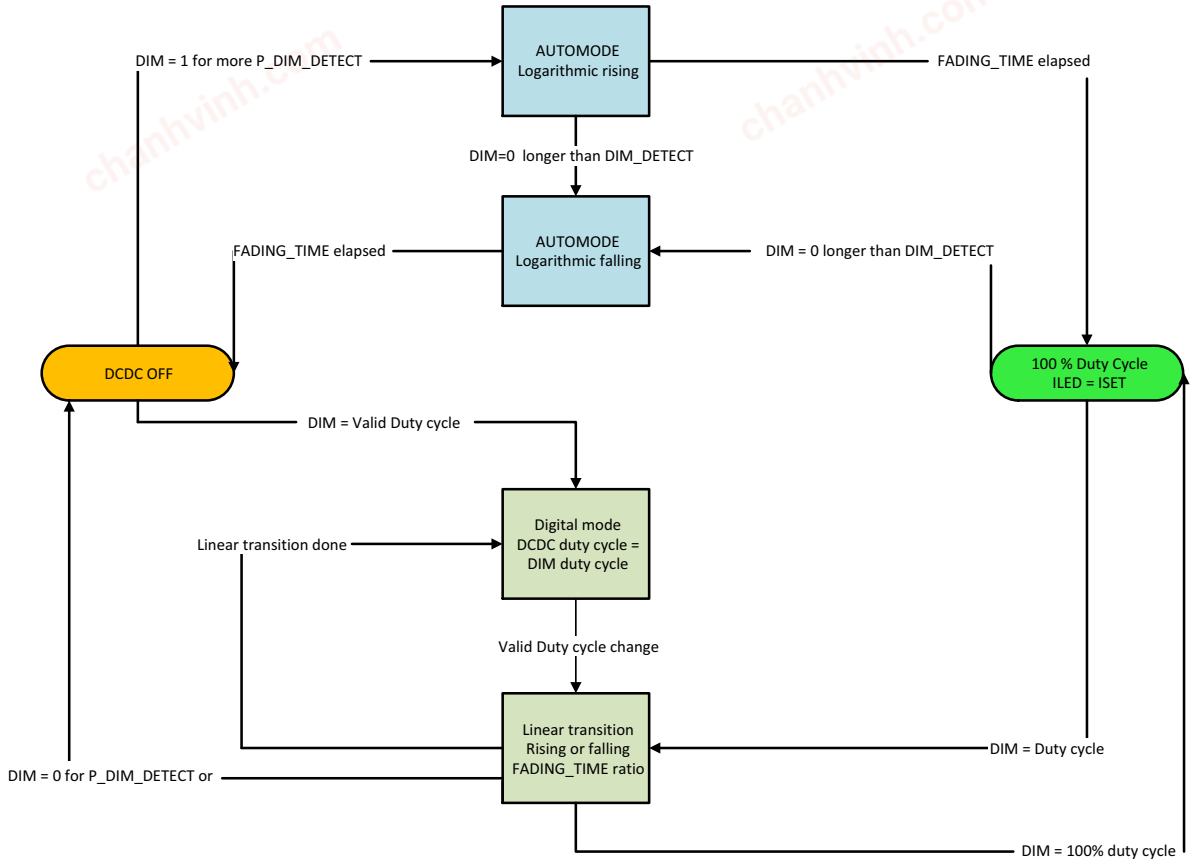

Figure 6. Dimming Modes Functional Flow Diagram

Important remark:

For EMC conductive emission performance, Pi filters must be placed on:

- BAT line
- and recommended on the output of the DCDC converter (after the Rsense resistor), in case of separate module application.

The sizing of the Pi filters (please see the bill of material) is done to achieve a good stability of the Buck − Boost.

Any other component choice will have an impact on the turn on time in dimming mode, as for the duty cycle accuracy (DIM_DC_ACC) or overall stability.

The turn on time in Normal Mode and DIM Mode are respectively FULL_STARTUP and DIMMING_STARTUP.

Upon removal of the DIM signal, the LED current is turned off only after a delay of DIM_MISS.

LED CURRENT SETTING

RSET Pull Down

The LED current is set through the ISET pin, with a pull−down resistor.

Granularity of the current setting is achieved though the resistor series choice and tolerance of them.

$$\text{ILED (A)} = \frac{1000\ (\Omega \cdot \text{A})}{\text{RSET}\ (\Omega)} + 0.1\ (\text{A}) \qquad \text{(eq. 1)}$$

For example, RSET = 1 kΩ => 1.1 A.

The identification of the RSET is initiated by BAT > P_UVLO_STARTING, rising edge.

During IC's wake up time, a first read of RSET is performed in order to provide current into LEDs within the P_FULL_STARTUP. The RSET is continuously done during P_SET_RSET to achieve the more accurate value in this time frame. After this period, a value out of the P_RSET_RANGE, longer than P_TIMEOUT_RSET is considered as an out of range, and LED current is turned off. A new power on reset sequence is then required.

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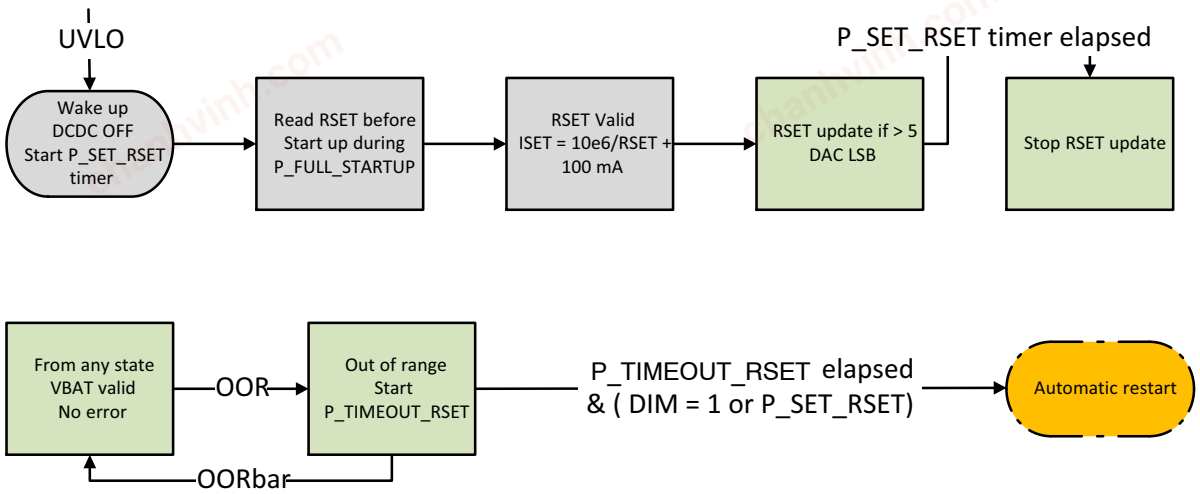

Figure 7. Flow Diagram of the R_COD Identification

LED CURRENT DERATING MANAGEMENT

To limit overheating of the IC an ILED current de−rating mechanism is managed by the controller itself. The different de−rate mechanisms are described below.

When two or more derating mechanisms are active, the one which derates more is applied to ILED current.

Both BAT pin, TCS pin and internal junction temperature sensor are monitored by integrated ADC.

Battery cranking

In case of a low Battery voltage (BAT pin), the LED current is gradually decreased. In order to avoid glare and flickering, the duration of the current derating is set at P_DTC_BAT. A violent battery crancking, can trigger Ipeak protection. The input current and output power are then limited by the IPEAK clamp. The current derating will take hand if the BAT voltage continues to decrease down to the undervoltage comparator. No error is reported on DIM pin in case of IPEAK event

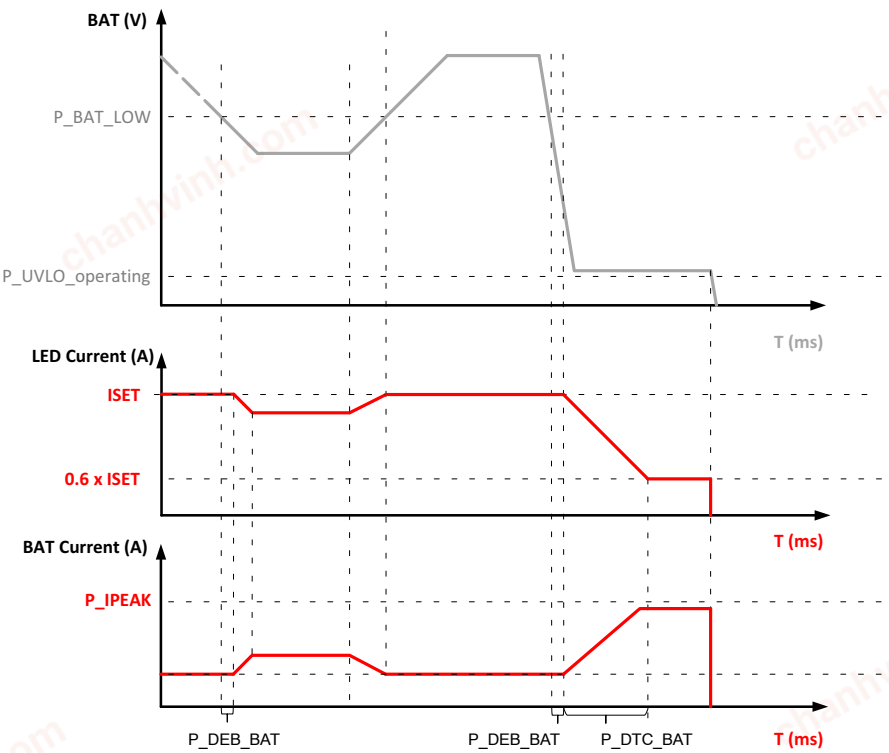

Figure 8. Current Derating, Battery Voltage

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When VBAT falls under P_BAT_LOW, ILED is derated following the formula with a minimum of P_ILED_CLAMP value:

$$ILED = ISET \times \frac{(BAT + 1)}{10} \quad \text{(eq. 2)}$$

IC Temperature Monitoring

The junction temperature of the IC is monitored thanks to an internal thermometer.

In the situation where the junction temperature exceeds gradually the P_TJWARN, a current de−rating is immediately applied to the LED current, with a controlled slope upon P_DTC_BAT timing.

If the junction temperature continues to increase and crosses the P_TJ_REG threshold, the LED current is maintained around P_ILED_TJ.

If the IC temperature exceeds the P_TJ_OFF, the current into the LED is stopped, and an error is reported on DIM pin. A power on reset is required to reset the error.

In case of a very fast temperature increase (no derating is engaged) and P_TJ_OFF is crossed, the LED string will be rearmed when the junction temperature falls below the P_TJ_HYST threshold, and the error reporting on DIM pin is stopped.

The current derating and management are defined as following:

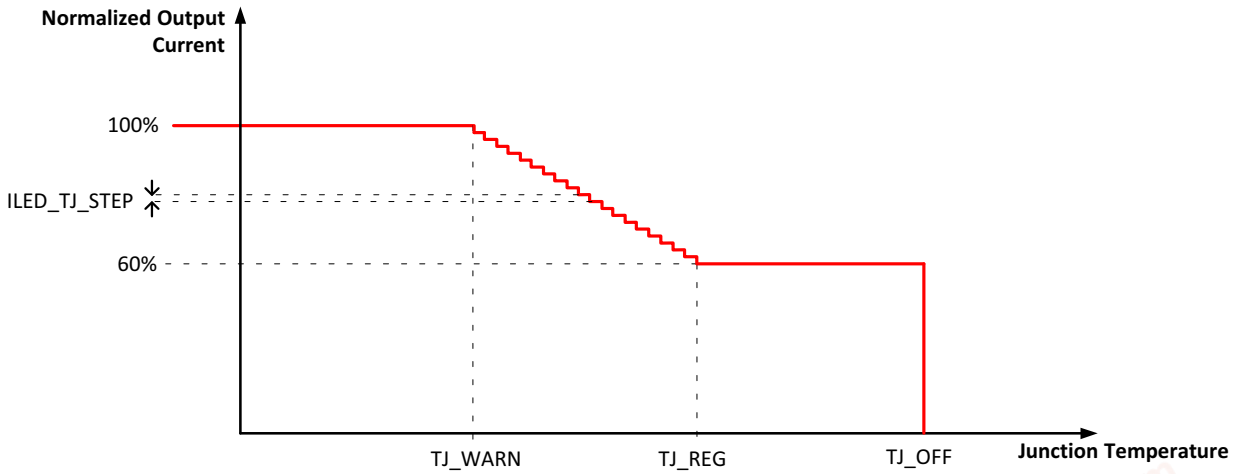

Figure 9. LED Current Derating versus Junction Temperature

LED String Temperature Monitoring

A derating is also applied to ISET in case the LED string temperature is too high, and a temperature coefficient resistor is used (same PCB or separate LED module).

Both negative temperature coefficient (NTC) or positive temperature coefficient (PTC) can be used with a pull−up or pull−down resistor respectively.

In case of a module approach, NTC is recommended to save one wire on the connector between the controller and the Led module.

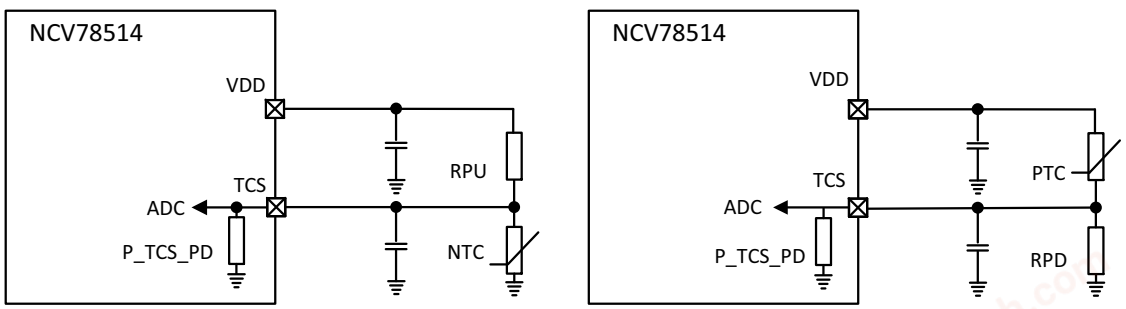

Figure 10. NTC (left side) and PTC (right side) Connection Options

The sampling period of the temperature sensor is defined by the sampling rate of the internal ADC.

RPUP and RNTC (or RPD and RPTC) ratio is selected to start the ILED derating when V_{TCS} is crossing $V_{TCSTART}$.

During the derating time frame, AR_P_DER_SLOPE is applied on the LED current to avoid glare or flickering effect.

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PTC choice makes the derating more direct due to the exponential intrinsic variation of this resistor type. The derating slew rate is then blended with the TDISDER slope control.

For safety reasons, an internal pull−down resistor is connected between TCS pin and and GND. Indeed, in case of a floating pin, the TCS pin is automatically tied to GND, and a maximum derating is applied on the LED current.

$$RPD = RPTC@85°C * \left(\frac{VTCS_{START}}{VDD - VTCS_{START}}\right) \approx 6250\ \Omega \quad \text{(eq. 3)}$$

Temperature calculation at ISTOP value (60% of ISET by default).

$$RPTC@END = RPD(6250\ \Omega) * \left(\frac{VTCS_{START}}{VDD - VTCS_{START}}\right) = 9775\ \Omega \approx 90°C \text{ with\&a PRF18BE471} \quad \text{(eq. 4)}$$

Because the PTC value changes by 50% with 5°C temperature difference, the same temperature difference creates larger change of output current than NTC.

If the LED temperature stays excessive longer than TFAULT timer, with a maximum derating applied, a fault is reported on DIM pin.

Derating example with a positive temperature coefficient sensor.

PTC ref: PRF18BE471QS5RB (470 Ω @ 25 °C, 4700 Ω @ 85°C)

Derating example with a negative temperature coefficient sensor: NCG18XH103F0SRB

$$RPU = RNTC@85°C * \left(\frac{VDD - VTCS_{start}}{VTCS_{START}}\right) \approx 1100\ \Omega \quad \text{(eq. 5)}$$

Temperature calculation at ISTOP value (60% of ISET by default).

$$RNTC@END = RPD(1100\ \Omega) * \left(\frac{VDD - VTCS_{START}}{VTCS_{START}}\right) = 698\ \Omega \approx 115°C \text{ with\&a NCG18XH103} \quad \text{(eq. 6)}$$

If unused, TCS pin is to be connected with an external resistor divider, to set TCS pin voltage to half of VLDO.

In case both junction temperature and LED temperature required current derating, the current is controlled by the thermal sensor (NTC/PTC or TJ) which requires the higher current derating (whichever results in lower LED current).

Optional Behavior: STOP Over $VTCS_{END}$ Threshold

Optionally, it is proposed to the end user to reshape the derating profile by turning off the DCDC in case of VTCS_END threshold is exceeded longer than TSTOP. If so, the profile is expressed below.

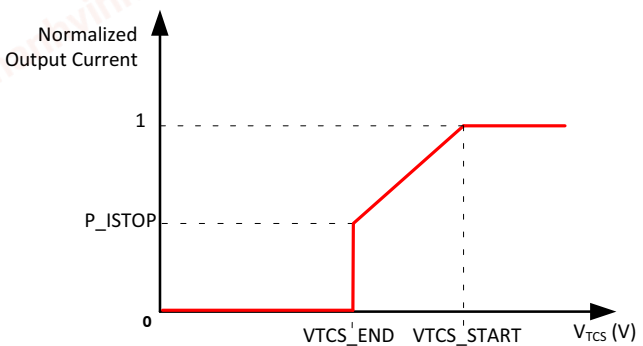

Figure 11. Current Derating TCS Voltage

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PROTECTIONS AND ERROR MANAGEMENT

Due to several embedded protection systems, the NCV78514 is able to manage different errors and fault types.

Depending on the error, the controller informs the system through the DIM pin by changing current consumption.

The different errors types are described below.

Overvoltage

When BAT pin voltage is larger than P_OVLO_operating threshold, the light is turned off or maintained off. An error is reported to DIM pin in this case.

To retrieve normal operation, the BAT must be below OVLO operating minus hysteresis. Error is not reported on DIM pin, when BAT voltage falls below OVLO minus hysteresis.

LED String Error

The device is able to detect several faults on the LED string, through the SNSP and SNSN sense pins.

For the two error situations described below, the DC to DC controller will instantaneously turn off the LED current, and report error via DIM pin.

The first situation is when anode of LED string shorts to cathode, or to GND. These events are detected, when SNSN voltage drops below P_VOUT_L.

During the turn on sequence of the DC DC converter, this protection mechanism is deactivated during P_VOUT_L_IDLE_SU in order to avoid unexpected fault detection. In case of an error is detected and the part goes to error mode, a new start up sequence is started. The brightness is recovered as soon as the error disappear.

The second situation occurs, when LED string opens.

In this case the SNSN will cross the P_VOUT_H threshold due to the boost mode. An auto−rearming is started as soon as the output capacitor is fully discharged (below UV out threshold).

A LED string error is reported via DIM pin.

The auto−rearming sequence is running as long as the led string is opened.

RSET Out of Range Value

An out of range RSET is considered as an error (See Error Table) if RSET < 400 Ω, RSET > 15 kΩ for longer than P_TIMEOUT_RSET.

This out of range detection acts after the P_SET_RSET start up timer is elapsed or if the LEDs are already ON.

The out of range error is reported via DIM pin. The system automatically rearms until the RSET recovers a valid value.

Feedback Loop Issue

SNSP and SNSN pins are used for the regulation loop. A physical error making the pins shorted or opened, latch an error and the LED current is stopped.

DIM Pin Status Function

In case of some specific errors, the DIM pin is used as a status pin.

The current consumption on the pin will switch from P_DIM_IQ to P_DIM_IFAULT input current consumption, in case of error.

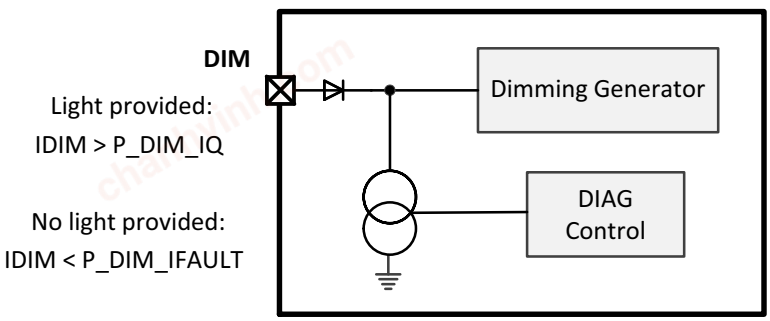

Figure 12. DIM Pin, Diagnostic Current Sink

Depending on the kind of error, the output may be turned off, requiring a BAT removal to reset the error mode condition.

At power up, the P_DIM_IQ is activated when P_VOUT_L is reached to make sure the current is present into the LED string.

The P_DIM_IQ is de−activated on UVLO, falling edge.

The different errors are described in the below table.

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Table 14. ILED DERATING SUMMARY TABLE

ILED Derating List	Reset	DIM Current Sink	Output State
IC over temperature (Warning)	–	> P_DIM_IQ	ILED Derated
Low BAT voltage	–	> P_DIM_IQ	ILED Derated following (BAT +1)/10 rule
PTC or NTC Over temperature (ILED < ISTOP)		> P_DIM_IQ	ILED Derate
Inductor I PEAK	–	> P_DIM_IQ	ON but limited power

Table 15. PROTECTIONS AND ERROR MANAGEMENT SUMMARY TABLE

Protections and Errors List	Reset	DIM Current Sink	Output State
Overvoltage	Comp. Hysteresis	< P_DIM_IFAULT	LED OFF
BAT < UVLO	Comp Hysteresis	< P_DIM_IFAULT	LED OFF
IC over temperature (TJ_OFF)	Comp. Hysteresis	< P_DIM_IFAULT	LED OFF
IC over temperature (TJ_OFF) – 40 % ILED derate	BAT POR	< P_DIM_IFAULT	LED OFF
ILED = ISTOP more than TFAULT	BAT POR	< P_DIM_IFAULT	LED OFF
LED + shorted to GND or LED –	BAT POR	< P_DIM_IFAULT	LED OFF
LED + string opened	BAT POR	< P_DIM_IFAULT	LED OFF
SNS P or N opened	BAT POR	< P_DIM_IFAULT	LED OFF
SNS P and N shorted	BAT POR	< P_DIM_IFAULT	LED OFF
RSET out of range	Auto restart	< P_DIM_IFAULT	LED OFF

Table 16. TIMING TABLE SUMMARY

Parameter	Timings
VREG_OK	No debounce, 2 μs response time
VREF_OK	No debounce, 2 μs response time
VDRV_OK	No debounce, 2 μs response time
UVLO	No debounce, 2 μs response time, Functional State Machine. Synchro rise & fall
OVLO	No debounce, 2 μs response time, Functional State Machine. Falling + 20 ms FAULT state timer
TSD	No debounce, 2 μs response time, Functional State Machine. Falling + 20 ms FAULT state timer
VLED H	Debounce 8 μs rising
VLED L	Debounce 5 ms after bob_running. Debounce 8 μs in running mode.
SNSP&N opened	Debounce 150 μs in running mode.
SNSP&N shorted	Blanking 8 ms after bob_running. Debounce 150 μs in running mode.
RSET OOR	90 ms
BAT	10 ms before derating
BAT derating	256 ms (de)rating slope
PTC/NTC derating	256 ms (de)rating slope
DIM slope	P_DIM_SLOPE (Option)
IC temp	Direct derating

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MAIN FUNCTIONAL STATE MACHINE

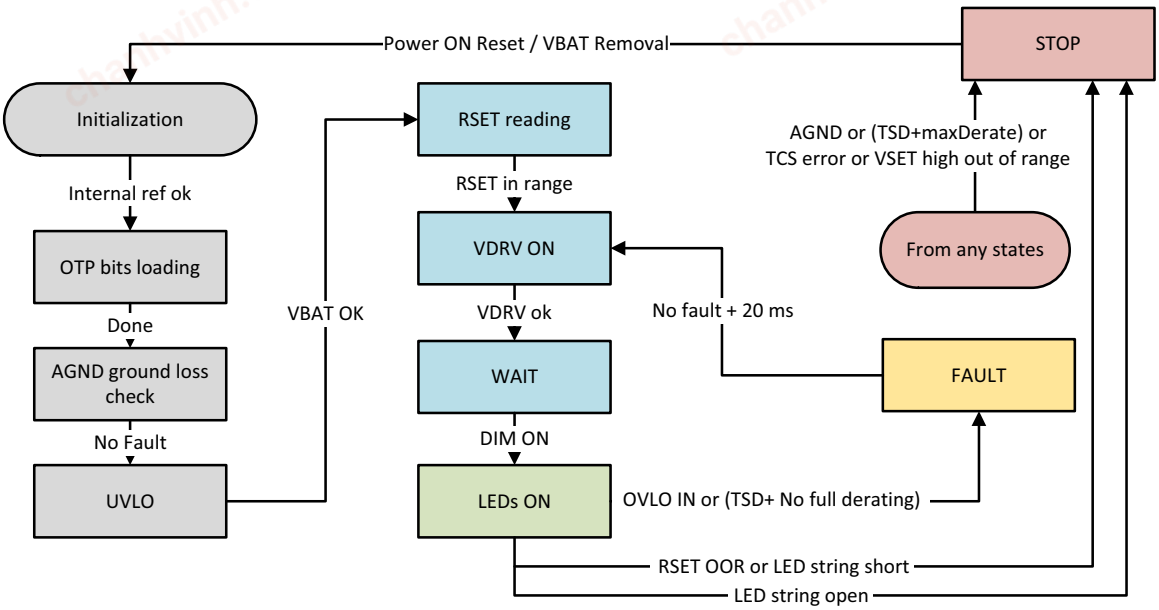

Figure 13. Functional State Machine

COMPONENT LEVEL ELECTROMAGNETIC COMPATIBILITY (EMC)

EMC is a critical item in automotive systems. **onsemi** commits to cooperate technically with the customer to target to build an integrated circuit which is sufficiently EMC−robust in the application environment of the customer.

To make the application successful for EMC, following items need to be taken into account, explicitly, during the concept phase:

- **onsemi** is specialized in IC design and IC manufacturing, but cannot be considered as expert in the automotive IC−application. The know how on application−level−EMC needs to be provided by the customer.
- The customer needs to inform **onsemi** explicitly during the concept phase about any EMC item which is considered as critical for the application and which may be of importance for the IC design.
  - ♦ If the customer is aware about any potential particular EMC marginalities or any potential EMC issues – for example from experience with previous generations of the particular application – , which may have an impact on the IC design, they need to inform **onsemi** explicitly (beyond general wordings or general frame agreements) during the concept phase about the associated EMC risks.
  - ♦ In case there are particular EMC requirements embedded in the IC requirement spec, these need to be explicitly flagged by the customer, discussed explicitly with **onsemi**, and mutually agreed during the concept phase.
  - ♦ EMC items which turn out to be critical in a later phase of the project and have impact on the IC design cannot be considered as implicitly agreed if they have not been explicitly discussed and documented in writing (somehow) during the concept phase.
- Proposals for solutions in the IC design to address the critical EMC items for the application need to be discussed explicitly and documented in writing during the concept phase.
- It needs to be well understood that external components may eventually be necessary to meet the application's EMC requirements.
  - ♦ In case of lack of discussion or documentation during the concept phase of an item which turns out later to be EMC−critical, it cannot be implicitly assumed that the IC can meet all application−level−EMC−requirements without the help of external components.
- For proper design and validation by **onsemi**, it is important that realistic "conductive" EMC performance targets are agreed during the concept phase.
  - ♦ On IC−level, only conductive requirements (DPI levels for susceptibility, emission levels to be verified with conductive 150 Ohm method – ref. IEC−62132−4/IEC−61967−4) can be taken into account for the IC design by **onsemi**.

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Application level EMC performance will depend on the use of the IC (ASIC) component in an application environment:

- The influence of the application environment is typically caused by or related to (but not limited to) the board design, values and tolerances of external components, presence of external non−linear elements, size, housing, wire harness and the variations of all these over different applications.
  - For example, EMC signals disturbing directly within the signal band of normal operation cannot be distinguished by the IC from normal operating signals.
- Therefore, **onsemi** cannot take responsibility on application level EMC testing, application EMC performances or application solutions for EMC.
- **onsemi** is willing to cooperate with the customer to find root causes for application level EMC issues, if the necessary information is provided to document that a potential root−cause for application level EMC issues may be in the ASIC. A potential correction in the ASIC itself for an application level EMC issue (if feasible) will need to follow an agreed change procedure.

Remark: please refer to the application schematic for recommended components.

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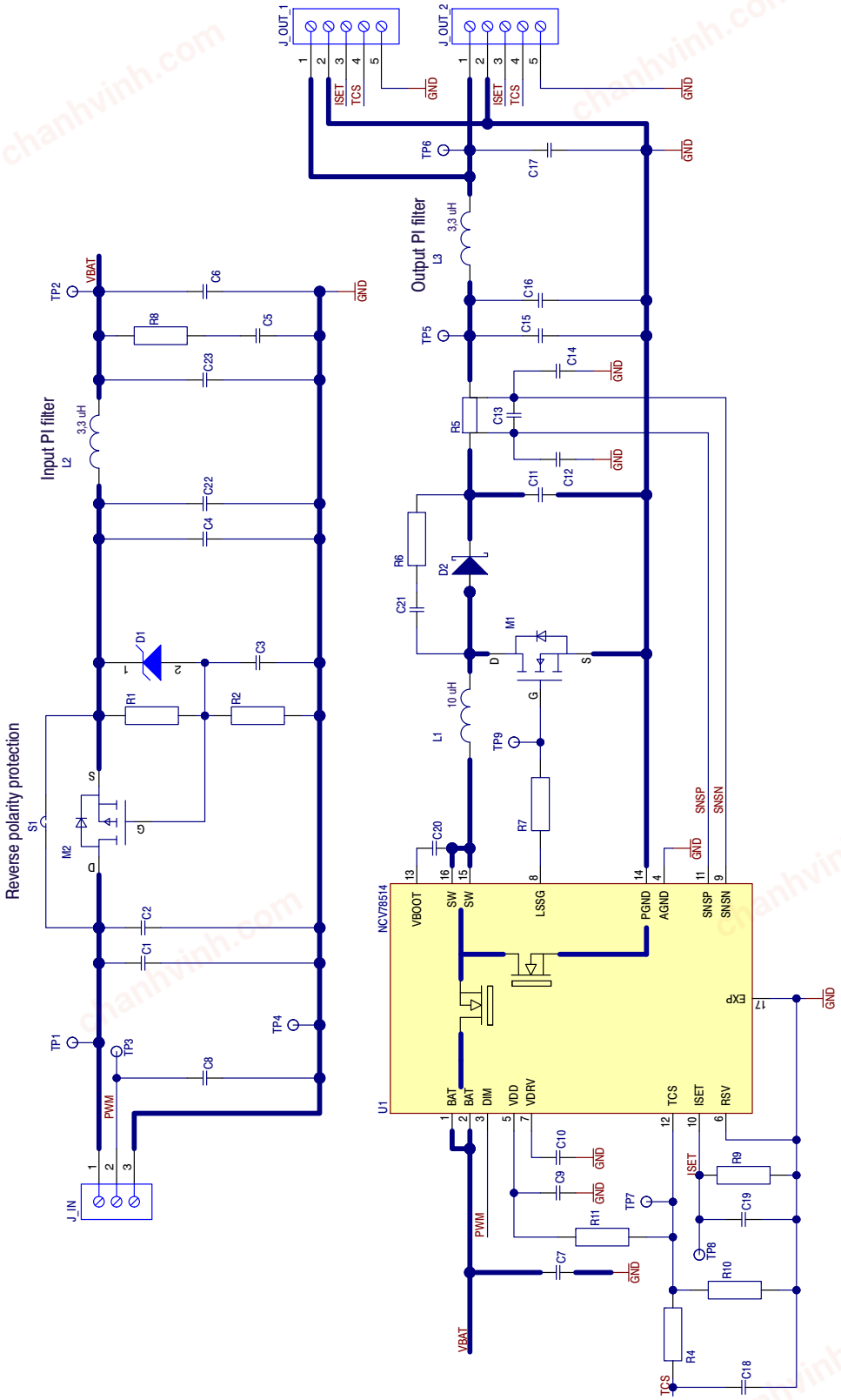

Figure 14. Application Board Schematic

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Table 17. BILL OF MATERIAL

Reference	Manufacturer	Manufacturer Reference	Value
C1	Murata	GCJ188R72A104KA01D	100 nF
C2	Murata	GCM32EL8EH106KA07	10 μF
C3	Murata	GCJ188R72A104KA01D	100 nF
C4	Murata	GCM32EL8EH106KA07	10 μF
C5	Murata	GCM32EL8EH106KA07	10 μF
C6	Murata	GCM32EL8EH106KA07	10 μF
C7	Murata	GCJ32DC72A475KE01L	4.7 μF
C8	Murata	GCM21BC72A105KE36L	1 μF
C9	Murata	GCM21BR71C475KA73L	4.7 μF
C10	Murata	GCM21BR71C475KA73L	4.7 μF
C11	Murata	GCJ32DC72A475KE01L	4.7 μF
C12	Murata	GCJ188R72A104KA01D	100 nF
C13	Murata	GCJ188R72A104KA01D	100 nF
C14	Murata	GCJ188R72A104KA01D	100 nF
C15	Murata	GCJ32DC72A475KE01L	4.7 μF
C16	Murata	GCJ32DC72A475KE01L	4.7 μF
C17	Murata	GCM21BC72A105KE36L	1 μF
C18	Murata	GCJ188R72A104KA01D	100 nF
C19	Murata	GCJ188R72A104KA01D	100 nF
C20	Murata	GCJ188R72A104KA01D	100 nF
C21	Murata	GCJ188R72A102KA01	1 nF
C22	Murata	GCJ188R72A104KA01D	100 nF
C23	Murata	GCJ188R72A104KA01D	100 nF
D1	**onsemi**	MM5Z20VT1	MM5Z15VT1G
D2	**onsemi**	NRVTS8100PFST3G	NRVTS8100PFST3G
M2	**onsemi**	NVTFS5116PLT	NVTFS5116PLTWG
U1	**onsemi**	NCV78514	NCV78514
M1	**onsemi**	NVTFS6H860NL	NVTFS6H860NL
L1	TDK	SPM7054VT − 100M−D	10 μH
L2	TDK	SPM4030VT−3R3−D	3.3 μH
L3	TDK	SPM4030VT−3R3−D	3.3 μH
R1	Vishay	MCT06030C2002FP5	20 kΩ
R2	Vishay	MCT06030C1002FP5	10 kΩ
R4	Vishay	MCT06030Z0000ZP5	0R − Optional
R5	Susumu	RL1632R−R100−F	R100
R6	Vishay	MCT0603PD1009DP5	100R − Optional
R7	Vishay	MCT06030Z0000ZP5	0R − Optional
R8	Vishay	MCT06030Z0000ZP5	0R − Optional
R9	Vishay	MCT06030Z0000ZP5	0R − Module Option
R10	Vishay	MCT06030Z0000ZP5	0R − NTC/PTC
R11	Vishay	MCT06030Z0000ZP5	0R − NTC/PTC
J_IN	Wurth	691709710303	Wurth Header 3
J_OUT_1	Molex	502352−0500	Molex Header 5
J_OUT_2	Wurth	691709710305	Wurth Header 5

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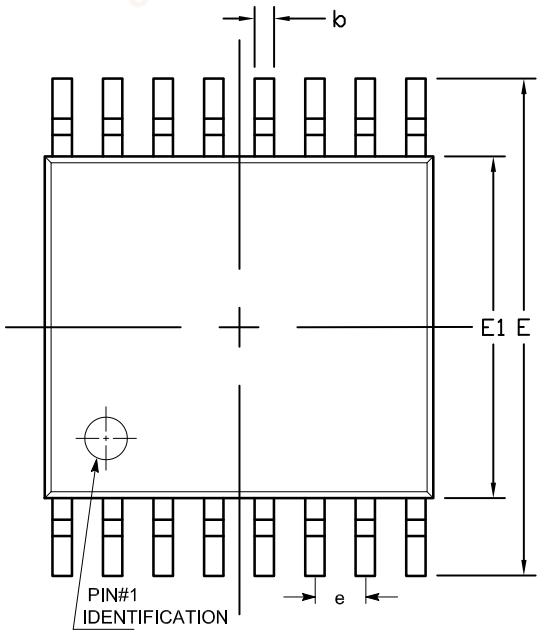
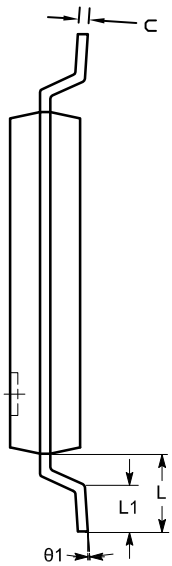
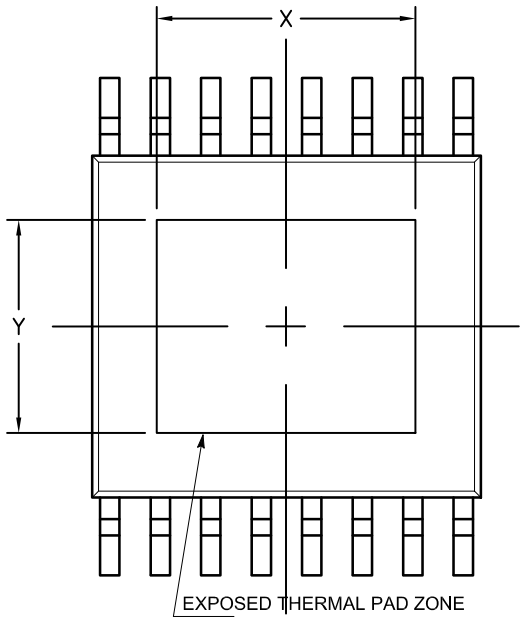
DATE 22 JUN 2017



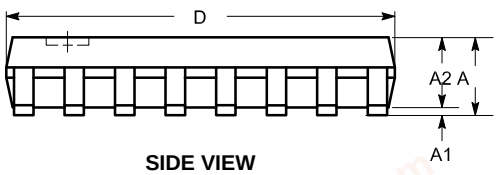
TOP VIEW



END VIEW

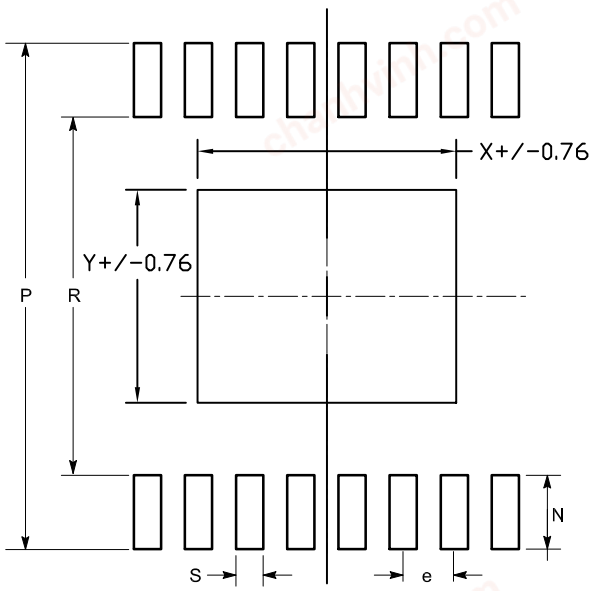


BOTTOM VIEW



SIDE VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.45		0.75
N	0.90		1.00
P	6.50		6.70
R	4.60		4.80
S	0.37		0.47
θ	0°		8°
X		3.33 REF	
Y		2.76 REF	



LAND PATTERN

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153 variations ABT.

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